ME VLSI DESIGN

CURRICULUM AND SYLLABI 2023

FACULTY OF ENGINEERING

KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University, Established Under Section3 of UGC Act 1956)

Eachanari post, COIMBATORE 641021, INDIA

KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University Established Under Section 3 of UGC Act 1956)
(Accredited with A+ Grade by NAAC in the Second Cycle)
Coimbatore – 641 021. INDIA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN (FULL TIME)
COURSE OF STUDY AND SCHEME OF EXAMINATIONS
(2023 BATCH ONWARDS)

SUB CODE	TITLE OF THE COURSE	OBJECTIVES AND OUT COMES		INSTRUCTION HOURS/ WEEK			CREDITS	MAXIMUM MARKS		
		PSO's	PO's	L	T	P		CIA	ESE	TOTAL
								40	60	100
SEMESTER - I										
22MEVL101	GRAPH THEORY AND OPTIMIZATION TECHNIQUES	1,2	1,2,8	3	1	0	4	40	60	100
22MEVL102	DIGITAL CMOS VLSI DESIGN	1,2	1,2,4,8,	3	0	0	3	40	60	100
22MEVL103	ANALOG INTEGRATED CIRCUIT DESIGN	1,2	1,5,6,7, 8,	3	0	0	3	40	60	100
22MEVL104	PCB DESIGN AND FABRICATION	1,2	1,2,6,8	3	0	0	3	40	60	100
22MEVL105	CAD FOR VLSI	1,2	1,2,3,8	3	0	0	3	40	60	100
22MEVL106	SEMICONDUCTOR DEVICES AND MODELING	1,2	2,3,4,8	3	0	0	3	40	60	100
22MEVL111	FPGA DESIGN LABORATORY	1,2	1,2,3,8	0	0	4	2	40	60	100
22MEVL112	PRINTED CIRCUIT BOARD DESIGN AND COMPONENT ASSEMBLING LABORATORY	1,2	1,2,3,4, 8	0	0	4	2	40	60	100
Total				**18**	**1**	**8**	**23**	**320**	**480**	**800**
SEMESTER - II										
22MEVL201	TESTING OF VLSI CIRCUITS	1,2	3,4	3	0	0	3	40	60	100
22MEVL202	LOW POWER VLSI DESIGN	1,2	5,6	3	0	0	3	40	60	100
22MEVL203	ASIC DESIGN	1,2	2,6	3	0	0	3	40	60	100
22MEVL204	MACHINE LEARNING IN VLSI	1,2	2,6	3	0	0	3	40	60	100

22MEVLE**	PROFESSIONAL ELECTIVE 1	1,2	2	3	0	0	3	40	60	100
22MEVL211	INDUSTRIAL TRAINING (MINI PROJECT)	1,2	4,5	0	0	0	2	40	60	100
22MEVL212	ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY	1,2	1,2,8	0	0	4	2	40	60	100
22MEVL213	MINI PROJECT WITH SEMINAR	1,2	1,2,3	0	0	2	2	40	60	100
Total				**15**	**0**	**s 6**	**21**	**320**	**480**	**800**
SEMESTER - III										
22MEVL301	VLSI SIGNAL PROCESSING	1,2	1,2,6	3	0	0	3	40	60	100
22MEVLE**	PROFESSIONAL ELECTIVE 2	1,2	1,2,3,6	3	0	0	3	40	60	100
22MEVLE**	PROFESSIONAL ELECTIVE 3	1,2	3,4,5,6 ,7,8,9	3	0	0	3	40	60	100
	AUDIT COURSE - I	1,2	3,4,5,6 ,7,8,9	2	0	0	0	40	60	100
22MEVL391	PROJECT WORK – PHASE I	1,2	1,2,3,8	0	0	1 2	6	40*	60	100
Total				**11**	**0**	**1 2**	**15**	**200**	**300**	**500**
SEMESTER - IV										
22MEVL491	PROJECT WORK – PHASE II	1,2	3,4,5,6 ,7,8	0	0	2 4	12	120 **	180	300
Total				**0**	**0**	**2 4**	**12**	**120**	**180**	**300**

L-Lecture T-Tutorial P-Practical C-Credit
CIA – Continuous Internal Assessment
ESE – End semester Examination

Total Credits = 71
Total Marks = 2400

*** To be evaluated internally by a committee of members**
Review 1 & 2 – 40 marks
Phase 1 Final presentation and viva voce – 60 marks
** **To be evaluated internally by a committee of members**
Review 1, 2 & 3 – 120 marks
Phase 2 Final presentation and viva voce – 180 marks

PROGRAM ELECTIVE COURSES (PEC)

S. NO	COURSE CODE	SUBJECTS	PERIODSPER WEEK			CONTACT PERIODS	CREDITS
			L	T	P		
1.	22MEVLE001	Wireless Sensor Networks	3	0	0	3	3
2	22MEVLE002	Advanced Microprocessors and Microcontrollers	3	0	0	3	3
3	22MEVLE003	Electronics for Solar Power	3	0	0	3	3
4	22MEVLE004	Robotics and Intelligent Systems	3	0	0	3	3
5	22MEVLE005	RF System Design	3	0	0	3	3
6	22MEVLE006	Signal Integrity for High Speed Design	3	0	0	3	3
7	22MEVLE007	EMI and EMC in System Design	3	0	0	3	3
8	22MEVLE008	Hardware and Software Co-design	3	0	0	3	3
9	22MEVLE009	Reconfigurable Computing	3	0	0	3	3
10	22MEVLE010	Evolvable Hardware	3	0	0	3	3
11	22MEVLE011	Power Management and Clock Distribution Circuits	3	0	0	3	3
12	22MEVLE012	SoC Design	3	0	0	3	3
13	22MEVLE013	Data Converters	3	0	0	3	3
14	22MEVLE014	Advanced Digital System Design	3	0	0	3	3

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			Lecture	Tutorial	Practical	
1.	AX5091	English for Research Paper Writing	2	0	0	0
2.	AX5092	Disaster Management	2	0	0	0
3.	AX5093	Sanskrit for Technical Knowledge	2	0	0	0
4.	AX5094	Value Education	2	0	0	0
5.	AX5095	Constitution of India	2	0	0	0
6.	AX5096	Pedagogy Studies	2	0	0	0
7.	AX5097	Stress Management by Yoga	2	0	0	0
8.	AX5098	Personality Development Through Life Enlightenment Skills	2	0	0	0
9.	AX5099	Unnat Bharat Abhiyan	2	0	0	0
				Total Credits		**0**

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SI. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
			L	T	P		
1.	22MEVL213	Mini Project with Seminar	0	1	2	3	2
2.	22MEVL391	Project Work – Phase I	0	0	12	12	6
3.	22MEVL491	Project Work – Phase II	0	0	24	24	12

23MECC10 GRAPH THEORY AND OPTIMIZATION TECHNIQUES 4H-4C

Instruction Hours/week: L: 3 T: 1 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical modelfor a linear programming problem in a real life situation.
- To provide knowledge and training using non-linear programming under limited resourcesfor engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

COURSE OUTCOMES:

At the end of the course, students will be able to

- Apply graph ideas is solving connectivity related problems.
- Apply fundamental graph algorithms to solve certain optimization problems.
- Formulate and construct mathematical models for linear programming problems and solvethe transportation and assignment problems.
- Model various real-life situations as optimization problems and effect their solution throughNon-linear programming.
- Apply simulation modeling techniques to problems drawn from industry management andother engineering fields.

UNIT I GRAPHS **12**

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM **12**

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth –First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING **12**

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING **12**

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING **12**

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60

REFERENCES:

1. Taha H.A, "Operation Research: An Introduction", Ninth Edition, Pearson Education, NewDelhi, 2010.
2. Gupta P. K, and Hira D.S., "Operation Research", Revise Edition, S. Chand and CompanyLtd., 2012.
3. Sharma J.K., "Operation Research", 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, "Introduction to Graph Theory", Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., " A text book of Graph Theory", Springer Science andBusiness Media, New Delhi, 2012.
6. Narasingh Deo, "Graph Theory with Applications to Engineering and Computer Science",Prentice Hall India,1997.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL102 **DIGITAL CMOS VLSI DESIGN** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To recall the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital back end of all wireless systems etc
- To develop the combinational logic designs
- To develop the sequential logic designs
- To model arithmetic building blocks
- To construct the memory architectures

COURSEOUTCOMES:

At the end of the course the students will be able to

- Understand mathematical methods and circuit analysis models in analysis of CMOS digital circuits
- Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches
- Select design methodology of arithmetic building blocks
- Model functional units including ROM and SRAM
- Examine the parameters size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

UNIT II COMBINATIONAL LOGICCIRCUITS 9

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non bistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDINGBLOCKS 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V MEMORY ARCHITECTURES 6

Memory Architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-write memories(RAM), dynamic memory design,6 transistor SRAM cell, Sense amplifiers.

TOTAL: 45

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective",Prentice Hall of WIndia,2nd Edition,Feb2003,
2. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition,1993
3. MJ Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL103 ANALOG INTEGRATED CIRCUIT DESIGN 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To explain analog circuits, play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology.
- To categorize the concept of frequency and noise performance of amplifiers
- To explain the design of op amp and analyze feedback amplifiers and one stage op amps
- To construct the stability and frequency design of two stage op amps
- To gain the knowledge in use of current mirrors design and current sinks with MOS devices

COURSE OUTCOMES:

At the end of the course the students will be able to

- Explain the amplifiers with their various specifications
- Summarize the concept of frequency and noise performance of amplifiers
- Identify the design of op amp and analyse feedback amplifiers and one stage op amps
- Demonstrate the stability and frequency design of two stage op amps
- Demonstrate use current mirrors design and current sinks with MOS devices

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers — to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.

UNIT II HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and sourcefollower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps,Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis of two stage Op amp — two stage Op amp single stage CMOS Cs as second stageand using cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation,Constant-Gm Biasing.

TOTAL: 45

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.
3. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons,Inc.,2003.
4. Phillip E.Allen, DouglasR.Holberg, "CMOS Analog Circuit Design", Oxford University Press,2nd edition, 2002.
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", WileyIEEE Press, 3rd Edition, 2010

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To demonstrate the students to the basics of PCB design
- To explain the new users of the software through a very simple design
- To apply the mechanical aspect of PCB design and to aid in understanding thedesign issues, manufacturing processes.
- To show the electrical aspect of PCB design
- To outline the state of art technology in PCB design and manufacturing

COURSE OUTCOMES

At the end of the course the students will be able to

- Develop the basics, industry standards organizations related to the design and fabrication of PCBs.
- Interpret new users of the software through a very simple design
- Construct Capture parts using the Capture Library Manager and Part Editorand the PSpice Model Editor.
- Learn PCB design for signal integrity
- Summarize the fabricate process of PCBs.

UNIT I BASICS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS 9

Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Postprocess (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard HoleDimensions, Soldermask Tolerance.

UNIT II PCB DESIGN FLOW USING CAD TOOL 9

Overview of Computer-Aided Design. Project structures and the layout toolset- Project Setup and Schematic Entry Details, the Layout Environment and Tool Set. Creating a Circuit Design with Capture- Starting a new project placing parts, Wiring (connecting) the parts, creating the Layout netlist in Capture. Designing the PCB with Layout- Starting Layout and importing the netlist, Performing a design rule check, Making a board outline, Placing the parts, Auto routing the board Manual routing, Cleanup Locking traces, Post processing the board design for manufacturing. Setting up a user account, Submitting Gerber files and requesting a quote, Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

UNIT III DESIGN FOR MANUFACTURING 9

PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices. Component Spacing for Surface Mounted Devices SMDs, Mixed THD and SMD Spacing Requirements. Footprint and Padstack Design for PCB Manufacturability- Land Patterns for Surface-Mounted Devices- Land Patterns forThrough-hole Devices, Padstack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Soldermask and solder paste dimensions.

UNIT IV PCB DESIGN FOR SIGNAL INTEGRITY 9

Circuit Design Issues Not Related to PCB Layout, Issues Related to PCB Layout, Ground Planes and Ground Bounce, PCB Electrical Characteristics, PCB Routing Topics, Making and editing capture parts, The Capture Part Libraries, Types of Packaging, Pins, Part Editing Tools, Constructing Capture Parts, making and editing layout footprints.

UNIT V EMERGING ADDITIVE PROCESSES FOR PCB MANUFACTURING 9

Fundamentals of additive manufacturing, classification, advantages and standards on Additive manufacturing. Stereo lithography (SL), Stereo lithography (SL), Fused Deposition Modelling (FDM), Three Dimensional Printing (3DP), Materials, Applications. Voltera-V-one PCB double side Printer, Bot Factory- SV2-multi layer PCB printer, LPKF circuit board plotter and LDS Prototyping.

TOTAL : 45

REFERENCES:

1. Kraig Mitzner, Complete PCB Design Using OrCad Capture and Layout, Newness, 1st Edition, 2009.
2. Simon Monk, "Make Your Own PCBs with EAGLE: From Schematic Designs to FinishedBoards", McGraw-Hill Education TAB, 2nd Edition, 2017.
3. Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design", PrenticeHall PTR, 2003.
4. Lee W. Ritchey , John Zasio, Kella J. Knack, " Right the First Time: a PracticalHandbook on High Speed Pcb and System Design", Speeding Edge , 2003.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL105 **CAD FOR VLSI** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To introduce the VLSI Design Methodologies and Design Methods.
- To introduce Data Structures and Algorithms required for VLSI Design.
- To study Algorithms for Partitioning and Placement.
- To study Algorithms for Floor planning and Routing.
- To study Algorithms for Modelling, Simulation and Synthesis.

COURSE OUTCOMES:

- Use various VLSI Design Methodologies and Design Methods.
- Understand different Data Structures and Algorithms required for VLSI Design.
- Develop Algorithms for Partitioning and Placement.
- Develop Algorithms for Floor planning and Routing.
- Design Algorithms for Modelling, Simulation and Synthesis.

UNIT I INTRODUCTION 9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI DesignCycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles –Review of VLSI Design Automation Tools.

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS 9

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT 9

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTING 9

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing –Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS 9

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – BinaryDecision Diagrams – High Level Synthesis.

TOTAL: 45

REFERENCES:

1. Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India,2017.
2. Naveed A. Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition,Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, "Handbook of Algorithms forPhysical Design Automation, CRC Press, 1st Edition, 2

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL106 SEMICONDUCTOR DEVICES AND MODELING 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theoryand devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

- Explore the properties of MOS capacitors.
- Analyze the various characteristics of MOSFET devices.
- Describe the various CMOS design parameters and their impact on performance of thedevice.
- Discuss the device level characteristics of BJT transistors.
- Identify the suitable mathematical technique for simulation.

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–OxideInterface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNIT V MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

TOTAL: 45

REFERENCES:

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge UniversityPress, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd,2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analogand RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition,2014
7. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, ‘-' - No Correlation

23MEVL111 **FPGA DESIGN LABORATORY** **4H-2C**

Instruction Hours/week: L: 0 T: 0 P: 4 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

COURSE OBJECTIVES:

- To help engineers read, understand, and maintain digital hardware models andconventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog.

COURSE OUTCOMES:

On successful completion of this course, students will be able to

- Understand and use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces.
- Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.
- The implementation of higher level of abstraction to design and verification
- Develop Verilog test environments of significant capability and complexity.
- Integrate scoreboards, multichannel sequencers and Register Models

LIST OF EXPERIMENTS

1. Introduction to Verilog and System Verilog
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types
4. Experiment with blocking and non-blocking assignments
5. Model and verify simple ALU
6. Model and verify an Instruction stack
7. Use an interface between testbench and DUT
8. Developing a test program
9. Create a simple and advanced OO testbench
10. Create a scoreboard using dynamic array
11. Use mailboxes for verification
12. Generate constrained random test values
13. Using coverage with constrained random tests

TOTAL: 60

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL112 PRINTED CIRCUIT BOARD DESIGN AND COMPONENT ASSEMBLING LABORATORY 4H-2C

Instruction Hours/week: L: 0 T: 0 P: 4 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

OBJECTIVES

- To impart hands on experience in single, double and multi layer PCB design so that students would be able to design and to fabricate and develop electronic systems for various applications.

COURSE OUTCOMES:

- Ability to use CAD software tools
- Ability to design a schematic diagram
- Ability to convert a schematic diagram to board/layout diagram
  Implement routing in board/layout diagram
- Ability to fabricate a PCB from board diagram
- Ability to skillfully perform assembling and soldering of components

LIST OF EXPERIMENTS:

1. Introduction to PCB and EDA software tools.
2. To prepare design layout of PCBs using software tools.
3. To fabricate simple PCB by chemical and mechanical process and drilling of PCB.
4. To fabricate PCB using additive technology and testing of electronics circuit on PCB.
5. To perform Assembly Processes -Manual assembly processes,
6. To perform automated assembly processes (pick and place).
7. Identification of various types of Printed Circuit Boards (PCB) and soldering Techniques.
8. Convert the power supply circuit into PCB and simulate its 2D and 3D view.
9. Design and create single sided PCB Layout for Full wave rectifier circuit.
10. Design and create PCB Layout for DC Motor controller.
11. Design and create single sided PCB Layout for Flashing LEDs using 555 IC.
12. LED Scrolling Display Board using microcontroller
13. To perform continuity tester of PCB project.
14. To implement a Digital Counter To fabricate the PCB for the same.
15. To fabricate PCB dual power supply, analog design.
16. To fabricate PCB with Split power and ground planes.

TOTAL : 60

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL201 **TESTING OF VLSI CIRCUITS** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To list the various VLSI testing techniques
- To summarize logic and fault simulation and testability measures.
- To develop the test generation algorithms for combinational and sequential circuits.
- To apply the design for testability concept for device under test (DUT).
- To categorize the various fault diagnosis methods.
- To determine the usage of various testing techniques in different VLSI circuit.

COURSE OUTCOMES:

At the end of the course the students will be able to

- Understand VLSI Testing Process.
- Summarize Logic Simulation and Fault Simulation.
- Develop test generation algorithms for Combinational and Sequential Circuits.
- Apply the design for testability concept for device under test (DUT).
- Categorize the Design for Testability

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship among Fault Models.

UNIT II LOGIC &FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – SCOAP Controllability and Observability.

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture –Built-In Self-Test – Random Logic BIST – DFT for other Test Objectives.

UNIT V FAULT DIAGNOSIS 9

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation for Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL: 45

REFERENCES:

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017.
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge UniversityPress, 2017.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL202 **LOW POWER VLSI DESIGN** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To identify sources of power in an IC.
- To utilize the power reduction techniques based on technology independent and technology dependent methods
- To develop suitable techniques to reduce the power dissipation.
- To estimate Power dissipation of various MOS logic circuits.
- To develop algorithms for low power dissipation.
- To evaluate the synthesis for low power design

COURSE OUTCOMES:

At the end of the course the students will be able to

- Identify the power sources in CMOS devices.
- Design and analyze various power reduction techniques
- Apply low power techniques for reduction of power dissipation
- Estimate the power dissipation of ICs
- Ability to develop algorithm to reduce power dissipation by software.
- Evaluate the synthesis for low power design

UNIT I POWER DISSIPATION IN CMOS **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation inCMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9**

Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, lowpower design.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9**

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV POWER ESTIMATION **9**

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

TOTAL: 45

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
6. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, JohnWiley and sons, inc. 2001.
7. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, ‘-' - No Correlation

23MEVL203 **ASIC DESIGN** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To demonstrate the concepts of ASIC library design
- To develop semi-custom IC with logic cells, I/O cells and interconnect architecture using various programming technology
- To categorize different ASIC architecture based on the application
- To explain ASIC interconnects, design software for placement, routing and synthesis
- To apply the designing rules to design System On Chip (SOC) ASICs

COURSE OUTCOMES:

At the end of the course the students will be able to

- Explain the ASIC library design concept
- Develop semi-custom IC using various programming technology
- Distinguish different ASIC architecture based on the application
- Explain the algorithms for floor planning and placement of cells and to apply routingalgorithms for optimization of length and speed.
- Utilize the design rules to design System on Chip (SOC)

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE 9

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs — Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning,Floor planning tools ,I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing,Special routing.

UNIT V SYSTEM-ON-CHIP DESIGN 9

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation ofSignal Processing Systems”, Wiley, 2008.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5. Douglas J. Smith, “HDL Chip Design”, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits forTelecommunication and Signal Processing", Prentice Hall, 1994.
7. S.Pasricha and N.Dutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsveir, 2008.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, ‘-' - No Correlation

23MEVL204 **MACHINE LEARNING IN VLSI** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To use machine learning technologies in VLSI CAD to further automate the design, verification and implementation of the most advanced chips.
- To relate the usage of machine learning algorithms for Compact Lithographic Process Models.
- To apply Machine Learning in Mask Synthesis and Physical Verification to bear on CAD problems such as hot-spot detection, efficient test generation, post-silicon measurement minimization.
- To predict the Yield and Reliability of VLSI chips using machine learning methods.
- To comprehend the appropriate application of the various supervised, unsupervised and statistical learning in thevarious layers of chip design hierarchy.

COURSE OUTCOMES:

At the end of the course the student will be able to

- Use machine learning technologies in VLSI CAD to further automate the design, verification and implementation of the most advanced chips.
- Relate to the usage of machine learning algorithms for Compact Lithographic Process Models.
- Apply Machine Learning in Mask Synthesis and Physical Verification to bear on CAD problems such as hot-spot detection, efficient test generation, post-silicon measurement minimization.
- Predict the Yield and Reliability of VLSI chips using machine learning methods.
- Comprehend the appropriate application of the various supervised, unsupervised and statistical learning in thevarious layers of chip design hierarchy.

UNIT 1 A PRELIMINARY TAXONOMY FOR MACHINE LEARNING IN VLSI CAD 9

Machine learning taxonomy, VLSI CAD Abstraction levels, **Machine Learning for Compact Lithographic Process Models:** Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process –Mask, Imaging, Resist & Etch Transfer Function.

UNIT 2 MACHINE LEARNING OF COMPACT LITHOGRAPHIC PROCESS MODELS (CONT.,) 9

Compact process model machine learning problem statement, CPM Task, CPM Training Experience, Performance metrics, Supervised learning of a CPM, **Neural Network Compact Patterning Models:** Neural Network Mask Transfer Function, Neural Network Image Transfer Function, Neural Network Resist Transfer Function, Neural Network Etch Transfer Function.

UNIT 3 MACHINE LEARNING FOR MASK SYNTHESIS 9

Introduction, Machine Learning guided OPC, MLP Construction, ML-EPC, EPC, **Machine Learning in Physical Verification:** Introduction, Machine Learning in Physical Verification – layout feature extraction & encoding,models for hotspot detection.

UNIT 4 MACHINE LEARNING IN MASK SYNTHESIS AND PHYSICAL DESIGN 9

Machine Learning inMask Synthesis – mask synthesis flow, Machine Learning for sub-resolution assist features, Machine Learning for optical proximity correction. Machine Learning inPhysical Design - for datapath placement, routability driven placement, clock optimization, lithography friendly routing, **Machine Learning for Manufacturing:** Gaussian Process-Based Wafer-Level Correlation Modeling and Its Application s(Text Book: 1 – 5.1).

UNIT 5:MACHINE LEARNING FOR YIELD AND RELIABILITY 9

High-volume manufacturing yield estimation – Histogram with random sampling, Histogram with GP-ST-PS, Kernel density estimation. Machine learning based aging analysis .Learning from limited data in VLSI CAD, Iterative feature search (Comparative study of Assertion mining algorithms in GoldMine.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN		**2023-2024**
		Semester I
23MEVLE**	**PROFESSIONAL ELECTIVE 1**	**3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

M.E VLSI DESIGN		**2023-2024**
		Semester I
23MEVL211	**INDUSTRIAL TRAINING (MINI PROJECT)**	**0H-2C**

Instruction Hours/week: L:0 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

23MEVL212 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY 4H-2C

Instruction Hours/week: L: 0 T: 0 P: 4 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

OBJECTIVES:

- To choose analog circuit design starting with transistor characterization and finally realizing an IA design.
- To interpret performance analysis for CMOS inverter & frequency comparison of ring oscillator
- To design single stage amplifier & instrumentation amplifier using OPAMP
- To develop Layout editor tools.
- To model a differential amplifier.

COURSEOUTCOMES:

At the end of the course the students will be able to

- Design digital and analog Circuit using CMOS given a design specification.
- Make use of EDA tools like Cadence, Mentor Graphics or other open-source software tools like LT Spice.
- Develop layout designs using above tools
- Construct different amplifiers
- Experiment with CAD tools

List of Experiments:

1. Extraction of process parameters of CMOS process transistors
   - **a.** Plot I_D vs. V_{GS} at different drain voltages for NMOS,PMOS.
   - **b.** Plot I_D vs. V_{GS} at particular drain voltage (low) for NMOS,PMOS and determine Vt.
   - **c.** Plot log I_D vs. V_{GS} at particular gate voltage (high) for NMOS, PMOS and determine I_{OFF} and sub-thresholds lope.
   - **d.** Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   - **e.** Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage to extract V_{th} use the following procedure.
     - Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
     - Plot $y=I_D/(g_m)$ as a function of VGS using SPICE.
     - Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   - **f.** Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.
2. CMOS inverter design and performance analysis

a.

i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transition voltage and gain g. Calculate V_{IL},V_{IH},NM_H,NM_L for the inverter.

ii. Plot VTC for CMOS inverter with varying V_{DD}.

iii. Plot VTC for CMOS inverter with varying device ratio.

b. Perform transient analysis of CMOS inverter with no load and with load and determine t_{pHL},t_{pLH},20%-to-80%$t_r$and80%-to-20%t_f.

c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis

a. Draw small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.

b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.

i. Establish a test bench to achieve $V_{DSQ}=V_{DD}/2$.

ii. Calculate input bias voltage for a given bias current.

iii. Use spice and obtain the bias current. Compare with the theoretical value

iv. Determine small signal voltage gain,-3dBBWandGBWoftheamplifier
Using small signal analysis in spice, considering load capacitance.

v. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from-3dBBW.

vi. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier.

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10.Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

a. Draw the schematic of op-amp macromodel.

b. Draw the schematic of INA.

c. Obtain parameters of the op-amp macromodel such that it meets a given specification for:

i. low-frequency voltage gain,

ii. unity gain BW(fu),

iii. input capacitance,

iv. output resistance,

v. CMRR

d. Draw schematic diagram of CMRR simulation setup.

e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistor from CMOS process library. Use Metal1 as interconnect line between inverters.

b. Run DRC,LVS and RC extraction. Make sure there is no DRC error.

c. Extract the netlist. Use extracted netlist and obtain tPHL tPLH for the inverter using Spice.

d. Use a specific interconnect length and connect and connect three inverters in a chain. Extract the new netlist and obtain tPHL and tPLH of the middle inverter.

e. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,

b. unity gain BW(fu),

c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.

ii. Perform time domain simulation and verify low frequency gain.

iii. Perform AC analysis and verify.

TOTAL:60

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVL213 MINI PROJECT WITH SEMINAR LTPC

0 0 0 2

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVL301 VLSI SIGNAL PROCESSING L T P C

3 0 0 3

OBJECTIVES:

- To understand DSP system, pipelining concept & filters
- To interfere retiming, algorithmic strength reduction
- To outline fast convolution, pipelining and IIR filters
- To understand bit-level arithmetic architectures

- To identify numerical strength reduction, different pipeling concepts
- To model efficient designofDSParchitectures suitableforVLSI

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLELPROCESSINGOFFIRFILTERS 9

Introduction to DSP systems — Typical DSP algorithms,Data flow and Dependencegraphs-criticalpath,Loopbound,iterationbound,Longestpathmatrixalgorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing forlowpower.

UNIT II RETIMING,ALGORITHMIC STRENGTH REDUCTION 9

Retiming–definitionsandproperties,Unfolding–analgorithmforunfolding,propertiesof unfolding, sample period reduction and parallel processing application, Algorithmicstrength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter,DCTarchitecture,rank-order filters, Odd-Even merge-sortarchitecture,parallel rank-orderfilters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined andparallel recursive filters — Look-Ahead pipelining in first-order IIR filters, Look-Aheadpipelining with power- of-2 decomposition, Clusteredlook-ahead pipelining, ParallelprocessingofIIRfilters,combined pipeliningandparallelprocessingofIIRfilters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures — parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟srule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule forprecisionimprovement,DistributedArithmetic fundamentals andFIRfilters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numericalstrengthreduction—subexpressionelimination,multipleconstantmultiplication, iterative matching, synchronous pipelining and clocking styles, clock skewinedge-triggeredsinglephaseclocking,two phaseclocking,wavepipelining.Asynchronouspipeliningbundleddataversusdualrailprotocol.

TOTAL: 45 PERIODS

COURSEOUTCOMES:

At the end of the course the students will be able to

- Ability to determine the parameters influencing the efficiency of DSP architectures andapplypipeliningandparallelprocessingtechniquestoalterFIRstructuresforefficiency
- Analyze andmodifythedesignequationsleadingtoefficientDSParchitecturesfortransforms
- Infer speedupconvolutionprocessanddevelopfastandareaefficientIIRstructures
- Model to develop fast and area efficient multiplier architectures

- Solve to reducemultiplicationsandbuildfasthardwareforsynchronousdigitalsystems
- Experiment with CAD Tools

REFERENCES

1. KeshabK.Parhi,"VLSIDigitalSignalProcessingSystems,Designandimplementation",Wiley ,Interscience,2007.
2. U.Meyer— Baese,"DigitalSignalProcessingwithFieldProgrammableGateArrays",Springer,2nd Edition,2004.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVLE PROFESSIONAL ELECTIVE 2 LTPC**
3 0 0 3

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVLE PROFESSIONAL ELECTIVE 3 LTPC**
3 0 0 3

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

AUDIT COURSE - I **LTPC**

2 0 0 0

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVL391 **PROJECT WORK – PHASE –I** **L T P C**

0 0 12 6

COURSE OBJECTIVESS:

To impart knowledge on

- Developing analytical skills of the students to address any specific structural related problems.
- Select suitable experimental method to solve the structural engineering problems.
- Execution of the project using suitable techniques
- On completion of the project work students will be in a position to take up any research and challenging practical problem for finding better solutions.
- To take up any research and challenging practical problem for finding better solutions.
- To provide a clear idea of his/her area of work and they are in a position to carry out the work in a systematic way.

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Identify the problem by analyzing the gap through literature survey
- Conduct the experimental work to solve structural engineering problems
- Validate the experimental results using simulation models
- Write a technical report related to selected topic
- Present outcome of the study with the help of ppt.
- Manage any type of design and construction projects.

SYLLABUS:

The student individually works on a specific topic approved by faculty member who is familiar in this area of interest. The student can select any topic which is relevant to his/her specialization of the programme. The topic may be experimental or analytical or case studies. At the end of the semester, a detailed report on the work done should be submitted which contains clear definition of the identified problem, detailed literature review related to the area of work and methodology for carrying out the work. The students will be evaluated through a viva-voce examination by a panel of examiners including one external examiner.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVL491 **PROJECT WORK – PHASE –II** **L T P C**

0 0 24 12

COURSE OBJECTIVESS:

To impart knowledge on

- Developing analytical skills of the students to address any specific structural related problems.
- Select suitable experimental method to solve the structural engineering problems.

- Execution of the project using suitable techniques
- On completion of the project work students will be in a position to take up any research and challenging practical problem for finding better solutions.
- To take up any research and challenging practical problem for finding better solutions.
- To provide a clear idea of his/her area of work and they are in a position to carry out the work in a systematic way.

COURSE OUTCOMES:

At the end of the course, the students will be able to

- Identify the problem by analyzing the gap through literature survey
- Conduct the experimental work to solve structural engineering problems
- Validate the experimental results using simulation models
- Write a technical report related to selected topic
- Present outcome of the study with the help of ppt.
- Manage any type of design and construction projects.

SYLLABUS:

The student should continue the phase I work on the selected topic as per the formulated methodology. At the end of the semester, after completing the work to the satisfaction of the supervisor and review committee, a detailed report should be prepared and submitted to the head of the department. The students will be evaluated through based on the report and the viva-voce examination by a panel of examiners including one external examiner.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE001 WIRELESS SENSOR NETWORKS L T P C

3 0 0 3

OBJECTIVES:

- To identify and Distinguish between the notion of Wired and Wireless Networks.
- To analyse the basic concepts for designing a routing Protocol for MANETs.
- To learn the concepts of Security issues for designing a routing protocol for MANETs.
- To understand the Basic concepts of Sensor Networks for Communication in Mobile computing.
- To apply Fundamental Principles Characteristics for designing Sensor Networks for Communication.
- To develop the Sensor management, sensor network middleware, operating systems.

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

UNIT II ARCHITECTURES 9

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

UNIT III MAC AND ROUTING 9

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy- Efficient Routing, Geographic Routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT AND SECURITY 9

Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Define the fundamentals of Mobile ad-hoc Networks.
- Understand and be able to use mobile computing more effectively.
- Apply different routing technologies for designing a routing protocol.
- Understand the infrastructure establishment, topology control and joint routing and information aggregation.
- Develop the sensor network platform and tools state-centric programming.
- Demonstrate the ability to solve security related problems using a routing Protocol.

REFERENCES

1. Ian F. Akyildiz, Mehmet Can Vuran, “Wireless Sensor Networks”, John Wiley, 2010
2. Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”,Springer, 2008.
3. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless SensorNetworks" , John Wiley, 2005.
4. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-s Technology, Protocols, And Applications”, John Wiley, 2007.
6. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
7. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press,2005.
8. Mohammad Ilyas And Imad Mahgaob, “Handbook Of Sensor Networks: CompactWireless And Wired Sensing Systems”, CRC Press,2005.
9. Wayne Tomasi, “Introduction To Data Communication And Networking‖, Pearson Education”, 2007.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, ‘-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE002 ADVANCED MICROPROCESSORS & MICROCONTROLLERS L T P C
3 0 0 3

OBJECTIVES:

- To demonstrate the fundamentals of microprocessor architecture.
- To develop the high performance features in CISC architecture
- To summarize the high performance features in RISC architecture
- To explain the basic features in Motorola microcontrollers.
- To understand the students to PIC Microcontroller
- To Build systems using microcontrollers for real time applications.

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache –Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging — Multitasking — Exception and Interrupts — Instruction set — addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU — Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MSP430 16 - BIT MICROCONTROLLER 9

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter

–PWM and introduction to C-Compilers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Understand the fundamentals of microprocessor architecture.
- Develop the high performance features in CISC architecture.
- Summarize the high performance features in RISC architecture.
- Explain the basic features in Motorola microcontrollers.
- Understand the PIC Microcontroller.
- Build systems using microcontrollers for real time applications.

REFERENCES:

1. Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 1995
2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education , 1997.
3. Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , 2000.
4. Gene .H.Miller ." Micro Computer Engineering ", Pearson Education , 2003.
5. John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, 1997.
6. John H.Davis , "MSP 430 Micro controller basics", Eelsevier, 2008.
7. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", PearsonEducation 1999.
8. Barry.B.Breg, "The Intel Microprocessors Architecture , Programming and Interfacing " , PHI,2002.
9. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001. Readings: Web links -- www.ocw.mit.edu, www.arm.com

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVLE003 ELECTRONICS FOR SOLAR POWER L T P C

3 0 0 3

OBJECTIVES

- To understand basics of solar energy harnessing and solar panel and array.
- To demonstrate the fundamentals of solar energy conversion and familiarize with solar geometry.
- To learn the concepts of maximum power point tracking techniques.
- To apply the solar energy policies.
- To categorize the Basic concepts of Battery and its Types.
- To develop the simulation concepts of PV module & converters

UNIT I INTRODUCTION TO SOLAR POWER 9

Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface — Sun path diagrams — Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, Vmp, I_{MP}, Voc, I_{SC} – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II DC-DC CONVERTER 9

Principles of step-down and step-up converters – Analysis and design issues of buck, boost,buckboost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.

UNIT III MAXIMUM POWER POINT TRACKING 9

Direct Energy transmission, Impedance Matching, Maximum Power PointTracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques,Development of hardware, algorithms using processors for Standalone and Grid tied systems.

UNIT IV BATTERY 9

Types of Battery, Battery Capacity — Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, Circuits for Battery Management System (BMS), selection of Battery and sizing.

UNIT V SIMULATION OF PV MODULE & CONVERTERS 9

Simulation of PV module - VI Plot, PV Plot, finding V_{MP}, I_{MP}, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Learn the Photo Voltaic Cell concepts and its Characteristics.
- Categorize the DC convertor techniques.
- Apply the concepts of maximum power point tracking techniques.

- Understand the concepts of Battery and its Types.
- Demonstrate the simulation of PV modules.
- Understand the battery issues and selection

REFERENCES:

1. Chetan Singh Solanki, "Solar Photovoltaic: Fundamentals, Technologies and Applications", PHI Ltd., 2013
2. Tommarkvart, Luis castaner, "Solar cells; materials, manufacture and operation", Elsevier, 2005.
3. G.D .Rai, "Solar energy utilization ", Khanna publishes, 1993
4. Ned Mohan, Undeland and Robbin, "Power Electronics: converters, Application and Design", John Wiley and sons.Inc, Newyork, 1995.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE004 ROBOTICS AND INTELLIGENT SYSTEMS L T P C

3 0 0 3

OBJECTIVES:

- To learn the basic concepts in robotics.
- To demonstrate the various design aspects in robot grippers.
- To classify various drives and control systems.
- To outline knowledge on machine vision systems.
- To apply robot based concepts for automation
- To model plant automation process

UNIT I INTRODUCTION: 9

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution,accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II ROBOT GRIPPERS: 9

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III DRIVES AND CONTROL SYSTEMS: 9

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.

UNIT IV MACHINE VISION SYSTEM 9

Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines,

Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9

Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy decision and control, robots and application of robots for automation. Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robotdesign, Safety for robot and associated mass, New Trends & recent updates in robotics.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Learn to implement simple concepts associated with Robotics and Automation
- Demonstrate to use various Robotic sub-systems
- Explain to use kinematics and dynamics to design exact working pattern of robots
- Outline to implement computer vison algorithms for robots
- Identify and be aware of the associated recent updates in Robotics
- Organize plant automation process

REFERENCES:

1. John J. Craig, "Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 2nd Edition, 2004
2. Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications, McGraw — Hill International", 1986.
3. Shimon Y. Nof , "Handbook of Industrial Robotics" , John Wiley Co, 2001.
4. Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover,Pearson Education.
5. W.P. David, "Industrial Automation", John Wiley and Sons.
6. Richard D. Klafter , Thomas A. Chemielewski, Michael Negin, "Robotic Engineering : An Integrated Approach" , Prentice Hall India, 2002.
7. R.C. Dorf, "Handbook of design, manufacturing & Automation", John Wiley and Sons.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE005 **RF SYSTEM DESIGN** **L T P C**

3 0 0 3

OBJECTIVES:

- To study the operation and device characteristics of RF Active components.
- To construct RF filter and RF amplifier
- To learn the importance and issues in the design of RF
- To construct and analyze basic resonators and RF Filters
- To study the operation of mixers and oscillators.
- To understand the operation of PLL and frequency synthesizers in RF design

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model — Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATORS 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Show the user specifications for RF systems
- Analyze and design RF amplifiers
- Build the RF power amplifiers
- Explain the RF mixers and oscillators
- Design PLL for RF applications

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer AcademicPublishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
5. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-

CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE006 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To find sources affecting the speed of digital circuits.
- To illustrate the methods to improve the signal transmission characteristics
- To build system organization with improved signal integrity
- To examine proper circuitry models that minimizes the corruption of signals
- To examine the power considerations for system design concepts.
- To inspect the clock distribution and oscillators clock signals

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs.* circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations — L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out,logic switching , input impedance into a transmission-line section, reflection coefficient, skin- effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far- end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination,balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths — gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Infer the sources affecting the speed of digital circuits.
- Explain methods to improve the signal transmission characteristics
- Illustrate transmission line losses
- Select models appropriate for designing components
- Utilize clocking system and oscillators for distributing it in tree design
- Identify and testing signal integrity using eye diagram

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic,Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice HallPTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo ofInterconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 **PCB DESIGN AND FABRICATION** **3H-3C**

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVLE007 EMI AND EMC IN SYSTEM DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To understand the concepts related to Electromagnetic interference in PCBs.
- To provide solutions for minimizing EMI in PCBs .
- To learn various EMI coupling principles.
- To indulge knowledge on EMI control techniques and design procedures to make EMI compatible PCBs
- To learn electromagnetic compatibility issues with regard to the design of PCBS
- To learn, EMI standards and measurements in the design of PCBs

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL:45 PERIODS

COURSE OUTCOMES:

- Gain enough knowledge to understand the concept of EMI / EMC related to productdesign & development.
- To analyze the different EM coupling principles and its impact on performance ofelectronic system.
- Analyze electromagnetic interference, highlighting the concepts of both susceptibility andimmunity
- Interpret various EM compatibility issues with regard to the design of pcbs and ways toimprove the overall system performance
- To obtain broad knowledge of various EM radiation measurement techniques and thepresent leading edge industry standards in different countries

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house, Norwood, 3rd Edition, 1986.
4. C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 1992.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE008 HARDWARE SOFTWARE CO-DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To acquire the knowledge about system specification and modeling
- To gain the knowledge about hardware and software partitioning
- To learn the formulation of partitioning
- To learn the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.
- To study the different technical aspects about prototyping and emulation
- To categorize the different design specification and verfication

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous implementation - Processor Synthesis, Single- Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures, Comparison of Co-Design approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures andApplication System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- Explain the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.
- Summarize the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.
- Explain the concept of translating between software and hardware descriptions through co- design methodologies.
- Outline the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.

- Identify the concurrent specification from an algorithm, analyze its behavior and Partition the specification into software (C code) and hardware (HDL) components
- Summarize the design specification and its verification.

REFERENCES:

1. Patrick Schaumont, "A Practical Introduction to Hardware/Software Codesign", Springer,2010.
2. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated EmbeddedSystems", Kluwer Academic Publisher, 1998.
3. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice",Kluwer Academic Publisher,1997.
4. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design",Kaufmann Publisher,2001.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE009 RECONFIGURABLE COMPUTING L T P C

3 0 0 3

OBJECTIVES:

- To classify about the reconfigurable computing architectures
- To understand the concepts of software flexibility and hardware performance
- To Interpret of high speed computing fabrics like field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs)
- To develop the applications of dynamic and partial reconfigurable computing systems
- To outline mapping designs to reconfigurable platforms
- To summarize the FPGA applications

UNIT I RECONFIGURABLE COMPUTING HARDWARE 9

Domain specific processors, Application specific processors, Reconfigurable Computing Systems, Evolution of reconfigurable systems, Characteristics of RCS, advantages and issues. Device Architecture, Reconfigurable Computing Architectures, Reconfigurable Computing Systems, Reconfiguration Management

UNIT II PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models and System Architectures, Programming FPGA Applications in Verilog HDL, Compiling C for Spatial Computing, Programming Streaming FPGA Applications Using Block Diagrams in Simulink, Programming Data Parallel FPGA Applications, Operating System Support for Reconfigurable Computing, The JHDL Design and Debug System

UNIT III MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

Technology Mapping, Placement for General-purpose FPGAs, Datapath Composition, Specifying Circuit Layout on FPGAs, PathFinder: A Negotiation-based, Performance-driven Router for FPGAs, Retiming, Repipelining, and C-slow Retiming, Configuration Bitstream Generation, Fast Compilation Techniques

UNIT IV APPLICATION DEVELOPMENT 9

Implementing Applications with FPGAs, Instance-specific Design, Precision Analysis for Fixed- point Computation, Distributed Arithmetic, CORDIC Architectures for FPGA Computing, Hardware/Software Partitioning

UNIT V CASE STUDIES OF FPGA APPLICATIONS 9

SPIHT Image Compression, Automatic Target Recognition Systems on Reconfigurable Devices, Multi-FPGA Systems: Logic Emulation, The Implications of Floating Point for FPGAs, Evolvable FPGAs, Network Packet Processing in Reconfigurable Hardware, Active Pages:Memory-centric Computation

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Demonstrate the fundamentals of the reconfigurable computing and reconfigurable architectures.
- Explain the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels.
- Constrate the performance trade-offs involved in designing a reconfigurable computing platform with a specific focus on the architecture of a configurable logic block and the programmable interconnect.
- Summarize the state of the art reconfigurable computing architectures spanning fine grained (look up table based processing elements) to coarse grained (arithmetic logic unit level processing elements) architectures.
- Model how to architect reconfigurable systems
- Organize how to utilize solving challenging computational problems.

REFERENCES:

1. Scott Hauck and Andre` DeHon, "Reconfigurable Computing: The Theory and Practice ofFPGA-Based Computation", Morgan Kaufmann, 2008.
2. Stephen M. Trimberger, "Field – programmable Gate Array Technology", Springer, 2007.
3. CliveMaxfield, "The Design Warrior's Guide to FPGAs: Devices, Tools and Flows", Newnes, Elsevier, 2006.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

M.E VLSI DESIGN **2023-2024**

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE010 EVOLVABLE HARDWARE L T P C

3 0 0 3

OBJECTIVES:

- To Learn about the Evolvable Systems algorithms, multi-objective utility functions
- To apply the concepts of reliability, design-in redundancy, fault tolerance and defecttolerance
- To of evolvable systems using programmable logic devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms
- To analyze the possible circuits for evolution
- To analyze the evolutionary algorithms
- To demonstrate to implement reconfigurability in analog devices

UNIT I INTRODUCTION 9

Traditional hardware systems and its Limitations, Evolvable hardware, Characteristics of evolvable circuits and systems, Technology-Extrinsic and intrinsic evolution Offline and online evolution, Applications and scope of EHW

UNIT II EVOLUTIONARY COMPUTATION 9

Fundamentals of Evolutionary algorithms, Components of EA, Variants of EA, Genetic algorithms, Genetic Programming, Evolutionary strategies, Evolutionary programming, Implementations — Evolutionary design and optimizations, EHW — Current problems and potential solutions

UNIT III RECONFIGURABLE DIGITAL DEVICES 9

Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAs), Using reconfigurable hardware – Design phase, Execution phase, Evolution of digital circuits

UNIT IV RECONFIGURABLE ANALOG DEVICES 9

Basic architectures – Field Programmable Transistor arrays (FPTAs), Analog arrays, MWMs,Using reconfigurable hardware – Design phase, Execution phase, Evolution of analog circuits

UNIT V APPLICATIONS OF EHW 9

Synthesis vs. adaptation, Designing self-adaptive systems, Fault-tolerant systems, Real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- Understand the fundamentals of computational models and computers which have appeared at the intersection of hardware and artificial intelligence to solve hard computational problems.
- Understand the principles of bio-inspired and unconventional computational systems.
- Discuss about the reconfigurable digital architectures and its computational intelligence techniques.
- Discuss about the reconfigurable analog architectures and its computational intelligence techniques.
- Discuss about the typical applications of bio-inspired and other unconventional techniques in the phase of design, implementation and runtime of a computational device.
- Identify and Carry out the design of evolvable circuits

REFERENCES:

1. Garrison W. Greenwood and Andrew M. Tyhrrell, "Introduction to Evolvable Hardware: A Practical Guide for Designing Self- Adaptive Systems", Wiley-IEEE Press, 2006.
2. Tetsuya Higuchi, Xin Yao and Yong Liu, "Evolvable Hardware", Springer-Verlag, 2004.
3. Lukas Sekanina, "Evolvable Components: From Theory to Hardware Implementations",Springer, 2004.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60** Total**:100**

End Semester Exam: 3 Hours

22MEVLE01 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS L T P C

3 0 0 3

OBJECTIVES:

- To develop the reference circuits and low drop out regulators for desiredspecifications.
- To learn the concepts of regulators.
- To apply the concepts of oscillator circuits
- To understand the clock distribution circuits.
- To explain oscillator choice and requirements for clock generation circuits
- To design the clock generation and recovery in the context of high speedsystems

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, Performance Metrics, AC Design, Stability, Internal and External Compensation, PSRR – Internal and External compensation circuits.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise in Differential LC Oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLL Building blocks, Jitter and Phase Noise performance, DLL fundamentals.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

- Develop the reference circuits and low drop out regulators for desiredspecifications.
- Learn the concepts of regulators.
- Apply the oscillator circuits
- Understand the clock distribution circuits.
- Explain oscillator choice and requirements for clock generation circuits
- Design the clock generation and recovery in the context of high speedsystems.

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits", Johnwiley& Sons Inc, 2002.
2. Gabriel.A. Rincon-Mora, "Analog IC Design With Low-Dropout Regulators", McGraw-Hill Professional Pub, 2009.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
4. Floyd M. Gardner ,"Phase LocK Techniques" John wiley& Sons, Inc 2005.
5. Michiel Steyaert, Arthur H.M. van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-performance Amplifiers Power Management", springer, 2008.
6. BehzadRazavi, "Design of Integrated circuits for Optical Communications", McGraw Hill, 2003.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE012 SoC DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To understand the formulation of SoC based designs
- To explain the design and verification of Application Specific Instruction set Processors.
- To teach SoC based design approaches
- To categorize the low power SoC on electronic design with different methods.
- To teach low power SoC design approaches
- To Understand impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT I ASIC 9

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC , architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II NISC 9

NISC Control Words methodology, NISC Applications & Advantages, Architecture, Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modelling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III SIMULATION 9

Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV LOW POWER SOC DESIGN / DIGITAL SYSTEM 9

- Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V SYNTHESIS 9

- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph.Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power

consumption, Fault tolerant designs

TOTAL: 45 PERIODS

COURSE OUTCOMES:

- Explain the different design strategies & formulate a given problem in framework of SoC based design approaches
- Identify the design and verification of Application Specific Instruction set Processors.
- Identify the SoC design based system for engineering applications
- Demonstrate based on various simulation with different analyses.
- Summarize the low power SoC on electronic design with different methods.
- Identify impact of SoC on electronic design philosophy and Macro-electronics therebyincline towards entrepreneurship & skill development.

REFERENCES:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006.
3. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & DCenter, 2000.
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008.
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip", Wiley,2011.

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

Semester I

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE013 DATA CONVERTERS L T P C

3 0 0 3

OBJECTIVES:

- To learn A to D and D to A characteristic
- To demonstrate the concept of switched capacitor based circuits
- To apply the design of A/D and D/A converters
- To categorize different architecture based on the application
- To explain first order and second order sigma delta converters
- To classify various ADCs and DACs converters

UNITI INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

UNIT III NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues incurrent element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCs 9

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V SIGMA DELTA CONVERTERS 9

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

TOTAL : 45 PERIODS

COURSE OUTCOMES:

- Demonstrate the design calculations for developing the various blocks associatedwith a typical CMOS AD or DA converter.
- Explain circuits using switched capacitor concepts
- Ability to analyze and design D/A converters
- Distinguish different types of A/Ds
- Ability to analyze and design sigma delta converters
- Outline On-chip realization of AD and DA converters

REFERENCES:

1. Shanthi Pavan, Richard Schreier, Gabor C. Temes , "Understanding Delta-Sigma Data Converters", Willey –IEEE Press, 2nd Edition, 2017.
2. Behzad Razavi, "Principles of data conversion system design", IEEE press, 1995.
3. M. Pelgrom, "Analog-to-Digital Conversion", Springer, 2010.
4. Rudy van de Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-AnalogConverters" Kluwer Acedamic Publishers, Boston, 2003.
5. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing Principles, Algorithms and Applications", Prentice Hall, 4th Edition, 2006.
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

CO, PO, PSO Mapping

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

1 - Low, 2 - Medium, 3 - High, '-' - No Correlation

23MEVL104 PCB DESIGN AND FABRICATION 3H-3C

Instruction Hours/week: L: 3 T: 0 P: 0 **Marks:** Internal**:40** External**:60 T**otal**:100**

End Semester Exam: 3 Hours

22MEVLE014 ADVANCED DIGITAL SYSTEM DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To identify the design of synchronous sequential circuits
- To select various design technique for asynchronous sequential circuit and eliminate the hazards
- To illustrate the fault testing procedure for combinational circuits and PLA circuits
- To classify the various architectures of programmable devices
- To model the system using Verilog
- To design digital system based on the requirement

COURSE OUTCOMES:

At the end of the course the students will be able to

- Analyze and design synchronous sequential circuits
- Analyze hazards and design asynchronous sequential circuits
- Infer the testing procedure for combinational circuit and PLA
- Distinguish the various architectures of programmable devices
- Design digital circuits using Verilog
- Design and use programming tools for implementing digital circuits of industry standards

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit — flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit- Static, dynamic and essential hazards — mixed operating mode asynchronous circuits — designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method - D algorithm – Kohavi algorithm — Tolerance techniques — The compact algorithm — Fault in PLA — Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis –Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers — counters — sequential machine — serial adder — Multiplier- Divider — Design ofsimple microprocessor

TOTAL: 45

REFERENCES:

1. Charles H.RothJr "Fundamentals of Logic Design" Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001
5. ParagK.Lala "Fault Tolerant and Fault Testable Hardware Design" B S
6. Publications,2002
7. ParagK.Lala "Digital system Design using PLD" B S Publications,2003
8. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

9. **CO, PO, PSO Mapping**
10.

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO2	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO3	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO4	-	-	-	-	-	-	-	1	2	3	-	2	-	-
CO5	-	-	-	-	-	-	-	1	2	3	-	2	-	-
Average	-	-	-	-	-	-	-	1	2	3	-	2	-	-

11. **1 - Low, 2 - Medium, 3 - High, '-' - No Correlation**