KARPAGAM ACADEMY OF HIGHER EDUCATION
(Deemed to be University)
(Established Under Section 3 of UGC Act, 1956)
Pollachi Main Road, Eachanari Post, Coimbatore - 641 021, Tamil Nadu, India.
Phone: 0422 - 2980011- 14 | Fax: 0422 - 2980022 | Email : info@kahedu.edu.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REPORT

Program Name	FDP
Program Title	Two Days FDP on Analog and Digital Design Using CADENCE EDA Tools
Academic Year	2019-2020
Date & Time	**31-07-2019 & 01-08-2019 (9.00 am to 5.00 pm)**
Beneficiary Students	UG,PG, Research Scholars & Faculty
Resource Person Details	Mr.G.R.Mahendra Babu & Dr.K.G.Dharani, Dept of ECE , FoE, Karpagam Academy of Higher Education
Organized by	Mr.G.R.Mahendra Babu, & Dr.K.G.Dharani,
No of Participants	**35**

Department of ECE organized two days FDP on "Analog and Digital IC Design Using Cadence EDA Tools" on 31st July 2019 and 01st August 2019. 35 candidates participated including UG, PG & faculty members from in and around Coimbatore. It started with the welcome address by Dr. S.Bhavani, HoD/ECE and continued with the benefit of this workshop. Mr.G.R.Mahendra Babu & Dr.K.G.Dharani, Dept of ECE were the resource persons who delivered the session on the topic "Analog and Digital IC Design Using Cadence EDA Tools" which was very useful to the participants.

On day 1 Analog IC development flow is explained by Dr.K.G.Dharani. Particularly analog design flow, inverter design, power, area calculation, layout and DRC, LVS using cadence tools are explained. Hands on training are provided to the participants to explore the cadence tools.

On day 2 Digital IC development flow is explained by Mr.G.R.Mahendra Babu. Particularly digital logic design, verilog programming and synthesis using cadence tools are explained. Hands on training are provided to the participants to explore the cadence tools. The participants were getting interested in using the cadence tools.

Finally, the workshop concluded with a vote of thanks rendered by Dr. S.Bhavani, HoD/ECE and participant certificates were issued to the participants.

.

REGISTRATION FORM

Two Days FDP
On
"ANALOG AND DIGITAL DESIGN USING CADENCE EDA TOOLS"
31st July 2019 & 01st August 2019

Organized By
Department of Electronics &Communication Engineering
Karpagam Academy of Higher Education
Coimbatore-641 021, Tamil Nadu.

Name :
Designation :
Phone No :
Mail ID :
Amount :
Institution :
Address :

Signature of the participant

This is to certify that_____ _____is regular faculty of our Institution and is hereby permitted for attending two days FDP on "**ANALOG AND DIGITAL DESIGN USING CADENCE EDA TOOLS"** at Karpagam Academy of Higher Education, Coimbatore on 31st July, 2019 & 01st August, 2019.

Head of the Institution with seal

ORGANIZING COMMITTEE

Chief Patron

Dr.S.Sudalaimuthu
Vice Chancellor
Karpagam Academy of Higher Education

Patron

Dr.R.Sundararajan
Registrar
Karpagam Academy of Higher Education

Convenors

Dr.G. K. D.Prasanna Venkatesan
Dean
Faculty of Engineering
Karpagam Academy of Higher Education

Dr.S.Bhavani
Head of the Department
Department of Electronics and communication Engg
Faculty of Engineering
Karpagam Academy of Higher Education

Organizing Secretaries

Mr.G.R.Mahendra Babu, M.E & Dr.K.G.Dharani
Department of Electronics& Communication Engg
Faculty of Engineering
Karpagam Academy of Higher Education
Mail: *mahendrababu.gr@kahedu.edu.in*
Contact No: +91 **9965539275, +91 7795614984**

KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University)

Established Under Section 3 of UGC Act, 1956

Enable | Enlighten | Enrich
KARPAGAM
ACADEMY OF HIGHER EDUCATION
(Deemed to be University)
(Established Under Section 3 of UGC Act, 1956)

Two Days FDP
On
"ANALOG AND DIGITAL DESIGN USING CADENCE EDA TOOLS"
On
31st July, 2019 & 01st August 2019

Organized By

Department of Electronics& Communication Engg

Faculty of Engineering

Karpagam Academy of Higher Education

Coimbatore-641 021

Tamil Nadu, India

ABOUT THE INSTITUTION

Karpagam Academy of Higher Education (KAHE) established under Section 3 of UGC Act, 1956 is approved by Ministry of Human Resource and Development, Government of India. Dr. R. Vasanthakumar, the President of the Trust, a Philanthropist, Industrialist, Entrepreneur and Culture Promoter.

Contemporary infrastructure, modern teaching methodologies, career oriented training, excellent placements and the finest faculty have always been Karpagam's hallmark. Besides technical expertise, the Institution has made a mark for itself, since its inception by developing communication and soft skills, ensuring enlightening knowledge, extending holistic education and creating a strong value system.

ABOUT THE DEPARTMENT

Communication systems are transforming the way the world functions today. Innovations in networking are bringing the world together like never before. The field of Electronics and Communication is at forefront of exciting new possibilities.

In the faculty of Engineering, the dept of ECE is well geared to tune our students to the technologies revolution in this engineering discipline. Advance Devices and software's are available to enhance the practical knowledge of the student and that do develop research skills in the above field.

CADENCE EDA TOOLS

Chip design in India is poised to move into the big league with multinational, design service companies product companies, startups in the country grow day by day.

Senior semiconductor executives, Trade bodies such as NASSCOM see this as sunrises Industry and state that the only impediment is potential shortfall of the quality VLSI trained talent. Hence this FDP strives to build the manpower pool, with the main aim of producing India a VLSI Design power house in the global semiconductor design and development world. Cadence is committed to helping its customers by providing them with a pool of engineers experienced in EDA tools usage and methodologies.

OBJECTIVE OF THE FDP

Two days FDP on "ANALOG AND DIGITAL DESIGN USING CADENCE EDA TOOL" focuses on the design of Analog circuits & Digital circuits. It's a refresher course intended to faculty interested in VLSI circuit design & helpful to them in their academics. The course is hands on based using industry standard CADENCE tool.

TOPICS TO BE COVERED

- VLSI Design Flow(Analog & Digital)
- Digital Circuit design using cadence IES
- Synthesis using RTL compiler
- Analog Circuit design using cadence virtuoso tool
- Design & Simulation

RESOURSE PERSONS:

Mr.G.R.Mahendra Babu, AP / ECE / FoE
Karpagam Academy of Higher Education.

Dr.K.G.Dharani, Assoc.Professor / ECE / FoE
Karpagam Academy of Higher Education.

REGISTRATION DETAILS

- **No Registration Fee**

Please send the scanned copy of filled in registration form to the below mentioned address. Spot registration is subjected to availability of seats.

Intimation of acceptance by mail is on or before 30th July 2019.

Refreshment will be provided.

IMPORTANT DATES:

- Last date of Registration :29.07.19
- Intimation of confirmation:30.07.19
- Duration of program:31.07.19 & 01.08.19

ADDRESS FOR COMMUNICATION:

Dr.S.Bhavani, HOD/ECE,

Faculty of Engineering,

Karpagam Academy of Higher Education,

Pollachi Main Road,

Eachnari post,

coimbatore.641021,

Tamilnadu,INDIA.

Mobile No: +91 9942567658

FDP PHOTO

Session delivered by Dr.K.G.Dharani