Semester-IV

18BEEC402 **ANALOG CIRCUITS** **3H-3C**

Instruction Hours/week: L:3 T:0 P:0 **Marks:** Internal:**40** External:**60** Total:**100**

End Semester Exam:3 Hours

Course Objectives

- To learn various biasing arrangements for BJT and FET
- To know about various high frequency models for BJT
- To learn various feedback configurations
- To study Op-amp configurations with its applications
- Design simple circuits using OPAMPs
- Gain knowledge on Data converters

Course Outcomes

At the end of this course students will demonstrate the ability to

- Understand the characteristics of transistors.
- Design and analyze high frequency models
- Design sinusoidal and non-sinusoidal oscillators
- Understand the functioning of OP-AMP and design OP-AMP based circuits.
- Design ADC and DAC

UNIT IBIASING CIRCUITS AND SMALL SIGNAL MODELS

Voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier. Biasing schemes for BJT and FET amplifiers, bias stability, various configurations (such as CE/CS, CB/CG, CC/CD) and their features, small signal analysis, low frequency transistor models, estimation of voltage gain, input resistance, output resistance etc., design procedure for particular specifications, low frequency analysis of multistage amplifiers.

UNIT II HIGH FREQUENCY MODELS

High frequency transistor models, frequency response of single stage and multistage amplifiers, cascode amplifier. Various classes of operation (Class A, B, AB, C etc.), their power efficiency and linearity issues.

UNIT III FEEDBACK AND OSCILLATOR CIRCUITS

Feedback topologies: Voltage series, current series, voltage shunt, current shunt,
effect of feedback on gain, bandwidth etc., calculation with practical circuits, concept of stability, gain margin and phase margin. Review of the basic concept, Barkhausen criterion, RC

oscillators(phase shift, Wien bridge etc.), LC oscillators (Hartley, Colpitt, Clapp etc.), non-sinusoidal oscillators. Current

mirror: Basic topology and its variants, V-I characteristics, output resistance and minimum sustainable voltage (VON), maximum usable load.

UNIT IV OP-AMP AND ITS APPLICATIONS

Differential amplifier: Basic structure and principle of operation, calculation of differential gain, common mode gain, CMRR and ICMR. OPAMP design: design of differential amplifier for a given specification, design of gain stages and output stages, compensation. review of inverting and non-inverting amplifiers, integrator and differentiator, summing amplifier, precision rectifier, Schmitt trigger and its applications. Active filters: Low pass, high pass, band pass and band stop, design guidelines.

UNIT V DATA CONVERTORS

Digital-to-analog converters (DAC): Weighted resistor, R-2R ladder, resistorstring etc. Analog-todigital converters (ADC): Single slope, dual slope, successive approximation, flash etc. Switched capacitor circuits: Basic concept, practical configurations, application in amplifier, integrator, ADC etc.

Suggested Readings

1. J.V. Wait, L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory and applications, McGraw Hill, 1992.
2. J. Millman and A. Grabel, Microelectronics, 2nd edition, McGraw Hill, 1988.
3. P. Horowitz and W. Hill, The Art of Electronics, 2nd edition, Cambridge University Press,1989.
4. A.S. Sedra and K.C. Smith, Microelectronic Circuits, Saunder's College11 Publishing, Edition IV
5. Paul R. Gray and Robert G.Meyer, Analysis and Design of Analog Integrated Circuits, John
   Wiley, 3rd Edition

KARPAGAM ACADEMY OF HIGHER EDUCATION

COIMBATORE-21.

Faculty of Engineering

Department of Electronics and Communication Engineering

LESSON PLAN

NAME OF THE STAFF: G.R. MAHENDRA BABU

DESIGNATION : ASSISTANT PROFESSOR

CLASS : B.E-II YEAR ECE

SUBJECT : ANALOG CIRCUITS

SUBJECT CODE : 18BEEC402

S.No.	TOPICS TO BE COVERED	TIME DURATION	TEACHING AIDS
	UNIT-I BIASING CIRCUITS AND SMALL SIGNAL MODELS		
1	Introduction	2	
2	Voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier	1	T6-Pg.No: 180-188
3	Biasing schemes for BJT and FET amplifiers	1	T6-Pg.No: 188-213
4	bias stability	1	T6-Pg.No: 385-395 & 218-223
5	various configurations (such as CE/CS, CB/CG, CC/CD) and their features	2	T6-Pg.No: 243-246
6	small signal analysis	1	T6-Pg.No: 246-253
7	low frequency transistor models, estimation of voltage gain, input resistance, output resistance	1	T6-Pg.No: 436-439
8	design procedure for particular specifications	1	T6-Pg.No: 435-452
9	low frequency analysis of multistage amplifiers	1	
10	Tutorial	1	
	Total (Theory + Tutorial)	**12 Hrs (11+1)**	
	UNIT II HIGH FREQUENCY MODELS		
1	High frequency transistor models	1	T6-Pg.No: 435-452
2	frequency response of single stage and multistage amplifiers	2	T6-Pg.No: 373-398
3	Cascode amplifier	1	
4	Class A amplifier & power efficiency	1	T6-Pg.No: 466-485
5	Class B amplifier & power efficiency	1	
6	Class AB amplifier & power efficiency	1	
7	Class C amplifier & power efficiency	1	
8	Linearity issues	1	
9	Tutorial		
	Total (Theory + Tutorial)	**11 Hrs (9+2)**	
	UNIT III FEEDBACK AND OSCILLATOR CIRCUITS		
1	Feedback circuits: concept of feedback	1	T6-Pg.No: 544-551 & T2-560-566
2	Effects of negative feedback	1	T6-Pg.No: 581-586 & T2-569-570
3	Types of negative feedback topologies	1	T6-Pg.No: 570-588

4	Tutorial	1	
5	Oscillator circuits: oscillator principles	1	T6-Pg.No: 665
6	LC oscillators	1	T6-Pg.No: 670-678
7	RC oscillators	1	T6-Pg.No: 678-6814 & 666-670
8	crystal oscillators	1	T6-Pg.No: 701-706
9	Tutorial	1	
	Total (Theory + Tutorial)	**11 Hrs (9+2)**	
UNIT IV OP-AMP AND ITS APPLICATIONS			
1	Differential amplifier: Basic structure and principle of operation	1	T6-Pg.No: 820-865
2	calculation of differential gain, common mode gain, CMRR and ICMR	1	
3	OPAMP design: design of differential amplifier for a given specification	1	
4	design of gain stages and output stages, compensation	1	
5	review of inverting and non-inverting amplifiers	1	
6	integrator and differentiator	1	
7	summing amplifier, precision rectifier	1	
8	Schmitt trigger and its applications	1	
9	Active filters: Low pass, high pass, band pass and band stop-design guidelines	1	
10	Tutorial	1	
	Total (Theory + Tutorial)	**11 Hrs (9+2)**	
UNIT V DATA CONVERTORS			
1	Digital-to-analog converters (DAC): Weighted resistor	1	T6-Pg.No: 820-865
2	R-2R ladder	1	
3	resistor string	1	
4	Analog-todigital converters (ADC)	1	
5	Single slope	1	
6	dual slope	1	
7	successive approximation, flash	1	
8	Switched capacitor circuits: Basic concept, practical configurations	1	
9	application in amplifier, integrator, ADC	1	
10	Tutorial	1	
	Total (Theory + Tutorial)	**11 Hrs (9+2)**	

Total Lecture: 58 Hours (48+10)

Suggested Readings

1. J.V. Wait, L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory
   and applications, McGraw Hill, 1992.
2. J. Millman and A. Grabel, Microelectronics, 2nd edition, McGraw Hill, 1988.
3. P. Horowitz and W. Hill, The Art of Electronics, 2nd edition, Cambridge University Press,1989.
4. A.S. Sedra and K.C. Smith, Microelectronic Circuits, Saunder's College11 Publishing, Edition IV

5. Paul R. Gray and Robert G.Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley, 3rd Edition
6. S.Salivahanan, N.Suresh Kumar, “Electronic Devices and Circuits”, 3rd edition, 2014.

FACULTY IN-CHARGE **HOD/ECE**

ANALOG CIRCUITS

Presented By,
G.R.Mahendra Babu,
Assistant Professor,
Dept of ECE / FoE / KAHE.

BJT BIASING CIRCUIT

Introduction – Biasing

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal The analysis or design of any electronic amplifier therefore has two components:

- The dc portion

and

- The ac

portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

What is biasing circuit?

Biasing: Application of dc voltages to establish a fixed level of current and voltage.

Purpose of the DC biasing circuit

- To turn the device "ON"
- To place it in operation in the region of its characteristic where the device operates most linearly .
- Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
- Improper biasing cause Improper biasing cause
  - „ Distortion in the output signal
  - „ Produce limited or clipped at output signal

Important basic relationship

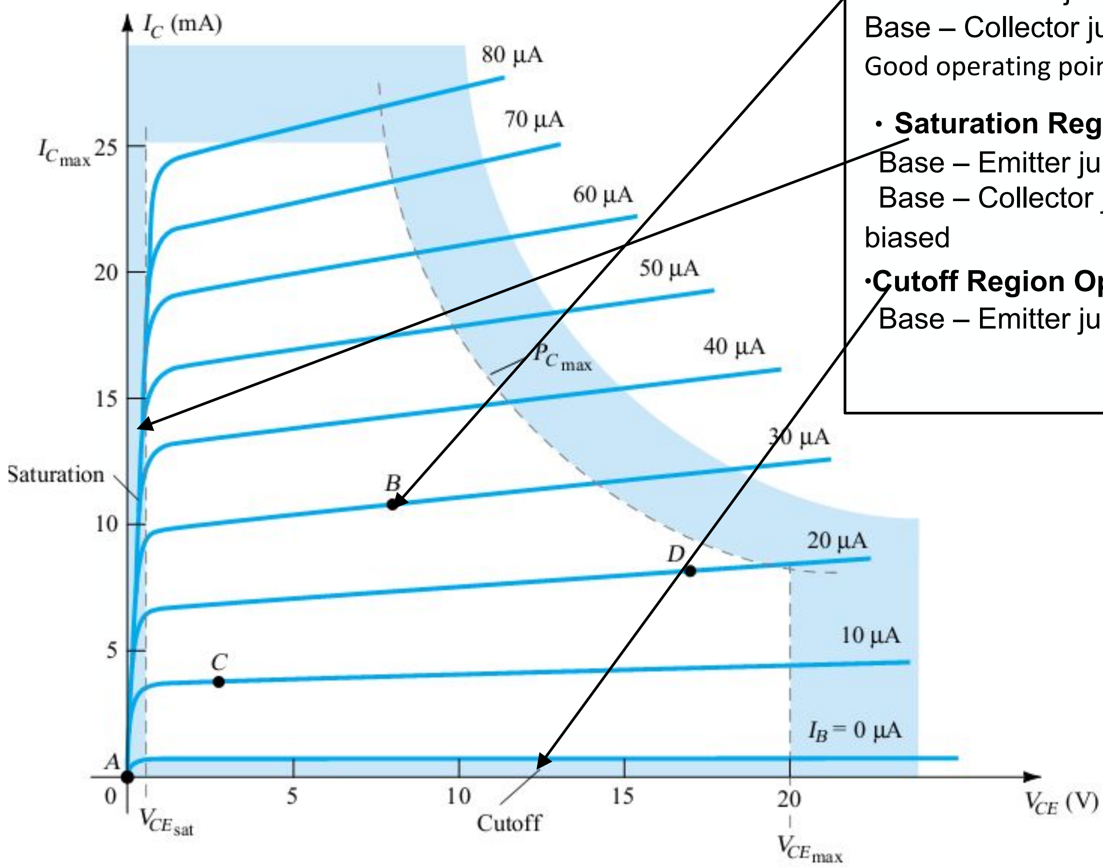
$$I_E = I_C + I_B$$

$$\beta = \frac{I_C}{I_B}$$

$$I_E = (\beta + 1) I_B \cong I_C$$

$$V_{CB} = V_{CE} - V_{BE}$$

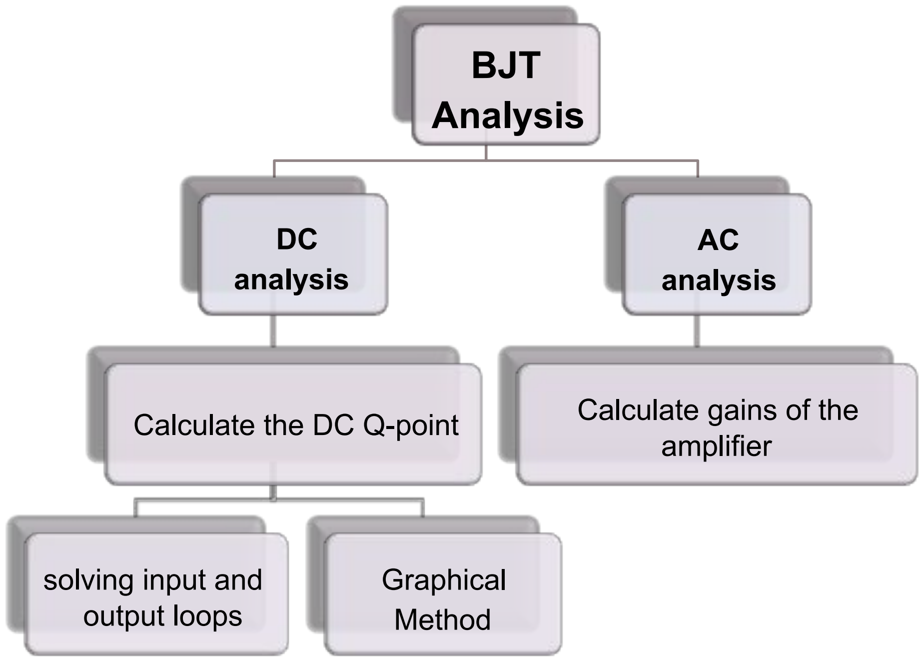
Operating Point



·Active or Linear Region Operation
Base – Emitter junction is forward biased
Base – Collector junction is reverse biased
Good operating point

- **Saturation Region Operation**
  Base – Emitter junction is forward biased
  Base – Collector junction is forward biased

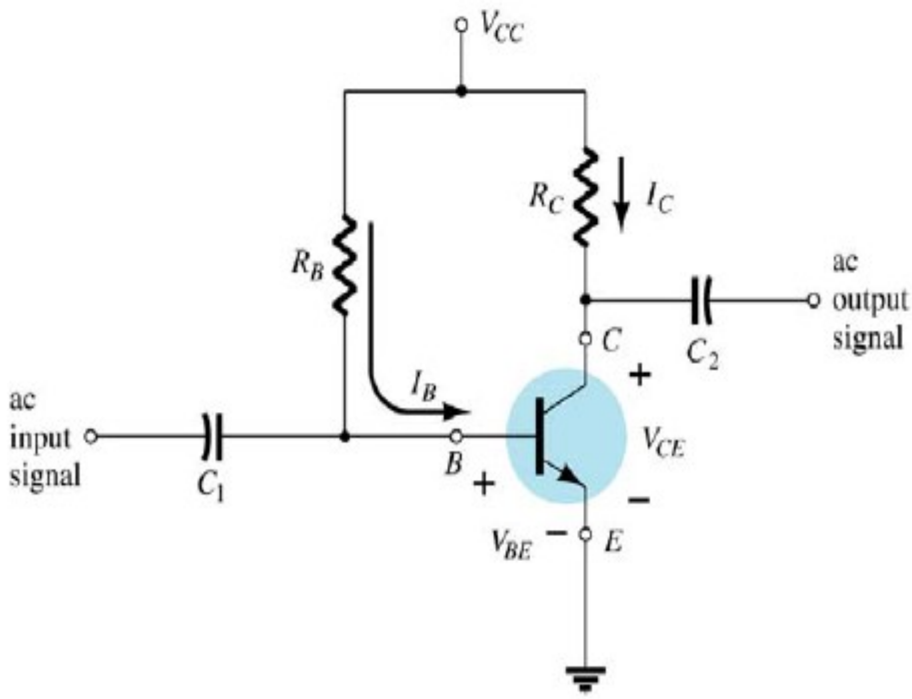
·Cutoff Region Operation
Base – Emitter junction is reverse biased



DC Biasing Circuits

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

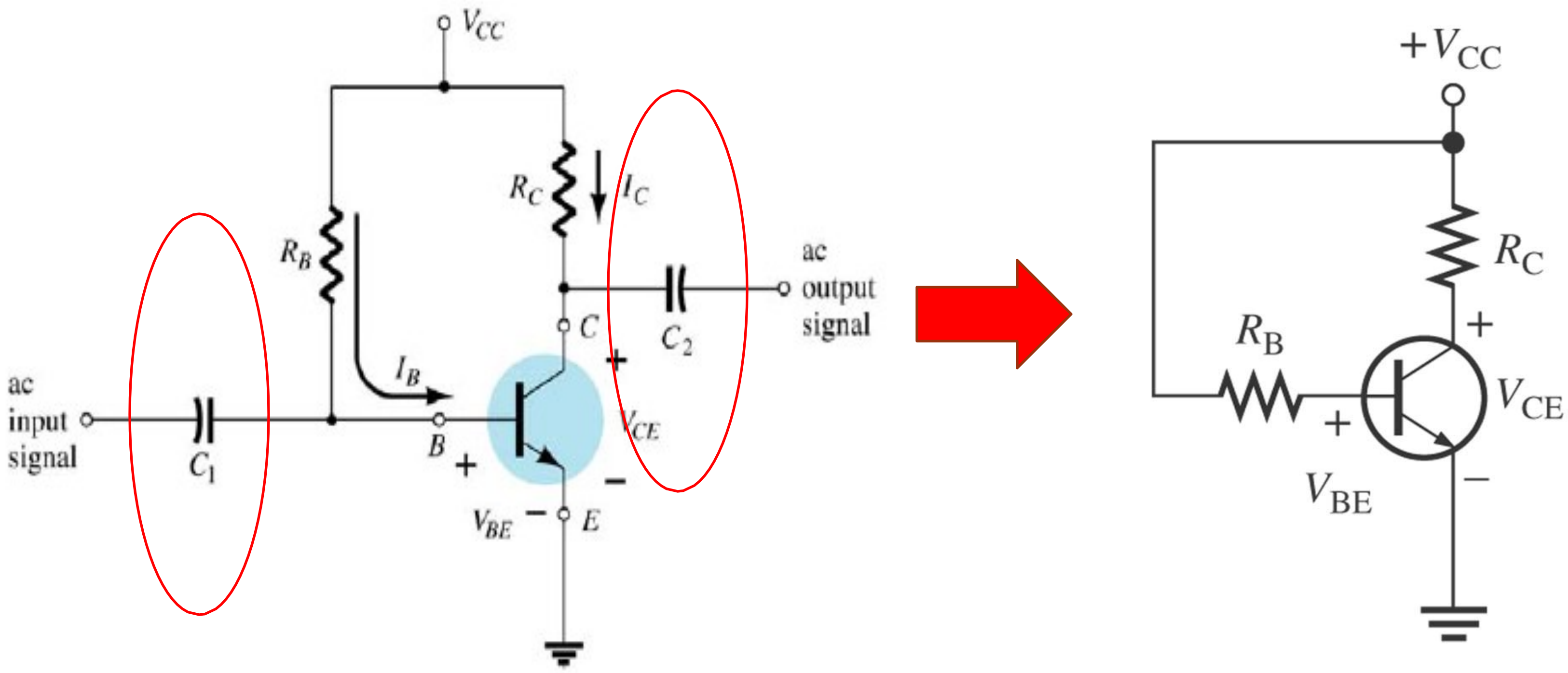
FIXED BIAS CIRCUIT



- This is common emitter (CE) configuration
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop (input loop)
  - CE loop(output loop)

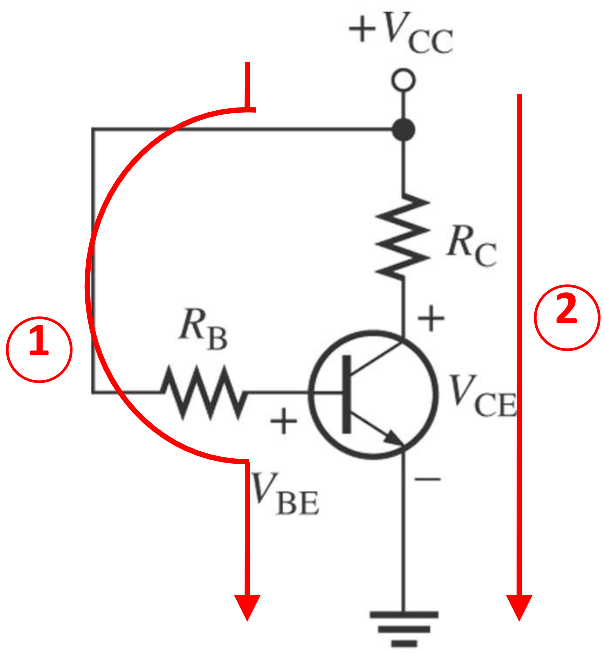
FIXED BIAS CIRCUIT

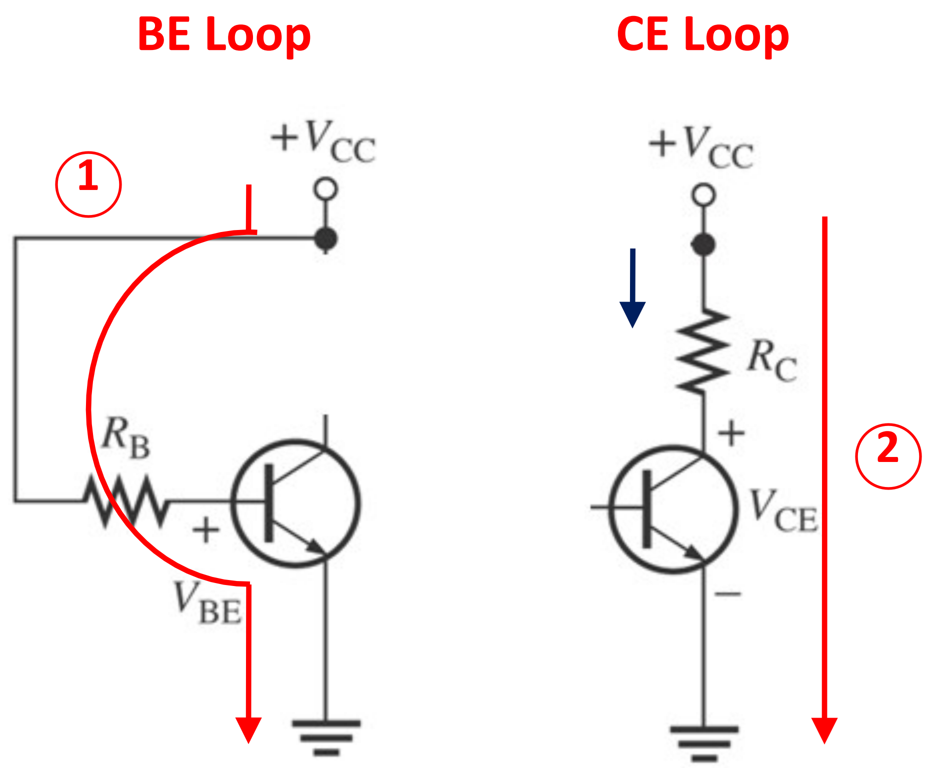
- 1_{st} step: Locate capacitors and replace them with an open circuit



FIXED BIAS CIRCUIT

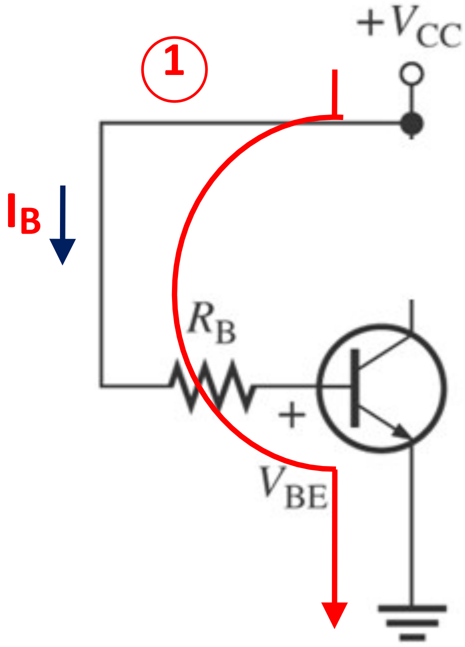
- 2nd step: Locate 2 main loops.





FIXED BIAS CIRCUIT

- BE Loop Analysis



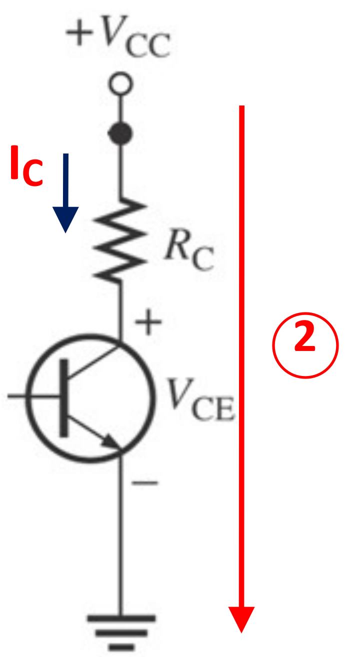
- From KVL;

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad \text{A}$$

FIXED BIAS CIRCUIT

- CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

- As we known;

$$I_C = \beta I_B \quad \text{B}$$

- Substituting A with B

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

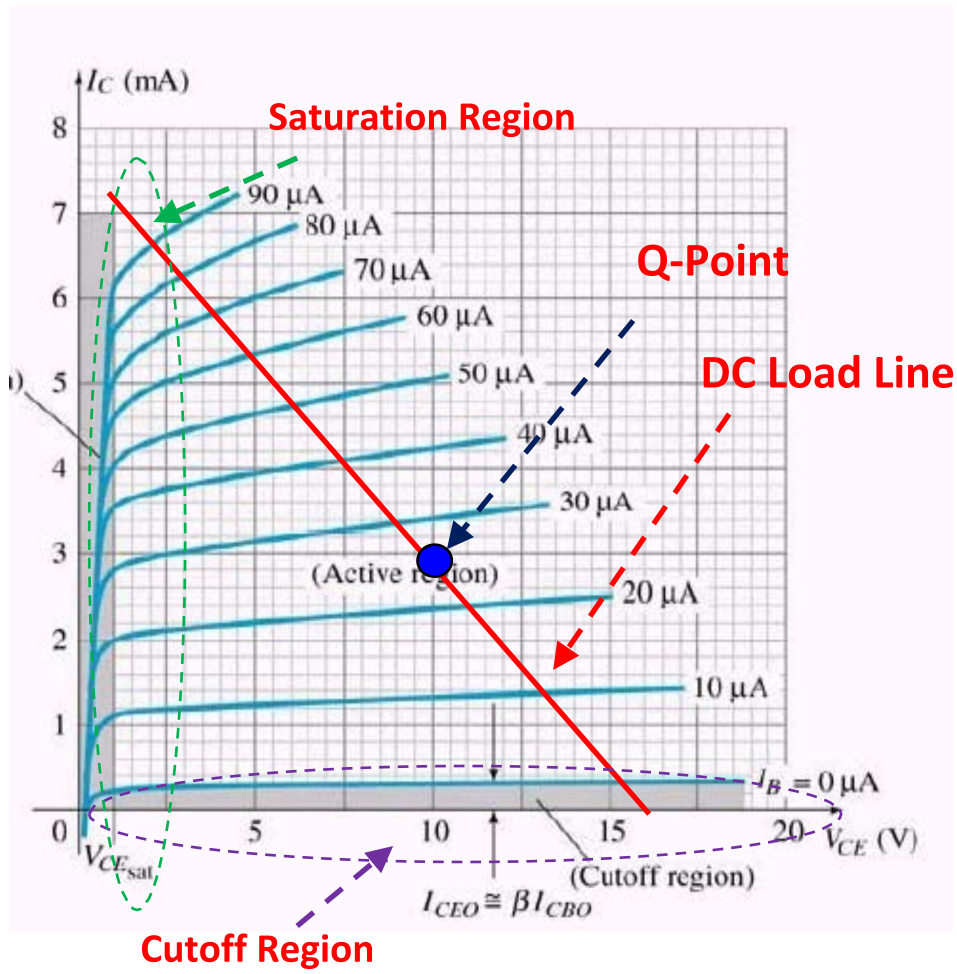
Note that R_C does not affect the value of Ic

FIXED BIAS CIRCUIT

- **DISADVANTAGE**
  - Unstable – because it is too dependent on β and produce width change of Q-point
  - For improved bias stability , add emitter resistor to dc bias.

Load line analysis

- A fixed bias circuit with given values of V_{CC}, R_C and R_B can be analyzed (means, determining the values of I_{BQ}, I_{CQ} and V_{CEQ}) using the concept of load line also.
- Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output lo[redacted]p KVL equation are made use of.



- Plot load line equation

$$V_{CE} = V_{CC} - I_C R_C$$

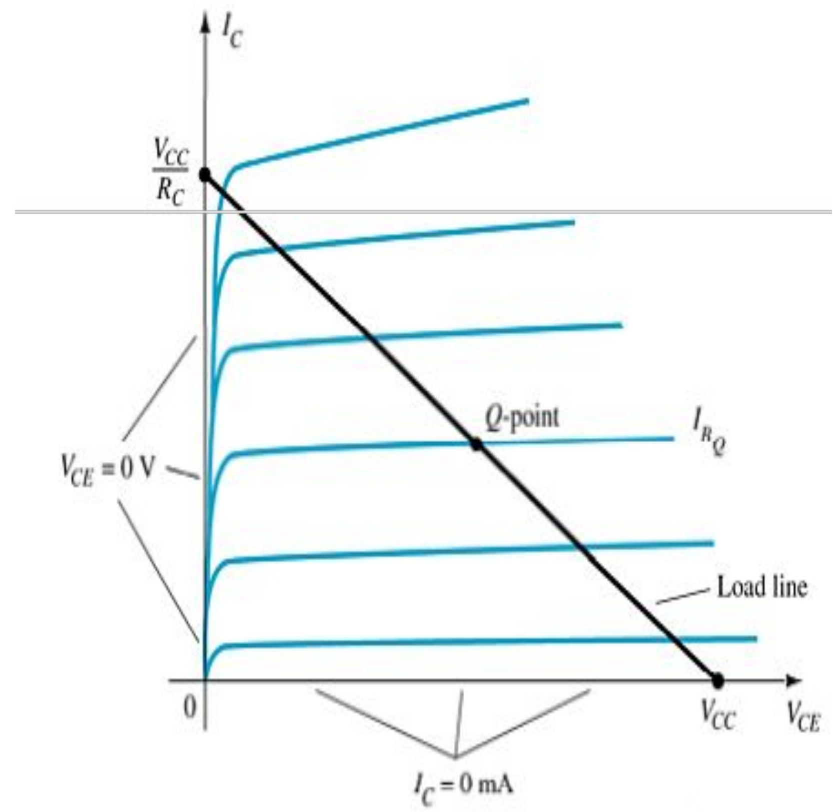
- $I_{C(sat)}$ occurs when transistor operating in *saturation region*

$I_{C(sat)}$ occurs when tra

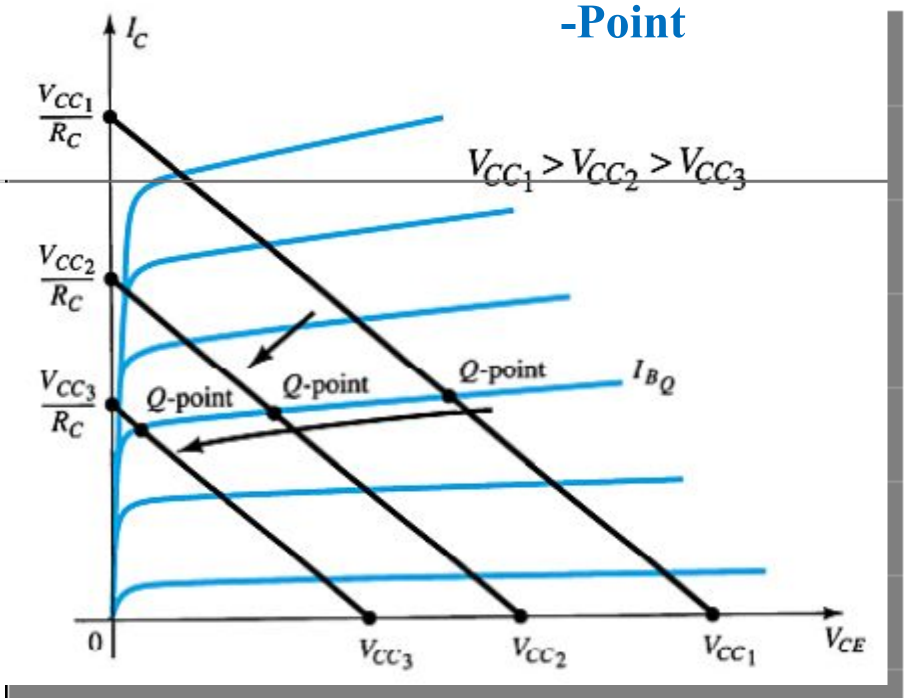
$$I_{C_{sat}} = \frac{V_{CC}}{R_C}\Big|_{V_{CE}=0}$$

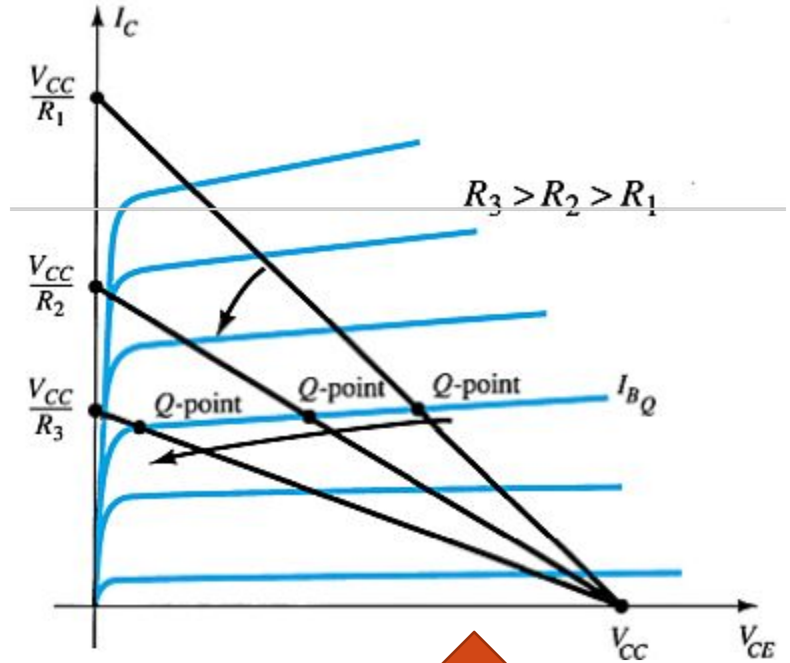
- $V_{CE(off)}$ occurs when transistor operating in *cut-off region*

$$V_{CE_{(off)}} = V_{CC} - I_C R_C\Big|_{I_C=0}$$



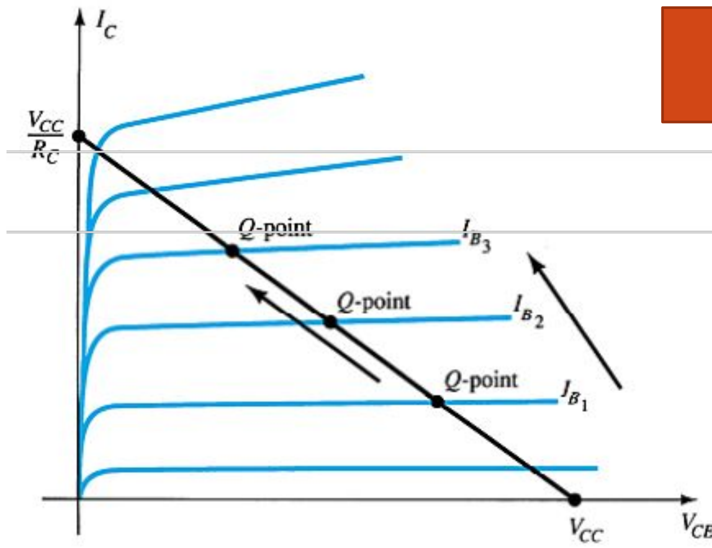
Circuit Values Affect the Q-Point





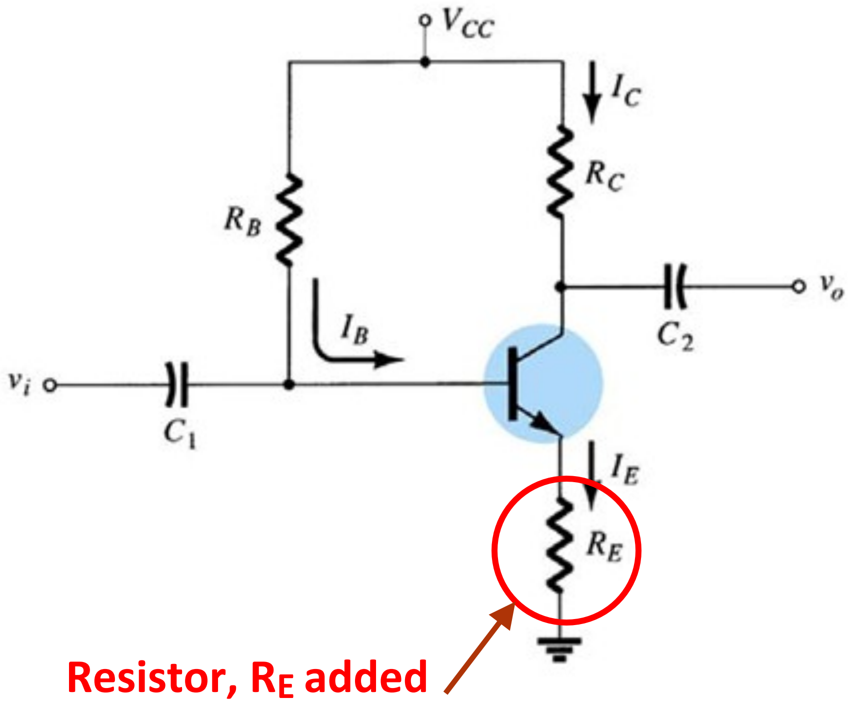
Increasing Rc

Decreasing Vcc



Varying Ib

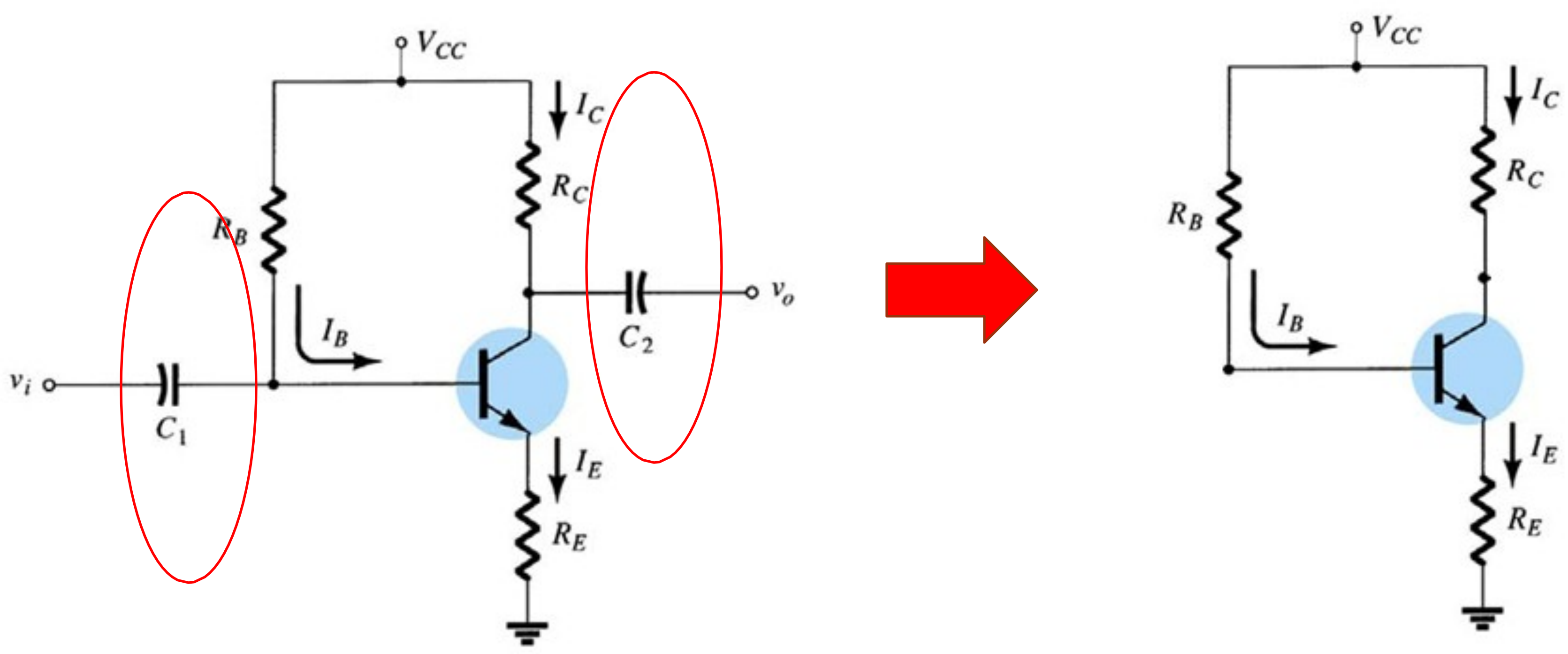
EMITTER-STABILIZED BIAS CIRCUIT



- An emitter resistor, R_E is added to improve stability
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop
  - CE loop

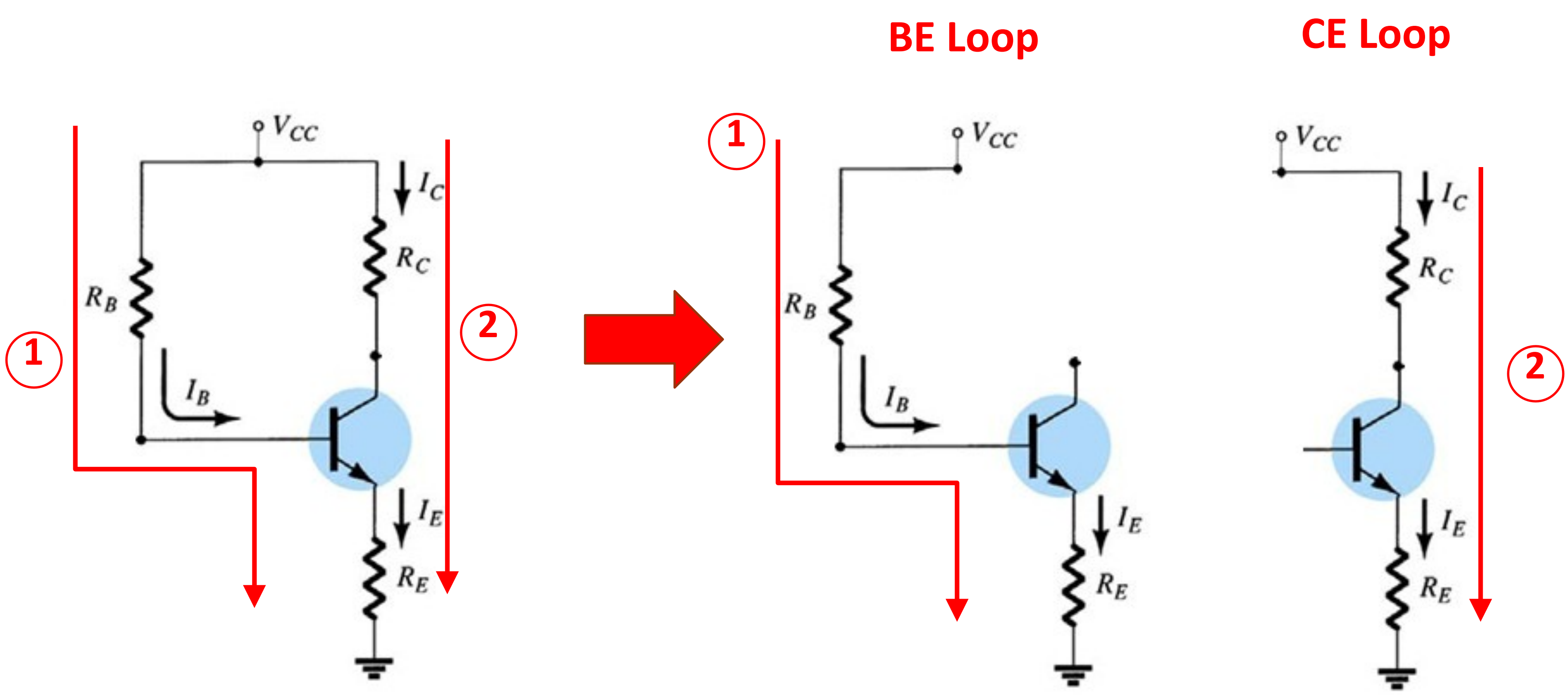
EMITTER-STABILIZED BIAS CIRCUIT

- 1_{st} step: Locate capacitors and replace them with an open circuit



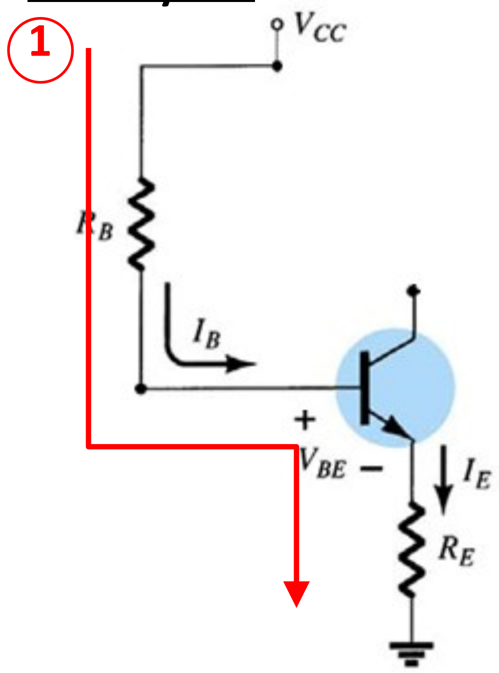
EMITTER-STABILIZED BIAS CIRCUIT

- 2_{nd} step: Locate 2 main loops.



EMITTER-STABILIZED BIAS CIRCUIT

- <u>BE Loop Analysis</u>



- From kvl;

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta + 1) I_B$

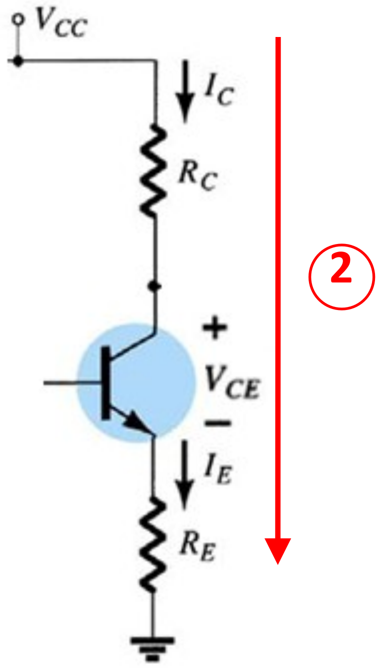
Substitute for I_E

$$-V_{CC} + I_B R_B + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

EMITTER-STABILIZED BIAS CIRCUIT

- CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

Without Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \beta$$

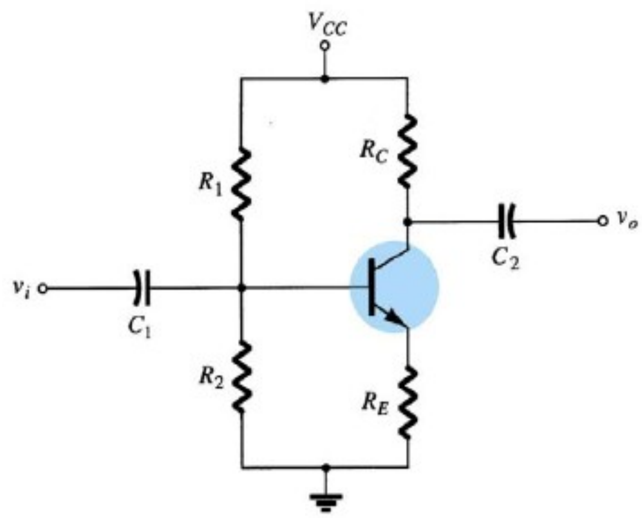
With Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \right) \beta$$

Note :it seems that beta in numerator canceled with beta in denominator

VOLTAGE DIVIDER BIAS CIRCUIT

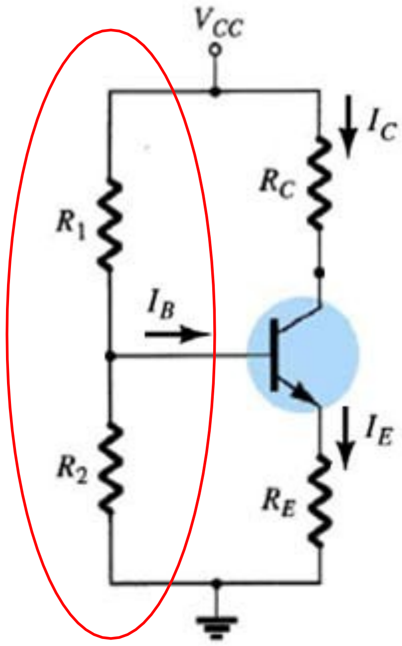
- Provides good Q-point stability with a single polarity supply voltage
- This is the biasing circuit wherein, ICQ and VCEQ are almost independent of beta.
- The level of IBQ will change with beta so as to maintain the values of ICQ and VCE
- Two methods of analyzing a voltage divider bias circuit are:
  - Exact method : can be applied to any voltage divider circuit
  - Approximate method : direct method, saves time and energy,
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Simplified circuit using Thevenin Theorem
- 3rd step: Locate 2 main loops which;
  - BE loop
  - CE loop



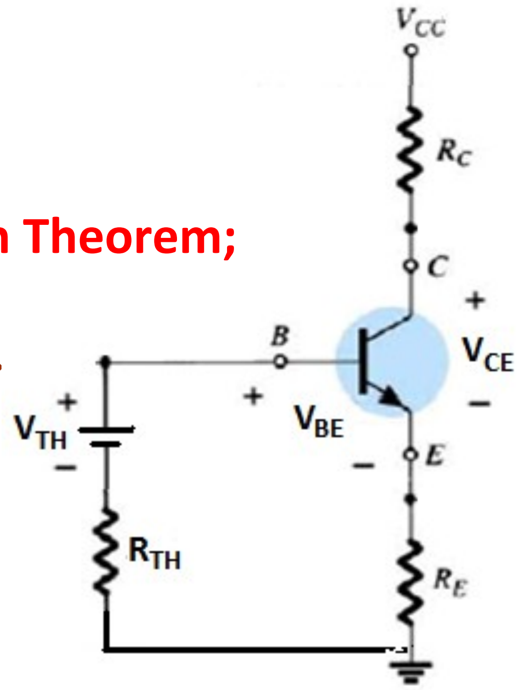
VOLTAGE DIVIDER BIAS CIRCUIT

Thevenin Theorem

<u>2nd step</u>: : Simplified circuit using



Thevenin Theorem;



Simplified Circuit

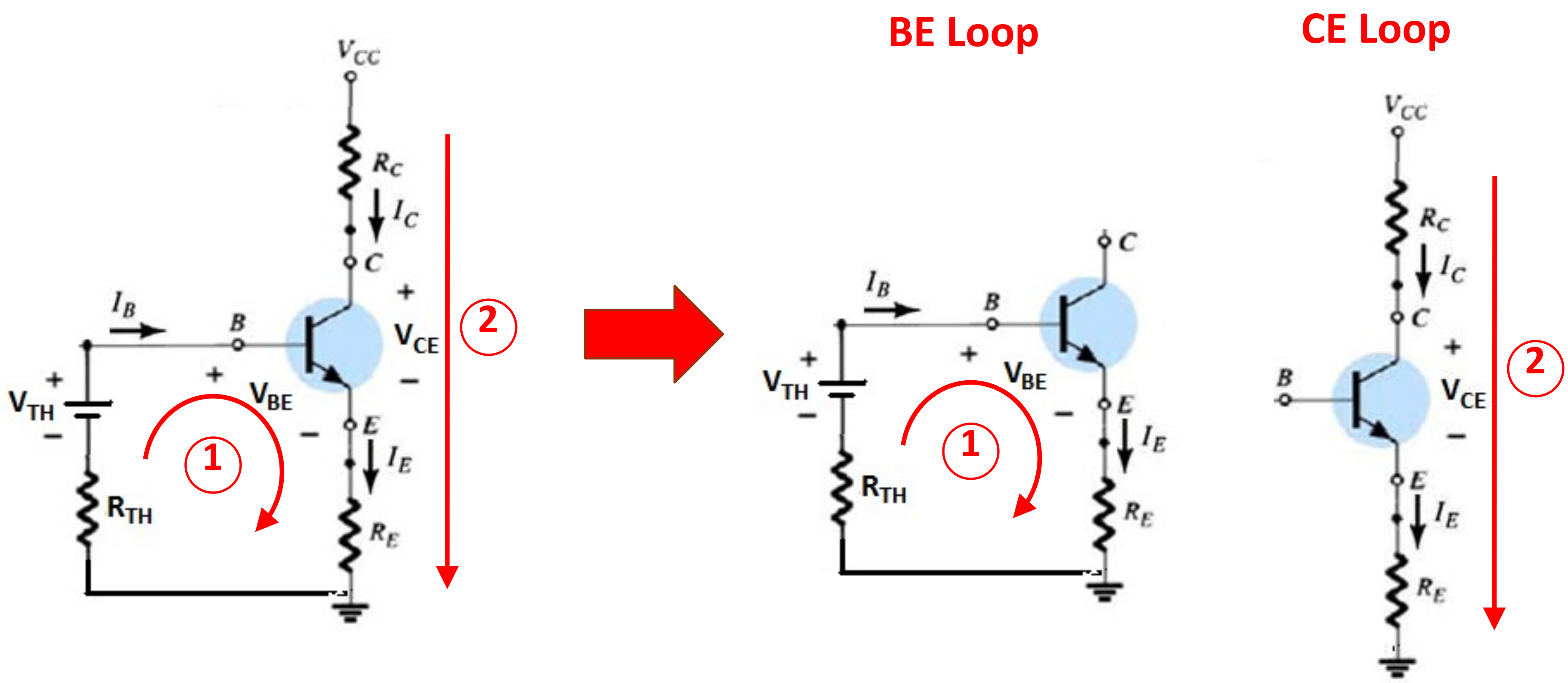
From Thevenin Theorem;

$$R_{TH} = R_1 \,//\, R_2 = \frac{\text{[redacted]}_1 \times R_2}{\text{[redacted]}_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2}\,\text{[redacted]}_{CC}$$

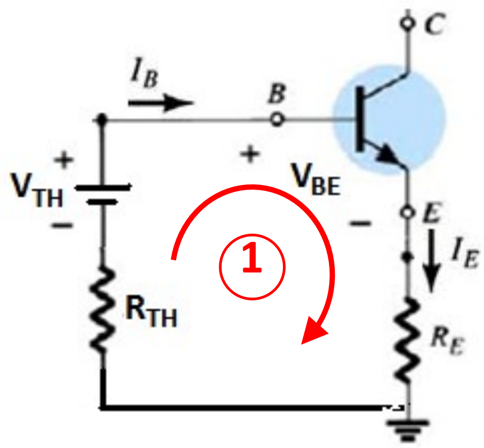
VOLTAGE DIVIDER BIAS CIRCUIT

- 2_{nd} step: Locate 2 main loops.



VOLTAGE DIVIDER BIAS CIRCUIT

- <u>BE Loop Analysis</u>



- From KVL;

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta + 1)I_B$

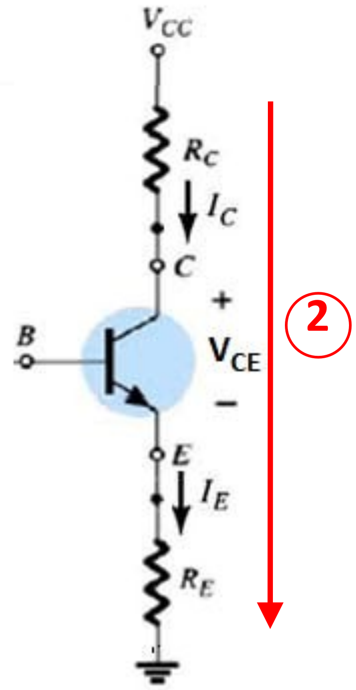
Substitute for I_E

$$-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1)I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

VOLTAGE DIVIDER CIRCUIT BIAS

- CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

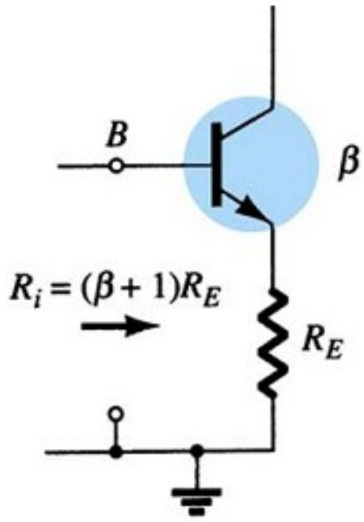
- Assume;

$$I_E \cong I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Approximate analysis:



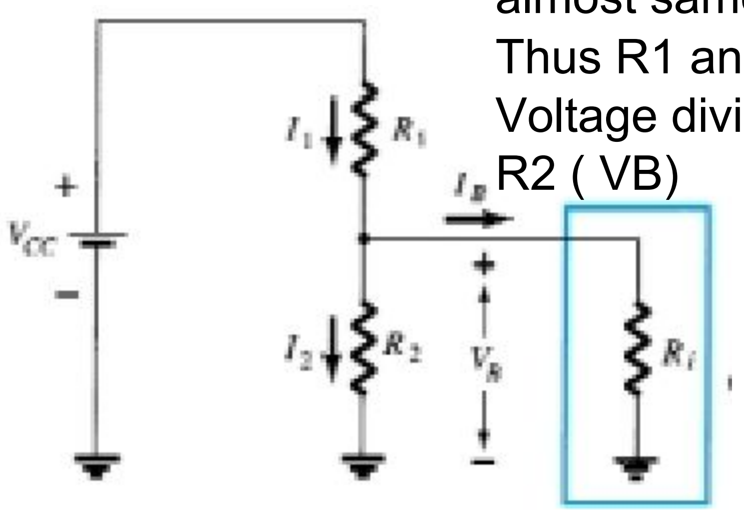
$$R_i \gg R_2 \rightarrow I_{R2} \gg I_b$$

$$(\beta + 1)R_E \gg R_2$$

$$\Rightarrow \boxed{\beta R_E > 10R_2}$$

❑If this condition applied then you can use approximation method .

❑This makes IB to be negligible. Thus I1 through R1 is almost same as the current I2 through R2.
Thus R1 and R2 can be considered as in series.
Voltage divider can be applied to find the voltage across R2 (VB)



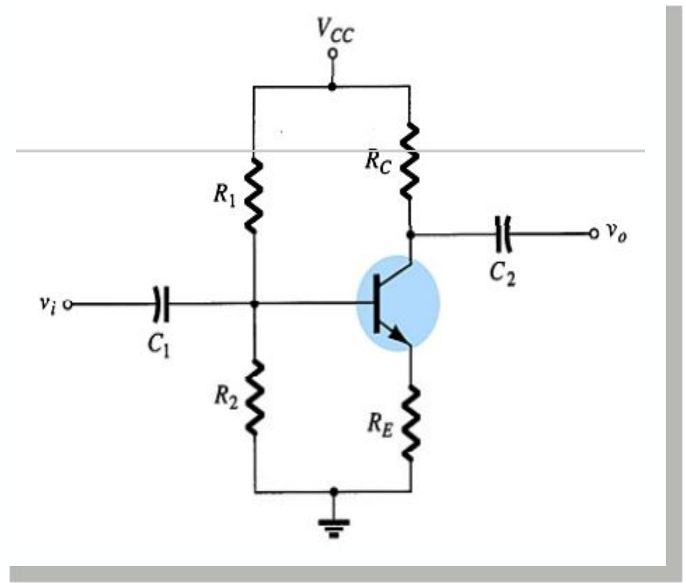
Approximate Analysis

When $\beta R_E > 10R_2$, Then $I_B \ll I_2$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_E}{R_E}$$



From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

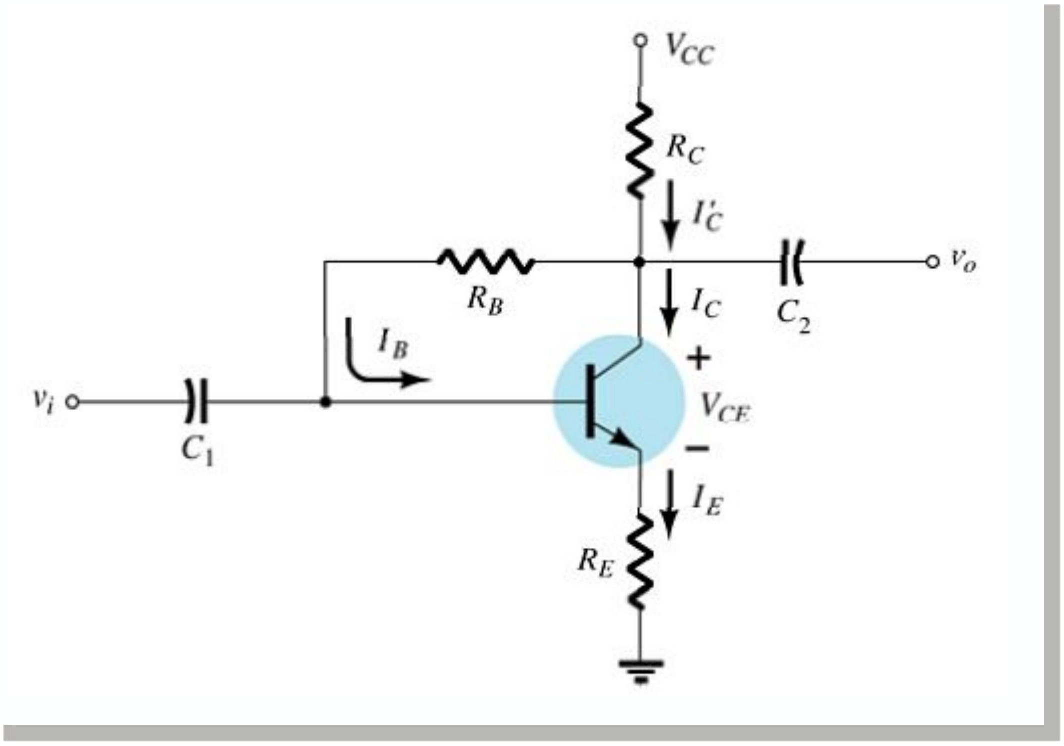
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

This is a very stable bias circuit. The currents and voltages are nearly independent of any variations in β.

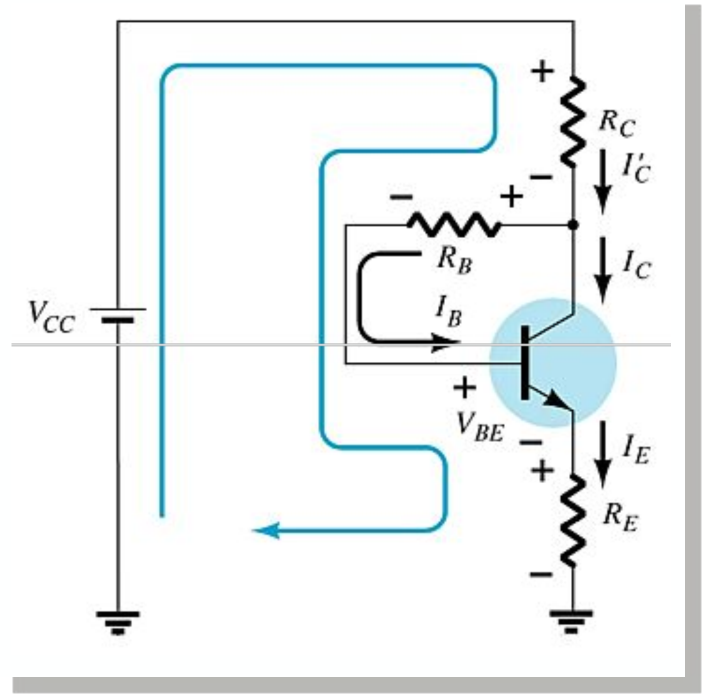
DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop



From Kirchhoff's voltage law:

$$-V_{CC} + I'_C R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

Where $I_B \ll I_C$:

$$I'_C = I_C + I_B \cong I_C$$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

Collector-Emitter Loop

Applying Kirchoff's voltage law:

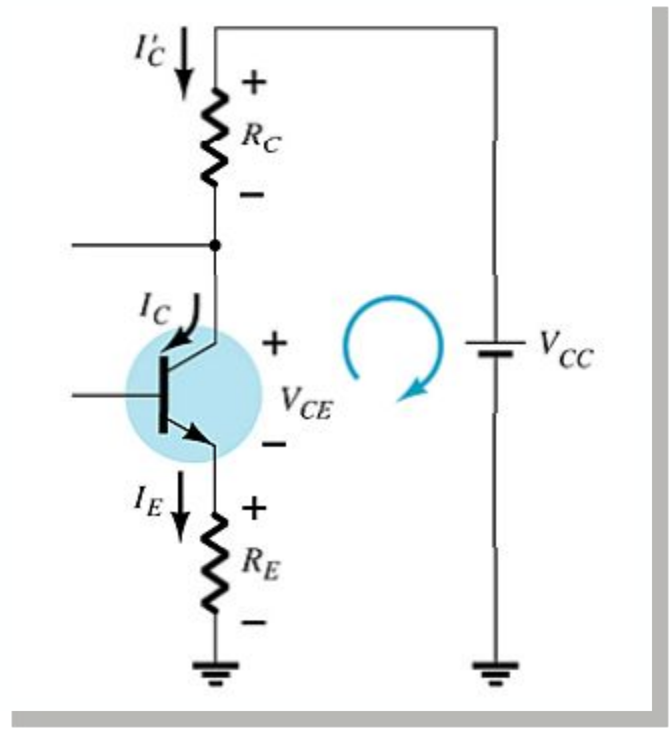
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



4- If the initial assumption is proven incorrect, then a new assumption must be made and the new circuit must be analyzed, Step 3 must then be repeated.

بالمختصر: ① افرض active ② تأكد من حالة الدايود اذا صح كمل اذا خطأ غير الفرضية وعيد حل.

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Tb = 5 &o

Tb

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$$I_E = I_B + I_C$$

Example 1: $V_{BE} = .7$, $\beta = 100$ find Q point

assume active :

T6 -=- - , 1- - cg 3~ r4 ,,4

u \o k- +S + ((3 '\-\) 5 = .

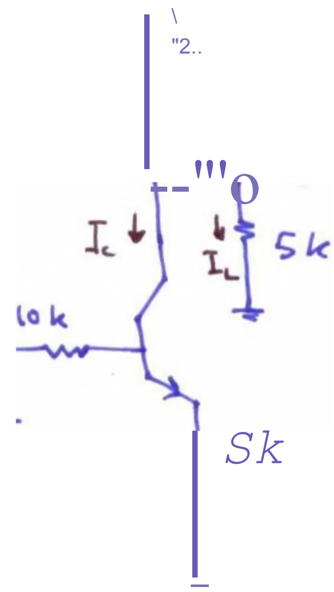
Tc -= k (3 , CZ M fl

Jt;

le ~rb L/1 s ' ~ 4J YV\ A.

-rlJ fh

$$I_C = I_1 - I_L$$



,~.? S s \ ""2...- ...J

$\frac{V_o}{5k} \Rightarrow V_o = 3.91$

..,-\. ~k

1, ~\· {,2 ~~ f 1I- :5 / f'~c.,,'-3

~ ~ ~ o 1' S It:. R.G -= Li· 1- -:) ..._ Gbt~~

c...E. >

ملاحظات مفيدة ① حاول تنسى المطلوب في السؤال وابدأ بحل السؤال مباشرة

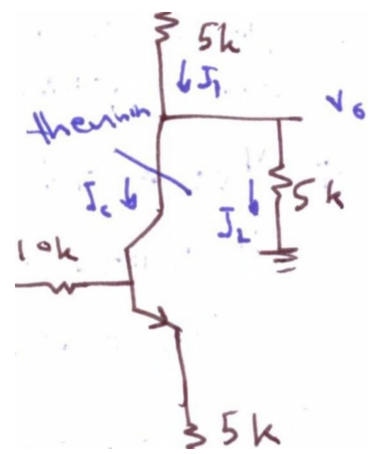
واحسب أي شيء بتقدر تحسبه

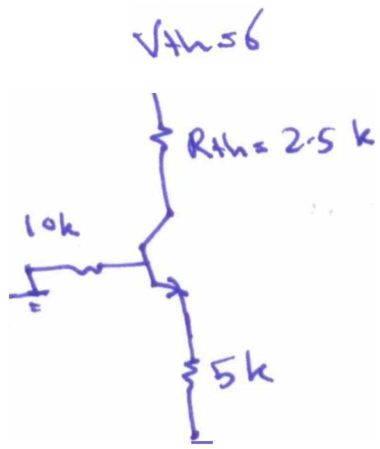
② حاول تستخدم كل المعلومات المعطاة.

③ دائماً أكتب input loop & output loop.

2

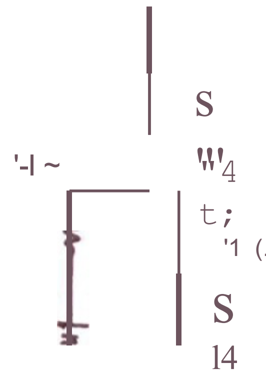
, find Q point , I_L





$$-6 + I_C R_{th} + V_{CE} + 5k \times I_E - 5 = 0$$

Q_1: if $V_B = 1$, find V_C, β, α



$\boxed{4}$

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$$I_c = \beta I_b = 100 \times .026 \times 10^{-3} = 2.6\ m.$$

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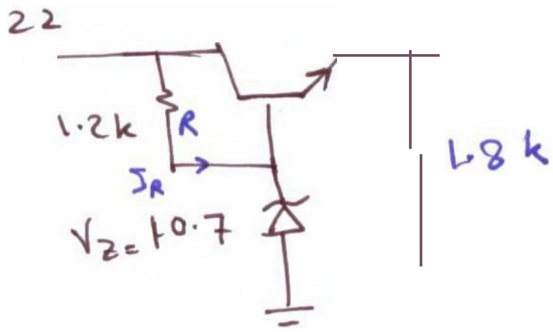
$\boxed{5}$

Example:

find V_o, P_z



--- ~'o - '1a £ -

- t.o ' - q. e/

'..T M./1

L, 1.. lf s:;s

Tet 2-2-- lo.-=7 q.'f ~ fl

$= 1.2k$

$I_C = I_E = 5.55\ mA.$

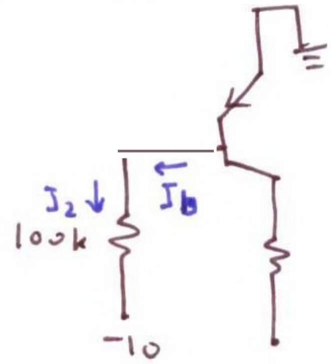
$I_\beta = I_C/\beta = \dfrac{5.55 \times 10^{-3}}{150} = 37\ \mu A.$

$I_Z = I_R - I_B = 9.416 \times 10^{-3} - 37 \times 10^{-6} = 9.379\ mA.$

$P_Z = 10.7 \times 9.379m = 100.36\ mW.$

Example: find Q point, V_C, V_E, V_B

assum

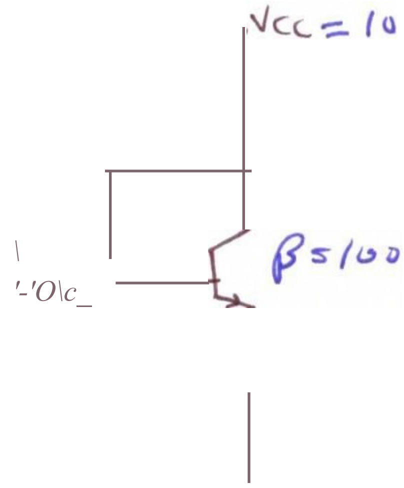


$$\frac{-.7+10}{100k} - \frac{10+.7}{100k} = .093 - .107 = -.014\,mA$$

$I_b = -.014\,mA \Rightarrow$ X wrong assumption

The transistor is cut-off

$V_C = -10$, $V_B = 0$



$> V_{CE}(sat)$

لاحظ هنه الدائرة مستحيل التصير

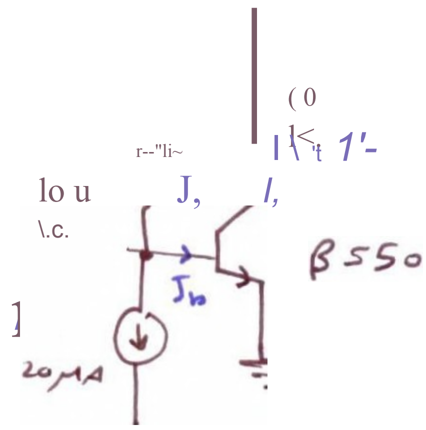
$\boxed{7}$

Example: find Q

$I_1 = I_b + 20\,\mu A$

$-10 + 10k\,(I_1 + I_c) + 100k \times I_1 + .7 = 0$

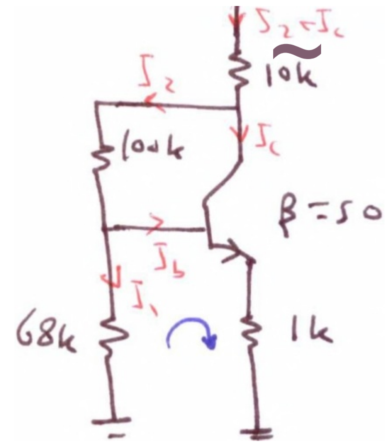
$+ .7 = 0$



$\boxed{8}$

Example: find Q

$+(\beta+1) I_b \times 1k = 0$



E~te; ttv1 Q

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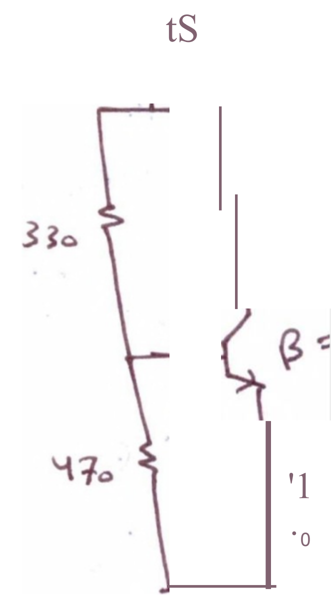

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$J_E =$ <i· -:=- ~
'_' oS k. LW\ Tc..

$V_{CE} = 15 - 2m(10k + 4.05k) = -13.14$ ∴ →
our assumption is wrong the
transistor is saturation → Resolve

~ o...ss\.t. y«u/""~ ,:;.....
~c:.
~ -- \lc.<;.(5-v\) s I(.. o' "1 ~~) ~ o
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=- 10k + 4.05k 10 + 4.05
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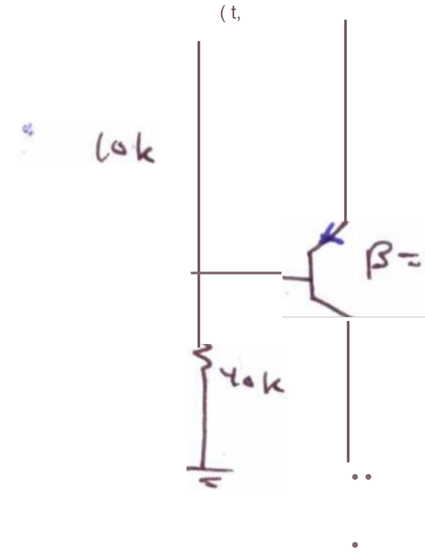
$\boxed{10}$

Example : (PNP).



$V_E = 8.7$

$I_E = \frac{10.7 - 8.7}{2k} = 1m$

$V_{CE} = 10.7 - 6k \times 1m = 4.7 > V_{CE(sat)}$.

ANALOG CIRCUITS

Presented By,
G.R.Mahendra Babu,
Assistant Professor,
Dept of ECE / FoE / KAHE.

BJT LL-SIGN L
SMA A ANALYSIS

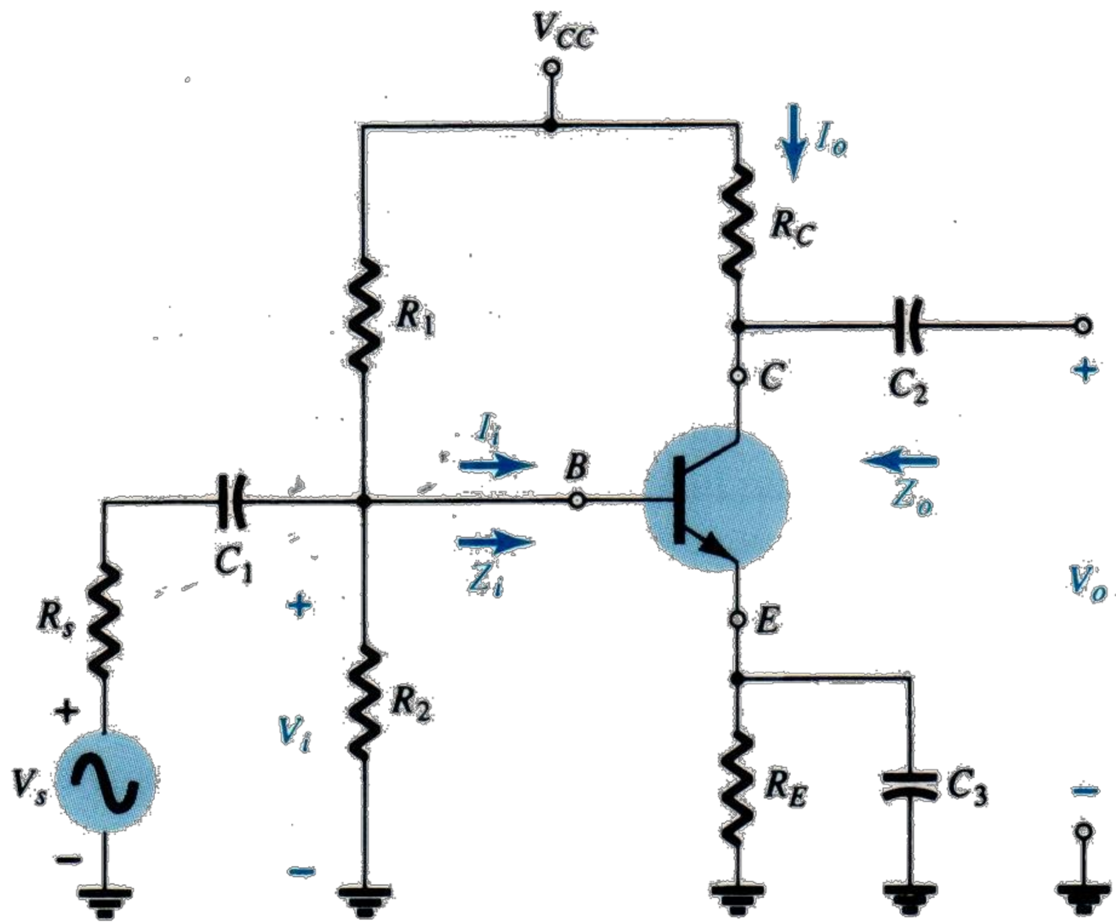
BJT Small Signal Analysis

- $\mathbf{r_e}$ transistor model – employs a diode and controlled current source to duplicate the behavior of a transistor in the region of interest.
- The $\mathbf{r_e}$ and hybrid models will be used to analyze small-signal AC analysis of standard transistor network configurations.

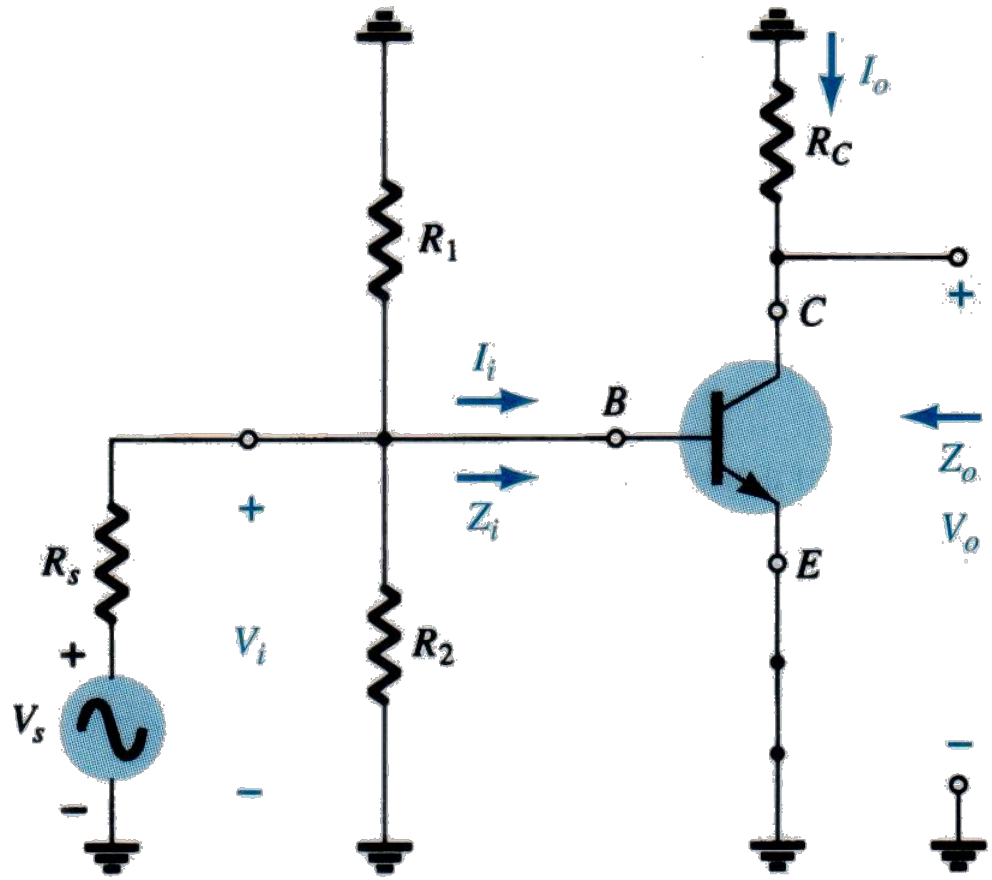
  Ex: Common-base, common-emitter and common-collector configurations.
- The network analyzed represent the majority of those appearing in practice today.

AC equivalent of a network is obtained by:

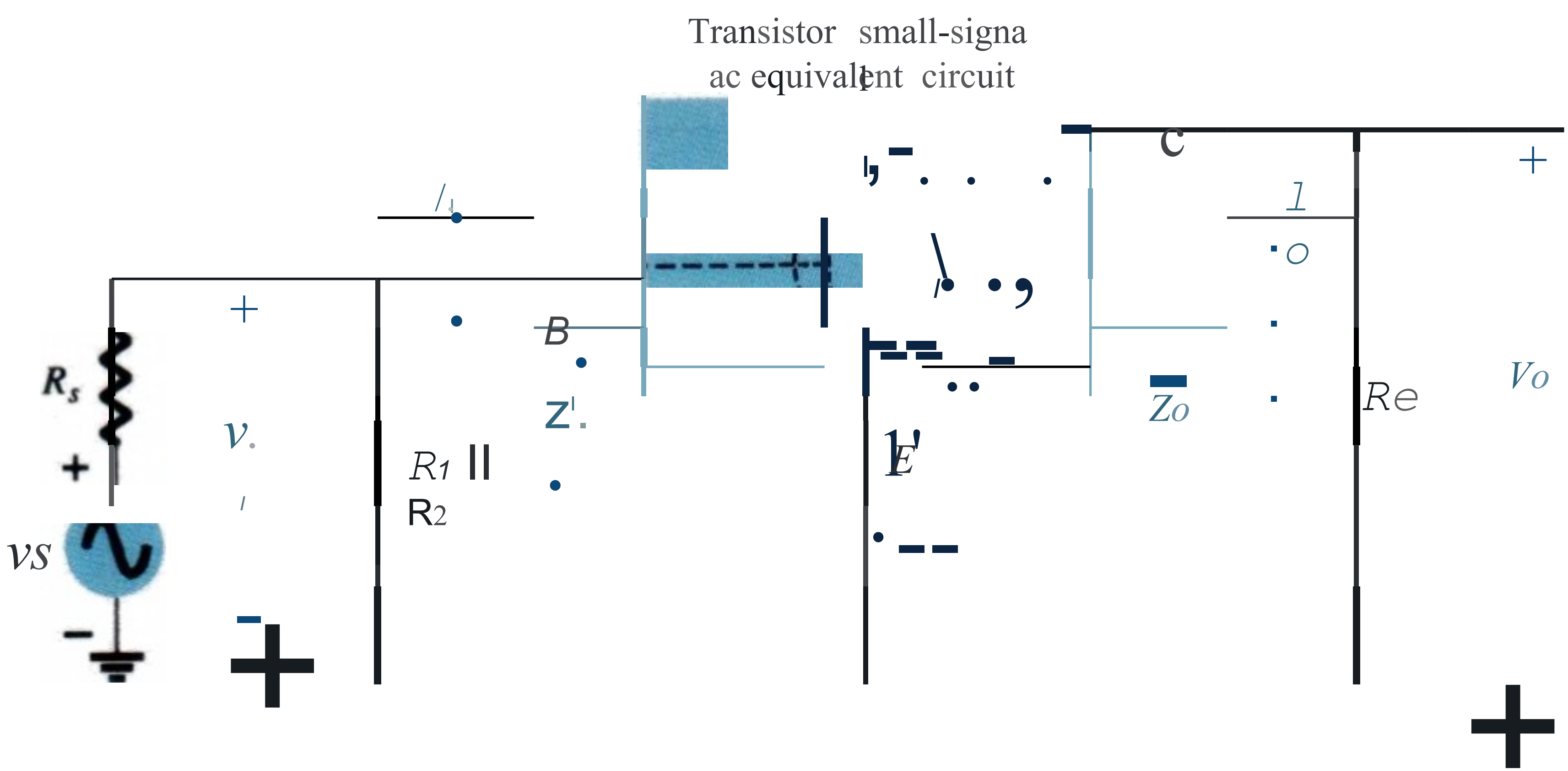
1. Setting all DC sources to zero
2. Replacing all capacitors by s/c equiv.
3. Redraw the network in more convenient and logical form



Transistor circuit under examination in this introductory discussion.

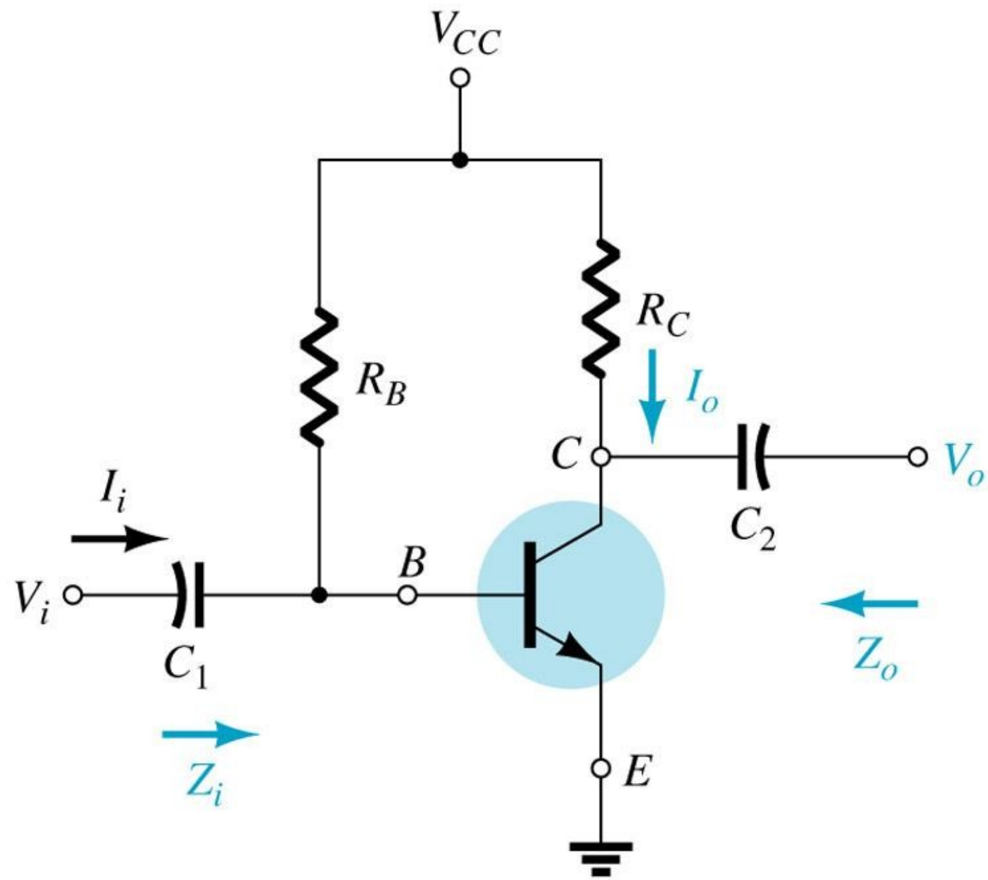


The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.



Circuit of Fig. 5.4 redrawn for small-signal ac analysis.

Common-Emitter (CE) Fixed-Bias Configuration



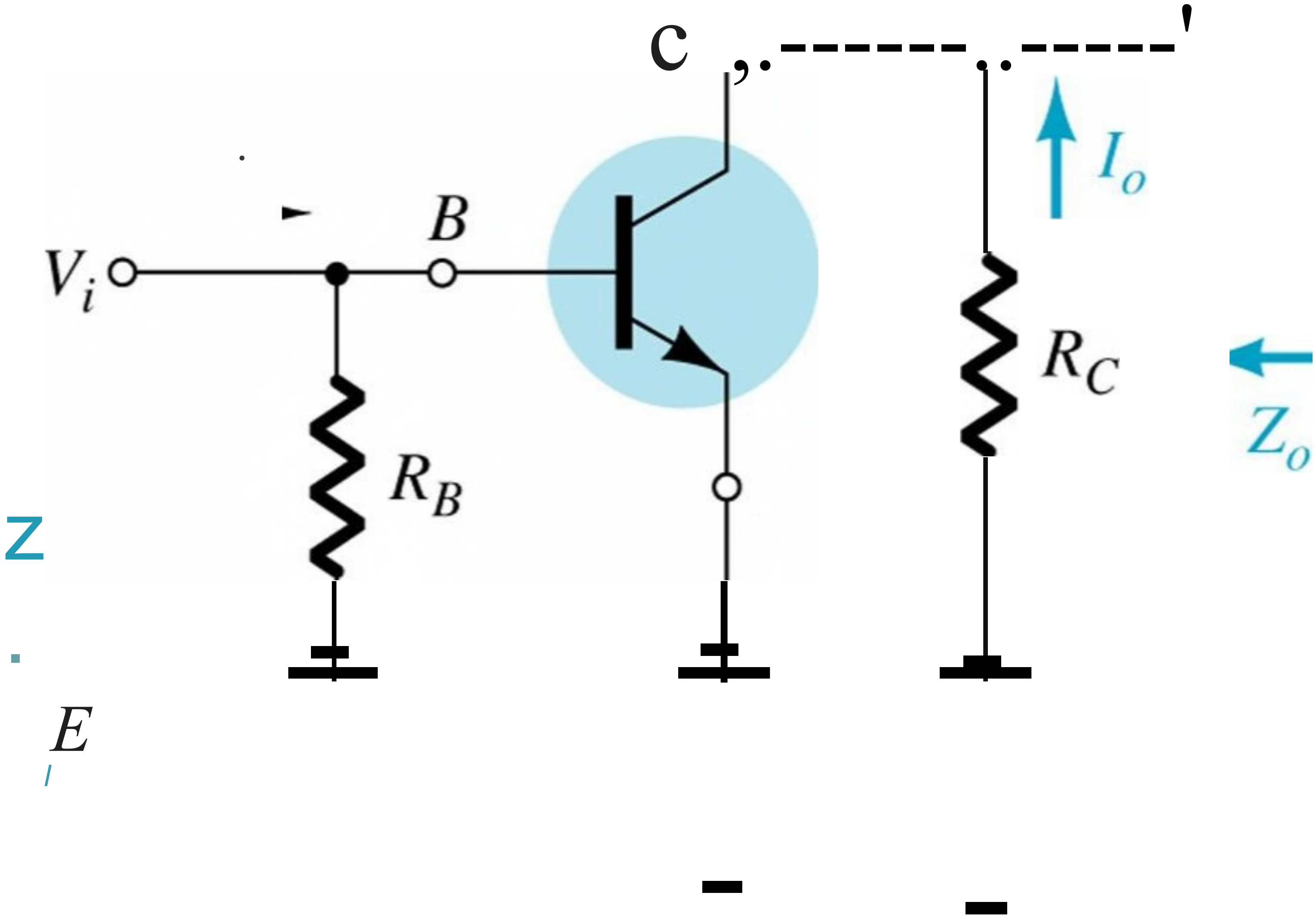
The input (Vi) is applied to the base and the output (Vo) is from the collector.

The Common-Emitter is characterized as having high input impedance and low output impedance with a high voltage and current gain.

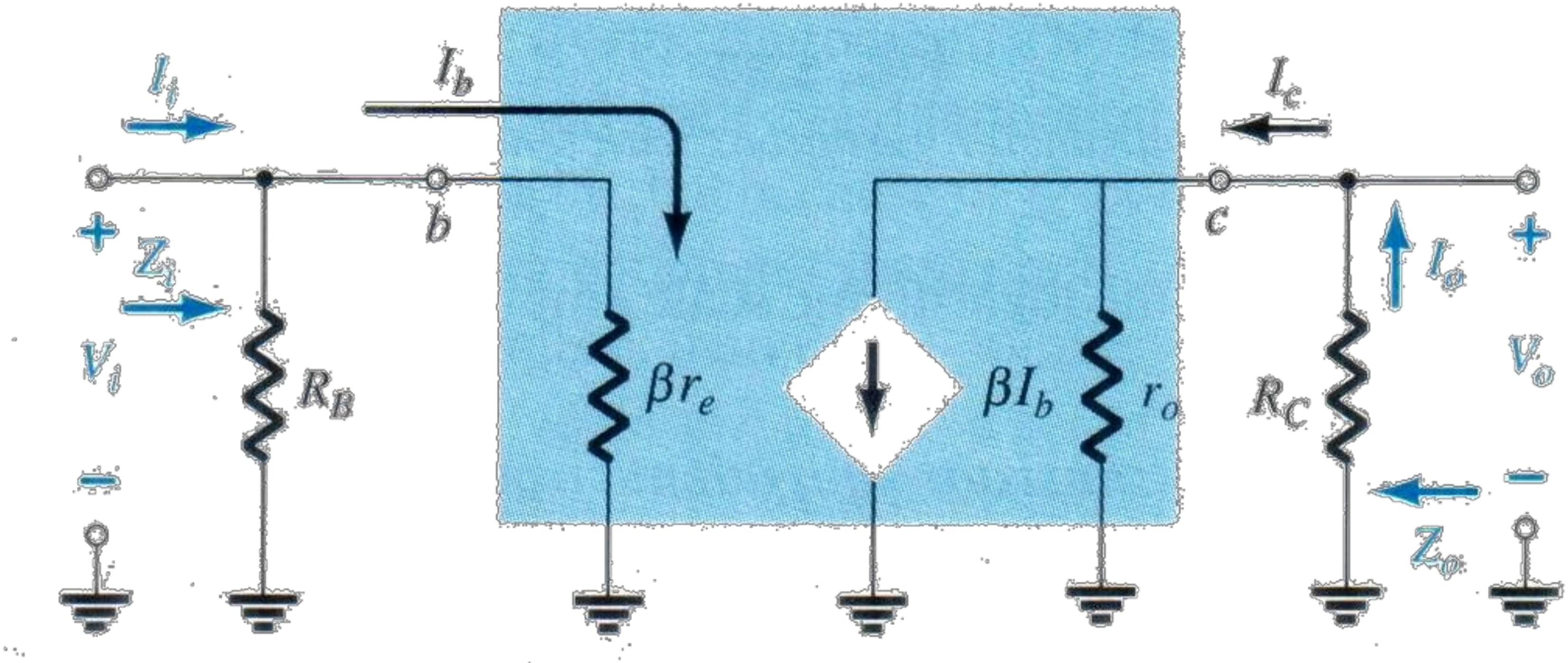
Asutosh Kar, IIIT

Common-Emitter (CE) Fixed-Bias Configuration

Removing DC effects of V_{CC} and Capacitors



re Model



Determine β, re, and ro:

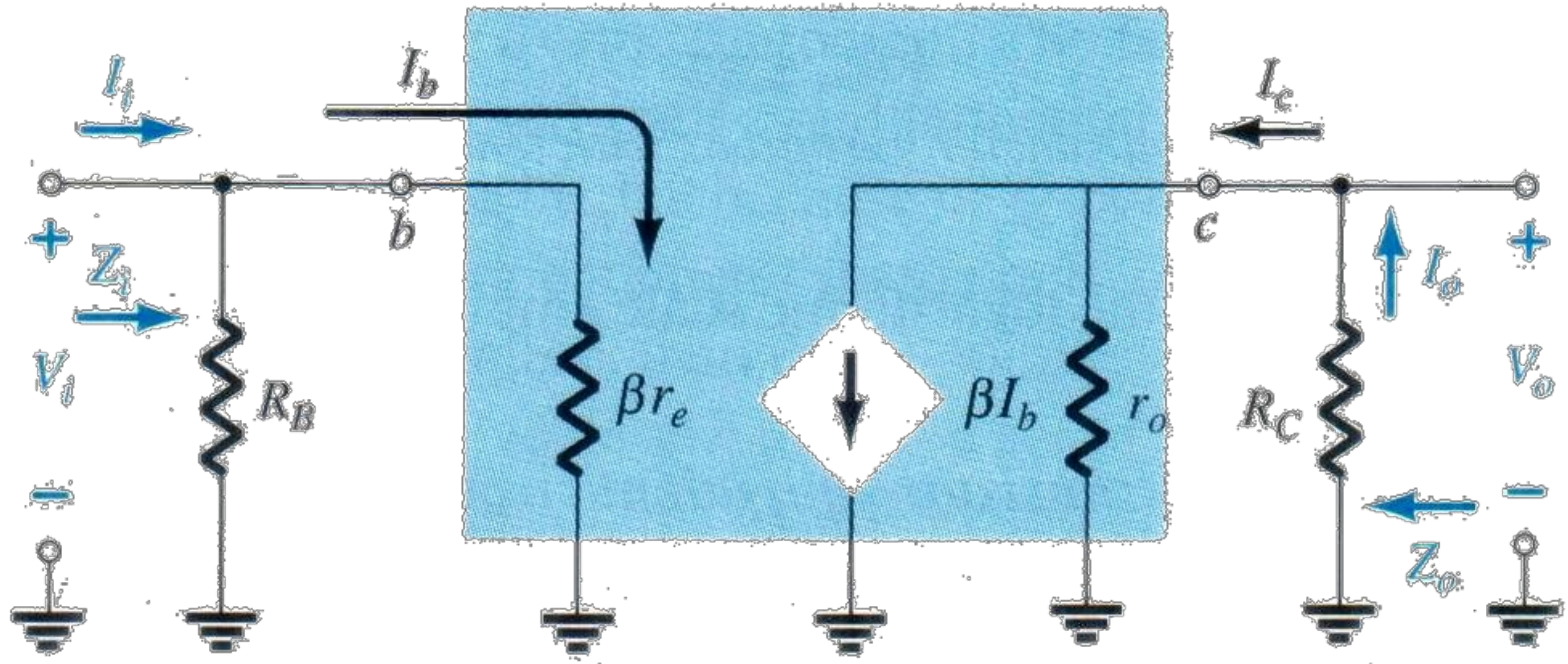
β ***and ro:*** look in the specification sheet for the transistor or test the transistor using a curve tracer.

re: calculate re using dc analysis:

$$r_e = \frac{26mV}{I_E}$$

Common-Emitter (CE) Fixed-Bias Configuration

Impedance Calculations



Input Impedance:

$$Z_i = R_B \parallel \beta r_e$$

$$Z_i \cong \beta r_e \quad / \quad R_B \geq 10\beta r_e$$

Output Impedance:

$$Z_o = R_C \parallel r_o$$

$$Z_o \cong R_c \quad / \quad ro \geq 10R_c$$

Common-Emitter (CE) Fixed-Bias Configuration

Gain Calculations

Voltage Gain (Av):

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \parallel r_o)}{r_e}$$

$$A_v = -\frac{R_C}{r_e} \Big/ r_o \geq 10R_C$$

Current Gain (Ai):

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$$

$$A_i \cong \beta \Big/ r_o \geq 10R_C,\ R_B \geq 10\beta r_e$$

Current Gain from Voltage Gain:

$$A_i = -A_v \frac{Z_i}{R_C}$$

Voltage Gain

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -\beta I_b (R_C \parallel r_o)$$

$$V_i = I_b \beta r_e$$

$$A_v = \frac{-\beta I_b (R_C \parallel r_o)}{I_b \beta r_e}$$

$$= \frac{(R_C \parallel r_o)}{r_e}$$

if $r_o = \infty\Omega$ or $\geq 10R_C$ $\quad A_v = \frac{R_C}{r_e}$

Common-Emitter (CE) Fixed-Bias Configuration

Current gain

The current gain is determined by ap p ly ingthe current - divider rule to the inp ut and outp ut circuits

$$I_o = \frac{r_o \beta I_b}{r_o + R_C} \quad \text{and} \quad \frac{I_o}{I_b} = \frac{r_o \beta}{r_o + R_C}$$

$$I_b = \frac{R_B I_i}{R_B + \beta r_e} \quad \text{and} \quad \frac{I_b}{I_i} = \frac{R_B}{R_B + \beta r_e}$$

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_b}\right)\left(\frac{I_b}{I_i}\right) = \left(\frac{r_o \beta}{r_o + R_C}\right)\left(\frac{R_B}{R_B + \beta r_e}\right)$$

$$\therefore A_i = \frac{I_o}{I_i} = \frac{r_o \beta R_B}{(r_o + R_C)(R_B + \beta r_e)}$$

if $r_o \ge 10 R_C$ and $R_B \ge 10 \beta r_e$,

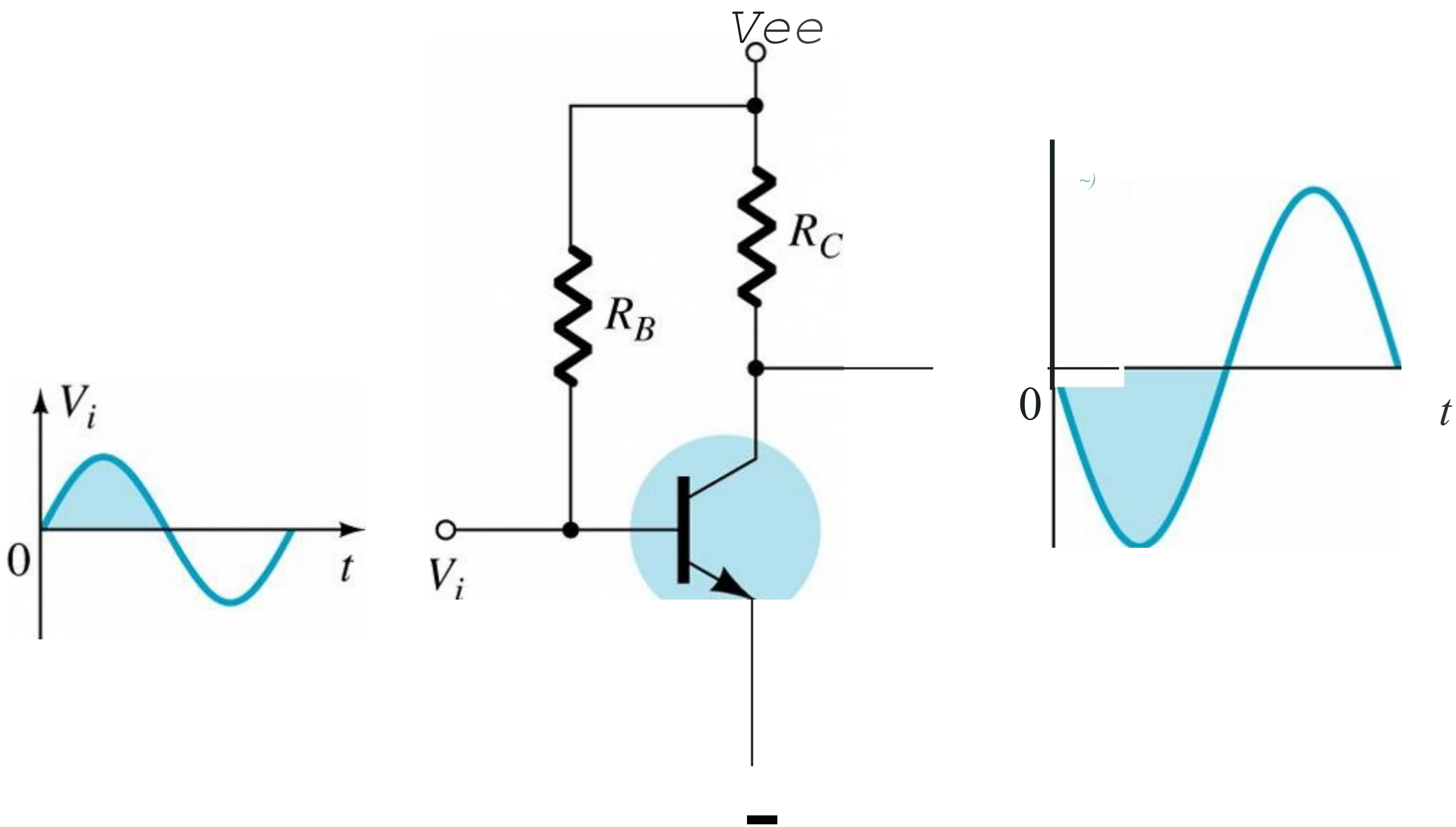
$$\therefore A_i = \frac{I_o}{I_i} \cong \frac{r_o \beta R_B}{(r_o)(R_B)} = \beta$$

or we can use this equation too

$$\therefore A_i = -A_v \frac{Z_i}{R_C}$$

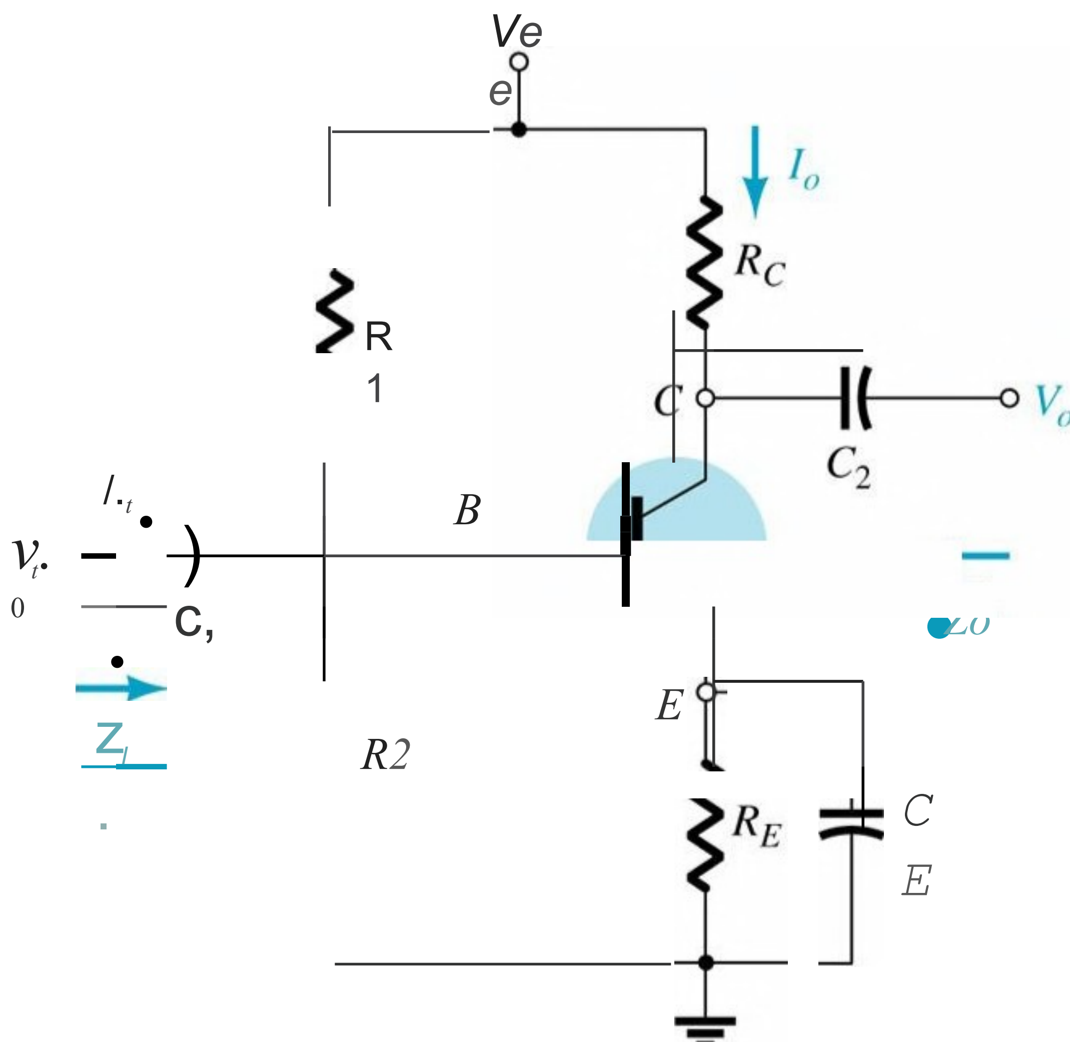
Common-Emitter (CE) Fixed-Bias Configuration

Phase Relationship



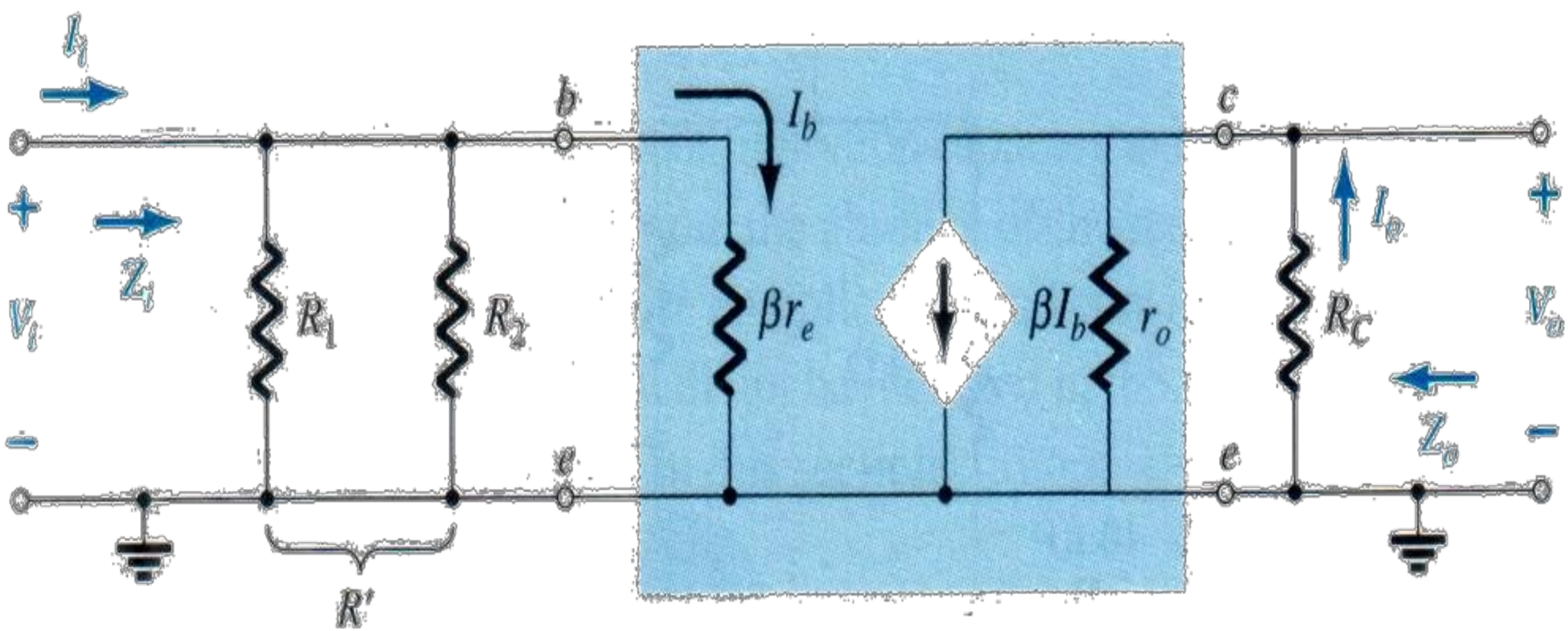
The phase relationship between input and output is 180 degrees. The negative sign used in the voltage gain formulas indicat$_{A}$e$_{s}$s$_{uto}$h$_{s}$e$_{h}$
$_{K}$in$_{a}$v$_{r}$e$_{I}$r$_{U}$s$_{T}$io$_{B}$n$_{h}$.$_{ubaneswar}$

CE – Voltage-Divider Bias Configuration



CE – Voltage-Divider Bias Configuration

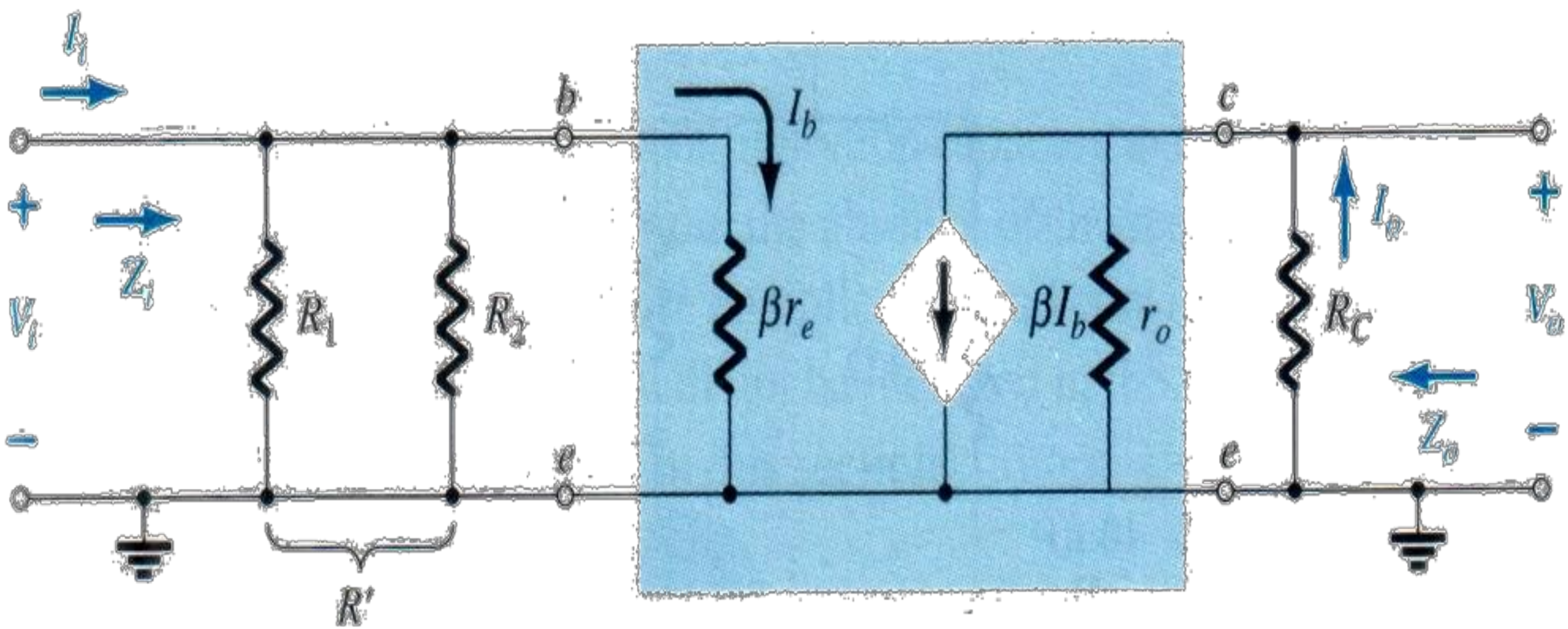
re Model



You still need to determine β, re, and ro.

CE – Voltage-Divider Bias Configuration

Impedance Calculations



Input Impedance:

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$Z_i = R' \| \beta r_e$$

Output Impedance:

$$Z_o = R_C \| r_o$$

$$Z_o \cong R_C \quad r_o \geq 10R_C$$

CE – Voltage-Divider Bias Configuration

Gain Calculations

Voltage Gain (Av):

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \parallel r_o}{r_e}$$

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \Big/ r_o \geq 10R_C$$

Current Gain (Ai):

$$A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)}$$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R'}{R' + \beta r_e} \Big/ r_o \geq 10R_C$$

Current Gain from Voltage Gain:

$$A_i = \frac{I_o}{I_i} \cong \beta \Big/ r_o \geq 10R_C,\ R' \geq 10\beta r_e$$

$$A_i = -A_v \frac{Z_i}{R_C}$$

Voltage Gain

$$V_O = -(\beta I_b)(R_C \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

$$\therefore A_v = \frac{-(R_C \| r_o)}{r_e}$$

$$\text{if } r_o = \infty\Omega \text{ or } \geq 10R_C \qquad \therefore A_v = \frac{-R_C}{r_e}$$

Current gain

since the network is so similar to that common - emitter fixed - bias configurat ion, excep t for the R', the equation for the current gain will have the same format.

$$R' = R_1 \| R_2 = R_B$$

$$A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)}$$

for $r_o \geq 10R_C$,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R' r_o}{r_o (R' + \beta r_e)} \cong \frac{\beta R'}{(R' + \beta r_e)}$$

CE – Voltage-Divider Bias Configuration

And if $R' \geq 10\beta r_e$,

$$A_i = \frac{I_o}{I_i} = \frac{\beta R'}{R'}$$

$$\therefore A_i = \frac{I_o}{I_i} \cong \beta$$

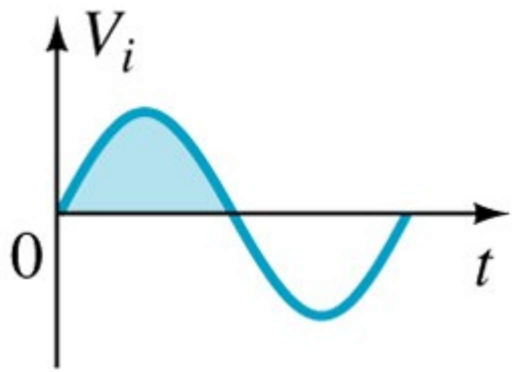
as an option

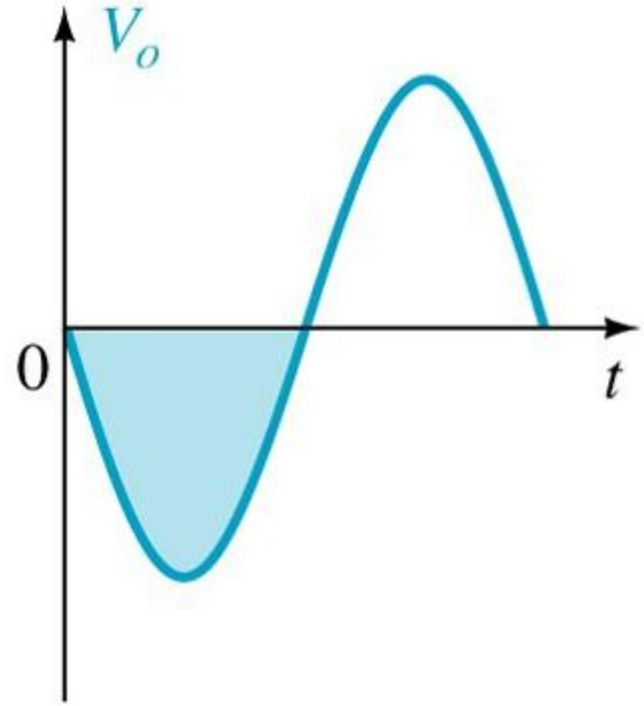
$$\therefore A_i = -A_V \frac{Z_i}{R_C}$$

CE – Voltage-Divider Bias Configuration

Phase Relationship

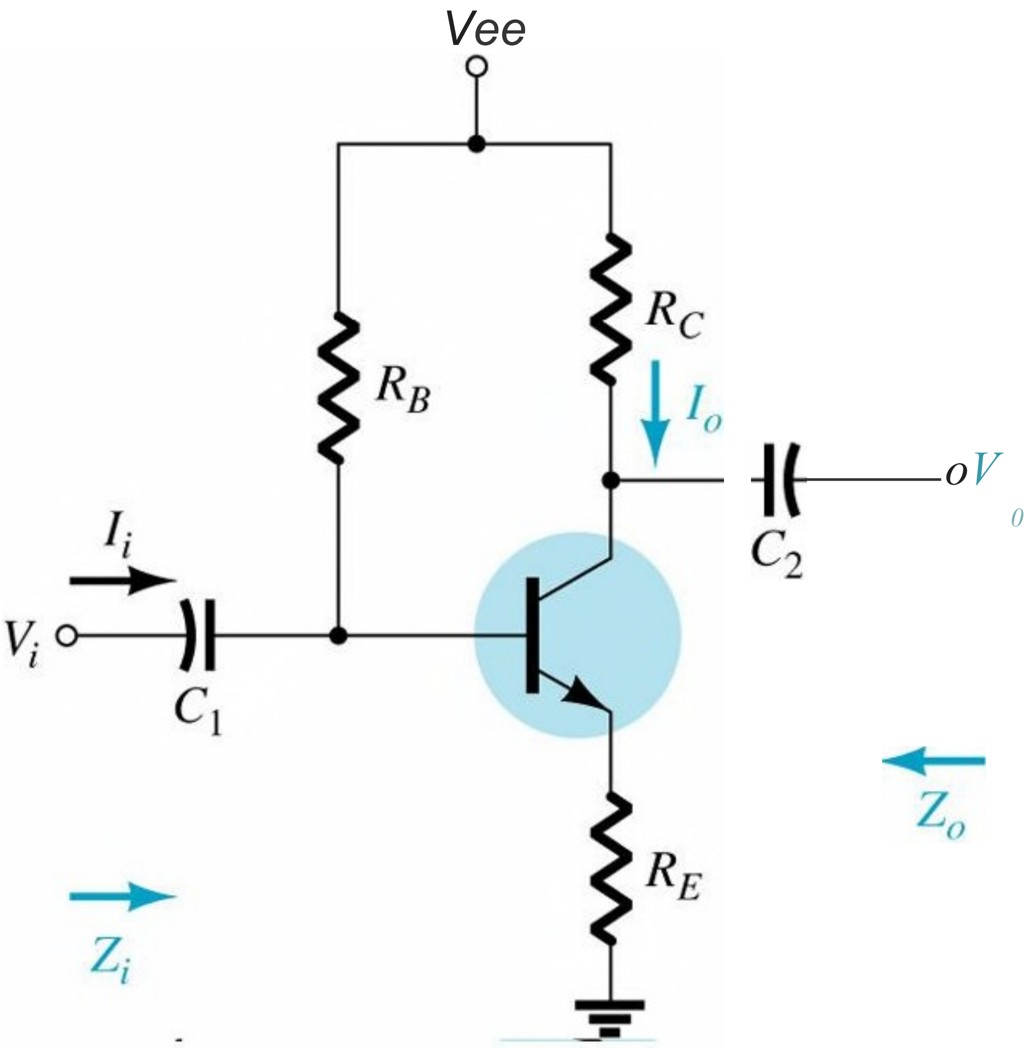
A CE amplifier configuration will always have a phase relationship between input and output is 180 degrees. This is independent of the DC bias.





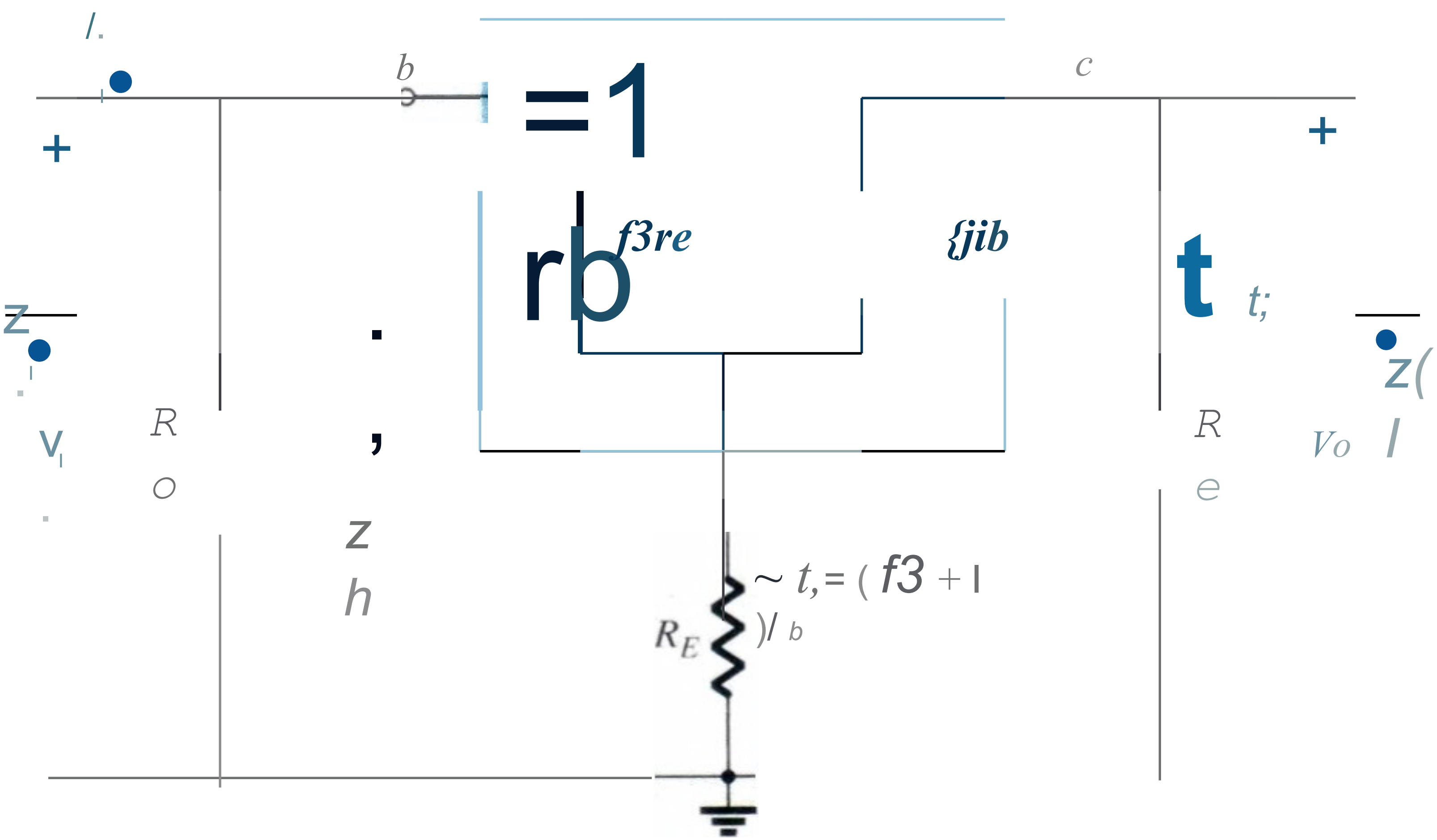
CE Emitter-Bias Configuration

Unbypassed R_E



CE Emitter-Bias Configuration

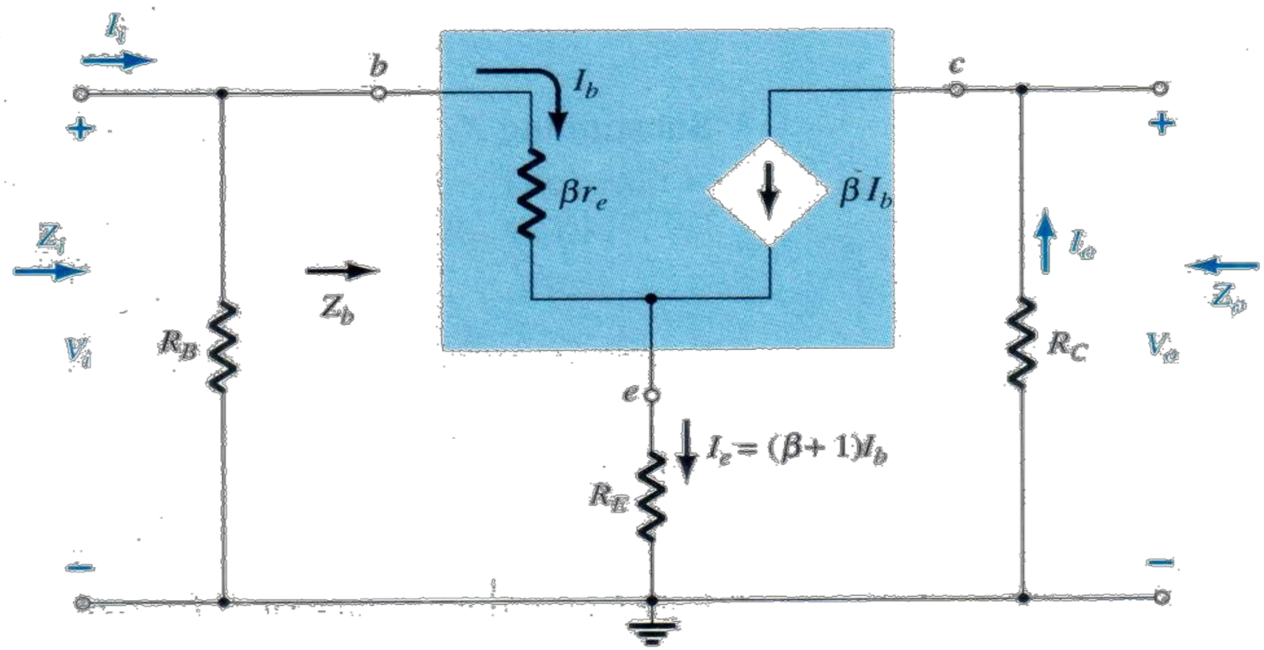
re Model



Again you need to determine β, re.

CE Emitter-Bias Configuration

Impedance Calculations



Input Impedance:

$$Z_b = \beta r_e + (\beta + 1)R_E$$

$$Z_b \cong \beta (r_e + R_E)$$

$$Z_i = R_B \,\|\, Z_b$$

$$Z_b \cong \beta R_E \quad \Big/ \; R_E >> r_e$$

Output Impedance:

$$Z_o = R_C$$

Defining the input impedance of a transistor with an unbypassed emitter resistor

Ap p ly ingKVL to the inp ut side :

$$V_i = I_b \beta r_e + I_e R_E$$

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

$$\therefore Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E$$

since β is normally greater than 1,

$$\therefore Z_b \cong \beta r_e + \beta R_E$$

since R_E is much greater than r_e, eqn above can be reduced to

$$\therefore Z_b \cong \beta R_E$$

CE Emitter-Bias Configuration

Gain Calculations

Voltage Gain (Av):

$$A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E} \Big/ Z_b = \beta (r_e + R_E)$$

or

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E} \Big/ Z_b \cong \beta R_E$$

Current Gain (Ai):

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{R_B + Z_b}$$

Current Gain from Voltage Gain:

$$A_i = -A_v \frac{Z_i}{R_C}$$

Voltage Gain

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right) R_C$$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{-\beta R_C}{Z_b}$$

substituting $Z_b = \beta(r_e + R_E)$ gives

$$\therefore A_V = \frac{V_o}{V_i} = \frac{-R_C}{r_e + R_E}$$

and for the approximation $Z_b \cong \beta R_E$

$$\therefore A_V = \frac{V_o}{V_i} = \frac{-R_C}{R_E}$$

Current Gain

The magnitude of R_B is often too close to Z_b to permit the approximation $I_b = I_i$. Applying the current-divider rule to the input circuit will result in:

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

$$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

$$I_o = \beta I_b$$

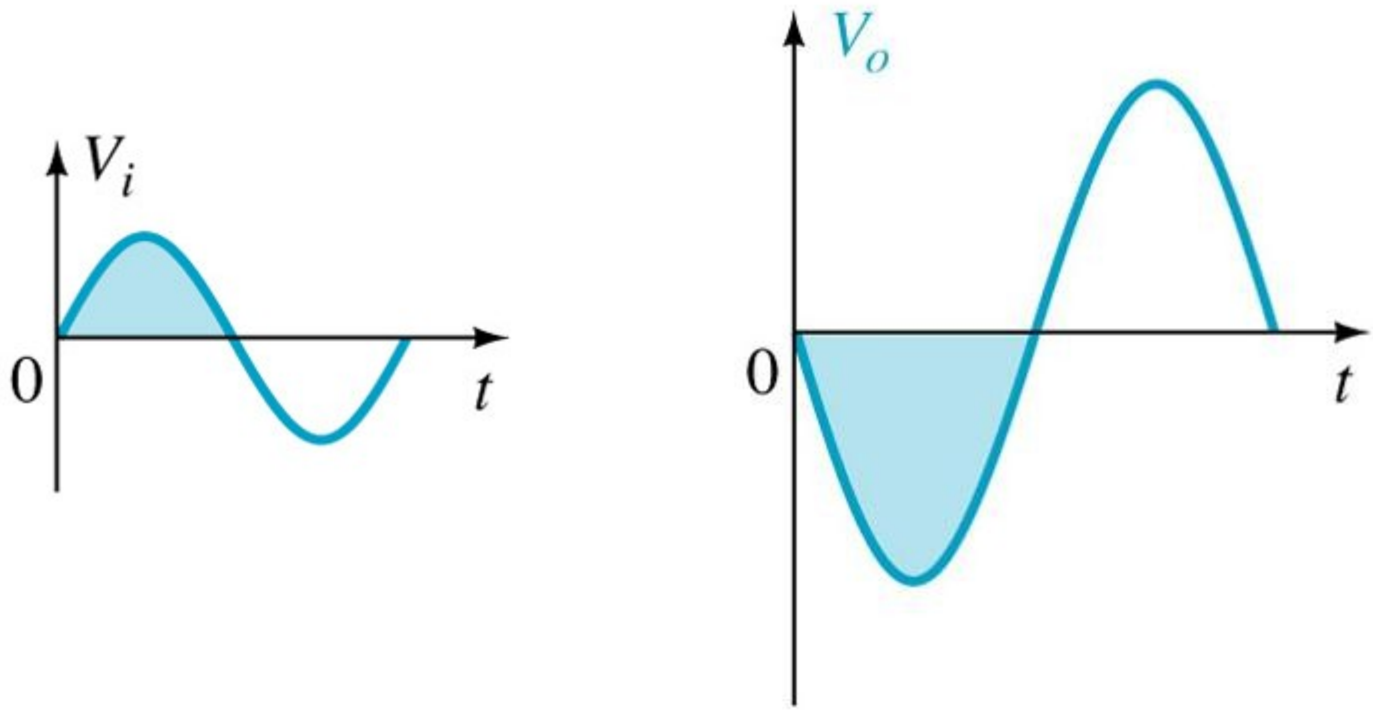
$$\frac{I_o}{I_b} = \beta$$

$$\therefore A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\frac{I_b}{I_i} = \beta \frac{R_B}{R_B + Z_b}$$

$$\therefore A_i = -A_v \frac{Z_i}{R_C}$$

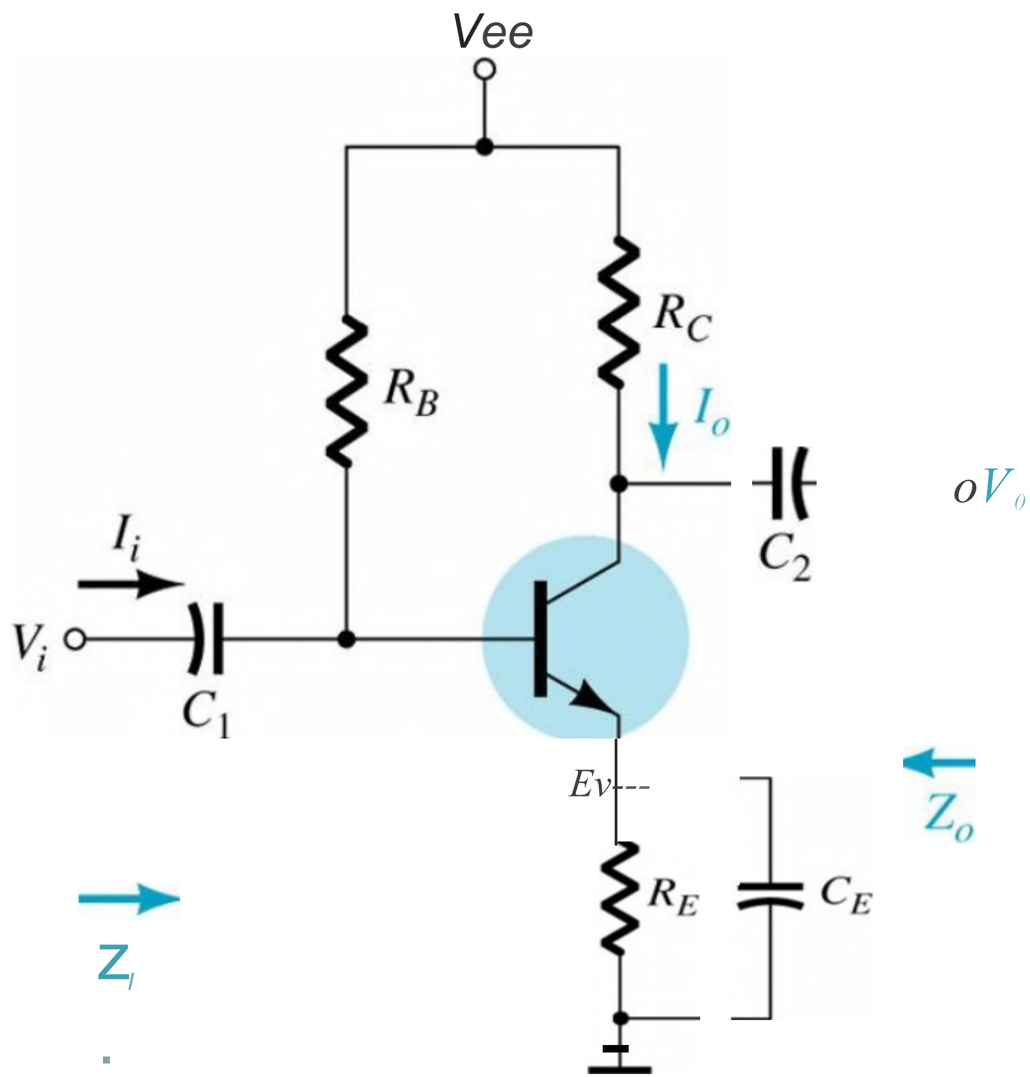
Phase Relationship

A CE amplifier configuration will always have a phase relationship between input and output is 180 degrees. This is independent of the DC bias.



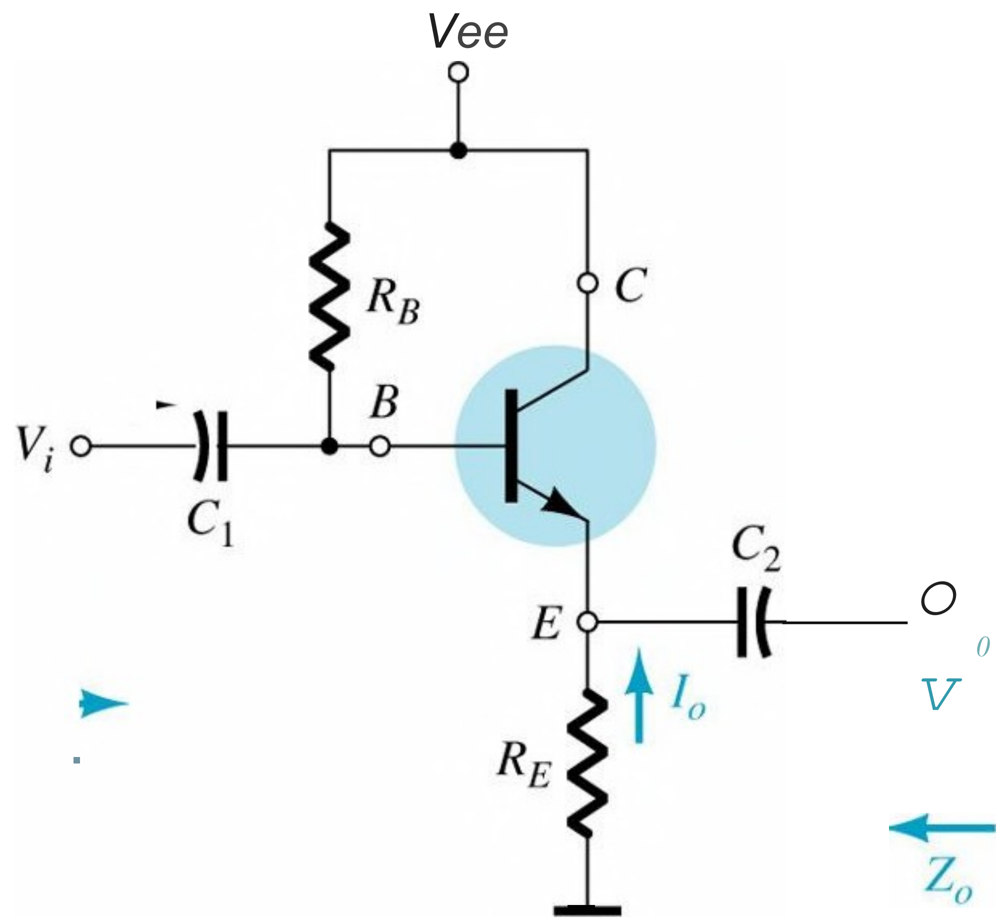
CE Emitter-Bias Configuration

Bypassed RE



This is the same circuit as the CE fixed-bias configuration and therefore can be solved

Emitter-Follower Configuration

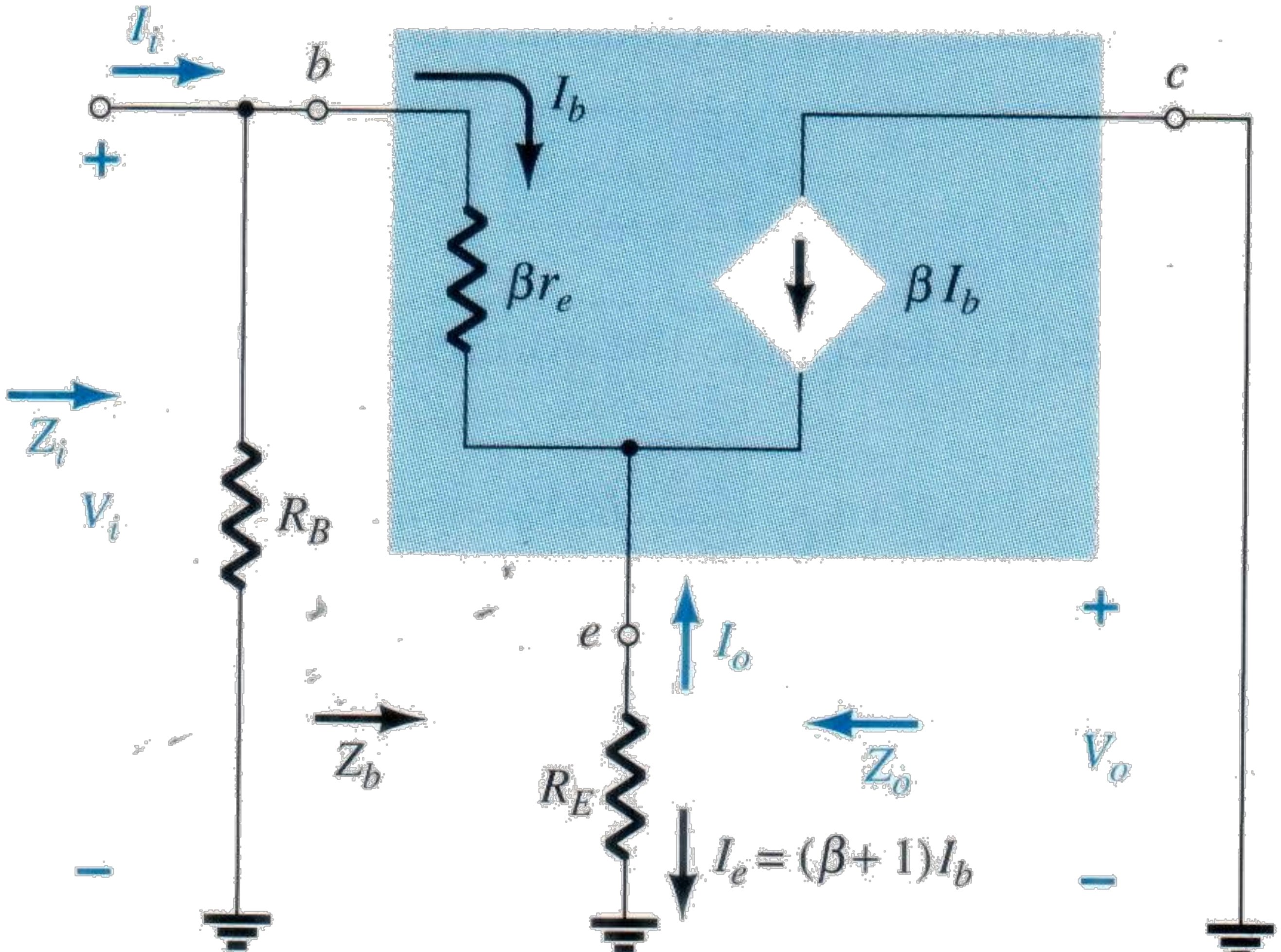


You may recognize this as the Common-Collector configuration. Indeed they are the same circuit.

Note the input is on the base and the output is from the emitter.

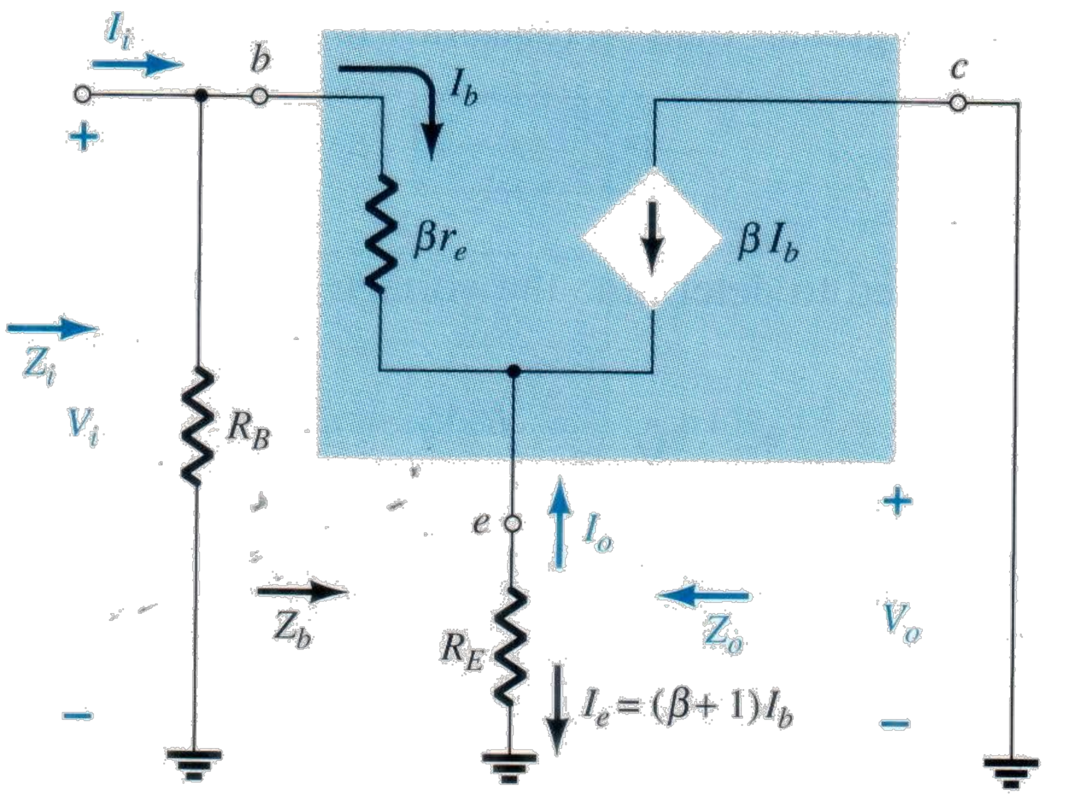
Emitter-Follower Configuration

re Model



You still need to determine β and re.

Impedance Calculations



Input Impedance:

$$Z_i = R_B \,||\, Z_b$$

$$Z_b \cong \beta (r_e + R_E)$$

$$Z_b = \beta r_e + (\beta + 1) R_E$$

$$Z_b \cong \beta R_E$$

Emitter-Follower Configuration

Calculation for the current I_e

$$I_b = \frac{V_i}{Z_b}$$

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

subtituting for Z_b gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

$$= \frac{V_i}{\left[\beta r_e / (\beta + 1)\right] + R_E} \qquad \text{but } (\beta + 1) \cong \beta$$

$$\text{and } \beta r_e / (\beta + 1) \cong \frac{\beta r_e}{\beta} = r_e$$

$$\therefore I_e = \frac{V_i}{r_e + R_E}$$

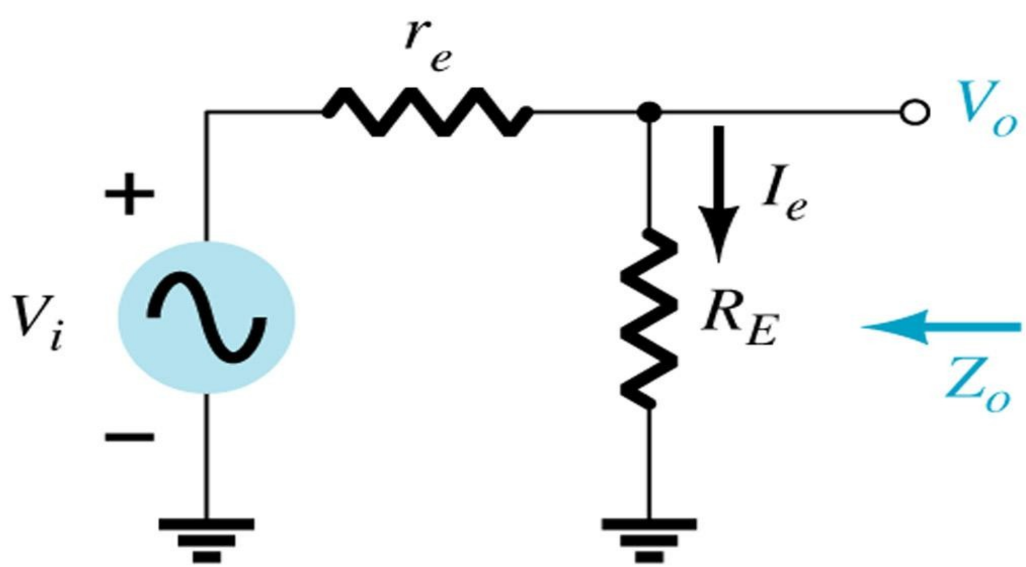
Emitter-Follower Configuration

Impedance Calculations (cont’d)

Output Impedance:

Defining the outp ut imp edence for the emitter follower configurat ion

$$\therefore I_e = \frac{V_i}{r_e + R_E}$$



$$\boxed{Z_o = R_E \,\|\, r_e}$$

$$\boxed{Z_o \cong r_e \Big/ R_E >> r_e}$$

Emitter-Follower Configuration

Gain Calculations

Voltage Gain (Av):

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

$$A_v = \frac{V_o}{V_i} \cong 1 \quad / \quad R_E >> r_e,\ R_E + r_e \cong R_E$$

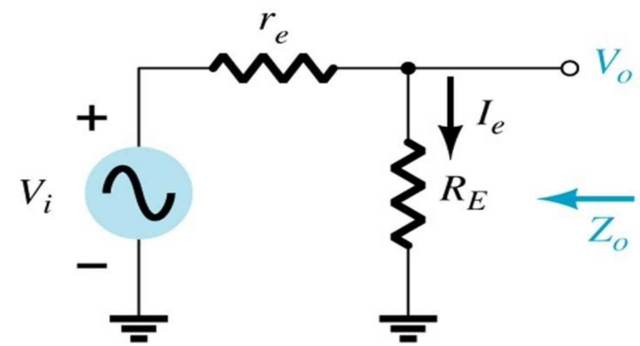
Current Gain (Ai):

$$A_i \cong -\frac{\beta R_B}{R_B + Z_b}$$

Current Gain from Voltage Gain:

$$A_i = -A_v \frac{Z_i}{R_E}$$

Voltage gain



$$V_o = \frac{R_E V_i}{R_E + r_e}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$

R_E usually much greater than r_e,

$$R_E + r_e \cong R_E$$

$$\therefore A_v = \frac{V_o}{V_i} \cong 1$$

Current Gain

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

$$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

$$I_o = -I_e = -(\beta + 1)I_b$$

$$\frac{I_o}{I_b} = -(\beta + 1)$$

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\frac{I_b}{I_i} = -(\beta + 1)\frac{R_B}{R_B + Z_b}$$

since $(\beta + 1) \cong \beta$,

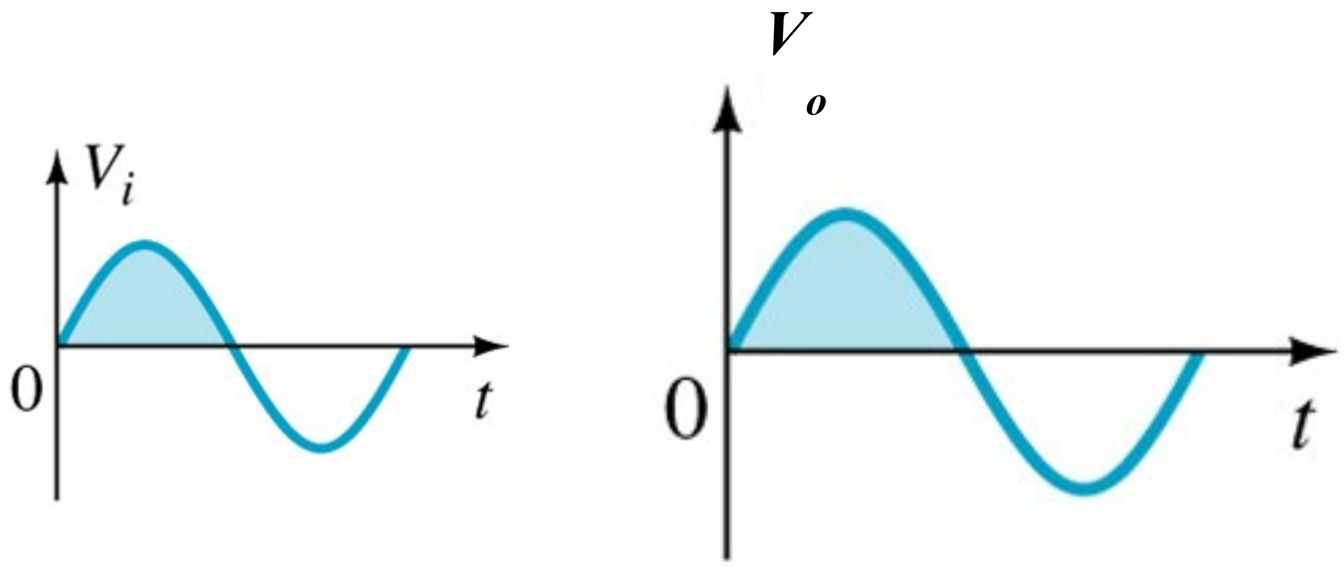
$$\therefore A_i \cong -\frac{\beta R_B}{R_B + Z_b}$$

$$\text{or} \quad A_i = -A_v \frac{Z_i}{R_L}$$

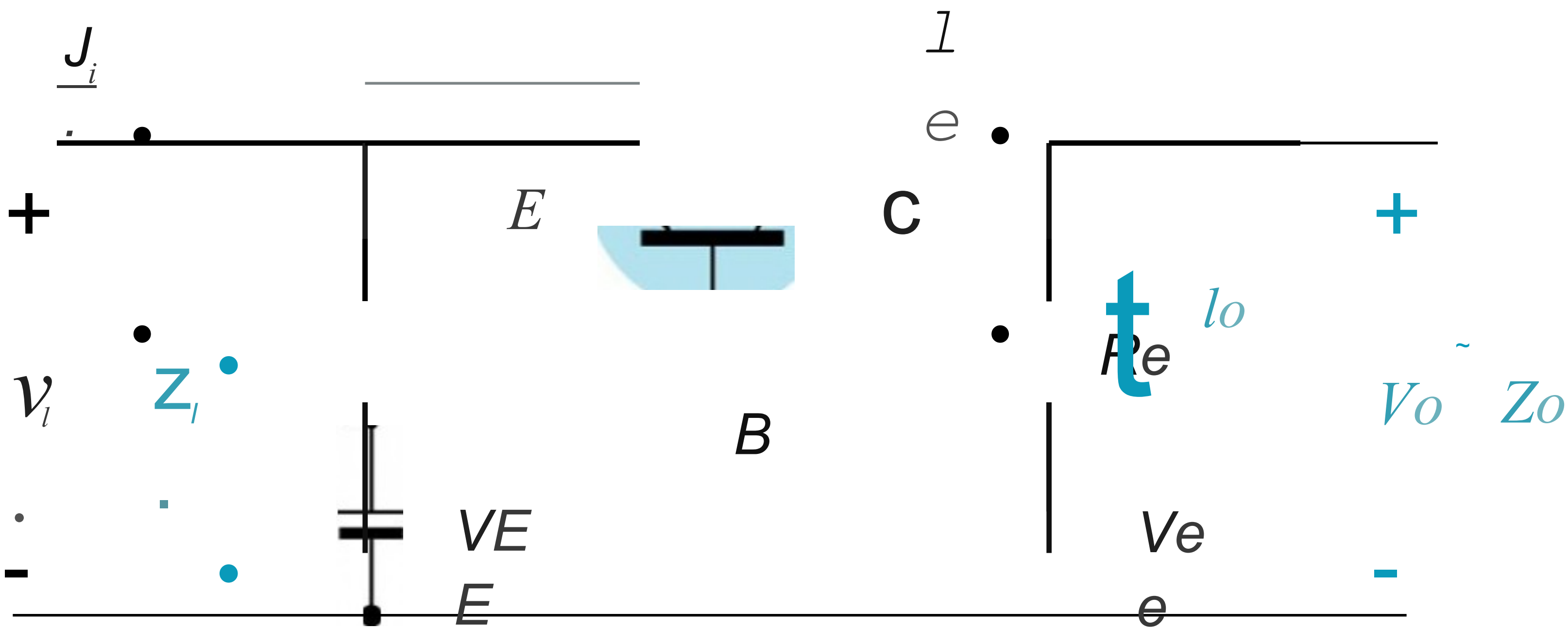
Emitter-Follower Configuration

Phase Relationship

A CC amplifier or Emitter Follower configuration has no phase shift between input and output.



Common-Base (CB) Configuration

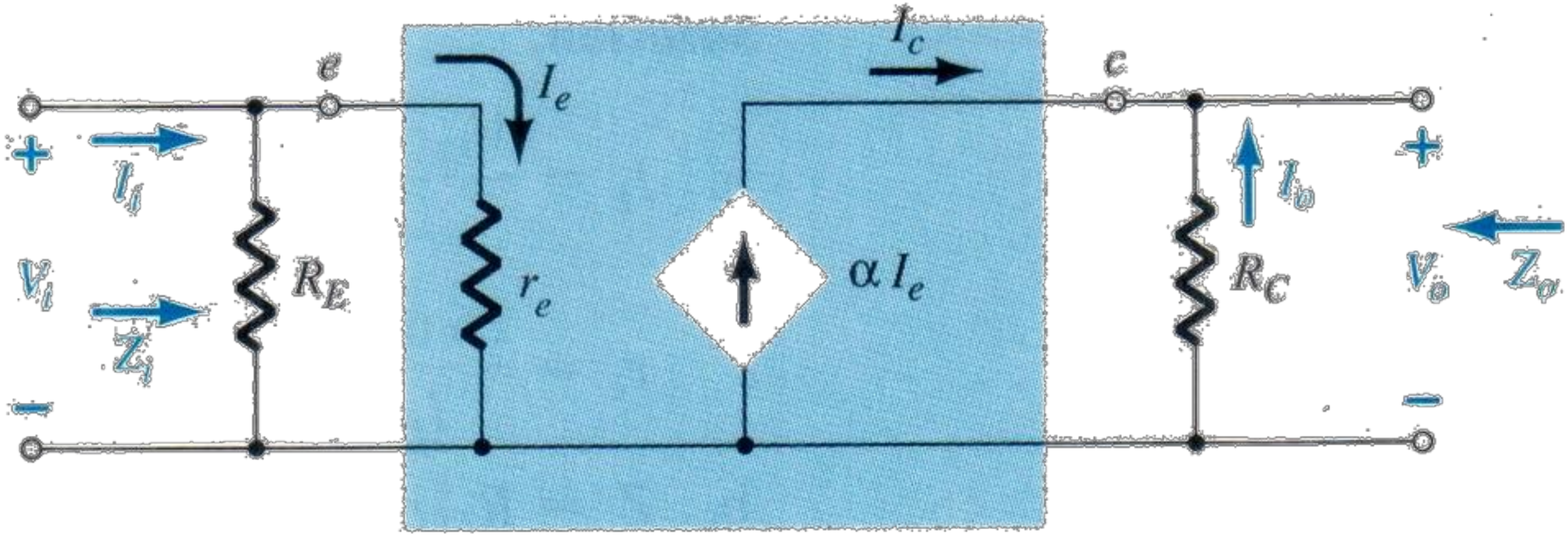


The input (Vi) is applied to the emitter and the output (Vo) is from the collector.

The Common-Base is characterized as having low input impedance and high output impedance with a current gain less than 1 and a very high voltage gain.

Common-Base (CB) Configuration

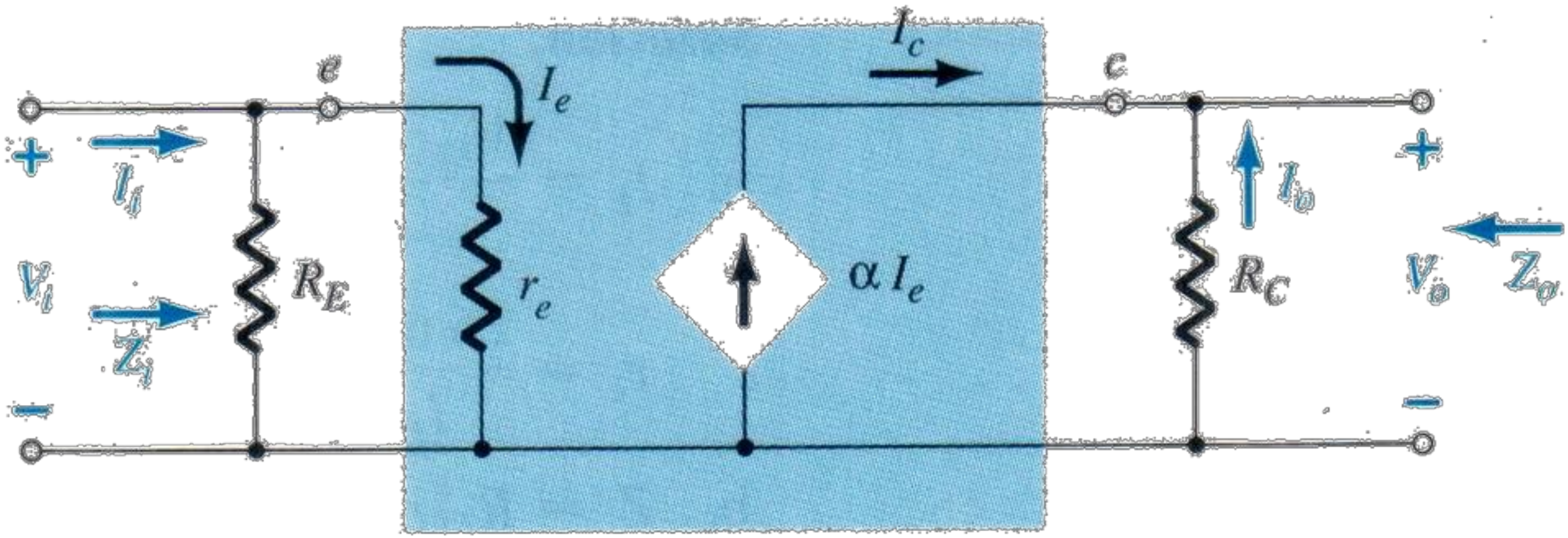
re Model



You will need to determine α and re.

Common-Base (CB) Configuration

Impedance Calculations



Input Impedance:

$$\boxed{Z_i = R_E \| r_e}$$

Output Impedance:

$$\boxed{Z_o = R_C}$$

Common-Base (CB) Configuration

Gain Calculations

Voltage Gain (Av):

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

Current Gain (Ai):

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

Voltage & Current gain

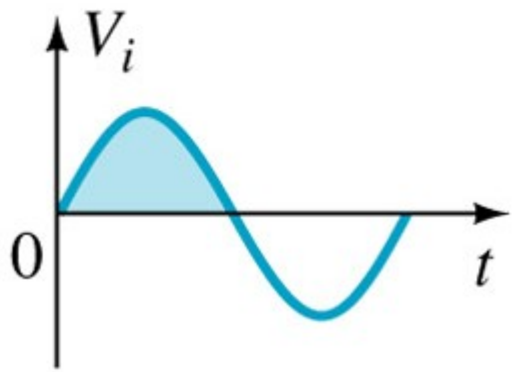
$$V_o = -I_o R_C = -(-I_c R_C)$$
$$= \alpha I_e R_C$$
$$I_e = \frac{V_i}{r_e}$$
$$V_o = \alpha \left(\frac{V_i}{r_e} \right) R_C$$
$$\therefore A_V = \frac{V_o}{V_i} = \alpha \frac{R_C}{r_e} \cong \frac{R_C}{r_e}$$

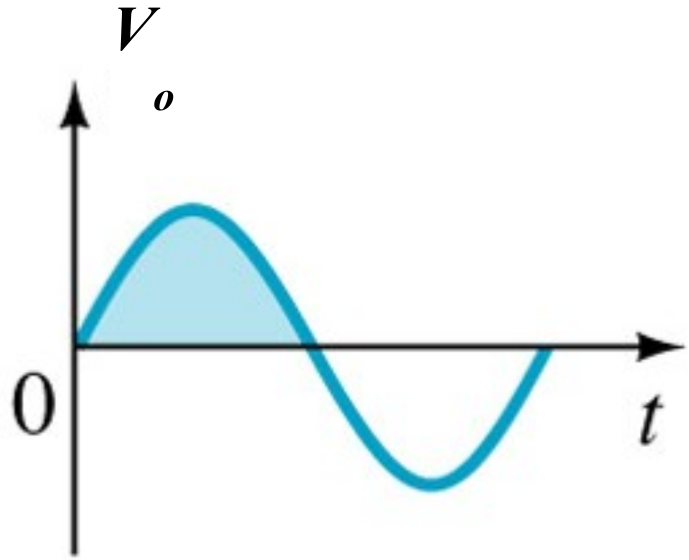
$$I_e = I_i$$
$$I_o = -\alpha I_e = -\alpha I_i$$
$$\therefore A_i = \frac{I_o}{I_i} = -\alpha = -1$$

Common-Base (CB) Configuration

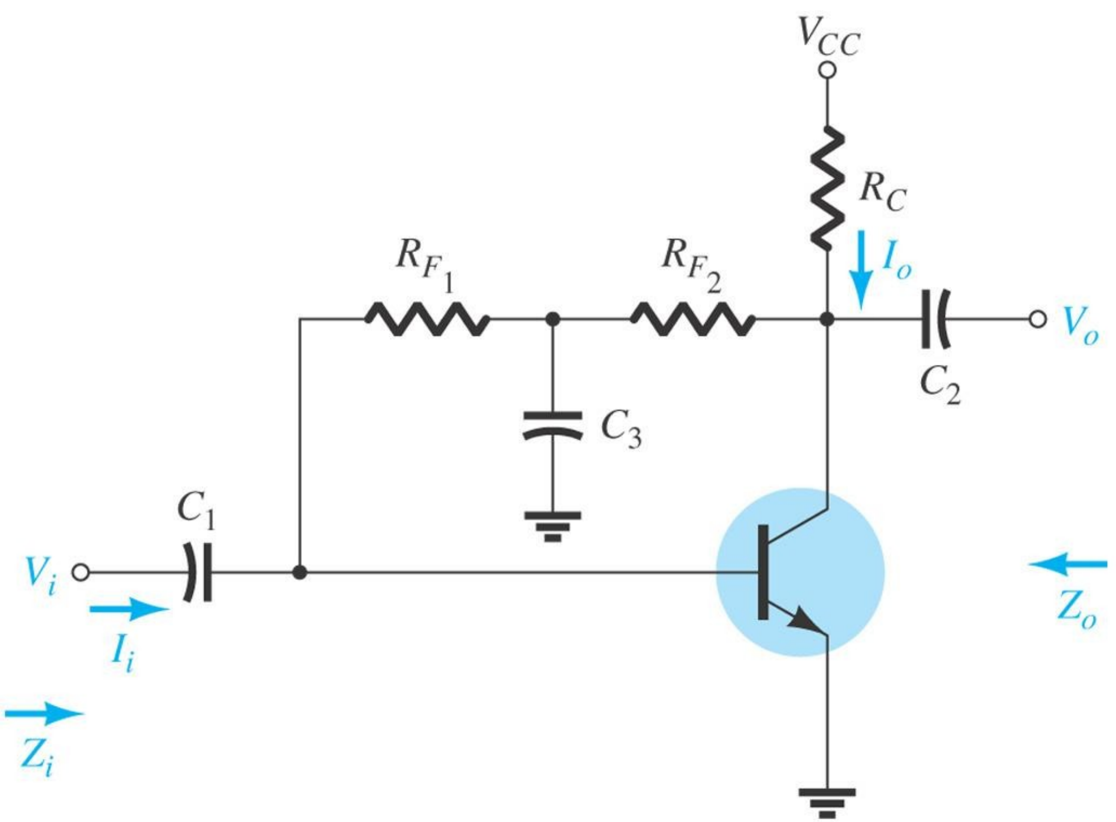
Phase Relationship

A CB amplifier configuration has no phase shift between input and output.





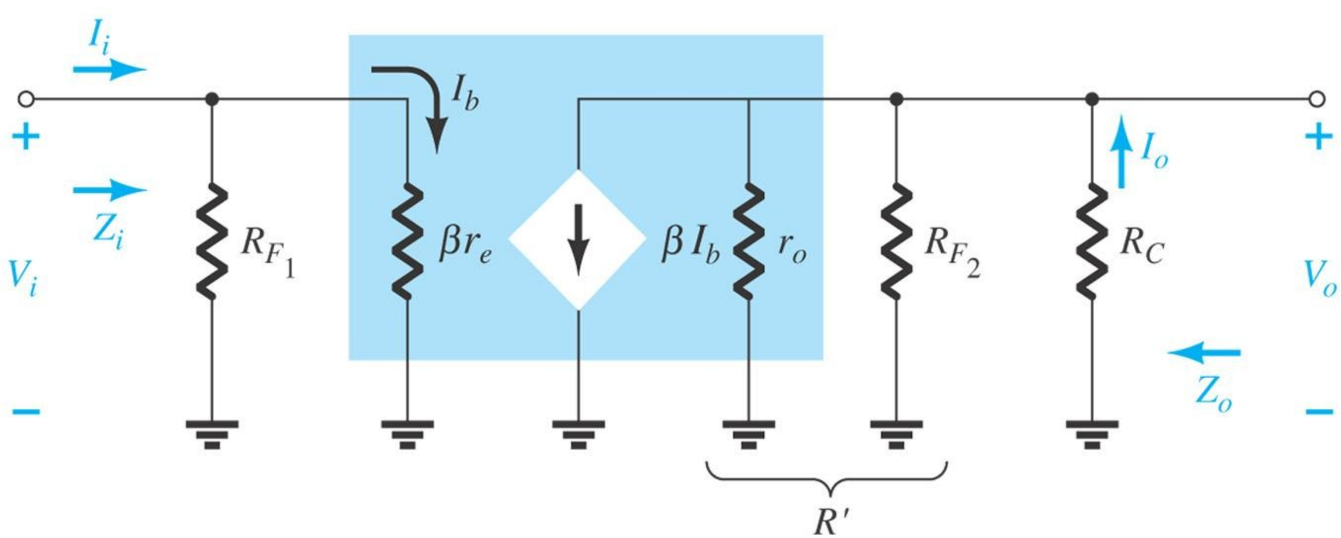
Collector DC Feedback Configuration



The network has a dc feedback resistor for increased stability, yet the capacitor C_3 will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of R_F shifted to the input or output side will be determined by the desired ac input and output resistance levels.

Collector DC Feedback Configuration

Impedance Calculations



Substituting the *re* equivalent circuit into the ac equivalent network

Input Impedance:

$$\boxed{Z_i = R_{F1} \parallel \beta r_e}$$

Output Impedance:

$$\boxed{Z_o = R_C \parallel R_{F2} \parallel r_o}$$

$$\boxed{Z_o \cong R_C \parallel R_{F2}}$$

Collector DC Feedback Configuration

Voltage Gain

$$R' = r_o \,\|\, R_{F2} \,\|\, R_C$$

$$V_o = -\beta I_b R'$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

$$\therefore A_v = \frac{V_o}{V_i} = -\frac{r_o \,\|\, R_{F2} \,\|\, R_C}{r_e}$$

for $r_o \geq 10R_C$,

$$\therefore A_v = \frac{V_o}{V_i} = -\frac{R_{F2} \,\|\, R_C}{r_e}$$

Collector DC Feedback Configuration

Current Gain

For the input side

$$I_b = \frac{R_F I_i}{R_F + \beta r_e} \quad \text{or} \quad \frac{I_b}{I_i} = \frac{R_F}{R_F + \beta r_e}$$

and for the output side using $R' = r_o \parallel R_{F2}$

$$I_o = \frac{R' \beta I_b}{R' + R_C} \quad \text{or} \quad \frac{I_o}{I_b} = \frac{R' \beta}{R' + R_C}$$

the current gain,

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i} = \frac{R' \beta}{R' + R_C} \, \frac{R_{F1}}{R_F + \beta r_e}$$

$$\therefore A_i = \frac{I_o}{I_i} = \frac{R' \beta R_{F1}}{(R' + R_C)(R_{F1} + \beta r_e)}$$

since R_{F1} is usually much larger than βr_e, $R_{F1} + \beta r_e \cong R_{F1}$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_{F1} (r_o \parallel R_{F2})}{R_{F1} \left((r_o \parallel R_{F2}) + R_C \right)}$$

$$\therefore A_i = \frac{I_o}{I_i} \cong \frac{\beta}{1 + \dfrac{R_C}{r_o \parallel R_{F2}}}$$

$$\text{or } \therefore A_i = \frac{I_o}{I_i} = -A_v \frac{Z_i}{R_C}$$

Approximate Hybrid Equivalent Circuit

The h-parameters can be derived from the re model:

$h_{ie} = \beta r_e$ $\qquad$ $h_{ib} = r_e$

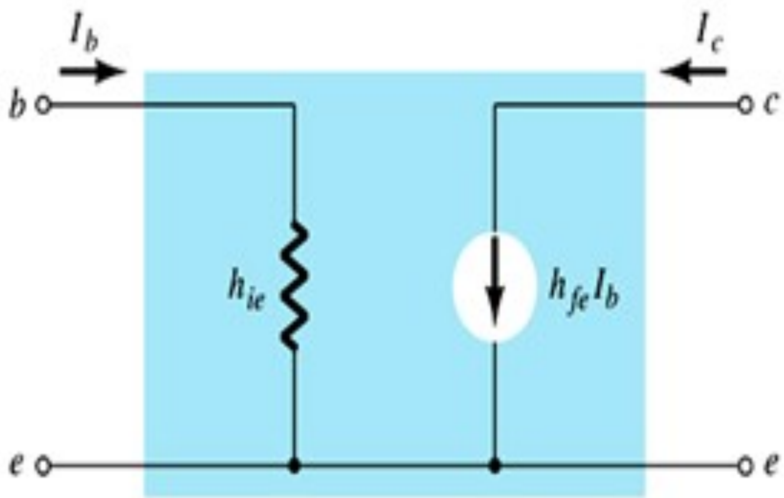
$h_{fe} = \beta$ $\qquad$ $h_{fb} = -\alpha$

$h_{oe} = 1/r_o$

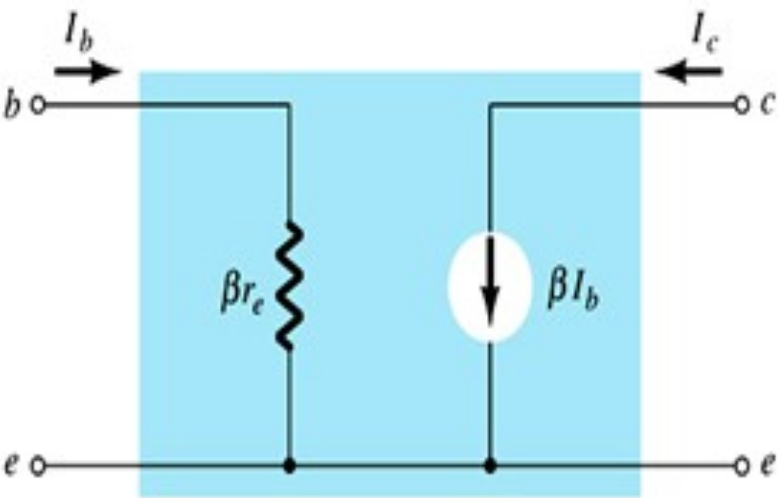
The h-parameters are also found in the specification sheet for the transistor.

Approximate Common-Emitter Equivalent Circuit

Hybrid equivalent model

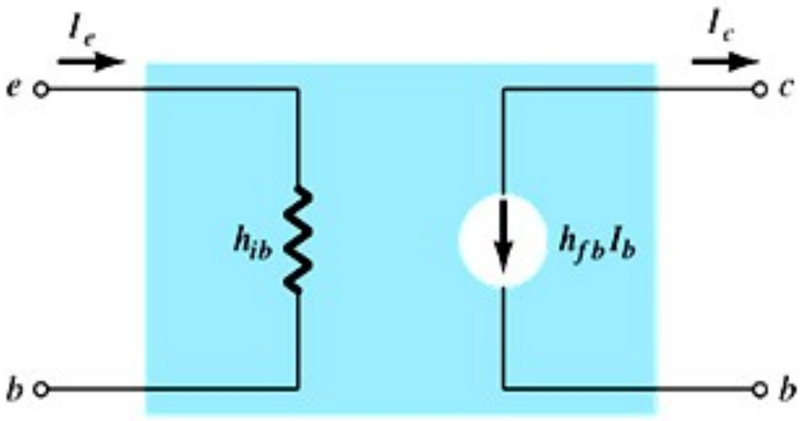


re equivalent model

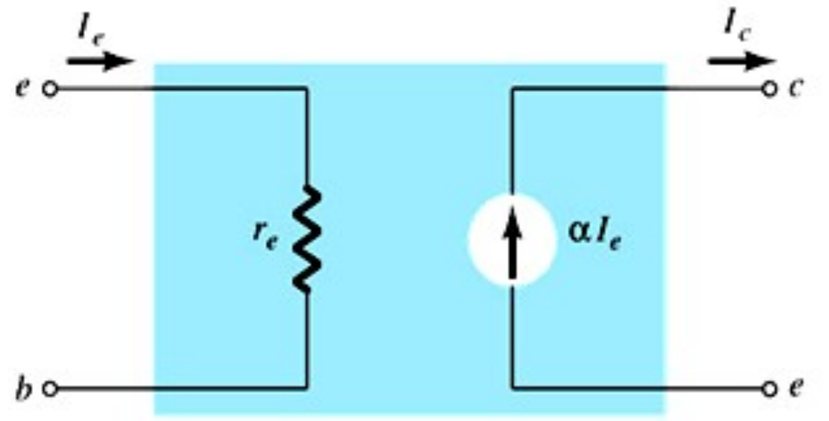


Approximate Common-Base Equivalent Circuit

Hybrid equivalent model



re equivalent model



Troubleshooting

1. Check the DC bias voltages – if not correct check power supply, resistors, transistor. Also check to ensure that the coupling capacitor between amplifier stages is OK.

2. Check the AC voltages – if not correct check transistor, capacitors and the loading effect of the next stage.

Practical Applications

- Audio Mixer
- Preamplifier
- Random-Noise Generator
- Sound Modulated Light Source

ANALOG CIRCUITS

Presented By,
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Assistant Professor,
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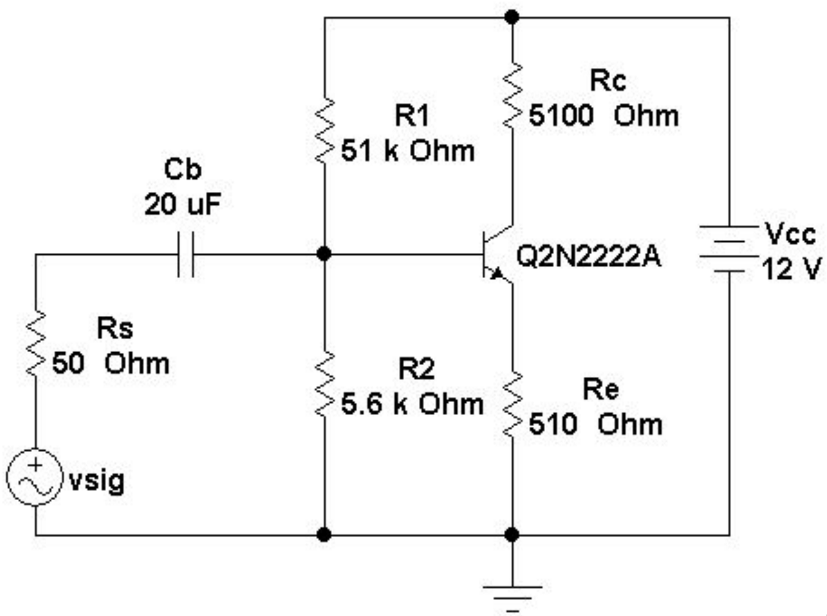
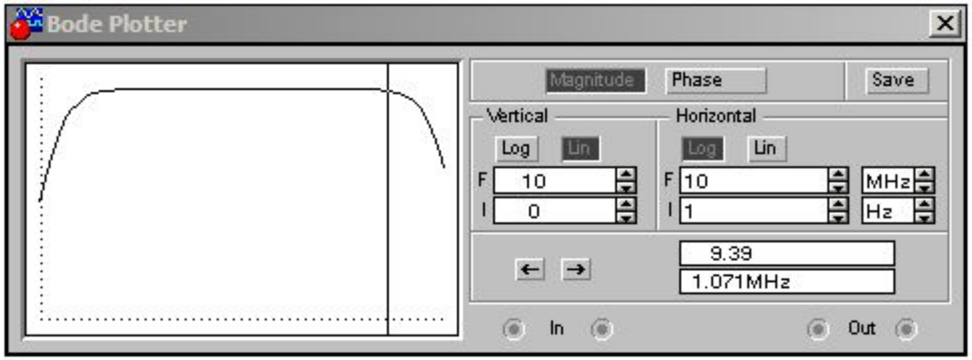
High Frequency BJT Model

Gain of 10 Amplifier – Non-ideal Transistor



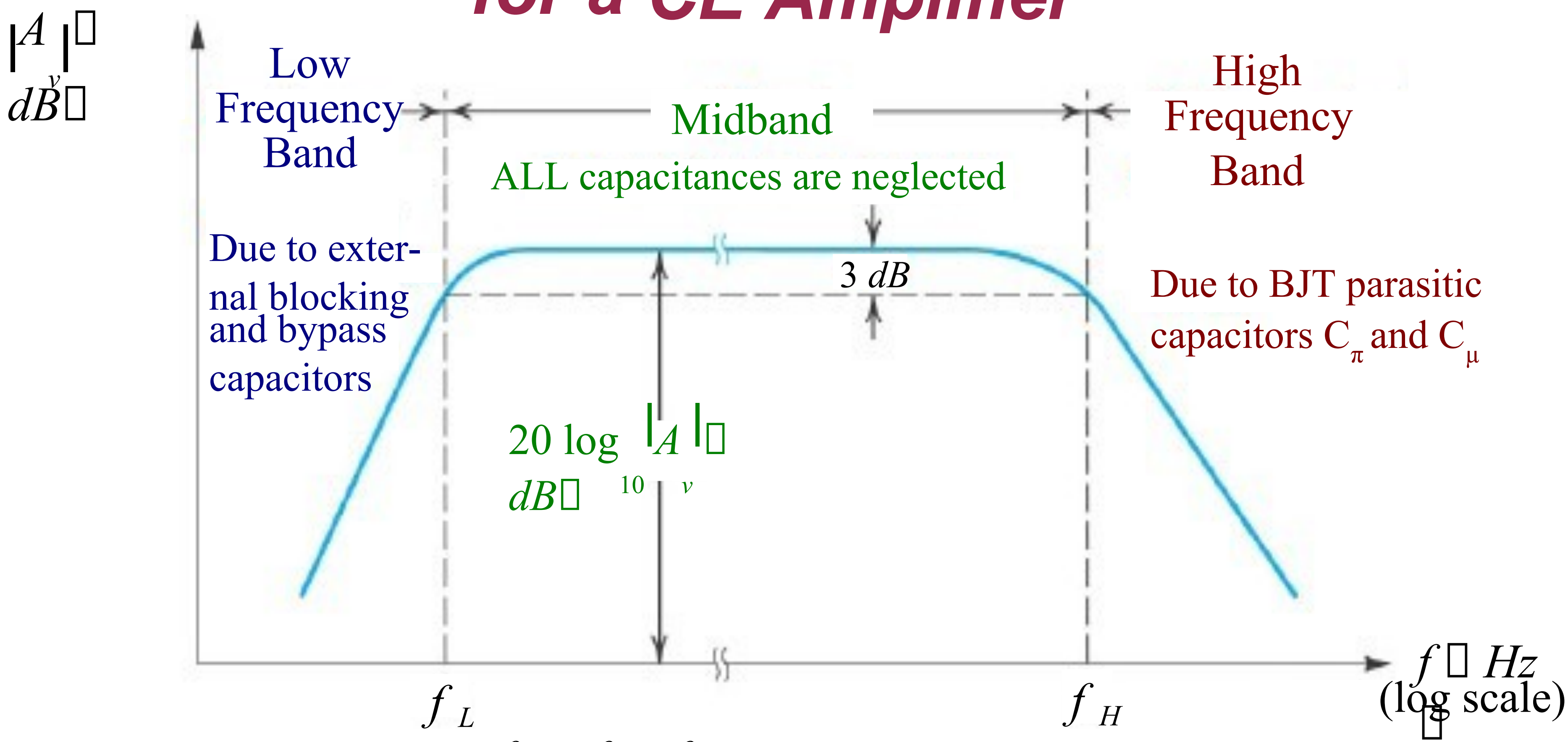


Gain starts dropping at about 1MHz.

Why!

Because of internal transistor capacitances that we have ignored in our models.

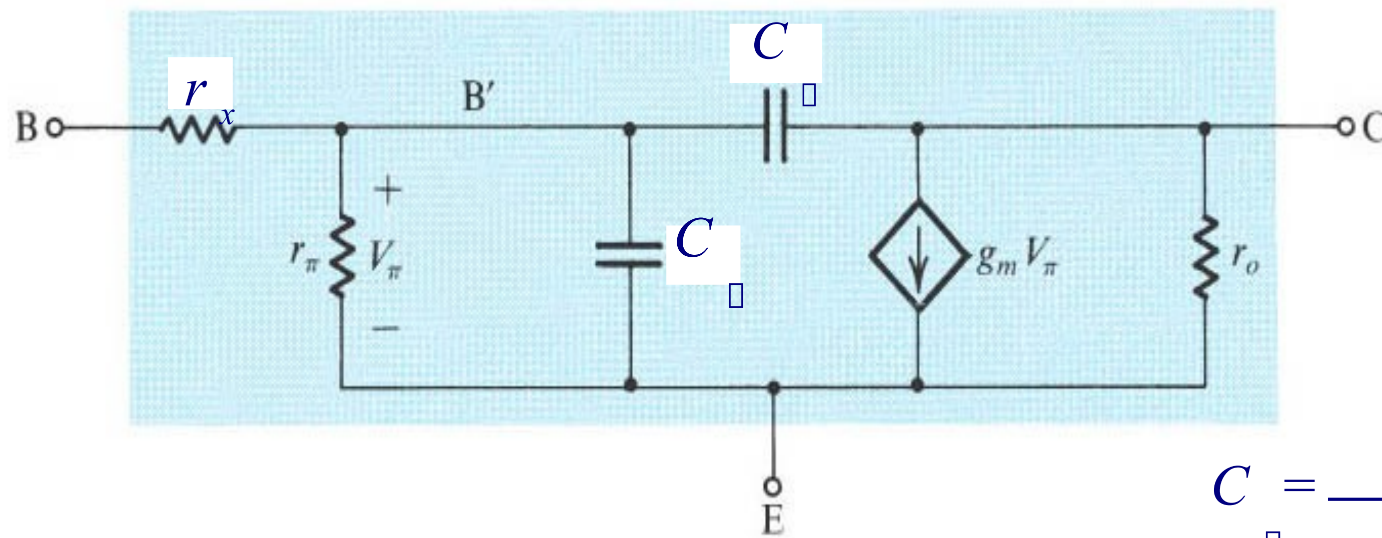
Sketch of Typical Voltage Gain Response for a CE Amplifier



$$BW = f_H - f_L \approx f_H$$

$$GBP = |A_v| BW$$

High Frequency Small-signal Model



SPICE
CJC = $C_{\mu 0}$
CJE = C_{je0}
TF = τ_F
RB = r_x

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m}$$

Two capacitors and a resistor added.

A base to emitter capacitor, C_π

A base to collector capacitor, C_μ

A resistor, r_x , representing the base terminal resistance ($r_x << r_\pi$)

$$C_\pi = C_{de} + \frac{C_{je0}}{\left(1 - \frac{V_{BE}}{V_{0e}}\right)^m} \approx C_{de} + 2\,C_{je0}$$

$$C_{de} = \tau_F\, g_m$$

τ_F = forward-base transit time

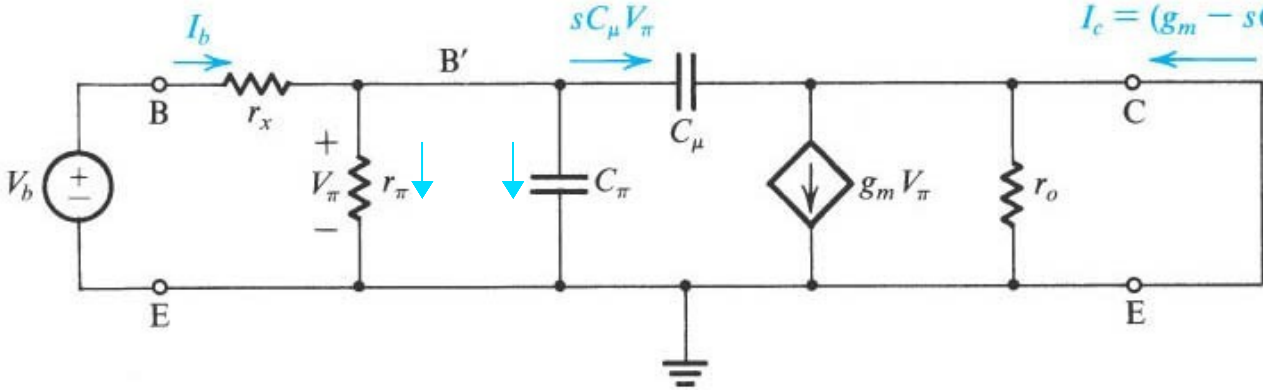
High Frequency Small-signal Model

The internal capacitors on the transistor have a strong effect on circuit high frequency performance! They attenuate base signals, decreasing v_{be} since their reactance approaches zero (short circuit) as frequency increases.

As we will see later C_μ is the principal cause of this gain loss at high frequencies. At the base C_μ looks like a capacitor of value $k\,C_\mu$ connected between base and emitter, where $k > 1$ and may be $>> 1$.

This phenomenon is called the *Miller Effect*.

Frequency-dependent "beta" h_{fe}



short-circuit current

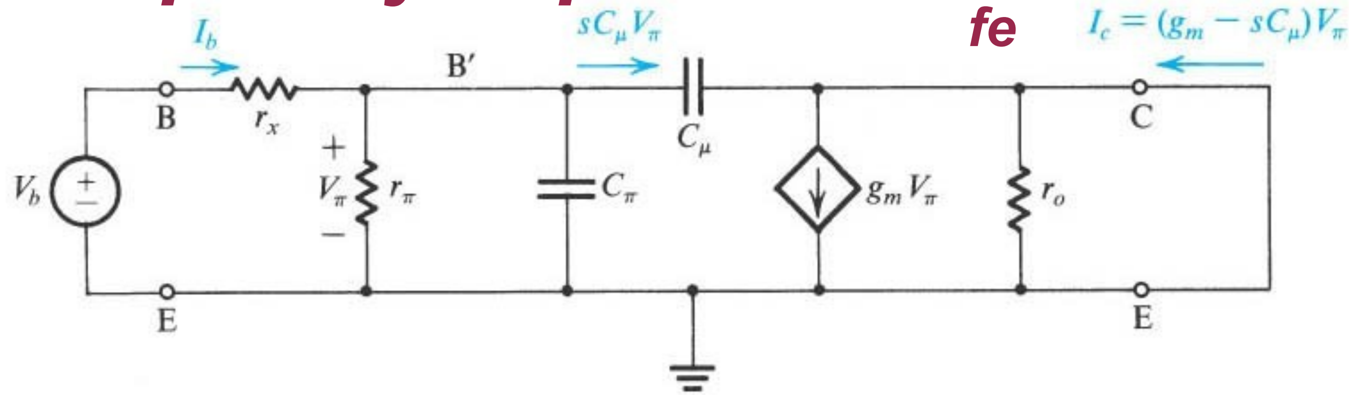
The relationship $i_c = \beta i_b$ does not apply at high frequencies $f > f_H$!

Using the relationship $i_c = f(V_\pi)$ – find the new relationship between i_b and i_c. For i_b (using *phasor notation* (I_x & V_x) *for frequency domain analysis*):

@ node B': $I_b = \left(\dfrac{1}{r_\pi} + sC_\pi + sC_\mu\right)V_\pi$ where $r_x \approx 0$ (ignore r_x)

$NOTE$: $s = \sigma + j\omega$, in sinusoidal steady-state $s = j\omega$.

Frequency-dependent h_{fe} or "beta"



$I_b = \left(\frac{1}{r_\pi} + sC_\pi + sC_\mu\right)V_\pi$ @ node C: $I_c = (g_m - sC_\mu)V_\pi$ (ignore r_o)

Leads to a new relationship between the I_b and I_c:

$$\boxed{h_{fe} = \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{\frac{1}{r_\pi} + sC_\pi + sC_\mu}}$$

Frequency Response of h_{fe}

$$h_{fe} = \frac{g_m - sC_\mu}{\frac{1}{r_\pi} + sC_\pi + sC_\mu}$$

multiply N&D by r_π and set $s = j\omega$

$$h_{fe} = \frac{(g_m - j\omega C_\mu)\, r_\pi}{1 + j\omega (C_\pi + C_\mu)\, r_\pi}$$

factor N to isolate g_m

$$h_{fe} = \frac{\left(1 - j\omega \frac{C_\mu}{g_m}\right) g_m r_\pi}{1 + j\omega (C_\pi + C_\mu)\, r_\pi}$$

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta V_T}{I_C}$$

For small $\omega = \omega_{low}$: $\omega_{low} \frac{C_\mu}{g_m} \ll 1 \; (\frac{1}{10})$

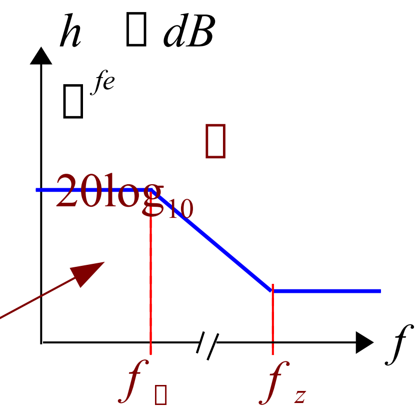
and: $\omega_{low} (C_\pi + C_\mu)\, r_\pi \ll 1 \; (\frac{1}{10})$

Note: $\omega_{low} (C_\pi + C_\mu)\, r_\pi = \omega_{low} (C_\pi + C_\mu) \frac{\beta}{g_m} \gg \omega_{low} \frac{C_\mu}{g_m}$

We have: $\boxed{h_{fe} = g_m r_\pi = \beta}$

Frequency Response of h_{fe} cont.

$$h_{fe} = \frac{\left(1 - j\omega \frac{C_\mu}{g_m}\right) g_m r_\pi}{1 + j\omega (C_\pi + C_\mu) r_\pi} = \beta_0 \left(\frac{1 - j\frac{f}{f_z}}{1 + j\frac{f}{f_\beta}} \right), \quad g_m r_\pi = \beta_0$$



$$(C_\pi + C_\mu) r_\pi = (C_\pi + C_\mu) \frac{\beta_0}{g_m} \gg \frac{C_\mu}{g_m} \Rightarrow f_z \gg f_\beta$$

Hence, the lower break frequency or $-3dB$ frequency is f_β

$$f_\beta = \frac{1}{2\pi (C_\pi + C_\mu) r_\pi} = \frac{g_m}{2\pi \beta_0 (C_\pi + C_\mu)}$$

the upper: $f_z = \dfrac{1}{2\pi C_\mu / g_m} = \dfrac{g_m}{2\pi C_\mu}$

where $f_z \geq 10 f_\beta$

Frequency Response of h_{fe} cont.

Using Bode plot concepts, for the range where: $f \ll f_{\beta}$

$$h_{fe} = g_m r_{\pi}$$

For the range where: $f_{\beta} \ll f \ll f_z$ s.t. $|1 - jf/f_z| \approx 1$

We consider the frequency-dependent numerator term to be 1 and focus on the response of the denominator:

$$h_{fe} = \frac{g_m r_{\pi}}{\left(1 + j\frac{f}{f_{\beta}}\right)}$$

Frequency Response of h_{fe} cont.

Neglecting numerator term: $h_{fe} = \dfrac{g_m r_\pi}{1 + j\dfrac{f}{f_\beta}} = \dfrac{\beta_0}{1 + j\dfrac{f}{f_\beta}}$

And for $f/f_\beta >> 1$ (but $< f/f_z$): $|h_{fe}| \approx \dfrac{\beta_0}{\dfrac{f}{f_\beta}} = \beta_0 \dfrac{f_\beta}{f}$

Unity gain bandwidth: $|h_{fe}| = 1 \Rightarrow \beta_0 \dfrac{f_\beta}{f}\Big|_{f = f_T} = 1 \Rightarrow f_T = \beta_0 f_\beta$

$$\boxed{f_T = \frac{\omega_T}{2\pi} = \beta_0 f_\beta}$$

BJT unity-gain frequency or GBP

Frequency Response of h_{fe} cont.

$\beta = 100 \quad r_{\pi} = 2500\ \Omega \quad C_{\pi} = 12\ pF \quad C_{\mu} = 2\ pF \quad g_m = 40\times10^{-3}\ S$

$$\omega_{\beta} = \frac{1}{(C_{\pi}+C_{\mu})r_{\pi}} = \frac{10^{12}\times10^{-3}}{(12+2)2.5} = 28.57\times10^{6}\ rps$$

$$f_{\beta} = \frac{\omega_{\beta}}{2\pi} = \frac{28.57}{6.28}10^{6}\,Hz = 4.55\ MHz \qquad f_T = \beta f_{\beta} = 455\ MHz$$

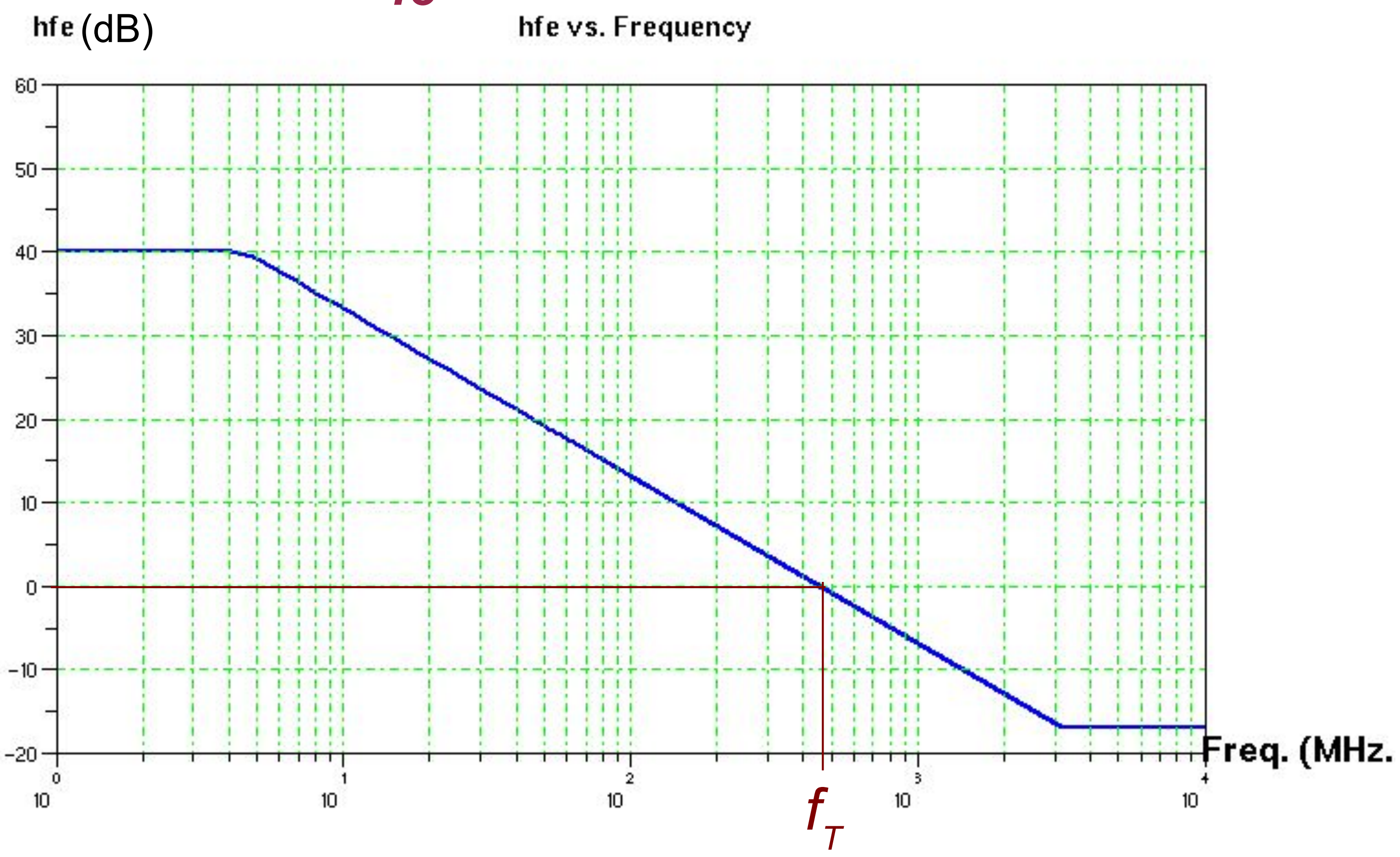
$$\omega_z = \frac{g_m}{C_{\mu}} = \frac{40\times10^{-3}}{2}\times10^{12}\,Hz = 20\times10^{9}\,rps$$

$$f_z = \frac{\omega_z}{2\pi} = 3.18\times10^{9}\,Hz = 3180\ MHz$$

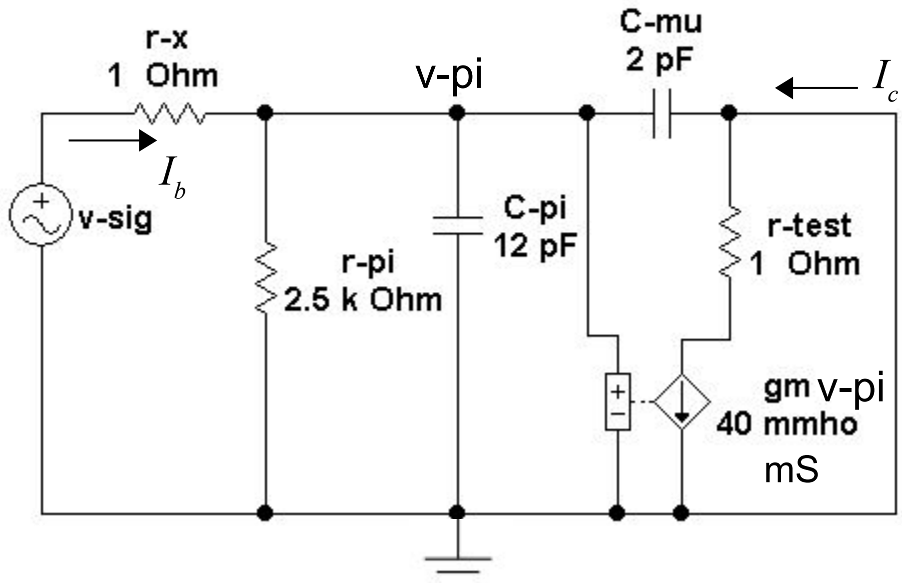
Scilab f_T Plot

```
//fT Bode Plot
Beta=100;
KdB= 20*log10(Beta);
fz=3180;
fp=4.55;
f= 1:1:10000;
term1=KdB*sign(f); //Constant array of len(f)
term2=max(0,20*log10(f/fz));  //Zero for f < fz;
term3=min(0,-20*log10(f/fp)); //Zero for f < fp;
BodePlot=term1+term2+term3;
plot(f,BodePlot);
```

h_{fe} Bode Plot



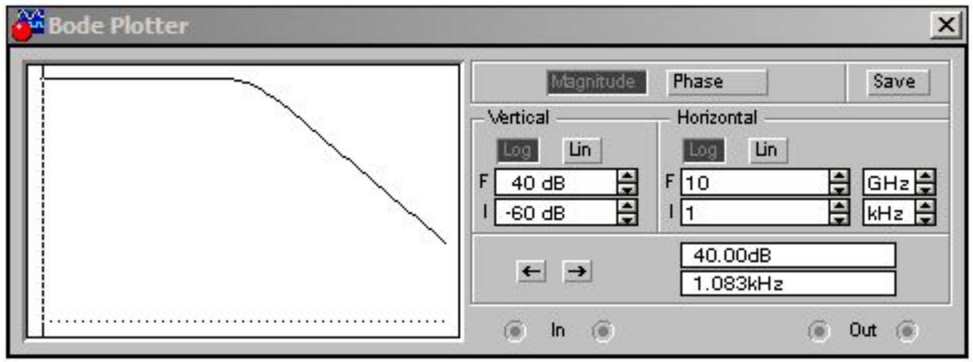
Multisim Simulation



Insert 1 ohm resistors – we want to measure a current ratio.

$$h_{fe} = \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{\frac{1}{r_\pi} + s\left(C_\pi + C_\mu\right)}$$

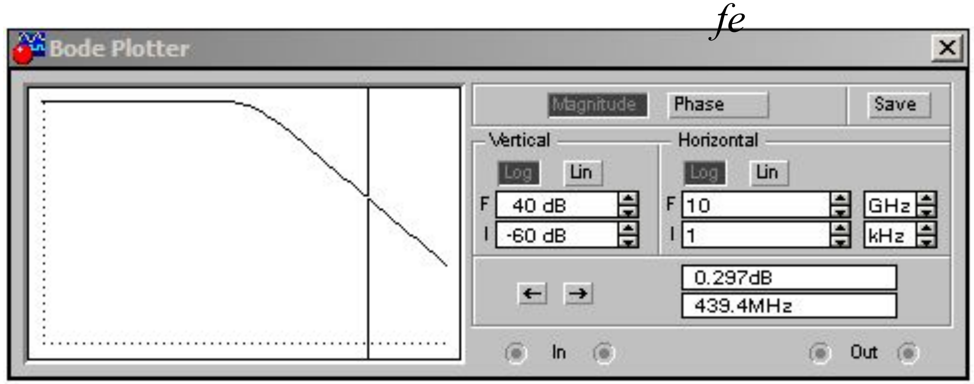
Simulation Results



Low frequency $|h_{fe}|$

Theory:

$f_T = \beta f_\beta = 455\ MHz$



Unity Gain frequency about $\boxed{\text{440 MHz}}$.

ANALOG CIRCUITS

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Assistant Professor,
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Feedback and Oscillators

9.1 Effect of Feedback on Gain

Closed-Loop Gain

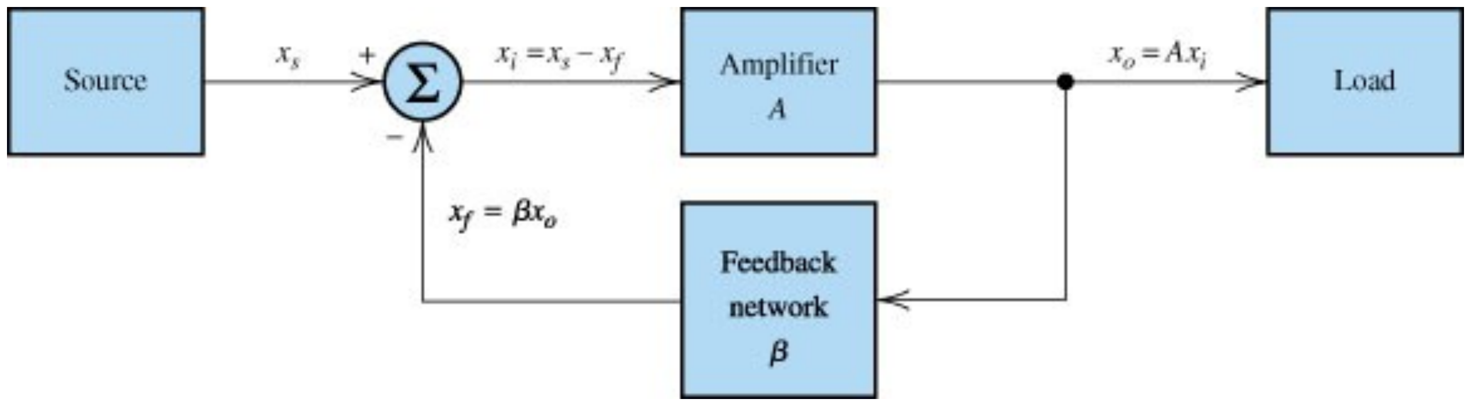


Figure 9.1 Feedback amplifier. Note that the signals are denoted as x_i, x_f, x_o, and so on. The signals can be either currents or voltages.

$$x_i = x_s - \beta x_o$$

$$x_o = A(x_s - \beta x_o)$$

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \qquad (9.1)$$

A_f – **closed-loop gain**;

A – **open-loop gain**;

$A\beta$ – **loop gain**;

If $A\beta > 0$ – **negative feedback**;

if $A\beta < 0$ – **positive feedback.**

Problems Associated With Positive Feedback

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \qquad (9.1)$$

1. Positive feedback:

Let A = -10; β = 0.099. $\boldsymbol{A_f = -10^4}$.

Let A = -9.9; β = 0.099. $\boldsymbol{A_f = -901}$.

1% change of A causes 91% change of A_f.

2. Negative feedback:

Let $A = 10^4$; β = 0.01. $\boldsymbol{A_f = 100}$.

Let A = 9000; β = 0.01. $\boldsymbol{A_f = 98.9}$.

10% change of A causes 1% change of A_f.

Conclusion: *Positive feedback* increases the gain, but the gain is unstable. In contrast *negative feedback* decreases the gain and stabilizes it.

Gain Stabilization

$$\frac{dA_f}{dA} = \frac{1 + A\beta - A\beta}{(1 + A\beta)^2} = \frac{1}{(1 + A\beta)^2}$$

$$dA_f = \frac{dA}{A}\frac{A}{(1 + A\beta)^2}; \quad A_f = \frac{A}{1 + A\beta}$$

$$dA_f = \frac{dA}{A}\frac{A_f}{(1 + A\beta)}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{(1 + A\beta)} \qquad (9.2)$$

dA_f/A_f – relative instability of the closed-loop gain;

dA/A – relative instability of the open-loop gain.

Exercise

9.2 (a) An amplifier has $A = 10^5 \pm 10\ \%$. Suppose that we want a feedback amplifier with A_f that varies by no more than $\pm 1\ \%$ due to variations in A. What is the maximum value of nominal gain A_f allowed?
(b) Repeat if A_f is allowed to vary by only $\pm 0.1\ \%$.

Solution:

(a) In (9.2)

$$\frac{dA_f}{A_f} = \frac{dA}{A}\frac{1}{(1 + A\beta)} \qquad (9.2)$$

$$\frac{dA}{A} = 10\% = 0.1; \qquad \frac{dA_f}{A_f} = 1\% = 0.01$$

$$0.1 = 0.01\frac{1}{(1 + A\beta)} \Rightarrow (1 + A\beta) = 10;$$

Since $A = 10^5$ the maximum gain with variation less than 1% is

$$A_f = \frac{A}{1 + A\beta} = \frac{10^5}{10} = 10^4$$

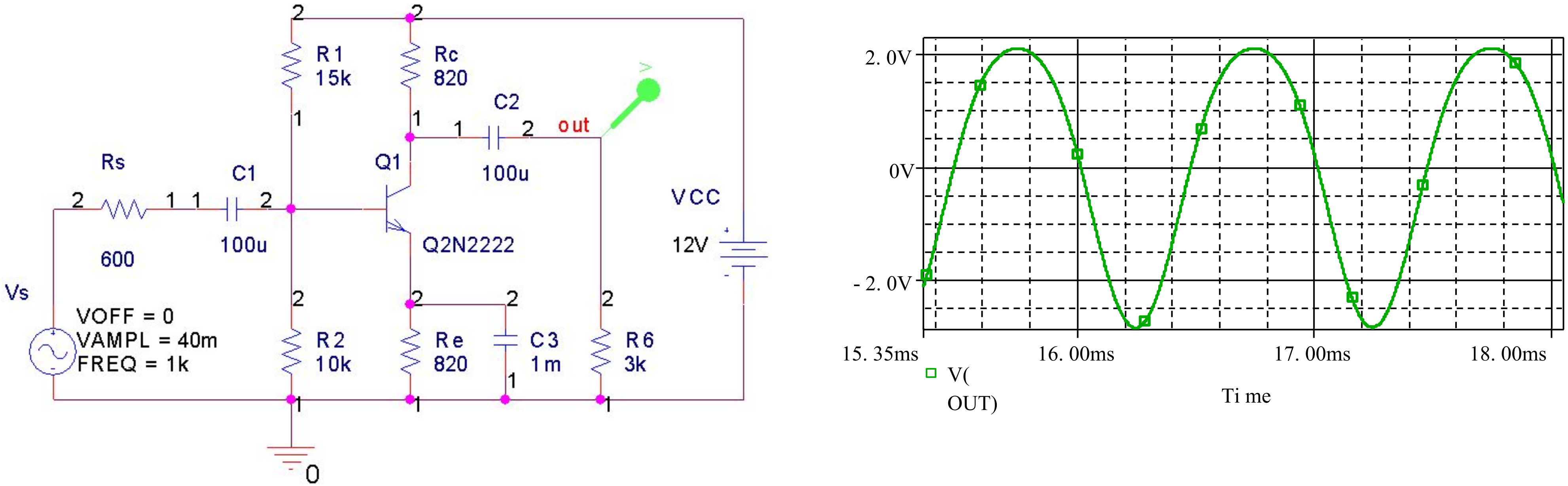
(b)

$$\frac{dA}{A} = 10\% = 0.1; \qquad \frac{dA_f}{A_f} = 0.1\% = 0.001$$

$$0.1 = 0.001\frac{1}{(1 + A\beta)} \Rightarrow (1 + A\beta) = 100;$$

$$A_f = \frac{A}{1 + A\beta} = \frac{10^5}{100} = 10^3$$

9.2 Reduction of Nonlinear Distortion and Noise



A circuit of common-emitter amplifier from BAC exercises (Exercise 8) and its output waveshape. The signal at the output is distorted.

The distortion of the output signal is basically due to the curvature of the input characteristic of the BJT.

The output signal is not any more sinusoidal and has harmonics.

Figure of merit of the distortion: the amplitudes of the harmonics.

Total harmonic distortion (THD:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1}$$

V_1 – amplitude of the fundamental harmonic;

V_2, V_3,… -amplitudes of the higher harmonics.

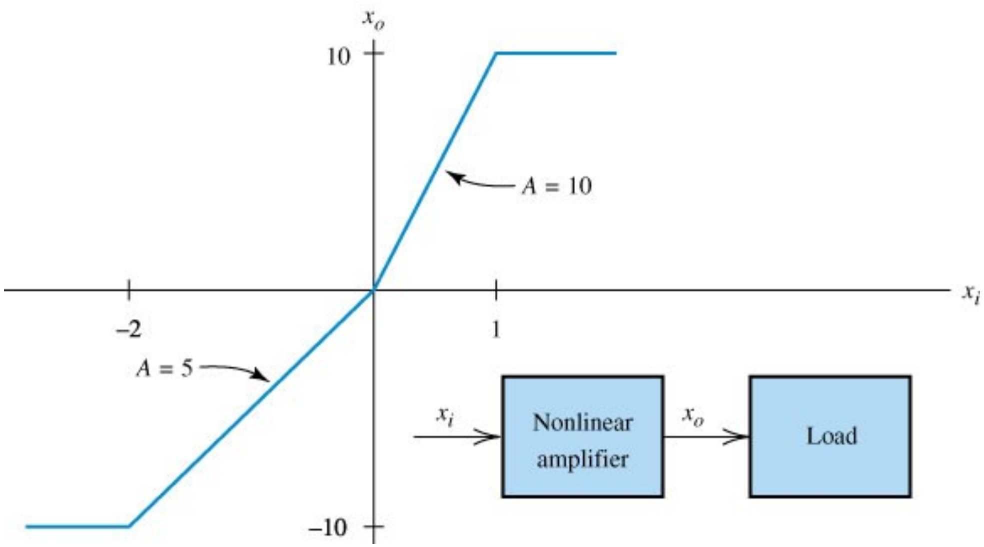


Figure 9.2 Transfer characteristic of a certain nonlinear amplifier.

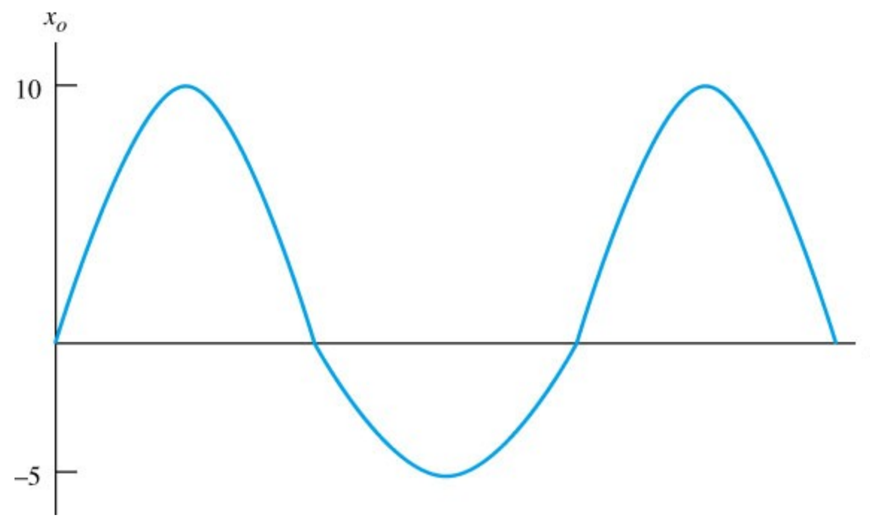


Figure 9.3 Output of amplifier of Figure 9.2 for $x_{in} = \sin(\omega t)$. Notice the distortion resulting from the nonlinear transfer characteristic.

Gain of the nonlinear amplifier in Figure 9.2:

- if $0 < x_i < 10$; $A = 10$;
- if $-10 < x_i < 0$; $A = 5$.

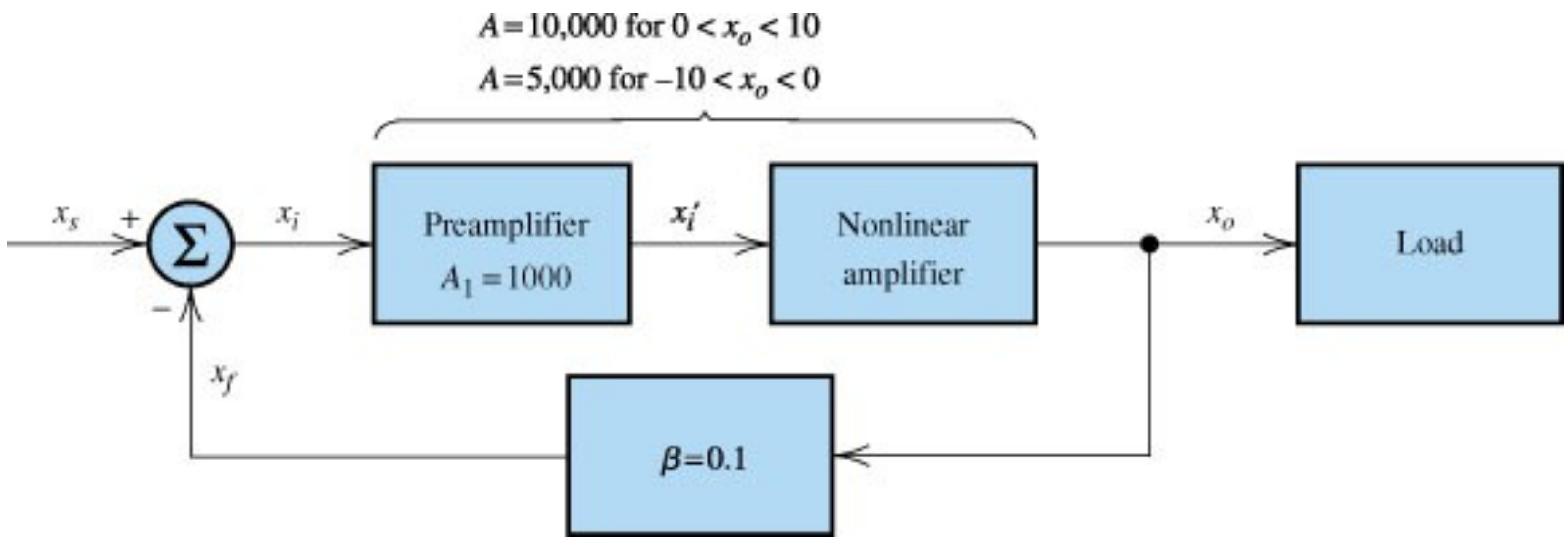


Figure 9.4 Addition of a linear high-gain preamplifier and negative feedback to reduce distortion.

Open loop gain of the cascade of preamplifier and nonlinear amplifier:

- if $0 < x_i < 10$; $A = 10_4$;
- if $-10 < x_i < 0$; $A = 5000$.

Closed loop gain of the whole amplifier:

- if $0 < x_i < 10$

$$A_f = \frac{A}{1 + A\beta} = \frac{10^4}{1 + 10^4 \times 0.1} = 9.99$$

- if $-10 < x_i < 0$

$$A_f = \frac{A}{1 + A\beta} = \frac{5000}{1 + 5000 \times 0.1} = 9.98$$

Compensatory Distortion of the Input Signal

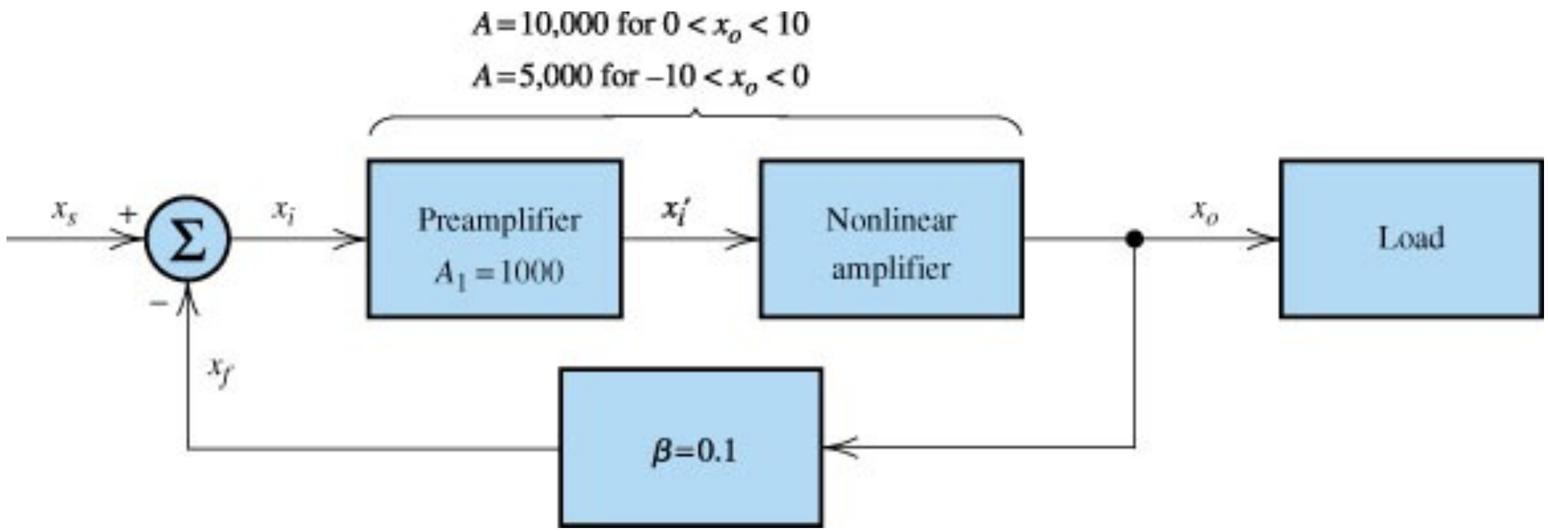


Figure 9.4 Addition of a linear high-gain preamplifier and negative feedback to reduce distortion.

$$x_i = x_s - x_f$$

$$x_i = x_s - x_s \frac{A\beta}{1 + A\beta} \qquad (9.4)$$

$$x_i = x_s \frac{1}{1 + A\beta} \qquad (9.5)$$

$$x_i = x_s / 1001 \quad \text{for} \quad 0 < x_i' < 10^{-3}$$

$$x_i = x_s / 501 \quad \text{for} \quad -2 \times 10^{-3} < x_i' < 0$$

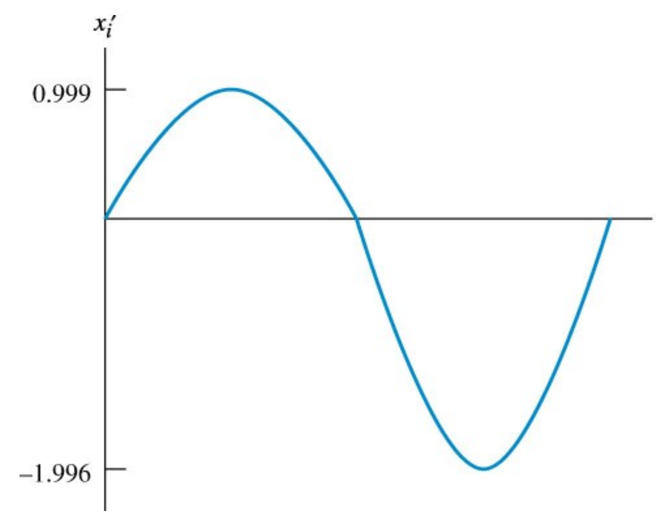


Figure 9.5 Predistorted input signal.

An Example with Crossover Distortion

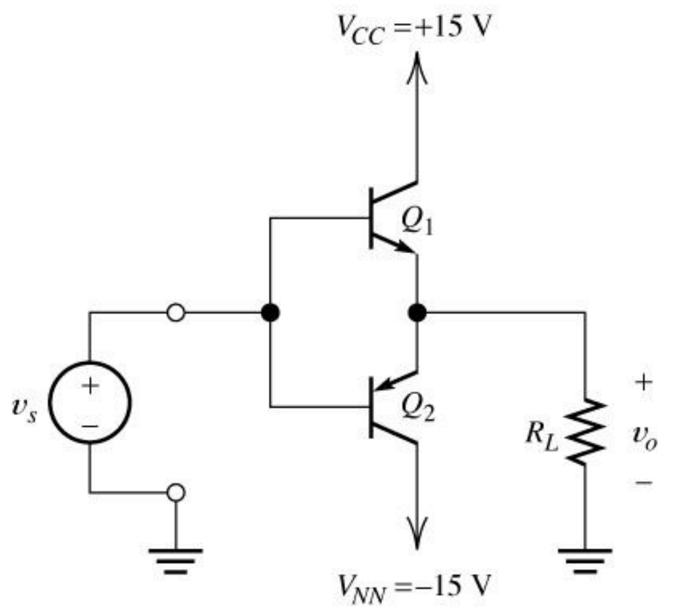


Figure 9.7 Nonlinear class-B power amplifier.

$$v_o = v_s - 0.6 \quad for \quad v_s > 0.6$$

$$v_o \cong v_s + 0.6 \quad for \quad v_s < -0.6$$

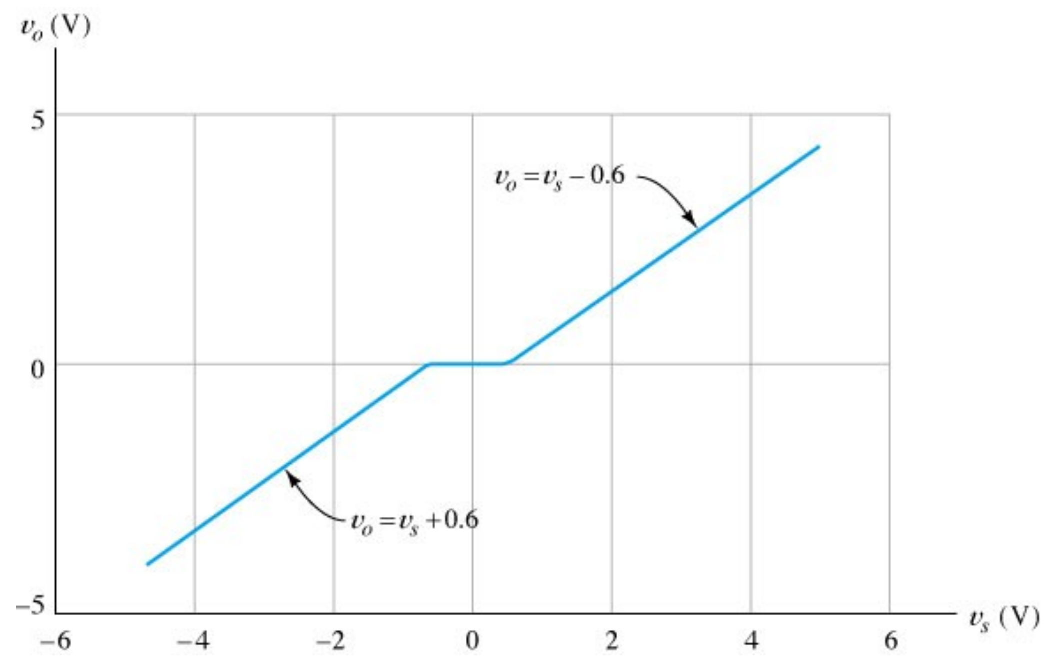
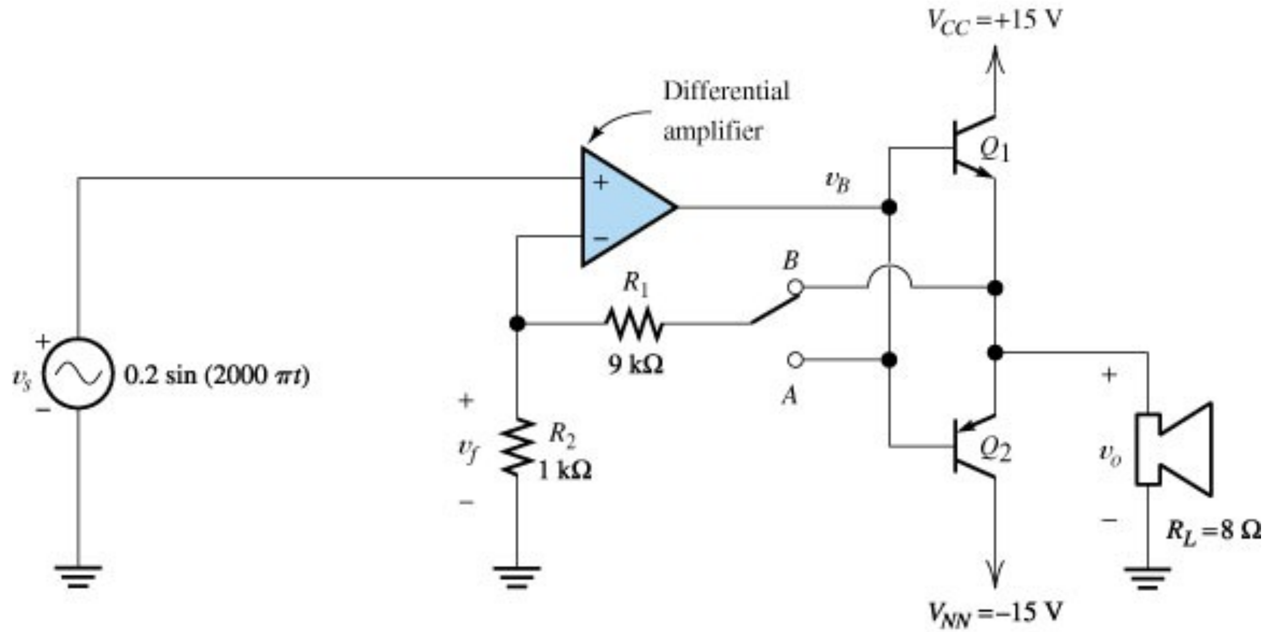


Figure 9.8 Transfer characteristic for the amplifier of Figure 9.7.



(a) Circuit diagram

Figure 9.9a Class-B power amplifier with feedback. The feedback has effect to reduce the distortion if the source of the distortion is included in the feedback loop. In the circuit above the switch must be in position B. If the switch is in position A, the feedback has no effect on the distortion.

Influence of the Feedback on the Noise in Amplifiers

Noise – a random signal, generated in the circuit or penetrating from outside in the circuit. The noise adds to the desired signal and deteriorates its quality. The noise generation in the circuit is basically due to the transfer of the current by charged particles (electrons and holes) and the thermal agitation.

All electronic elements, except capacitors and inductors generate noise.

Generally the **negative feedback doesn't reduce the noise in the amplifier**, since the feedback also generates noise.

The negative feedback can help in some particular cases, when the source of the noise is localized in one stage of the circuit only. Than including this stage in a feedback loop reduces the noise.

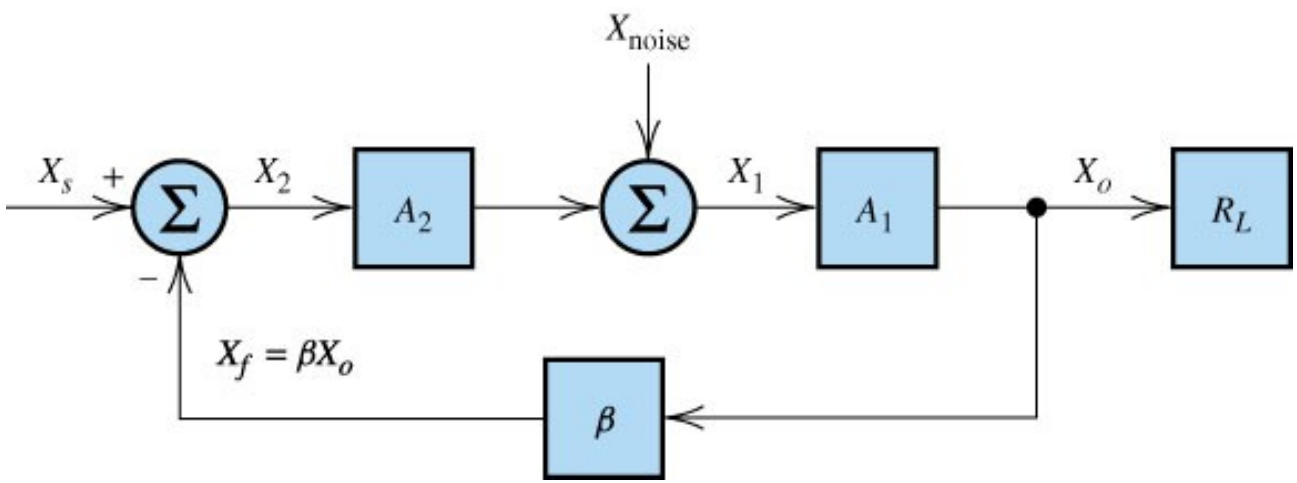


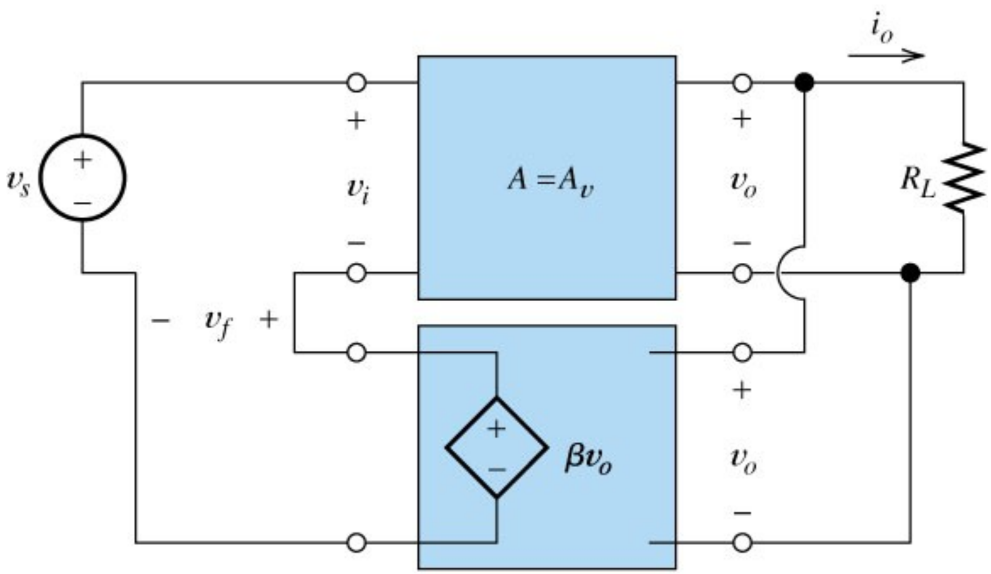
Figure 9.13 Feedback amplifier with a noise source. The noise is generated in one stage of the circuit (A_1) and the feedback can reduce this noise only.

9.3 Input and Output Impedance

Types of Feedback

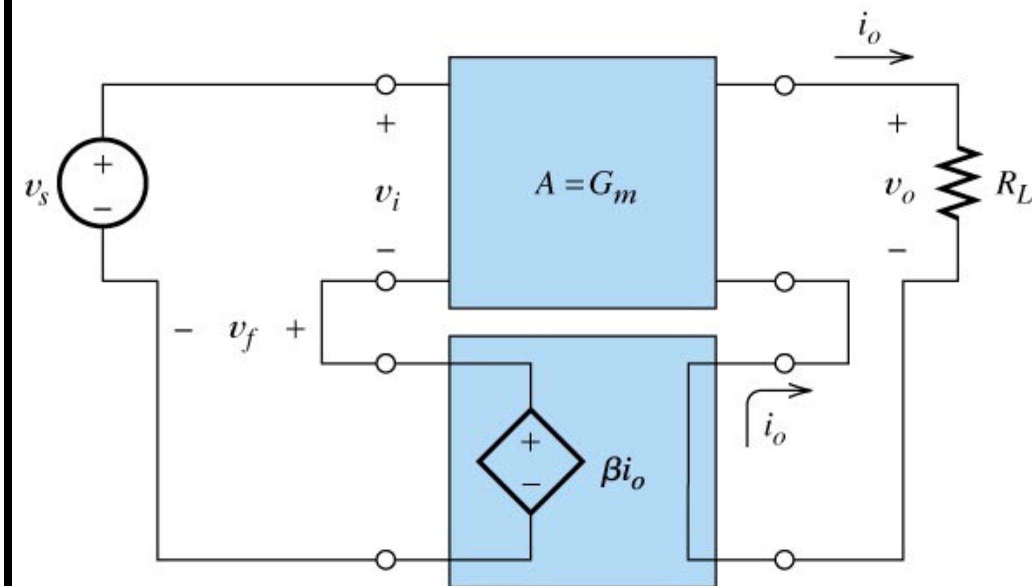
Conditionally the feedback is divided in 4 types:

- series voltage;
- series current;
- parallel voltage;
- parallel current.



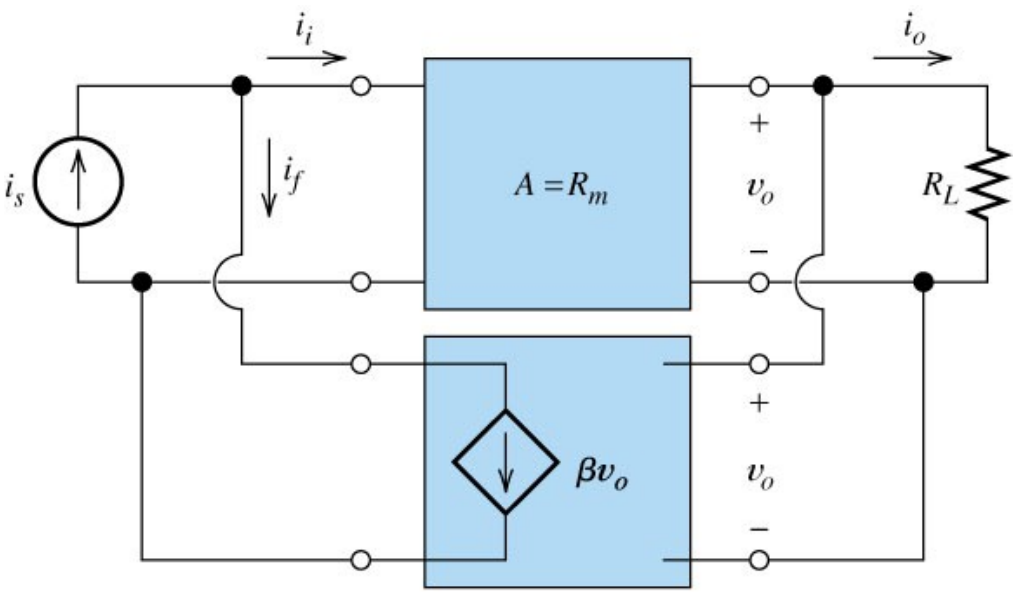
(a) Series voltage feedback

Figure 9.14 Types of feedback. (a) Series voltage feedback.



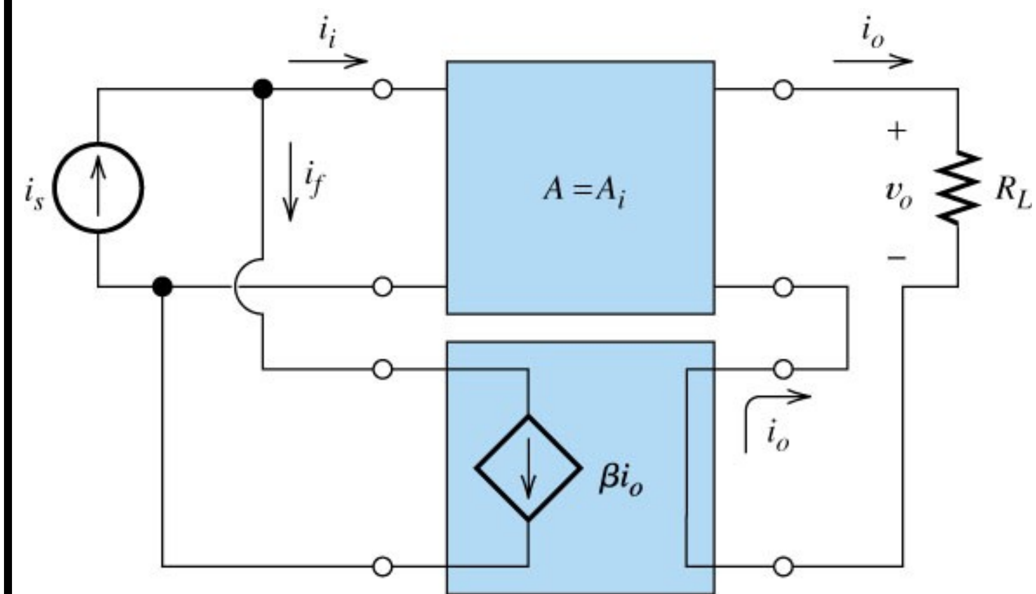
(b) Series current feedback

Figure 9.14 Types of feedback. (b) Series current feedback.



(c) Parallel voltage feedback

Figure 9.14 Types of feedback. (c) Parallel voltage feedback.



(d) Parallel current feedback

Figure 9.14 Types of feedback. (c) Parallel current feedback.

The Effects of Various Types of Feedback on Gain

The general formula

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta}$$

is valid for all feedback types. For the different feedback types the gains assumed as A_f, A and β are different quantities.

For series voltage feedback: $x_o = v_o$, $x_s = v_s$.
A_f, A and β are voltage gains.

For series current feedback: $x_o = i_o$, $x_s = v_s$.
A_f and A are transconductances: $G_m = i_o/v_s$;
β is a transresistance: $\beta = v_f/i_o$.

For parallel voltage feedback: $x_o = v_o$, $x_s = i_s$.
A_f and A are transresistances: $R_m = v_o/i_s$;
β is a transconductance: $\beta = i_f/v_o$.

For parallel current feedback: $x_o = i_o$, $x_s = i_s$.
A_f, A and β are current gains.

The Effects of Series Feedback on Input Impedance

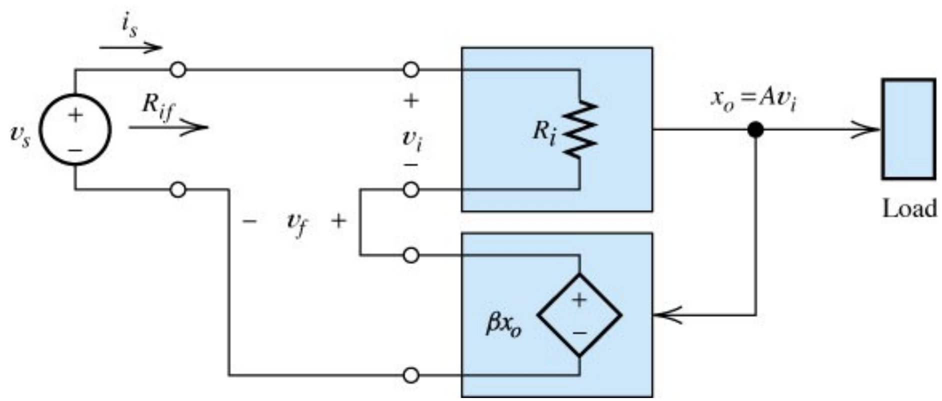


Figure 9.15 Model for analysis of the effect of series feedback on input impedance.

$$R_{if} = \frac{v_s}{i_s} = R_i(1 + A\beta) > R_i$$

The series feedback increases the input impedance.

The Effects of Parallel Feedback on Input Impedance

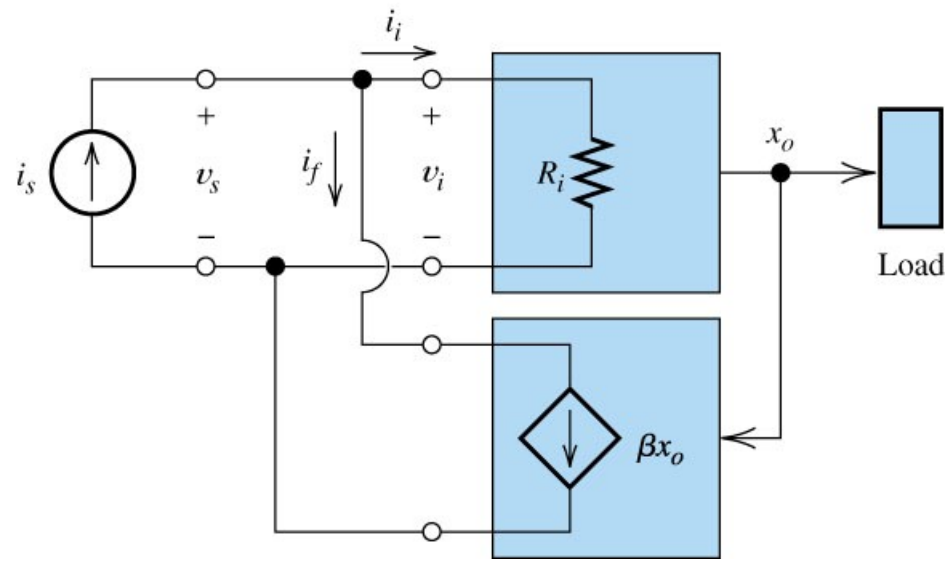


Figure 9.16 Model for analysis of the effect of parallel feedback on input impedance.

$$R_{if} = \frac{v_s}{i_s} = \frac{R_i}{1 + A\beta} < R_i$$

The parallel feedback decreases the input impedance.

The Effects of Voltage Feedback on Output Impedance

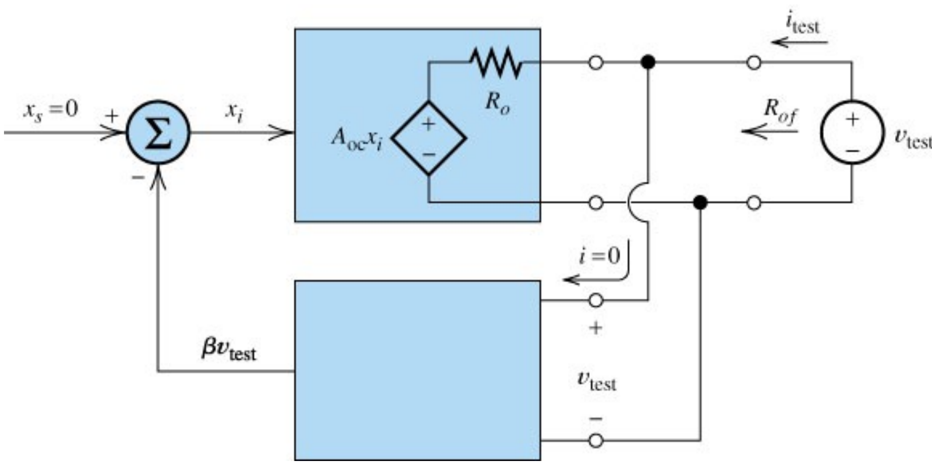


Figure 9.17 Model for the analysis of output impedance with voltage feedback.

$$R_{of} = \frac{v_{test}}{i_{test}} = \frac{R_o}{1 + A\beta} < R_o$$

The voltage feedback decreases the output impedance.

The Effects of Current Feedback on Output Impedance

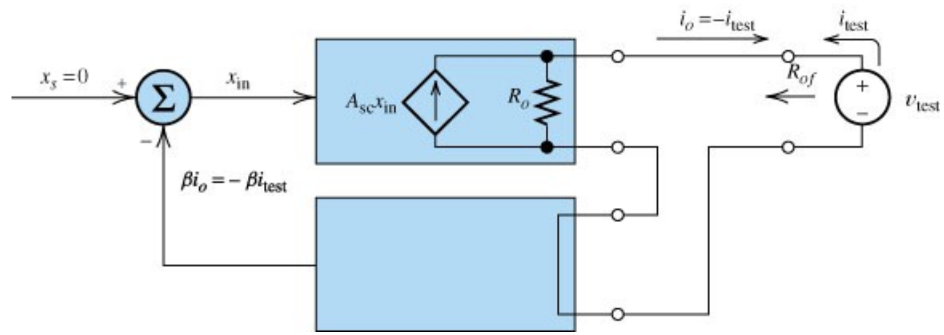


Figure 9.18 Model for the analysis of output impedance with current feedback.

$$R_{of} = \frac{v_{test}}{i_{test}} = R_o(1 + A\beta) > R_o$$

The current feedback increases the output impedance.

9.7 Effect of Feedback on Pole Locations

Dominant - Pole Amplifiers

Poles – roots of the denominator of the gain. Gain is expressed as a function of Laplace transform variable s.

Expression for open-loop gain

$$A(s) = \frac{A_0}{(s/2\pi f_b) + 1} \tag{9.42}$$

If β is constant, the closed-loop gain is

$$A_f(s) = \frac{\dfrac{A_0}{s/(2\pi f_b) + 1}}{1 + \dfrac{A_0 \beta}{s/(2\pi f_b) + 1}}$$

The closed-loop gain can be put into the form

$$A(s) = \frac{A_{0f}}{(s/2\pi f_{bf}) + 1} \tag{9.43}$$

The closed-loop dc gain is

$$A_{0f} = \frac{A_0}{1 + A_0 \beta} \tag{9.44}$$

The closed-loop break frequency

$$f_{bf} = f_b (1 + A_0 \beta) \tag{9.45}$$

Conclusion: **negative feedback increases the upper break frequency of the amplifier.**

Example 9.5 Bode Plots for a Dominant - Pole Amplifier with Feedback

A certain integrated - circuit operational amplifier has a single pole in its gain function. The open - loop dc gain is $A_0 = 10^5$ and the open - loop break frequency is $f_b = 10$ Hz. Prepare magnitude Bode plots for $A(f)$ and $A_f(f)$ if β = 0.01, 0.1, and 1.

Solution:

Open-loop dc gain in dB is

$$A_{0\,\mathrm{dB}} = 20\log_{10}|A_0| = 20\log_{10} 10^5 = 100\mathrm{dB}$$

For β = 0.01

$$A_{0f} = \frac{A_0}{1 + A_0\beta} = \frac{10^5}{1 + 0.01\times10^5} = 99.9 \approx 40dB$$

$$f_{bf} = f_b(1 + A_0\beta) = 10 \times \left(1 + 0.01\times10^5\right) \approx 10\mathrm{kHz}$$

For β = 0.1: A_{0f} = 20dB and f_{bf} = 100kHz.

For β = 1: A_{0f} = 0dB and f_{bf} = 1MHz.

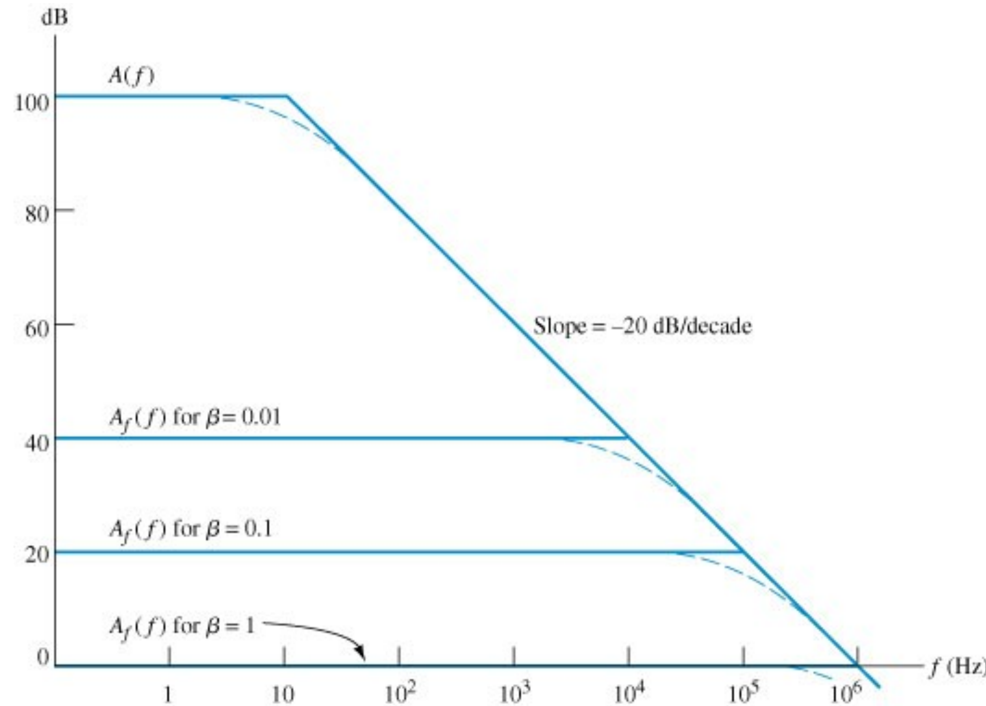


Figure 9.38 Bode plots for the feedback amplifier of, Example 9.5.

Gain Bandwidth Product

$$A_{0f} f_{bf} = \frac{A_0}{1 + A_0 \beta} \times f_b \left(1 + A_0 \beta\right) = A_0 f_b \tag{9.46}$$

The product of dc gain and the bandwidth of an amplifier is independent of the feedback. It is an important parameter of the amplifier and is called **gain-bandwidth product** or **unity gain frequency**.

Influence of Negative Feedback on Amplifiers - Summary

1. **Gain** is decreased and divided by $1 + \beta A$.
2. **Gain stability** is improved. Relative gain variation dA/A is divided by $1 + \beta A$.
3. **Nonlinear distortion** is reduced.
4. In general the **noise** is increased. Only in some particular cases, when the noise source is localized in a part of the amplifier, the negative feedback can reduce the noise from this source.
5. **Input and output impedances** are affected from the feedback. Depending on its type (series or parallel, voltage or current) input and output impedances are increased or decreased.
6. **Upper half-power frequency** is increased and multiplied by $1 + \beta A$.

9.11 Oscillator Principles

Linear Oscillators

Oscillators: circuits, which produce periodic ac signals with prescribed properties: waveform; frequency and amplitude.

Linear oscillators: the output is approximately sinusoidal. The transistors are operating basically in active region.

Switching oscillators: the electronic devices operate like switches. Usually rectangular pulses at the output.

Basic principle of the linear oscillator: part of the output signal is returned at the input of the amplifier via positive feedback loop. The returned signal is enough to produce after amplification the same output signal.

The Barkhausen Criterion

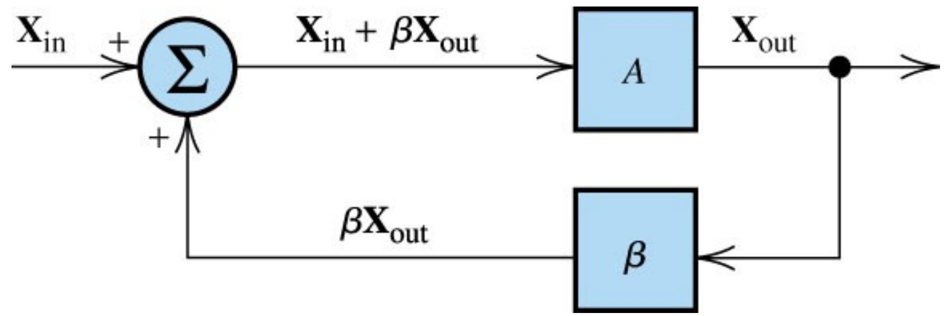


Figure 9.69 Linear oscillator with external signal X_{in} injected.

$$\mathbf{X}_{out} = A(f)\left[\mathbf{X}_{in} + \beta(f)\mathbf{X}_{out}\right] \qquad (9.52)$$

$$\mathbf{X}_{out} = \frac{A(f)}{1 - A(f)\beta(f)}\mathbf{X}_{in} \qquad (9.53)$$

To have output signal when $\mathbf{X}_{in} = 0$, closed-loop gain must be infinity. This is possible if its denominator is 0, i.e.

$$A(f)\beta(f) = 1 \qquad (9.54)$$

Example 9.12 Analysis of an Oscillator Circuit

An oscillator is shown in Figure 9.70. The amplifier is an ideal voltage amplifier (infinite input impedance and zero output impedance) with a voltage gain of A_v. The RC network connected from the amplifier output to the input forms the feedback network. Find the value of gain A_v required for oscillation, and find the frequency of oscillation of the circuit.

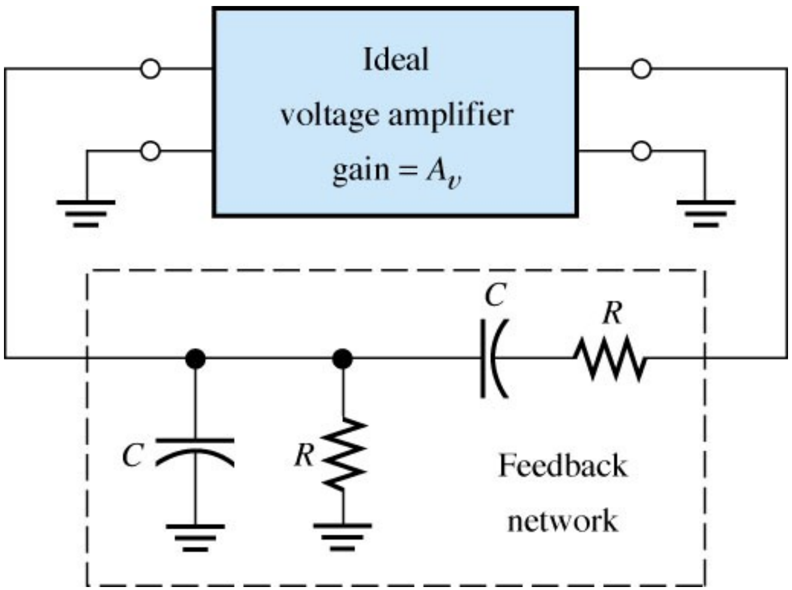


Figure 9.70 Typical linear oscillator.

Solution:

$$\beta(f) = \frac{V_o}{V_{in}} = \frac{\dfrac{R(1/j\omega C)}{R + 1/j\omega C}}{R + \dfrac{1}{j\omega C} + \dfrac{R(1/j\omega C)}{R + (1/j\omega C)}}$$

$$\beta(f) = \frac{R(1/j\omega C)}{R^2 + 3R/j\omega C - 1/\omega^2 C^2}$$

$$\beta(f) = \frac{R}{3R + j(\omega R^2 C - 1/\omega C)}$$

$$A_v \beta = 1$$

$$R\left(3 - A_v\right) + j\left(\omega R^2 C - \frac{1}{\omega C}\right) = 0$$

$$R\left(3 - A_v\right) = 0$$

$$A_{v\,min} = 3$$

$$\omega R^2 C - \frac{1}{\omega C} = 0$$

$$\omega = \frac{1}{RC}$$

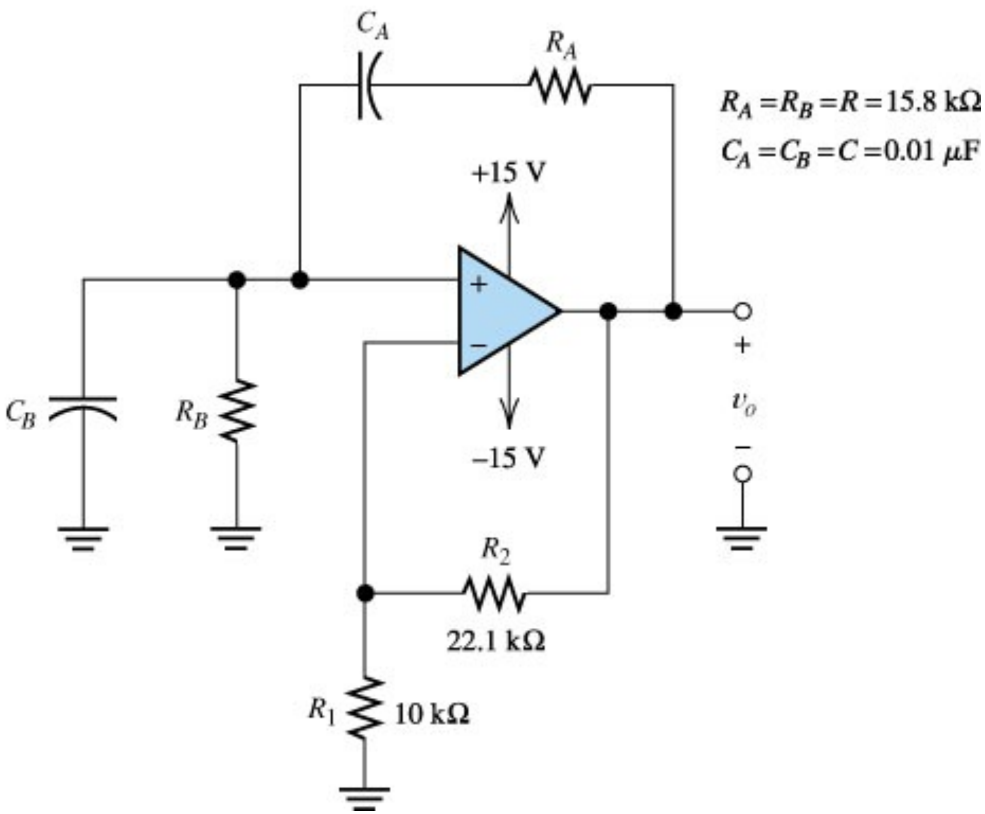


Figure 9.74 An example of a Wien-bridge oscillator designed on the basis of Example 9.12.

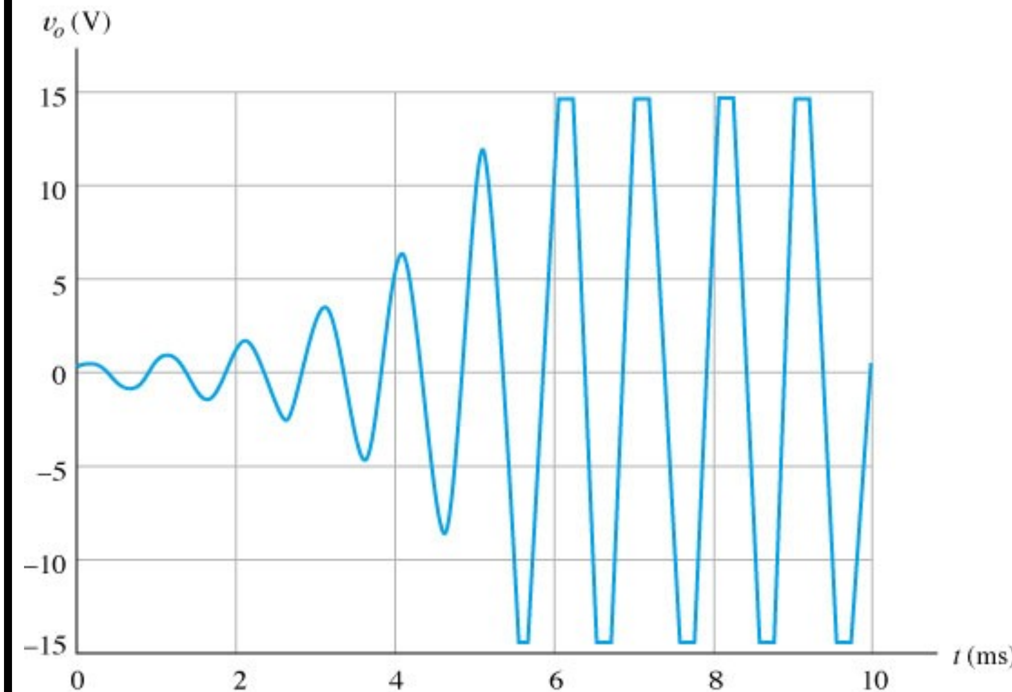


Figure 9.75 Output voltage of the oscillator in Figure 9.74.

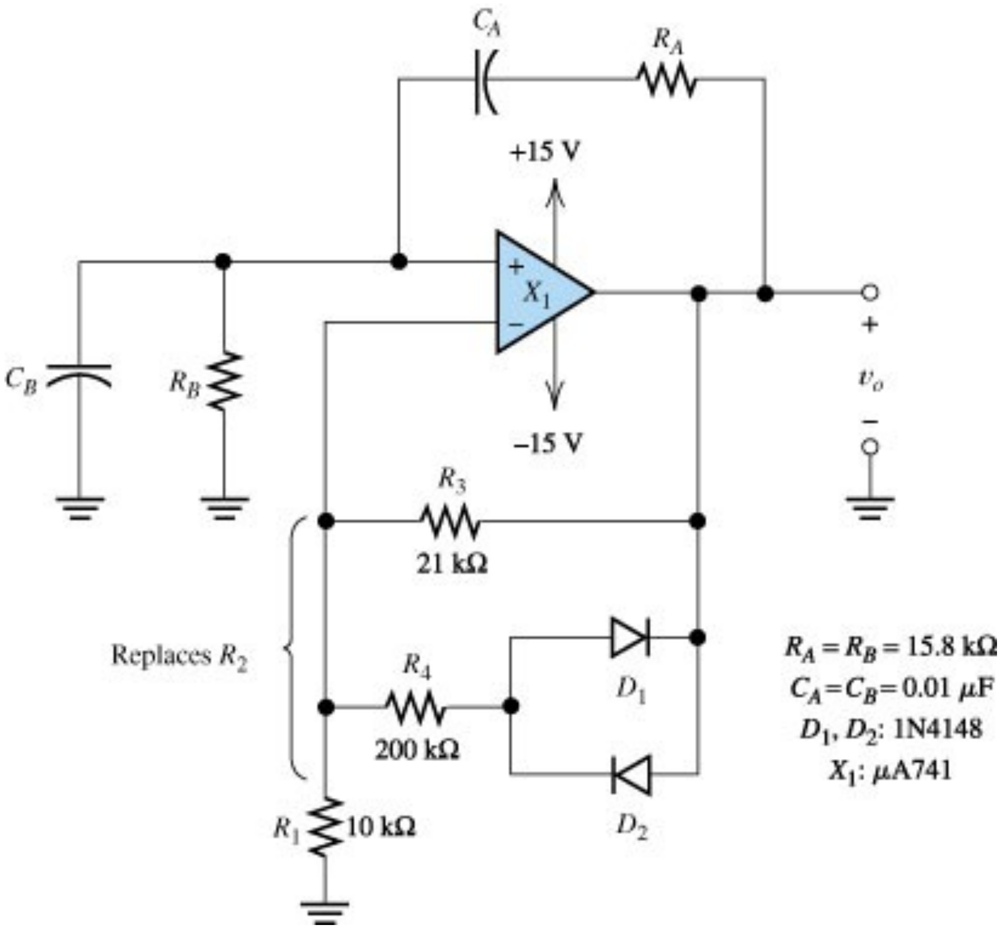


Figure 9.77 Modification of the circuit of the Wien-bridge oscillator. The diodes and the resistor R_4 limit the amplitude of the output signal. In this way is avoided its clipping.

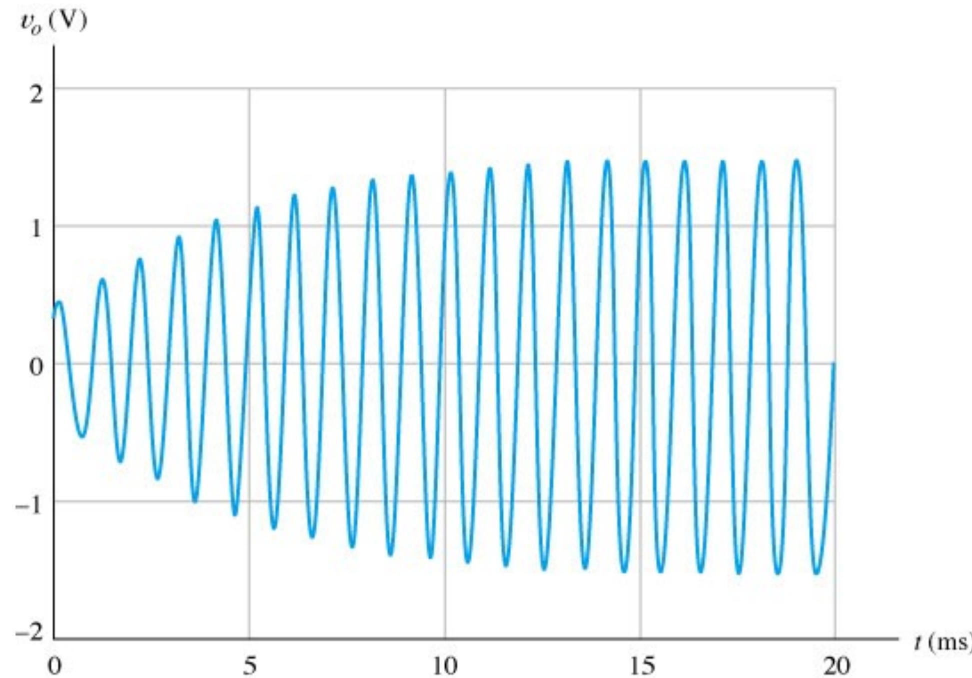


Figure 9.78 Output voltage of the oscillator of Figure 9.77.

Chapter IIIa
The operational Amplifier and applications.

III.1. Basic Model for the Operational Amplifier.

The OPerational AMPlifier (OPAMP) is a key building block in analog integrated circuit design. The OPAMP is composed by several transistors and passive elements (resistors and capacitors) and arranged such that its low frequency voltage gain is very high; the dc gain of the OPAMP-741 is around 10^5 V/V (10 μV at the input give us 1 V at the output). The design of such complex circuit is discussed in chapter 6; here we will use a simplified linear macromodel to analyze the principles of OPAMP based circuits and their operation. Several circuits are studied such as basic amplifiers, first order and second order filters and some non-conventional applications. The versatility of the OPAMP will be evident at the end of this chapter.

To define the fundamental parameters of a system, let us consider a linear two-port system with two terminals grounded, as the one shown in Figure 3.1. There are 4 variables vi, ii, vo and io to be studied. The interaction between the four variables can be defined in many different ways, depending on the definition of the dependent and independent variables; in real circuits these definitions depend on the input variable (current or voltage) and the most relevant output variable. Usually in voltage amplifiers the input signal is defined as vi while the output is vo.

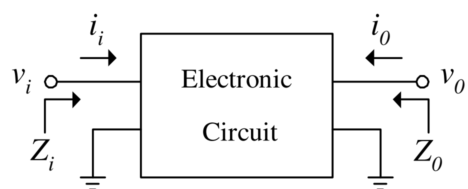


Fig. 3.1. Electronic circuit represented by a black box.

Since we are assuming that the circuit is linear, among other representations, we can describe the electronic circuit by using the following hybrid matrix representation:

$$\begin{bmatrix} i_i \\ v_o \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} v_i \\ i_o \end{bmatrix} \qquad \text{g-parameters} \tag{3.1a}$$

or

$$\begin{aligned} i_i &= g_{11} v_i + g_{12} i_o \\ v_o &= g_{21} v_i + g_{22} i_o \end{aligned} \tag{3.1b}$$

Notice that we are mixing currents and voltages in the matrix, then we call it hybrid representation of the circuit, and the resulting model is termed hybrid model. In many text books you can find at least 4 different set of parameters, but this is one of the most relevant ones for voltage amplifiers. Bipolar and MOS transistors models are based on another model called π-hybrid, to be discussed in the following chapters.

In equations 3.1b, the parameter g_{11} defines the input conductance, and it relates the input current and the input voltage needed by the circuit without considering the effect of the output current (i_o=0); the circuit's input conductance is formally defined as follows:

$$g_{11} = \frac{1}{Z_i} = \left.\frac{i_i}{v_i}\right|_{i_o=0} \tag{3.2}$$

This parameter is measured by applying an input voltage source and measuring the input current; the output node is left open such that i_o=0. Since g_{11} is the ratio of the input current to the input voltage, while the output is leaved open, its units are amps/volts or 1/Ω.
The parameter g_{12} defines the reverse current gain of the topology, and it is defined as

$$g_{12} = \left.\frac{i_i}{i_o}\right|_{v_i=0} \tag{3.3}$$

This parameter represents the reverse current gain: current generated at the input due to the output current. In the ideal case this parameter is zero since usually the operational amplifiers are unidirectional; e.g. the input signal applied to the system generates an output signal, but the output signals (current or voltage) should not generate any signal at the input. For measuring this parameter it is required to short circuit the input port such that v_i=0, then apply a current at the output and measure the current generated at the input port. In practical circuits this parameter is very small and usually it is ignored.
The Forward voltage gain is defined as the ratio of the output voltage and input voltage without any load connected at the output.

$$g_{21} = A_V = \left.\frac{v_o}{v_i}\right|_{i_o=0} \tag{3.4}$$

This is certainly one of the most important parameters of the two-port system; ***we also refer to A_V as the open-loop gain of the OPAMP***. It represents the circuit's voltage gain without any load impedance attached (output current equal zero).
Another important parameter is the system's output impedance, which relates the output voltage and the output current without taking the effects of the input signal. It is defined by

$$g_{22} = Z_0 = \left.\frac{v_o}{i_o}\right|_{v_i=0} \tag{3.5}$$

Thus, the two-port system can be represented by the four aforementioned parameters; the resulting macromodel is shown in Figure 3.2. For sake of clarification we are using impedances instead of admittances in this representation. Notice that a current controlled current source (ICCS) is used for the emulation of parameter g_{12} since it represents the input current (input port) being generated by the output current (output port). A resistor can not represent this parameter since current is flowing in one port but the voltage at the other port controls it. Similar comments apply to the voltage controlled voltage source represented by A_V v_i ($g_{21}v_i$).

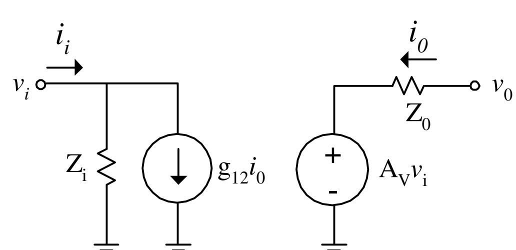


Fig. 3.2. Linear macromodel of a typical voltage amplifier using hybrid parameters.

Model for the OPAMP. The ideal OPAMP is a device that can be modeled by using the circuit of Fig. 3.2 with A_V=∞, g_{12}=0, Z_i=∞, and Z_o=0. This is of course an unrealistic model, but it is enough for understanding the basic circuits and their operation. We will see that when you connect several circuits in cascade for complex signal

processing, both input and output impedances are important parameters that affect the overall performance of the system. In this section, however these effects are not considered.
Discuss here the main limitations such as input impedance, limited DC gain and DC offsets and input bias current.

III.2. Basic configurations: Inverting and non-inverting amplifier.
Inverting configuration. The first topology to be studied is the inverting amplifier shown in fig. 3.3a. It consists of an impedance connected between the input source and the OPAMP's inverting terminal; the second impedance is connected from the inverting terminal to the output of the OPAMP. Z_2 provides a negative feedback (connecting the OPAMP's output and the negative input); this is the main reason for the excellent properties of this configuration. The simplified linear macromodel of the OPAMP is used for the representation of the inverting amplifier, and the equivalent circuit shown in fig. 3.3b. By using basic circuit analysis techniques it can be easily find that

$$\frac{v_i - v_x}{Z_1} + \frac{v_o - v_x}{Z_2} = 0 \tag{3.5}$$

and

$$v_o = -A_v v_x \tag{3.6}$$

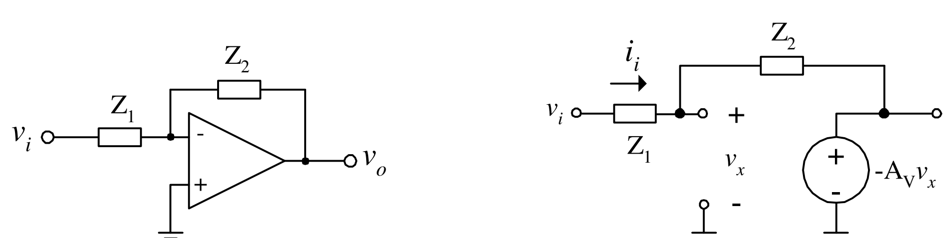
Solving these equations as function of the input and output voltages yields;

$$\frac{v_o}{v_i} = -\left(\frac{1}{1 + \frac{1 + Z_2/Z_1}{A_V}}\right)\left(\frac{Z_2}{Z_1}\right) \tag{3.7}$$

This relationship is also known as closed-loop amplifier's gain since the feedback resistor in combination with the OPAMP form a closed loop. If the open-loop gain of the OPAMP A_V is very large, then the first factor can be approximated as unity and the closed-loop voltage gain becomes

$$\frac{v_o}{v_i} = -\frac{Z_2}{Z_1} \tag{3.8}$$

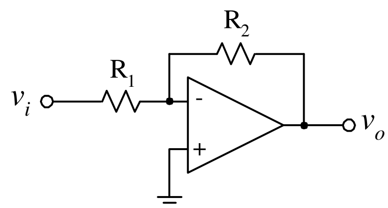
This result shows that **if negative feedback is used and if the open-loop gain of the OPAMP is large enough, the overall amplifier's voltage gain depends on the ratio of the two impedances**. Unlike to the gain of the open-loop gain of the OPAMP that can vary by more than 50 % due to transistor's parameters variations and temperature gradients, as will be explained in the following sections, the closed loop gain is quite accurate, especially if same type of impedances are used. Usually ratio of impedances is more precise than the absolute value of components; e.g. ratio of capacitors fabricated in CMOS technologies can be as precise as 99.5 % while the absolute value of the capacitance may change by more than 20%.



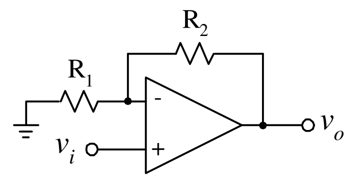
(a) (b)

Fig. 3.3. Inverting amplifier: a) the circuit and b) the linear macromodel assuming that OPAMP input is infinity and output impedance is zero.

Another important observation is that the differential voltage at the OPAMP input v_x (see Fig. 3b) is ideally zero. The reasoning behind this observation is as follows: according to 3.8, the output voltage is bounded (not infinity) if Z_1 is not zero or Z_2 is not infinite, hence v_i is also bounded. Under these conditions and according to expression 3.6 the OPAMP input voltage v_x is very small if A_v is large enough; the larger the OPAMP open loop gain the smaller signal at the input of the OPAMP. Therefore the ***inputs of the OPAMP can be considered as a virtual short; the voltage difference between the two input terminals (v_+ - v_-) is very small but they are not physically connected.*** The virtual short principle is extremely useful in practice; most of the transfer functions can be easily obtained if this property is used. To illustrate its use, let us consider again the circuit of fig. 3.3b. Due to the virtual ground at the input of the OPAMP, ***v_x=0 (virtual short) and the input current i_i is determined by v_i/Z_1.*** *Since the input impedance of the OPAMP is infinite,* ***i_i flows throughout Z_2, leading to an output voltage given by $-i_iZ_2$. As a result, the closed-loop voltage gain becomes equal to $-Z_2/Z_1$,*** as stated in equation 3.8.
If the impedances Z_1 and Z_2 are replaced by resistors as shown in Fig. 3.4a, we end up with the basic resistive inverting amplifier. The closed-loop gain is then obtained as



(a)



(b)

Fig. 3.4. Resistive amplifiers: a) inverting configuration and b) non-inverting configuration.

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \tag{3.9}$$

Notice that in the case of the inverting configuration, the amplifier's input impedance is determined by R_1; this is a result of the virtual ground present at the inverting terminal of the OPAMP. Hence, if several inverting amplifiers are connected in cascade we have to be aware that the amplifier must be able to drive the input impedance of the next stage.
Non-inverting voltage gain configuration. If the input signal is applied at the non-inverting terminal and R1 is grounded, as shown in fig. 3.4b, the non-inverting configuration is obtained. Notice that the ***feedback is still negative. If R_2 is connected to the positive terminal, the circuit becomes unstable*** and useless for linear applications; this will be evident in the following sections. The closed-loop voltage gain of the non-inverting configuration can be easily obtained if the virtual short principle is used. Due to the high gain of the OPAMP, the voltage difference between the inverting and non-inverting terminals is very small; hence *the voltage at the non-inverting terminal of the OPAMP is also v_i*. The current flowing through R_1 and R_2 is then given by v_i/R_1; therefore the output voltage is computed as

$$\frac{v_o}{v_i} = \frac{v_i + i_1R_2}{v_i} = \frac{v_i + (v_i/R_1)R_2}{v_i} = 1 + \frac{R_2}{R_1} \tag{3.10}$$

The voltage gain is therefore greater or equal than 1. An important characteristic of this configuration is that ideally its input impedance is infinity; hence several stages can be easily connected in cascade. A special case of the non-inverting configuration is the buffer configuration shown in figure 3.5. If $R_1=\infty$, according to equation 3.10, the voltage gain is unity; in this case the value of R_2 is not critical and can even be short-circuited (R_2=0). This topology is also known as unity gain amplifier or buffer, and it is very popular for driving small impedances; e.g. speakers, motors, etc.

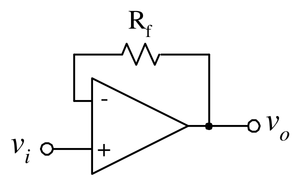


Fig. 3.5 OPAMP in unity gain buffer configuration

Emphasis on loading effects; discuss these issues in class!

III.3. Amplifier with multiple inputs and superposition.
Input signals can be applied to the two inputs of the OPAMP, as shown in Fig. 3.6. R1 and R2 are a voltage divider; the input voltage at the non-inverting (v_+) terminal is then

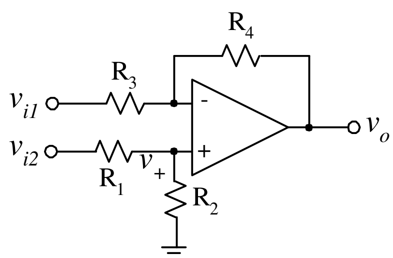


Fig. 3.6. Amplifier configuration with two input signals applied to the non-inverting and inverting terminals.

$$\frac{v_+}{v_{i2}} = \frac{R_2}{R_1 + R_2} \tag{3.11}$$

If a virtual short at the OPAMP inputs is assumed, the voltage at the inverting and non-inverting terminals is the same, and determined by v_+. Using KCL at the inverting terminal of the circuit leads to

$$\frac{v_o - v_+}{R_4} = \frac{v_+ - v_{i1}}{R_3} \tag{3.12}$$

Using equations 3.11 and 3.12, the output voltage is obtained, yielding

$$v_o = -\left(\frac{R_4}{R_3}\right)v_{i1} + \left(\frac{R_2}{R_1 + R_2}\right)\left(1 + \frac{R_4}{R_3}\right)v_{i2} \tag{3.13}$$

Notice that the output voltage is a linear combination of the two input signals: the first component is determined by the v_{i1} and the other one determined by v_{i2}. This analysis can always be used, but we can also take advantage of the properties of linear systems.

Superposition principle for a linear system. If the OPAMP is considered as a linear device and only linear impedances are used, then the output voltage is a linear combination of all the inputs applied. If several inputs are applied to the linear circuit, then the output can be obtained considering each input signal at a time; e.g. grounding all other input signals and applying the input signal under study. ***Therefore, the following property holds***: if

$$v_o(v_{i1}, v_{i2}, .., v_{iN}) = \sum_{j=1}^{N}\left(k_j v_{ij}\Big|_{v_{ik\; k\neq j}=0}\right) \tag{3.14a}$$

then

$$v_o(v_{i1}, v_{i2}, .., v_{iN}) = v_o(v_{i1}, 0..0) + v_o(0, v_{i2}, ..0) + \cdots + v_o(0, 0, ..v_{iN}) \tag{3.14b}$$

This property is known as the ***superposition principle***. Let us apply this principle to the topology shown in Fig. 3.6, where two inputs are applied to the amplifier. The circuit is analyzed by applying one input signal at a time: if v_{i1} is considered, v_{i2} is made equal zero. The equivalent circuit is shown in Fig. 3.7a.

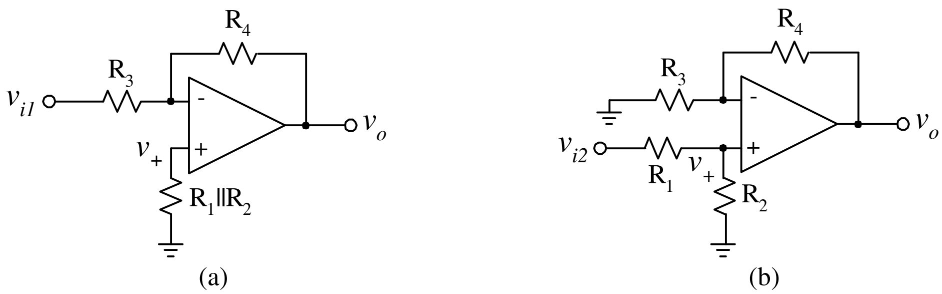


Fig. 3.7 Equivalent circuits for the computation of the output voltage: a) for v_{i1} and b) for v_{i2}.

Since the input impedance of the OPAMP is infinite, the current flowing through $R_1||R_2$ is zero, and $v_+=0$. The resulting circuit is the typical inverting amplifier where the output voltage is given by $-(R_4/R_3)v_{i1}$; notice that this output corresponds to the first term in equation 3.13. If the first input is grounded and signal v_{i2} is considered, the resulting equivalent circuit is depicted in fig. 3.7b. The voltage at the non-inverting terminal is given by equation 3.11, and the output voltage is equal to $v_o=(1+R_4/R_3)v_+$; the final result leads to the second term of equation 3.13.

Generalization of basic configurations. The concepts of infinite input impedance, zero output impedance, virtual short of the OPAMP inputs and linear superposition are especially useful when complex circuits are designed. An analog inverting adder is shown in fig. 3.8a; the output voltage can be easily found if we apply the superposition principle to each input. The equivalent circuit for the jth-input is depicted in fig. 3.8b. Since only R_j is connected to v_{ij}, the resistors connected to the other inputs must be grounded. These resistors are connected between the physical ground and the virtual ground generated by the negative feedback and the large open-loop voltage gain of the OPAMP, as a result of this the current flowing through all grounded resistors is zero, then i_j, generated by v_{ij}, R_j and the virtual ground node v_x (=0) flows throughout R_f. The output voltage is then obtained as $-(R_f/R_j)v_{ij}$. By using the same concept to all inputs, the amplifier's output voltage is found as

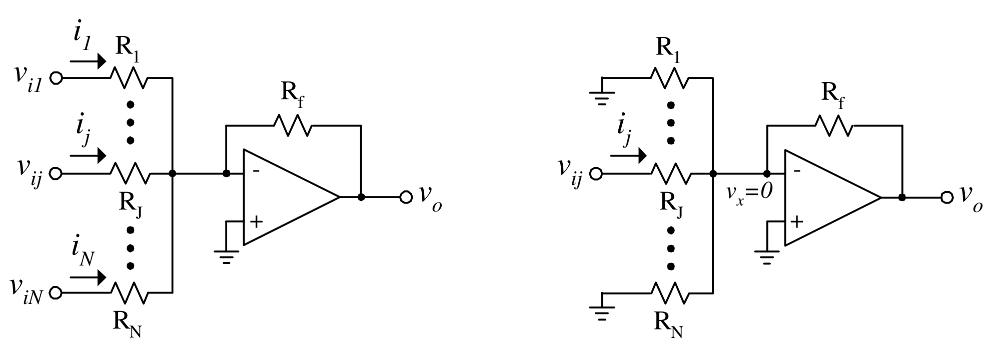


Fig. 3.8. a) Analog adder and b) equivalent circuit for analyzing the output voltage due to v_{ij}.

$$v_o = -\sum_{j=1}^{N}\left(\frac{R_f}{R_j}\right)v_{ij} \tag{3.15}$$

An interesting advantage of this circuit is that each one of the input resistors independently controls the voltage gain for each input. This is an important circuit property used for the design of analog-digital converters for instance where the addition of binary weighted signals are required.

An analog non-inverting adder is depicted in fig. 3.9a. Similarly to the previous case, the output voltage can be computed by using superposition. Shown in fig. 3.9b is the equivalent circuit for the jth-input signal, and making all other inputs equal zero. The voltage at the non-inverting terminal is the result of the voltage divider determined by the resistors lumped to node v_{+j} as follows:

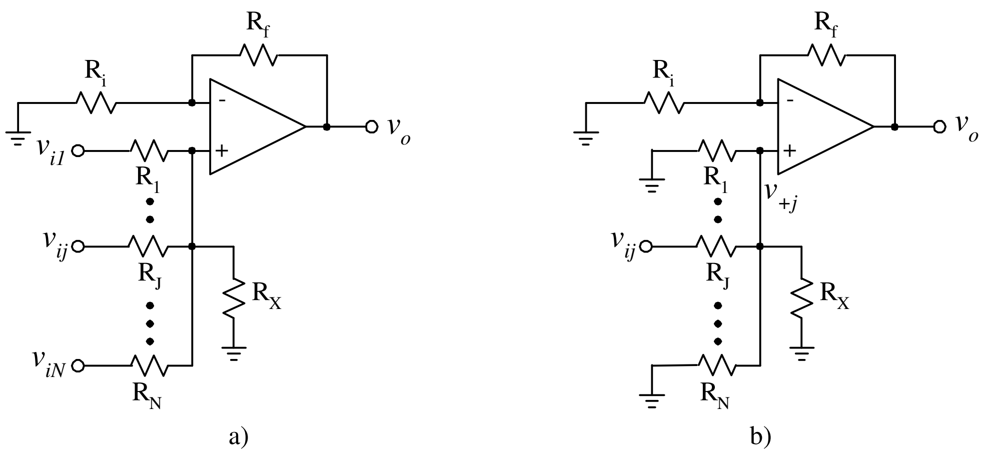


Fig. 3.9. a) Non-inverting amplifier with multiple inputs and b) equivalent circuit for the jth input.

$$\frac{v_{+j}}{v_{ij}} = \frac{R_1 \| R_2 \cdots R_{J-1} \| R_{J+1} \cdots \| R_N \| R_X}{\left(R_1 \| R_2 \cdots R_{J-1} \| R_{J+1} \cdots \| R_N \| R_X\right) + R_J} \tag{3.16}$$

Since many components are in parallel, for the analysis of this type of networks it is very often more convenient to use admittances instead of impedances. For this example, the previous equation can also be expressed as

$$\frac{v_{+j}}{v_{ij}} = \frac{\dfrac{1}{R_J}}{\dfrac{1}{R_J} + \dfrac{1}{R_1 \| R_2 \cdots R_{J-1} \| R_{J+1} \cdots \| R_N \| R_X}} \tag{3.16b}$$

The numerator ($1/R_j$) is identified as the admittance of the element connected between the input signal and v_{+j}. The denominator represents the parallel of all elements attached to v_+. The ***parallel connection of impedances is also equivalent to the reciprocal of the addition of their admittances***; then 3.16 can be expressed by the following equivalent expression

$$\frac{v_{+j}}{v_{ij}} = \frac{g_J}{\sum_{i=1}^{N}(g_i) + g_X} \tag{3.17}$$

where $g_i=1/R_i$. Once v_{+j} is obtained, the output voltage generated by v_{ij} can be obtained. Since v_{+j} is the voltage at the non-inverting terminal, to find the output voltage for this input is straightforward as $v_{oj}=(1+R_f/R_i)v_{+j}$. Taking into account all the input signals and applying the superposition principle, it can be shown that the overall output voltage is a linear combination of all inputs; the result of this analysis yields,

$$v_o = \left(1+\frac{R_f}{R_i}\right)\left(\sum_{J=1}^{N} v_{+j}\right) = \left(1+\frac{R_f}{R_i}\right)\left(\sum_{j=1}^{N}\left(\frac{g_J v_{ij}}{\sum_{i=1}^{N}(g_i)+g_X}\right)\right) = \left(\frac{1+\frac{R_f}{R_i}}{\sum_{i=1}^{N}(g_i)+g_X}\right)\left(\sum_{j=1}^{N} g_J v_{ij}\right) \tag{3.18}$$

Each input signal has a contribution to the output voltage that depends of all resistors, unlike the case of the inverting topology. The input impedance for each input depends on the array of resistors; for instance the input impedance seen by the jth-input signal is

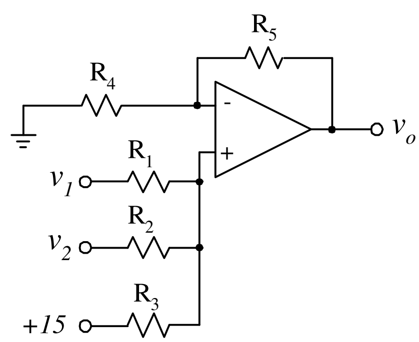
$$Z_j = R_J + \left(R_1 \| R_2 \cdots R_{J-1} \| R_{J+1} \cdots \| R_N \| R_X\right) \tag{3.19}$$

Similar expressions can be obtained for all other input sources.

Example: Design a circuit that implements the following equation:

$$vo(t) = 10v_1 + 20v_2 + 5$$

If needed use the supply voltages +/- 15 V. The circuit shown below can be used; this is not the only solution, combinations of inverting and non-inverting circuits might be used as well. The design process consists of finding the resistance values. For that purpose, the following equations must be solved:



$$10 = \left(1+\frac{R_5}{R_4}\right)\left(\frac{g_1}{g_1+g_2+g_3}\right)$$

$$20 = \left(1+\frac{R_5}{R_4}\right)\left(\frac{g_2}{g_1+g_2+g_3}\right)$$

$$5 = \left(1+\frac{R_5}{R_4}\right)\left(\frac{g_3}{g_1+g_2+g_3}\right)$$

Solve this set of equations, and find the numerical values; it is evident that $g_1=2g_3$ and that $g_2=4g_3$.

III.4. Amplifiers with very large gain/attenuation factors.

Very large gain amplifiers require large spread of the components. In analog integrated circuits design, it is difficult to control properly such large ratios, and very often they are very demanding of silicon area. Some configurations allow us to reduce this spread.

Large gain inverting amplifier using resistors in a T-array. Large voltage gain factors require very large resistors; the array of resistors shown in figure 3.10can be used to "increase" the effective feedback resistor. The circuit's transfer function can obviously be obtained by using conventional circuit analysis techniques such as KCL. It is however to useful to analyze the circuit based on the following observations:

1. Since the inverting terminal is at the ground potential due to the virtual short at the OPAMP input, the resistor R_2 is connected between node v_x and (virtual) ground; then it is in parallel with R3 if you analyze the circuit from the output. Therefore, the voltage v_x can be computed as

$$v_x = \left(\frac{R_2 \| R_3}{R_2 \| R_3 + R_4} \right) v_0 \tag{3.20}$$

   Notice that v_x is an attenuated version of the output voltage.

2. Also, as a result of the virtual ground at the OPAMP's input, the current flowing through R_2 is given by v_x/R_2. If the OPAMP is ideal, the current flowing through R1 is equal to the one flowing through R_2, and then the output voltage can be computed from the following expression:

$$\frac{v_i}{R_1} = -\frac{v_x}{R_2} = -\left(\frac{R_2 \| R_3}{R_2 \| R_3 + R_4} \right) \left(\frac{v_0}{R_2} \right) \tag{3.21}$$

Therefore, the voltage gain is

$$\frac{v_0}{v_i} = -\left(\frac{(R_2 \| R_3) + R_4}{R_2 \| R_3} \right) \left(\frac{R_2}{R_1} \right) \tag{3.22}$$

The voltage gain is therefore equivalent to the gain of a two-stage amplifier; larger gain factors are obtained with reduced resistive spread.

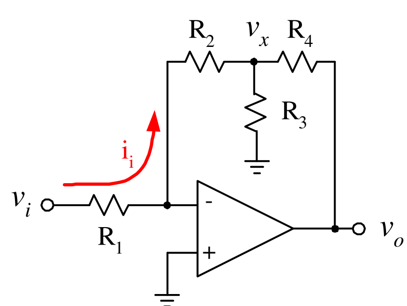


Fig. 3.10. Resistive voltage amplifier for high-gain applications.

If further reduction on the resistive spread is needed, two T-networks can be used as shown in Fig. 3.11. Similarly to the previous case, the voltage v_x is equal to $-(R_2/R_1)v_i$; notice that v_x is an attenuated version of v_y and this last voltage is an attenuated version of v_o. These voltages are related by the following expressions:

$$\frac{v_x}{v_y} = \frac{(R_2 \| R_3)}{(R_2 \| R_3) + R_4} \tag{3.23}$$

$$\frac{v_y}{v_0} = \frac{((R_2 \| R_3) + R_4) \| R_5}{[((R_2 \| R_3) + R_4) \| R_5] + R_6} \tag{3.24}$$

Then the closed loop voltage gain is obtained as

$$\frac{v_o}{v_i} = -\left(\frac{v_o}{v_y}\right)\left(\frac{v_y}{v_x}\right)\left(\frac{v_x}{v_{in}}\right) = -\left(\frac{[((R_2 \| R_3) + R_4) \| R_5] + R_6}{((R_2 \| R_3) + R_4) \| R_5}\right)\left(\frac{((R_2 \| R_3) + R_4)}{(R_2 \| R_3)}\right)\left(\frac{R_2}{R_1}\right) \tag{3.25}$$

This voltage gain can be very large; it is in fact determined by multiplication of 3 terms, which is equivalent to a 3-stage amplifier. Notice that the input impedance of the non-inverting circuit is determined by R_1.

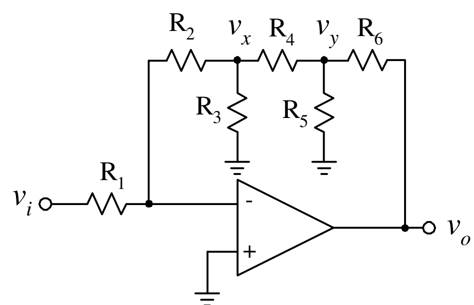


Fig. 3.11. Resistive amplifier using a T-configuration for large gain factors

Very large attenuation factors. The T-network can also be used for the design of large attenuation factors, for instance in applications related to power amplifiers where the input signal might be in the range of 100 V or more but the OPAMP can handle only 12 V or less. The resulting circuit using a T-network at the input is shown in figure 3.12. The voltage vx is an attenuated version of the incoming signal, and the voltage gain is adjusted to the proper level by the typical inverting configuration (R_3 and R_4). The attenuating factor, considering again a virtual ground at the input, is determined by R1 and the parallel of R2 and R3; the voltage gain between vx and vo is determined by the ratio of resistors R4 and R3. Therefore, the output voltage is given by:

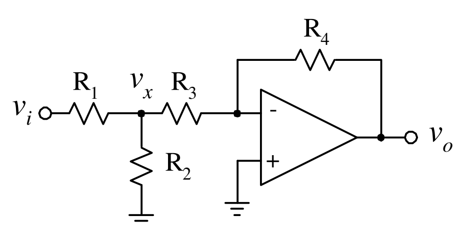


Fig. 3.12. Resistive amplifier using a T-configuration for large attenuation factors

$$\frac{v_0}{v_i} = \left(\frac{v_0}{v_x}\right)\left(\frac{v_x}{v_i}\right) = \left(-\frac{R_4}{R_3}\right)\left(\frac{R_2 \| R_3}{R_1 + (R_2 \| R_3)}\right) \tag{3.26}$$

The first factor is the result of the voltage divider at the input of the structure, while the second factor is the result of the non-inverting amplification of v_x. You can also use the double T-cell structure; it is left to the student to find out the voltage gain in that case; **DO IT, this can be a midterm question.**

III.5. RC Circuits: Integrators and differentiators.

Basic integrators. If the feedback resistor is replaced by a capacitor, we obtain a lossless integrator; the circuit is shown below. In this circuit, the input voltage vi is converted into a current by R1 and the virtual ground present at the input of the OPAMP, similarly to the case of the resistive amplifier. The resulting current is injected into the feedback capacitor C2 where it is integrated; the resulting output voltage is the integral of the injected current. The analysis of this circuit can easily be done in the frequency domain where the characteristic impedance of the capacitor is given by $1/(j\omega C_2)$. The transfer function of the inverting configuration is, as in the previous cases, determined by the ratio of the impedance in feedback and the input impedance, leading to the following result:

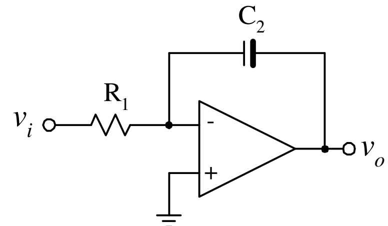


Fig. 3.13. Lossless inverting Integrator

$$H(s) = \frac{v_o}{v_i} = -\frac{1}{sR_2C_1} \tag{3.27}$$

where $s=j\omega$. This circuit has a pole at the origin and a "phantom" zero at $\omega=\infty$ (why?). The magnitude response is extremely large at low frequencies, and decreases at higher frequency with a rolloff of –20 dB/decade. The phase response is +90 (-270) degrees and independent of the frequency. Notice that at $\omega=1/R2C1$, the magnitude of the voltage gain is unity. Usually this circuit is not used as a standalone device, but is the key building block for high-order filters and analog-digital converters.

The combination of resistors and capacitors lead to the generation of poes and zeros; for example, the circuit implementation of a first order filter is shown in figure 3.14. This circuit is also known as a lossy integrator because while R1 injects charge into C2, the resistor R3 leaks (introduces losses) the charge stored in the capacitor. The gain of this circuit is also determined by the ratio of the equivalent impedance in feedback and the input impedance. In this circuit, the equivalent feedback impedance is composed by the parallel of the impedance of the capacitor ($1/j\omega C_2$) and R3. The low frequency gain, where the impedance of the capacitor can be ignored, is determined by the ratio of the two resistors; it is evident that the voltage gain is given by –R3/R1. At very high frequencies, the impedance of C2 dominates the feedback and the circuit behaves as the lossless integrator shown in figure 3.19 (gain defined by –1/sR1C2). The overall voltage gain is given by:

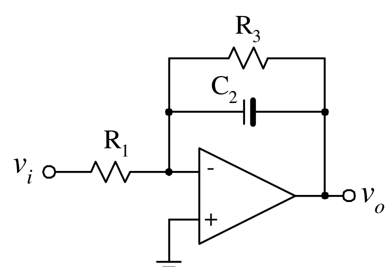


Fig. 3.14. First order lowpass filter

$$H(s) = -\frac{\frac{R_3}{R_1}}{1+sR_3C_2} \tag{3.28}$$

The low-frequency gain is, as expected, determined by the ratio of the resistors. The pole is located at $\omega=1/R3C2$, and for frequencies beyond this frequency the voltage gain decresases with a rolloff of –20 dB/decade.

The main differences between this circuit and the passive lowpass filter (voltage divider) are twofold: a) in the active realization (with OPAMP) the low frequency gain can be greater than 1 by adjusting the ratio of the resistors while in the passive filter the gain is always less than 1; b) the OPAMP allows us to connect the circuit to the next stage without affecting the transfer function; this is due to the small output impedance of the OPAMP. A typical transfer function obtained with this circuit is depicted in the following plot;

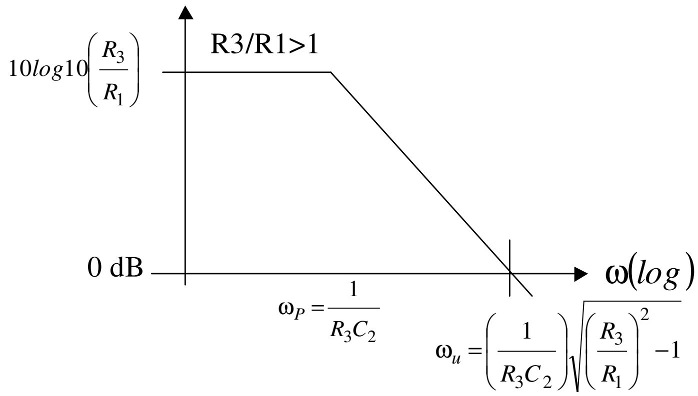


Fig. 3.15. Magnitude response for a first order filter.

The unity gain frequency is another important parameter; it can be obtained by taking the magnitude (or square magnitude) of equation 3.28, and equating it to 1. The resulting equation can be solved for the frequency, leading to the following result (find it yourself)

$$\omega_u = \left(\frac{1}{R_2C_1}\right)\sqrt{\left(\frac{R_2}{R_1}\right)^2 - 1} \tag{3.29}$$

For R2>>R1, this frequency is approximately given by ω_u=1/R1C1. Notice that for R2<R1 the solution is imaginary, meaning that the unity gain frequency does not exist; in fact you can not find any frequency where the gain is unity for an attenuator (dc gain less trhan 1). For R2<R1, the low frequency gain is less than 1; hence the transfer function does not have any intersection with the 0 dB curve.

The general first order transfer function can be implemented by using the topology shown in fig. 3.16. Since the elements are in parallel, it is very convenient o find the voltage gain as the ratio of the equivalent input addmittance and the equivalent feedback addmitance as follows:

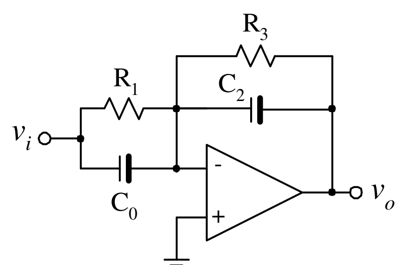


Fig. 3.16. General first order filter

$$H(s) = -\frac{g_1 + sC_0}{g_3 + sC_2} = -\left(\frac{R_3}{R_1}\right)\left(\frac{1 + sR_1C_0}{1 + sR_3C_2}\right) \tag{3.30}$$

With this circuit, you can design the following filters:

(a) Lowpass filters if C_0 is removed. The pole's frequency is given by 1/R3C2
(b) Amplifier if C_0 and C_2 are removed. Gain = -R3/R1
(c) Amplifier if the resistors are removed. Gain = - C0/C2 (not very practical, especially for low frequency applications)

(d) High-pass if R1 is removed. Pole's frequency at 1/R3C2, and high frequency gain = -C0/C2.

The high-pass transfer function can also be realized if a series of a capacitor and resistor is used, as shown in the figure below. Low frequency components are blocked by the capacitor due to its high impedance at low frequencies. At high frequencies the capacitor behaves as a short circuit, and the gain is given by the ratio of the resistors. Using typical circuit analysis techniques, the overall transfer function can be obtained as

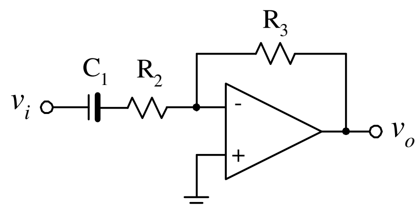


Fig. 3.17. First order High-pass filter using a series capacitor.

$$H(s) = -\frac{R_3}{R_2 + \frac{1}{sC_1}} = -\left(\frac{R_3}{R_2}\right)\left(\frac{sR_3C_1}{1+sR_2C_1}\right) \tag{3.31}$$

A DC zero and a pole located at ω=1/R2C1 can be observed. After the pole's frequency the voltage gain is mainly determined by the ratio of the resistors –R3/R2.

Non-inverting integrator. A non-inverting amplifier is implemented by using the following circuit. It is usually an expensive implementation, since the topology requires matched elements. The transfer function can be easily obtained by noting that the voltage at the non-inverting terminal is the result of a voltage divider between R and C (v+/vin=1/(1+sRC)). The voltage at the non-inverting terminal is then amplified by a factor 1 plus the ratio of the feedback impedance 1/sC' and the resistor R'. The resulting transfer function yields;

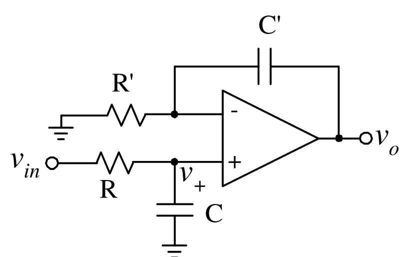


Fig. 3.18. Non-inverting lossless integrator

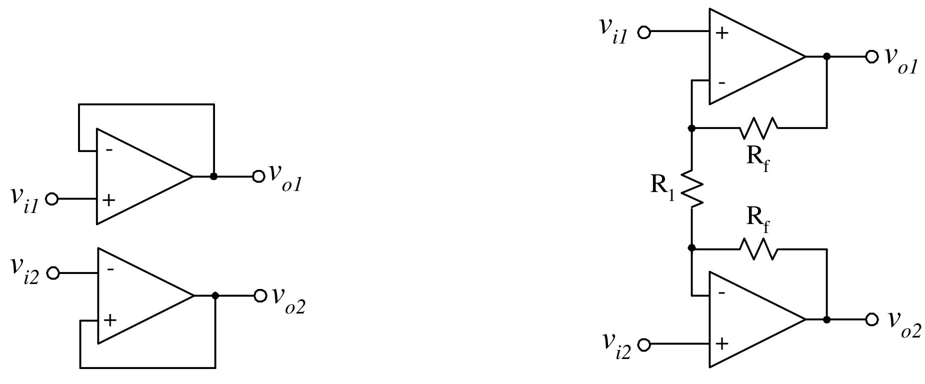
$$\mathrm{H(s)} = \left(\frac{1}{\mathrm{sR'C'}}\right)\left(\frac{1+\mathrm{sR'C'}}{1+\mathrm{sRC}}\right) \tag{3.32}$$

That corresponds to a non-inveting integrator if R'C' = RC; in this case, the voltage gain decreases when the frequency increases with a rolloff of -20 dB/decade and its phase is -90 degrees. The phase at DC is +90 degrees.

III.6. Instrumentation amplifiers.

In many practical applications, it is desirable to use amplifiers with very large input impedance and very low output impedance. This is the case when the sensors have large output impedance and or limited current driving capabilities. For those applications, the inverting amplifier based on two resistors can not be used since its input impedance is finite; e.g. defined by the input resistance. The only option is to use non-inverting amplifiers, as the ones shown in figure 3.19. In case the incoming signal is differential carried out by v_{i1} and v_{i2}, therefore two non-

inverting amplifiers are used. In a differential system, the information is determined by the voltage difference between the two inputs rather than by the voltage at each node.
The circuit shown in figure 3.19a is composed by 2 single-ended non-inverting amplifiers. The circuit is a particular case of the circuit shown in Fig. 7b; R1=0, R2=∞, R3=∞, R4=0 that leads to a unity-gain amplifier (buffer) with very large input impedance. Since the OPAMP output impedance is very small you can easily connect inverting amplifiers after this structure if required. The benefits of these buffers will be evident in the following chapters.



(a) (b)

Fig. 3.19. Fully-differential amplifiers based on: buffers and b) non-inverting amplifiers.

The topology shown in figure 3.19b is more useful and can provide voltage amplification greater than 1; the input impedance is very large as well and determined by the input impedance of the OPAMP. The analysis of this circuit is straightforward if we take advantage of the virtual short principle. As shown in figure 3.20, the voltages at the inverting terminals are given by v_{i1} and v_{12}, respectively. The current flowing through R1 is then given by (v_{i1}-v_{i2})/R1; this current flows throughout the resistors R_f, generating a voltage drop due to RF given by (v_{i1}-v_{i2}) Rf /R1. The output voltage vo1 is then equal to vi1+(vi1-vi2) Rf /R1 while the output voltage vo2 is given by vi2-(vi1-vi2) Rf /R1. The differential voltage gain is then computed as

$$\frac{v_{od}}{v_{id}} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = 1 + \frac{2R_f}{R_1} \tag{3.33}$$

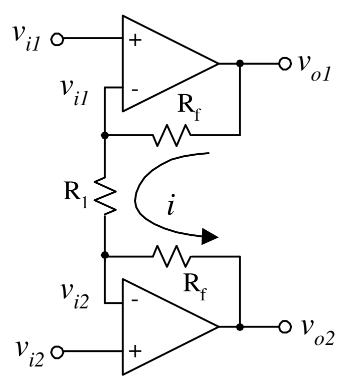


Fig. 3.20. Practical fully-differential instrumentation amplifier.

Notice in this expression that the output voltage is also differential v_{od}=v_{o1}-v_{o2}. Since the gain of the previous expression is defined as the ratio of the differential output voltage and the differential input v_{id} it is known as differential voltage gain.
Discuss here the properties of differential and common-mode signals.
Common-mode input impedance and differential mode input impedance.

The most popular single-ended instrumentation amplifier is depicted in Fig. 3.21; this topology is very useful for instrumentation applications. There are two inputs, and the important information is in differential format vid=vi1-vi2. A major advantage of fully-differential circuits is that they are little sensitive to noise and signal interferences that affect both inputs; e.g. common-mode signals. The single ended output then should be proportional to vid, and signals that are present in both inputs with same amplitude and same phase are cancelled by the differential nature of the amplifier. Applying the superposition principle to the circuit shown in fig. 3.21, it can be shown that the output voltage is given by a linear combination of v_{o1} and v_{o2} as follows:

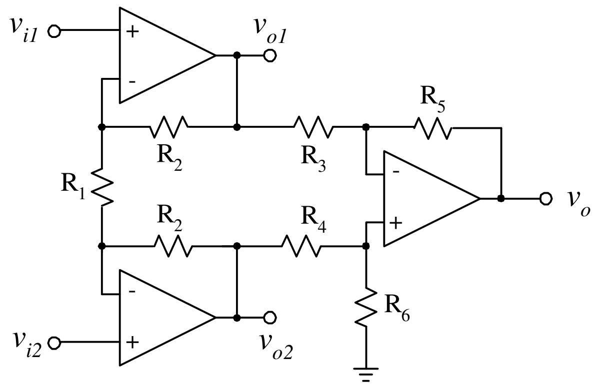


Fig. 3.21. Practical single-ended instrumentation amplifier.

$$v_o = \left(1+\frac{R_5}{R_3}\right)\left(\frac{R_6}{R_4+R_6}\right)v_{o2} - \left(\frac{R_5}{R_3}\right)v_{o1} \tag{3.34}$$

Using the previous equations 3.33 and 3.34, the output voltage can be obtained as

$$v_o = \left(\frac{R_6}{R_4+R_6}\right)\left(1+\frac{R_5}{R_3}\right)\left(\left(1+\frac{R_2}{R_1}\right)v_{i2} - \frac{R_2}{R_1}v_{i1}\right) - \left(\frac{R_5}{R_3}\right)\left(\left(1+\frac{R_2}{R_1}\right)v_{i1} - \frac{R_2}{R_1}v_{i2}\right) \tag{3.35}$$

After some algebra we get the following result:

$$v_o = \left[\left(\frac{R_6(R_3+R_5)}{R_3(R_4+R_6)}\right)\left(\left(1+\frac{R_2}{R_1}\right)+\left(\frac{R_5}{R_3}\right)\left(\frac{R_2}{R_1}\right)\right)\right]v_{i2} - \left[\left(\frac{R_6(R_3+R_5)}{R_3(R_4+R_6)}\right)\left(\frac{R_2}{R_1}\right)+\left(\frac{R_5}{R_3}\right)\left(1+\frac{R_2}{R_1}\right)\right]v_{i1}$$

. (3.36)

If we introduce the conditions R3=R4 and R5=R6, this equation simplifies to the required differential output

$$v_o = \left(\frac{R_5}{R_3}\right)\left(\frac{R_1+2R_2}{R_1}\right)(v_{i2}-v_{i1}) \tag{3.37}$$

The important properties of this amplifier are:

1. The **input impedance is extremely large** and determined by the OPAMP. Therefore, it can be easily connected to a number of sensors regardless the type of sensor's output impedance.
2. The **output voltage is sensitive to differential input voltage** vid=vi1-vi2.
3. **Common-mode noise present at both terminals is rejected** by the differential nature of the topology. The ability to reject common-mode noise (electromagnetic interference present at both amplifier's inputs for

instance) by an amplifier is measured by the common-mode rejection ratio (CMRR) parameter, to be discussed in next sections.

ELEN-325. Part III.b

7.- Design examples.
Workout some additional examples: e.g. fig. P3.19, Sedra-Smith 1st edition.

8.- Filters and other non-conventional circuits.
Filters are used in electronics for the selection of information that is located in a specific frequency band. A popular structure is the so-called multiple feedback topology shown in figure 3.1b. Two feedback paths can be observed in this circuit, the first one due to Y4 and the second one due to Y5. Both feedback trajectories provide negative feedback, that makes the circuit is stable. The voltage gain of this structure can be found by solving the nodal equations at node vx and the OPAMP's inverting terminal. Those equations can be written as (find it!):

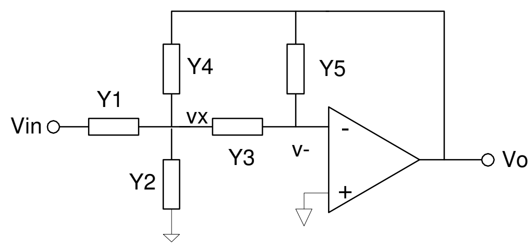


Fig. 3.1b. Mulitple feedback second-order filter.

$$\begin{bmatrix} Y_1+Y_2+Y_3+Y_4 & -Y_3 & -Y_4 \\ -Y_3 & Y_3+Y_5 & -Y_5 \end{bmatrix} \begin{bmatrix} v_x \\ v_- \\ v_o \end{bmatrix} = \begin{bmatrix} Y_1 v_{in} \\ 0 \end{bmatrix} \tag{3.1b}$$

Please write the equations and check the matrix (don't believe in professor's result!). Solving the system of equations we should be able to find the output voltage of the circuit. Notice that we are not writing any equation for the output node of the OPAMP, and we should not! The OPAMP output voltage is generated by a voltage controlled voltage source, where the current demanded by the elements connected to the OPAMP is provided by that element. For ideal OPAMPs, vo is controlled by the elements connected in feedback and the input voltage, and not by the elements connected at the OPAMP output! For the solution of the equations 3.1b make v_=0 since we have a virtual ground at the input of the OPAMP.
We might write these equations by inspection noticing that:

1. For the **first row we consider the nodal equation at node vx**. For the element 11 of the admittance matrix we have to consider all the admittances connected to vx; since vx is the first node we are considering. In fig. 3.1b, the elements connected to vx are Y1, Y2, Y3, and Y4.
2. The 12 element of the matrix is determined as the negative of the admittance between v and v-, since the second node considered in the admittance matrix is v-.
3. The element 13 is the negative of the element(s) connected between vx and vo, in this case -Y4.
4. For the **second row we considered the nodal equation at node v-**. Matrix term 21 is the negative of the admittance connected between v- and vx.
5. The element 22 is composed by all admittances connected to v- (the node under consideration).
6. Finally the matrix term 23 is the negative of the admittances connected between v- and vo.
7. For the right hand side of 3.1b, we considered the input voltage and the admittance connected between vin and vx.
8. Since we do not have any element connected between v- and vi the second term of the right hand side is zero.

Another approach for finding the transfer function is using the properties of linear circuits. Applying superposition, vx is a linear combination of vin and vo. Since the OPAMP inverting terminal is a virtual ground, computation of vx yields (check it!)

$$v_x = \frac{Y_1}{Y_1 + Y_2 + Y_3 + Y_4} v_{in} + \frac{Y_4}{Y_1 + Y_2 + Y_3 + Y_4} v_o \qquad (3.2b)$$

Also, notice that vo is generated by Y5, Y3 and vx as

$$v_o = -\frac{Y_3}{Y_5} v_x \qquad (3.3b)$$

Solving those equations, the voltage gain can be found as:

$$H(s) = \frac{v_o}{v_{in}} = \frac{-Y_1 Y_3}{Y_5 (Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4} \qquad (3.4b)$$

Both methods are useful.

A Particular case of this circuit is the **Second order LOW-PASS transfer function.** Replacing some of the admittances in Fig. 3.1b by the resistors and capacitors shown below, the circuit behaves as a second order lowpass filter. From equation 3.4b it can be found that

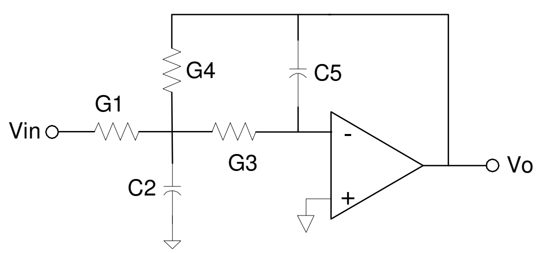


Fig. 3.2b. Mulitple feedback Low-pass filter.

$$H(s) = \frac{-G_1 G_3}{s^2 C_5 C_2 + s C_5 (G_1 + G_3 + G_4) + G_3 G_4} \qquad (3.5b)$$

The properties of this circuit are evident just analyzing the location of poles and zeros. There are two poles defined by the different components, and two zeroes at $\omega=\infty$ (why?). Therefore, the magnitude response will remain relatively flat until the frequency of the dominant poles if real poles are implemented. For frequencies above the first (dominant) pole, the magnitude response decreases monotonically with a roll-off of –20 dB/decade. Beyond the frequency of the second pole the roll-off becomes –40 dB/decade due to the effect of the second pole, as shown in the figure below.

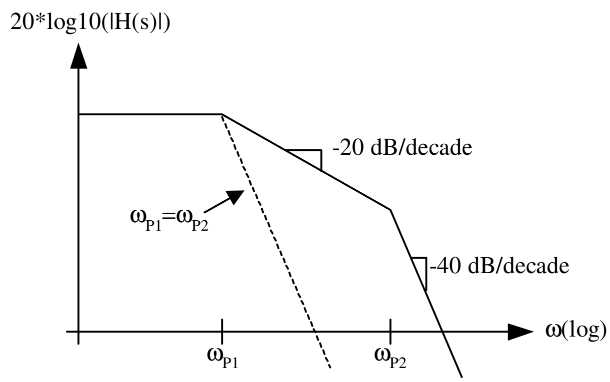


Fig. 3.3b. Magnitude response for a second order transfer function with two real poles.

For better rejection of high frequency components usually the poles are located close to each other as shown in the dashed curve; in this case the high-frequency rolloff of the magnitude response is –40 dB/decade. For the design of a low-pass second order transfer it is more convenient to express equation 3.5b as

$$H(s) = -\left(\frac{G_1G_3}{C_5C_2}\right)\left(\frac{1}{s^2 + s\frac{(G_1+G_3+G_4)}{C_2} + \frac{G_3G_4}{C_5C_2}}\right) \tag{3.6b}$$

The poles of the system are determined by the denominator of the previous equation and can be obtained as

$$\omega_{P1,2} = -\left(\frac{G_1+G_3+G_4}{2C_2}\right)\left(1 \pm \sqrt{1 - \frac{4\frac{G_3G_4}{C_5C_2}}{\left(\frac{G_1+G_3+G_4}{C_2}\right)^2}}\right) = -\left(\frac{G_1+G_3+G_4}{2C_2}\right)\left(1 \pm \sqrt{1 - \frac{4G_3G_4\left(\frac{C_2}{C_5}\right)}{(G_1+G_3+G_4)^2}}\right)$$

. (3.7b)

Selecting the proper values for the components, the poles can be real or complex conjugate; the conditions for these cases are the following:

$$\omega_{P1,2} = \begin{cases} Real \;\; if \;\; \dfrac{4G_3G_4\left(\frac{C_2}{C_5}\right)}{(G_1+G_3+G_4)^2} \le 1 \\ \\ Complex \;\; conjugated \;\; if \;\; \dfrac{4G_3G_4\left(\frac{C_2}{C_5}\right)}{(G_1+G_3+G_4)^2} > 1 \end{cases} \tag{3.8b}$$

The phase response is also important for the full characterization of the low-pass filter. The inverting filter configuration has a phase shift of –180 degrees at very low frequencies; this can be verified on the original transfer function, equation 3.6b, evaluating it at s=0. Each pole introduces a phase shift of -45 degrees around its pole frequency, as discussed in previous sections. If the poles are far away from each other, the phase response looks like the one depicted by the solid line in the following phase plot.

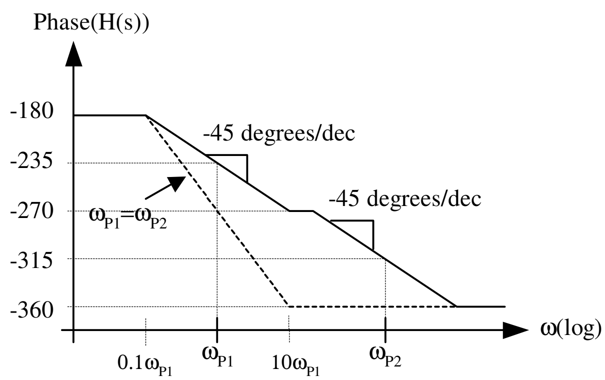


Fig. 3.4b. Phase response for an inverting second-order transfer function.

If the system have the two poles close to ω_{P1}, then the system's phase response presents a roll-off of –90 degrees/decade around ω_{P1}, due to phase contribution of two poles, as shown in the dashed plot.

The following design example will be discusssed in class:
Lowpass filter design: DC GAIN = 20 dB, $\omega_{p1}=\omega_{p2}$=100 Krad/sec. The design equations are obtained from the desired filter's transfer function as follows:

$$H(s) = -\left(\frac{10\omega_1^{\;2}}{(s+\omega_{P1})(s+\omega_{P1})}\right) = -\left(\frac{10\omega_{P1}^{\;2}}{s+2\omega_{P1}s+\omega_{P1}^{\;2}}\right)$$

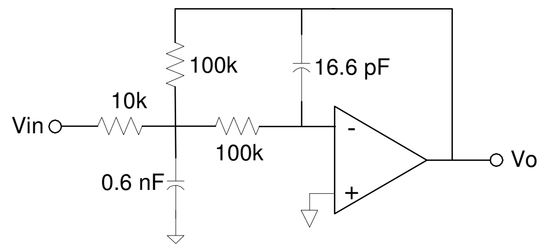
Note that the numerator $10\omega_{P1}^{\;2}$ is needed to obtain the desired DC voltage gain. Equation the terms of this equation with the ones of equation 3.6b, the design conditions are obtained

$R_4/R_1=10$
$(10^5)^2=1/(R_3R_4C_2C_5)$
$2(10^5)=(1/R_1+1/R_3+1/R_4)/\ C_2$

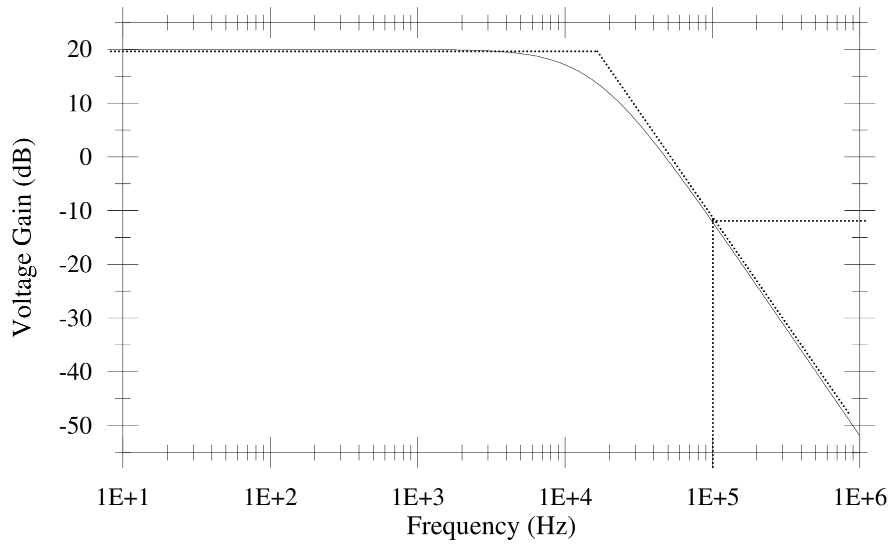
Lets design the filter based on power consumption considerations. To avoid the use of very small resistors, which implies very large currents and more power consumption, lets fix the smaller resistor to R_1=10 kΩ and to use $R_3=R_4$. Hence:

$R_3=R_4$ =100 kΩ
$C_2C_5 =1/(10^{10}x10^{10})= 10^{-20}$
$C_2=(1.2x10^{-4})/\ (2x10^5)=0.6x10^{-9}$

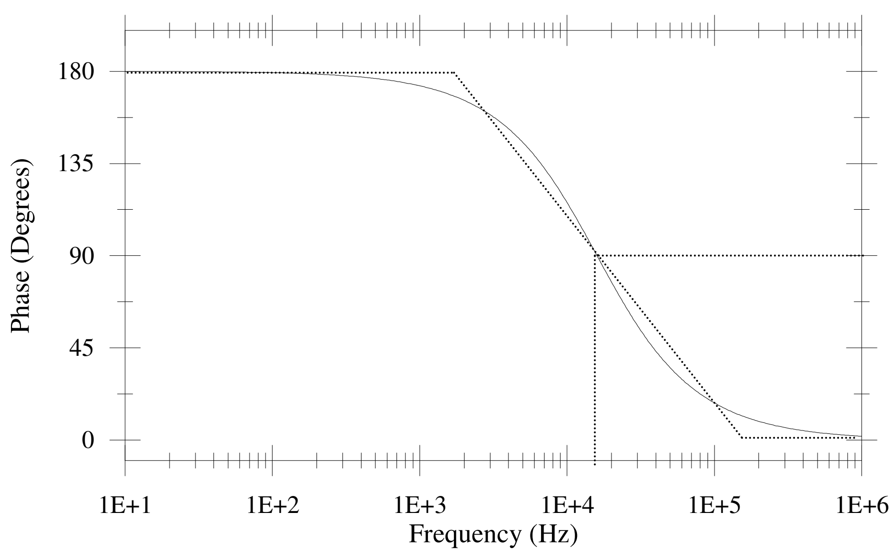
Then $C_5 =10^{-20}/0.6x10^{-9}=16.6x10^{-12}$. The final design is shown below. The circuit has been simulated in PSPICE, the magnitude and phase response are also shown.



Component values for the LOWPASS filter



Spice Results: Magnitude response



Spice Results: Phase response

Relationship between frequency domain and time domain. In many cases we are more interested into seee the response of the circuit in time domain; e.g. impulse and/or pulse response. An approach for the anaylisis of a circuit in time domain is to write the nodal or mesh equations in time domain using the integro-differential equations for capacitors and inductors. Another approach is to obtain the transfer function in the frequency domain as in the previous examples and to convert it into a differential equation by using the properties of the laplace transform. Among many other properties of the laplace transform, one of the fundamental ones is the following:

$$\ell\left(\sum_{i=0}^{N} a_i\left(s^i x\right)\right)=\sum_{i=0}^{N} a_i \frac{d^i x(t)}{dt^i} \tag{3.9b}$$

This property of the laplace transform is used for the conversion of rationale linear functions in the s-domain to the differential equation in the t-domain. To illustrate its use, let us consider the following s-domain (frequency domain) lowpass transfer function:

$$\frac{v_o(s)}{v_{in}(s)}=\frac{-a_0}{s^2+b_1 s+b_0} \tag{3.10b}$$

It can also be re-writeen as

$$\left(s^2+b_1 s+b_0\right)v_o(s)=-a_0 v_{in}(s) \tag{3.11b}$$

if the laplace transform is applied to both sides of this equation, the time-domain equivalent is obatined leading to the following second-order differential equation

$$\frac{d^2}{dt^2}\left(v_o(t)\right)+b_1\frac{d}{dt}\left(v_o(t)\right)+b_0 v_o(t)=-a_0 v_{in}(t) \tag{3.12b}$$

The next step is to solve this equation taking into account the type of input signal; e.g. impulse response, pulse response or even sinusoidal input response. It is not the purpose of this chapter to discuss the time domain analysis, and the student should be refereed to more specialized books for detailed analysis and more examples.

Bandpass transfer function. Very often the information to b processed is within a given pass band, hence lowpass and high pass filtering might not be the most efficient approach for signal detection. A bandpass filter is more suitable for this purpose; it can be obtained if in addition to the two poles of the lowpas transfer function, one of the zeros is located at low frequency and the other one at very high frequencies. These zeros can be easily implemented if they are located at $\omega=0$ and $\omega=\infty$, respectively. If the general multiple feedback transfer function, equation 3.4b, is considered the zero at low frequencies is generated if one of the two elements Y1 or Y3 is replaced by a capacitor while the other one is a conductance, respectively. A suitable option for filter realization is shown in the following figure. The analysis of this circuit is similar to the one used for the lowpass filter; the transfer function is

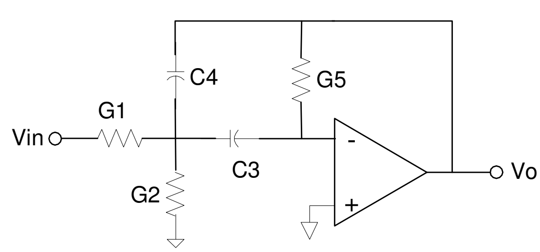


Fig. 3.5b. Mulitple feedback band-pass filter.

$$H(s)=\frac{-sG_1C_3}{s^2C_3C_4+sG_5(C_3+C_4)+(G_1+G_2)G_5}=-\left(\frac{G_1}{C_4}\right)\left(\frac{s}{s^2+s\frac{G_5(C_3+C_4)}{C_3C_4}+\frac{(G_1+G_2)G_5}{C_3C_4}}\right) \tag{3.13b}$$

The resulting transfer function has two zeros, one at DC and the other one (phantom) at $\omega=\infty$. If the poles are at the same frequency, the magnitude and phase responses can be approximated by piece wise linear functions as depicted in the following plots.

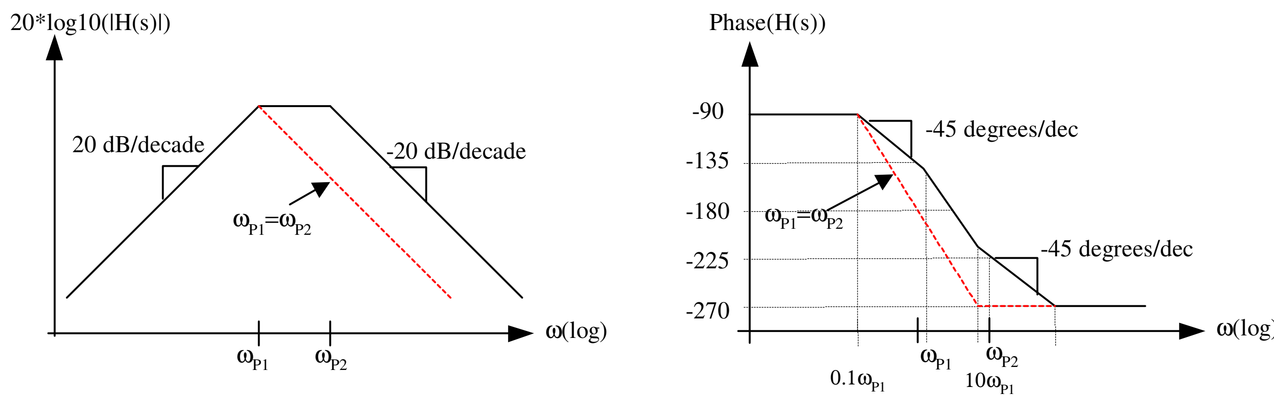


Fig. 3.6b. Magnitude and phase response of a second order bandpass transfer function.

Exercise: Design a Bandpass filter with both poles at 50 MHz and peak gain of 0 dB. Do it!

10.- Partial positive feedback.

10.1 Resistive amplifiers with partial positive feedback. Partial positive feedback can also be used for the implementation of demanding applications. For instance, negative resistors have to be used for the design of voltage controlled oscillators to cancel the effects of resistors lumped to inductors and capacitors (resistive losses). In partial positive feedback circuits, both terminals inverting and non-inverting are embedded in feedback loops; an example is the circuit shown in Fig. 3.7b. The voltage at the positive terminal is a sample of the output voltage vo, and then it can be found that

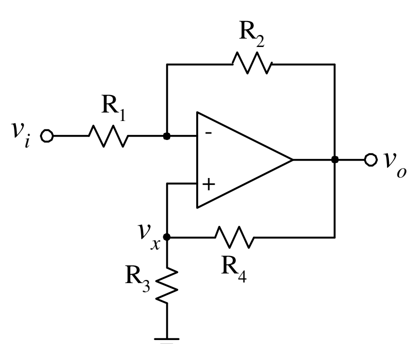


Fig. 3.7b. Resistive amplifier with negative and positive feedback

$$v_x=\frac{R_3}{R_3+R_4}v_o \tag{3.14b}$$

The output voltage is composed by the contribution of vi (inverting amplifier with a voltage gain =-R2/R1) and vx(non-inverting amplifier given by (1+ R2/R1)vx. Hence, the output voltage can be obtained as:

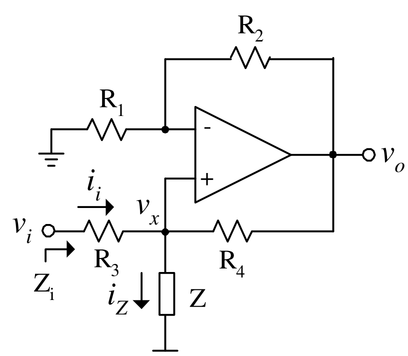
$$v_o = \left(1+\frac{R_2}{R_1}\right)v_x - \left(\frac{R_2}{R_1}\right)v_i = \left(\frac{R_3}{R_3+R_4}\right)\left(1+\frac{R_2}{R_1}\right)v_o - \left(\frac{R_2}{R_1}\right)v_i \tag{3.15b}$$

The solution of this expression for output voltage yields;

$$v_o = -\left(\frac{\frac{R_2}{R_1}}{1-\left(\frac{R_3}{R_1}\right)\left(\frac{R_1+R_2}{R_3+R_4}\right)}\right)v_i \tag{3.16b}$$

The positive feedback is reflected in the negative term of the denominator. The voltage gain can be further increased if R3(R1+R2)/(R1(R3+R4)) is close to unity. Notice that the gain can potentially be infinite. This situation is undesirable because a small variation in any of the components has a huge impact on the overall voltage gain; these variations could be due to temperature variations or aging of the components. Thus, if positive feedback is used, be sure that negative feedback is dominant and that variations on components do not drastically affects circuit's performances.

Realization of negative impedances.
The circuit shown below uses partial positive feedback as well since the R4 links the output voltage and the non-inverting terminal. To understand the operation of the circuit, let us find the voltage at the non-inverting terminal. Applying superposition, vx is composed by the contribution of vi and vo. The first component can be obtained by considering vi, and grounding vo; this can be done because the output of the OPAMP is a low-impedance node, and vo is defined by the voltages applied at the OPAMP inputs. The second component is obtained by considering vo and grounding vi, then



3.8b. Amplifier with partial positive feedback.

$$v_x = \frac{R_4 \,||\, Z}{R_3 + R_4 \,||\, Z} v_i + \frac{R_3 \,||\, Z}{R_3 \,||\, Z + R_4} v_o \tag{3.17b}$$

Once this voltage is obtained, the output voltage can be easily determined, because

$$v_o = \left(1+\frac{R_2}{R_1}\right)v_x = \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4 \,||\, Z}{R_3 + R_4 \,||\, Z}v_i + \frac{R_3 \,||\, Z}{R_3 \,||\, Z + R_4}v_o\right) \tag{3.18b}$$

After some algebra we can find the overall transfer function as

$$\frac{v_o}{v_i} = \frac{\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_4 \,||\, Z}{R_3 + R_4 \,||\, Z}\right)}{1-\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_3 \,||\, Z}{R_3 \,||\, Z + R_4}\right)} \tag{3.19b}$$

Once again, the positive feedback is reflected in the negative term of the denominator. An important special case is when R1=R2 and R3=R4; the previous equations can be simplified as follows:

$$\frac{v_o}{v_i} = \frac{2(R_3 \,||\, Z)}{R_3 - (R_3 \,||\, Z)} = \frac{2Z}{R_3} \tag{3.20b}$$

Therefore, the circuit behaves as a non-inverting amplifier. The most interesting properties of this circuit are associated with the input impedance. From 3.17b, it is obtained for the case R1=R2 and R3=R4 that

$$v_x = \left(\frac{Z}{R_3 + 2Z}\right)(v_i + v_o) = \left(\frac{Z}{R_3 + 2Z}\right)\left(1+\frac{2Z}{R_3}\right)v_i = \left(\frac{Z}{R_3}\right)v_i \tag{3.21b}$$

Therefore the current flowing throughout Z can now be obtained as

$$i_Z = \frac{v_x}{Z} = \frac{v_i}{R_3} \tag{3.22b}$$

As can be noticed in this result, the current flowing through Z is determined by R3; this current is independent of Z. Therefore, this circuit can be considered as a voltage controlled current source; the current is controlled by the input voltage and the resistors R3=R4, and this current is forced to flow through Z. On the other hand, the impedance at the input port is determined as follows (please work out the following expression).

$$Z_i = \frac{v_i}{i_i} = \frac{{R_3}^2}{R_3 - Z} \tag{3.23b}$$

For Z<R3 the input impedance is positive, and negative for Z > R3.
A useful circuit often used in filter's design is the negative impedance converter. The circuit, shown in Fig. 3.9b, is a variation of the schematic depicted in Fig. 3.8b. The input voltage is applied to the non-inverting terminal, and the output voltage vo is given by (1+R2/R1)v_i. The input current i_i is computed as (vi-vo)/Z, leading to the result given in expression 3.24b.

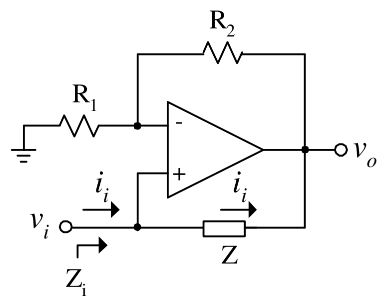


Fig. 3.9b. Negative impedance converter.

$$Z_i = \frac{v_i}{i_i} = \frac{v_i}{v_i - v_o} Z = -\left(\frac{R_1}{R_2}\right) Z \tag{3.24b}$$

Therefore, the equivalent impedance is negative. A negative impedance means that, contrary to the case of a positive impedance, the circuit delivers current when positive signals are applied. The reason for this behavior is that the OPAMP altogether with R1 and R2 amplify the input and the output voltage is greater or equal than vi. Hence positive vi generates vo > vi; since Z is connected between them it generates a current that flows from vo to vi.
Think about the following questions:
What is the meaning of negative impedance?
Difference between positive and negative impedance?

10.2. Sallen & Key Filter. Positive feedback has been use for the design of filters for long time. The filter based on finite gain amplifier uses 5 admittances and an amplifier with finite gain K. Since the amplifier is a non-inverting structure, the feedback produced by Y2 is positive leading to a filter with partial positive feedback. By following the analysis procedure used for the multiple feedback filters, the transfer function can be obtained by written the admittance matrix as follows:

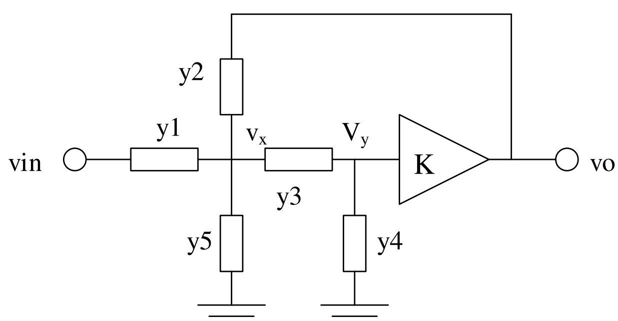


Fig. 3.10b. Sallen and Key second-Order filter.

$$\begin{bmatrix} y_1 + y_2 + y_3 + y_5 & -y_3 & -y_2 \\ -y_3 & y_3 + y_4 & -0 \\ -0 & -K & 1 \end{bmatrix} \begin{bmatrix} v_x \\ v_y \\ v_0 \end{bmatrix} = \begin{bmatrix} y_1 v_{in} \\ 0 \\ 0 \end{bmatrix} \tag{3.25b}$$

The first two rows correspond to the nodal equations of nodes vx and vy, respectively. The third row corresponds to the finite amplifier gain given by vo=Kvy. The solution of this system leads to the following filter's transfer function:

$$H(s) = \frac{y_1 y_3 K}{(y_1 + y_2 + y_5)(y_3 + y_4) + y_3(y_4 - y_2 K)} \tag{3.26b}$$

Selecting the proper elements lowpass, bandpass and highpass filters can be designed. These especial cases are:

- Selecting Y1 and Y3 as conductances, and Y2 and Y4 as capacitive admittances, the resulting transfer function leads to a lowpass transfer function. Even more, Y5 might be removed in this case; the resulting filter is shown in the figure below. Equation 3.27b show the transfer function.

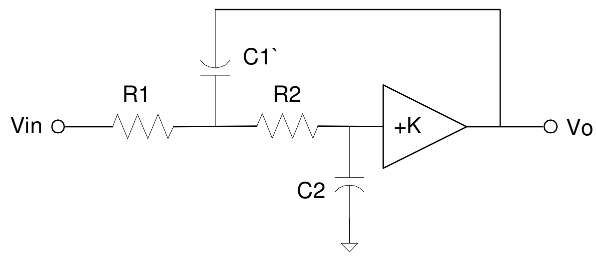


Fig. 3.11b. Second order Sallen and Key Filter. Notice that tthis filter uses partial positive feedback

$$H(s) = \frac{K\left(\frac{1}{R_1 R_2 C_1 C_2}\right)}{s^2 + s\left(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1}{R_2 C_2}(1-K)\right) + \frac{1}{R_1 R_2 C_1 C_2}} \tag{3.27b}$$

Similarly it can be shown that

- Y1 and Y4 conductances, and Y3 and Y5 capacitors lead to a bandpass transfer function.
- Y2 and Y4 conductances, and Y1 and Y2 capacitors lead to a high-pass transfer function.

Find yourself the resulting circuits! You may find one of these topologies in the first midterm.

11. Practical Limitations of the Operational Amplifiers. First at all, we must recognize that practical OPAMP are not even close to the ideal model: infinite input impedance, infinite gain, infinite bandwidth, and unlimited output current capability. Those parameters depends on the topology used (array of transistors , resistors and capacitors, technology used and power consumption); there are tons of different OPAMPs offered by different vendors; eg. Texas Instruments, Fairchild, National Semiconductor, etc. Although the origin of those limitations are not discussed in this course, the effects of on the overall transfer function of these parameters are briefly discussed in this section.
A more realistic OPAMP macromodel is depicted in the following schematic.

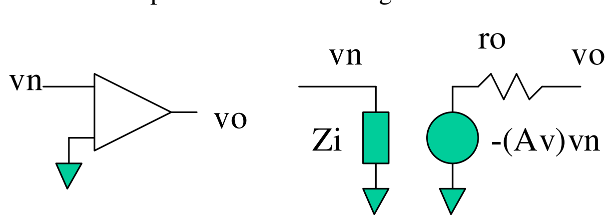


Figure 3.12b. Macromodel for the OPAMP.

Some values for comercially available OPAMPs are: Zi = 1MΩ, r_0=10Ω, and Av=10^5. These parameters introduce errors in the transfer function. Usually it is cumbersome to obtain the final results, and it is difficult to evaluate system degradation especially for complex circuits. Here we obtain some results for a single inverting amplifier but most of the conclusins for this circuit are also valid for complex circuits. Let us consider the circuit shown in Figure 3.13b; we are considering the finite input impedance of the OPAMP Z_i and the input impedance of the stage driven by the OPAMP. Using the macrodel of Fig. 3.12b with $r_0=0$, the equivalent circuit can be obtained as depicted in Figure 3.13 (b). The transfer function can be obtained if the nodal equation at node v_- is written; notice that nodal equation at the OPAMP output can not be written becausevo is controlled by the voltage dependent voltage source ($v_o=A_v(v_+-v_-)$. The current demanded by Z_F and Z_L is provided by the ideal voltage source. Solving the fundamental equation ($i_1=i_i+i_0$) the circuit's transfer funcion yields,

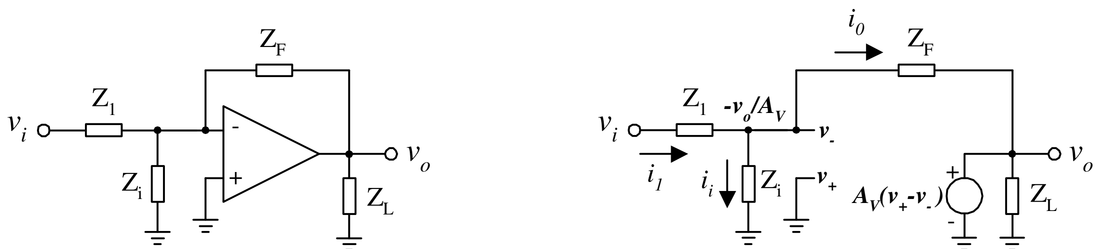


Fig. 3.13b. a) Inverting amplifier with OPAMP input impedance Z_i and load impedance Z_L, and b) equivalent circuit with $r_0=0$.

$$H(s)=-\left(\frac{Z_F}{Z_i}\right)\left(\frac{1}{1+\frac{(Z_F/Z_1)+(Z_F/Z_i)}{A_v}}\right) \tag{3.29b}$$

The effect of the finite DC gain and finite input impedance on the inverting amplifier can be better appreciated if the error function is considered; from equation 3.29b it follows that

$$H(s)=-\left(\frac{Z_F}{Z_i}\right)\left(\frac{1}{1+\xi}\right)\cong-\left(\frac{Z_F}{Z_i}\right)(1-\xi) \tag{3.30b}$$

where the error function ξ is defined as

$$\xi(s)=\frac{(Z_F/Z_1)+(Z_F/Z_i)}{A_v}=\left(\frac{1}{A_v}\right)\left(\frac{Z_F}{Z_1\|Z_i}\right) \tag{3.31b}$$

If the OPAMP DC gain is limited, the assumption of virtual ground is not longer valid since any output voltage variation generates a finite variation on the differential input signal given by v_o/Av. The smaller the OPAMP gain the larger the voltage variations at the OPAMP input are; hence the error should be inversely proportional to A_v. The voltage variations on the non-inverting terminal lead to current errors: firstly the input current is given by $(v_i-v_-)/Z_1$ hence an error proportional to Z_1 ($i_{error1}= -v_-/Z_1$) is introduced; Secondly, the OPAMP input impedance takes part of the current generated by Z_1, leading to a second current error given by $i_{error2}= v_-/Z_I$. These current errors are converted into voltage errors by the feedback resistor R_F, and are evident in equation 3.31b.

Notice that even if the OPAMP input impedance is infinite, a gain error due proportional to the ideal gain Z_F/Z_1 is present. For a given OPAMP open-loop gain Av, the larger the closed-loop amplifier's gain the larger the error is. The error that can be tolerated depends on the applications; notice that to kept the error below 1 % for instance it is required to satisfy

$$\xi(s) = \left(\frac{1}{A_v}\right)\left(\frac{Z_F}{Z_1 \| Z_i}\right) < 0.01 \qquad (3.32b)$$

For instance if Zi=1 MΩ, and voltage gain of –10, the voltage gain needed depends on the absolute values of the resistors used, as shown in table below

Z_F/Z_i	A_V
100/10	> 1000
10k/1k	> 1001
1M/100k	>1100
10M/1M	>2000

Notice that the errors are important when the input impedance Z1 is comparable with the OPAMP input impedance Zi. Another important limiting factor is of course the desired amplifier gain ZF/Zi. Notice that 3.31b can also be re-written as

$$\xi(s) = \left(\frac{1}{A_v}\right)\left(\frac{Z_F}{Z_1}\right)\left(\frac{Z_1 + Z_i}{Z_i}\right) \qquad (3.33b)$$

Effects of the OPAMP Finite bandwidth. Unfortunately the OPAMP bandwidth is very limited; believe or not, the bandwidth of the 741 is around 6 Hz only while he open-loop DC gain is around $2\text{x}10^5$V/V. The product of the open-loop DC gain and bandwidth is defined as OPAMP's Gain-BandWidth product GBW. For the OPAMP 741, GBW~1.2 MHz. These parameters are illustrated in the following plot

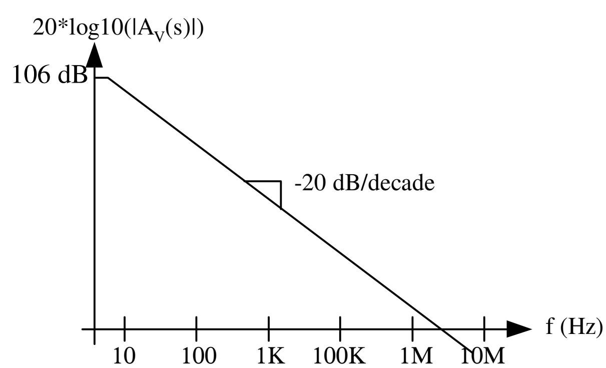


Fig. 3.14b. Typical open-loop magnitude response of an OPAMP

The OPAMP open-loop voltage gain can be modeled by a finite DC gain and a low-frequency pole as

$$A_V(s) = \frac{A_{DC}}{1 + \dfrac{s}{\omega_P}} \qquad (3.34b)$$

Notice that GBW=A_{DC}xω_P; it is also known as the unity gain frequency ω_u. This frequency is important because it defines the upper limit for the operation of the OPAMP: beyond this frequency the OPAMP is not longer an amplifier but an attenuator. That does not mean that you can always use the OPAMP until ω_u! Usually the useful frequency range is well below this limit. We learn in the previous discussion that an error is introduced if the open-loop gain of the OPAMP is finite. For the inverting configuration, the error determined by equation 3.33b. If Av is frequency dependent, then using 3.34b we can obtain a general form for the error function including the effects of the finite OPAMP bandwidth as shown in the following expression:

$$\xi(s) = \left[\left(\frac{1}{A_{DC}}\right)\left(\frac{Z_F}{Z_1}\right)\left(\frac{Z_1 + Z_i}{Z_i}\right)\right]\left(1 + \frac{s}{\omega_P}\right) \tag{3.33b}$$

Therefore, the pole of the OPAMP leads to a zero for the error transfer function as shown below. Therefore, the higher the bandwidth the larger the error is.

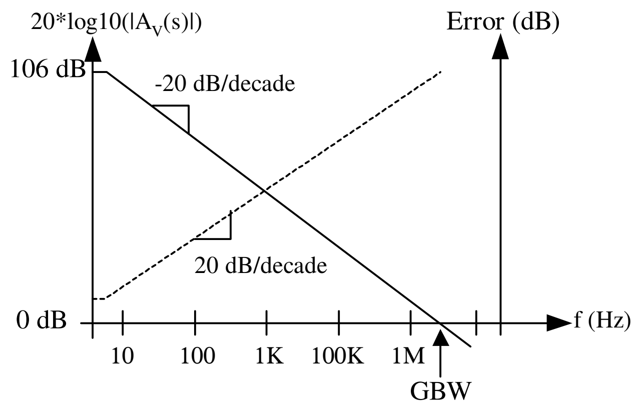


Fig. 3.15b. OPAMP open-loop magnitude response and error response for an inverting amplifier.

For the example discussed on the previous section we have: ADC=10^5v/v, Z_F/Z_1=10, Zi=1MΩ then it folows:

Z_1/Z_i	ω/ω_P	error
0.001	0.01	~ 10^{-4}
0.001	1	~1.4×10^{-4}
0.001	10	~10^{-3}
0.001	100	~10^{-2}
0.001	1000	~10^{-1}
0.01	100	~10^{-2}
0.1	100	~10^{-2}
1	100	~2×10^{-2}

Notice that the error increases further for high frequency applications. This is a result of the limited bandwidth of the OPAMP; we have to remember that the open-loop voltage gain reduces proportional to the frequency. The error is less than 1 % if and only if the frequency of the applied signal is below 100 times the OPAMP pole's frequency. For the OPAMP 741; f_P=6 Hz; hence the signal's frequency has to be less than 600 Hz for an ideal amplification factor of -10.

The effects of the OPAMP finite input impedance are not very relevant if the used impedances Z1 and ZF are lesser than Zi/10.

- Slew-rate limitations: will be discussed in class.
- Common-mode signals: will be discussed in class.

ANALOG CIRCUITS

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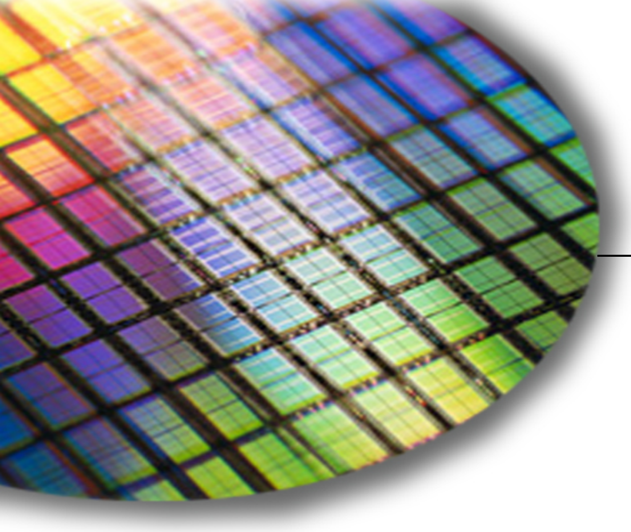
ANALOG DEVICES

Data Conversion Fundamentals

Analog-Digital Converters



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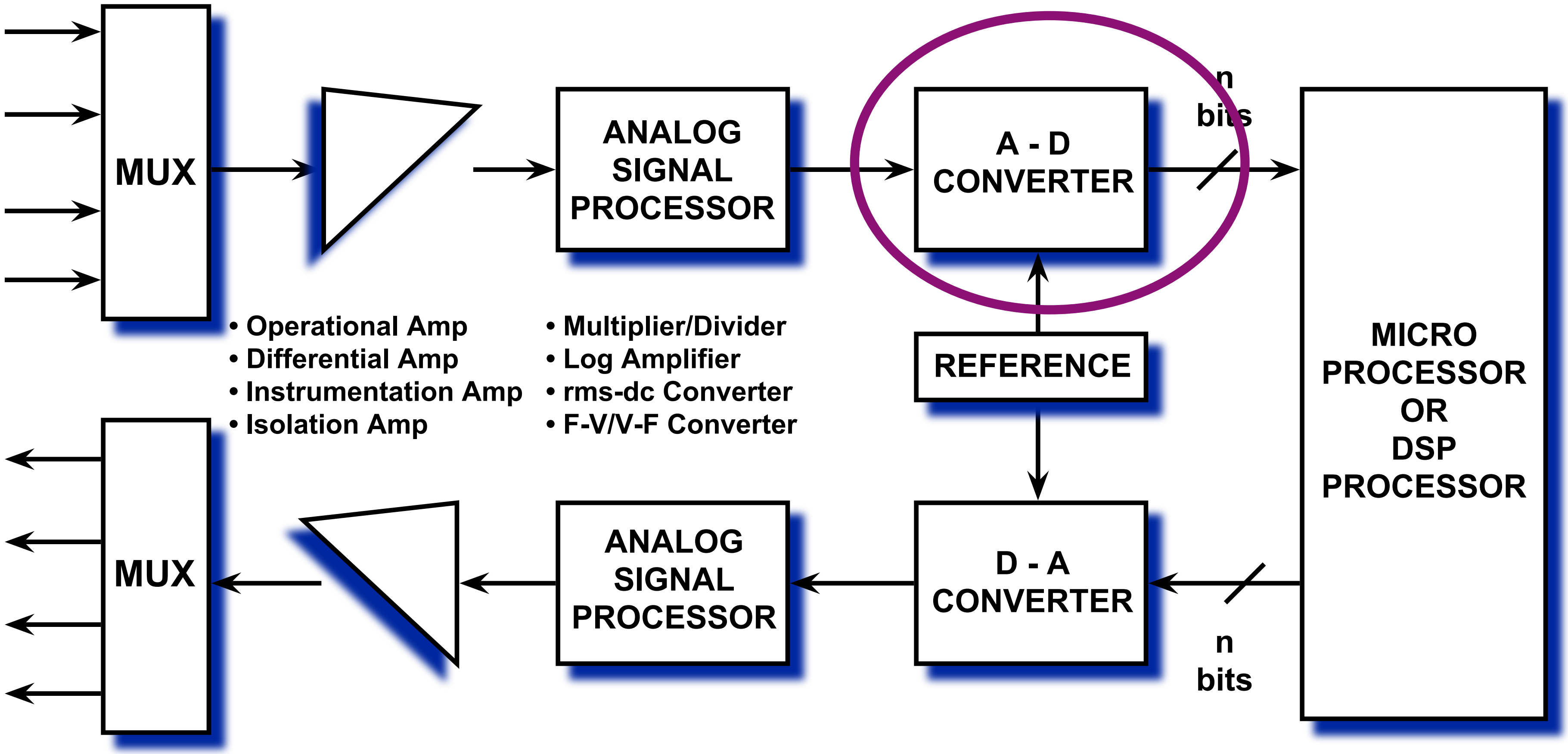
Introduction to A/D Converters

ANALOG DEVICES

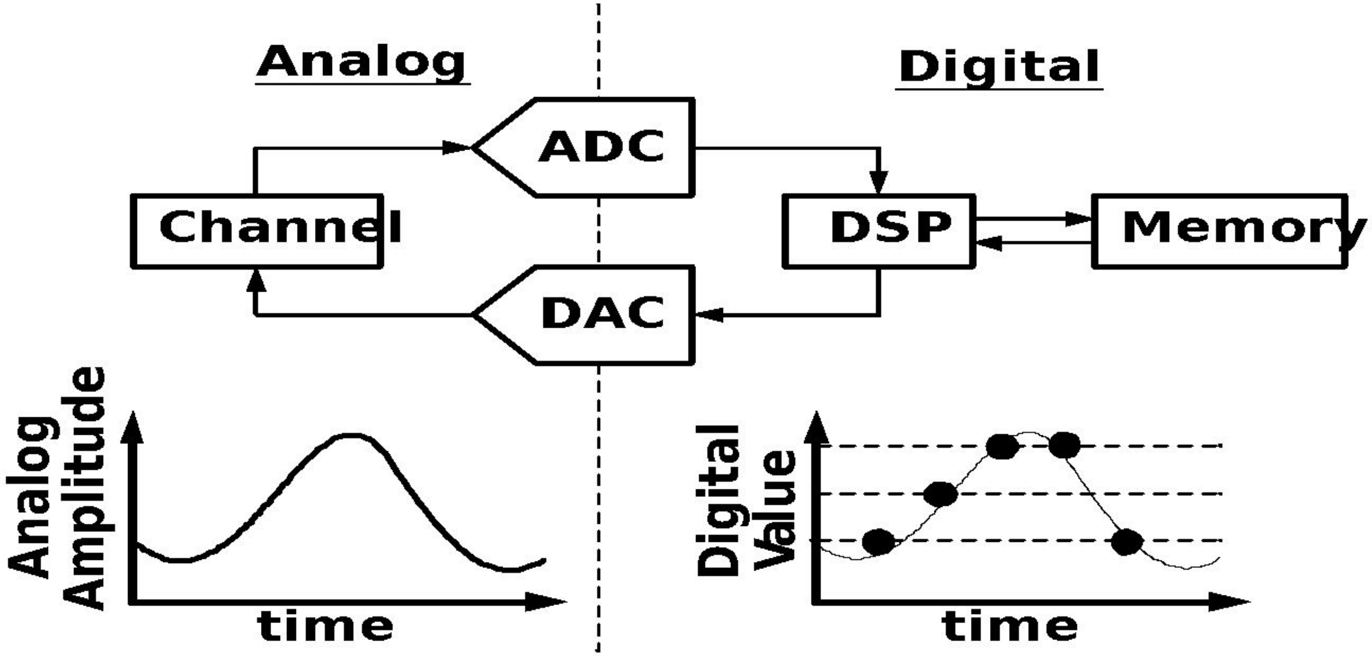
A/D Converter (ADC) Introduction

- A/D Fundamentals
  - Sampling
  - Quantization
- Factors Affecting A/D Converter Performance
  - Static Performance
  - Dynamic Performance
- ADC Architectures
  - SAR ADCs
  - Pipelined ADCs
  - Flash Type ADC
  - Sigma-Delta ADCs
- High Speed ADC Application Considerations

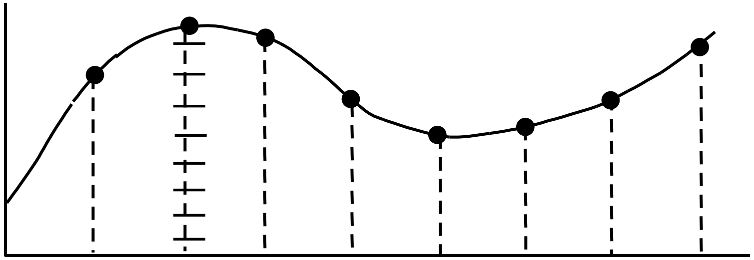
The Measurement & Control Loop



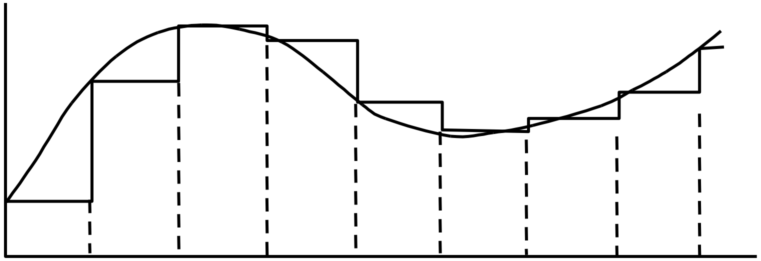
"REAL WORLD" SAMPLED DATA SYSTEMS CONSIST OF ADCs and DACs



ADC SAMPLED AND QUANTIZED WAVEFORM



DAC RECONSTRUCTED WAVEFORM



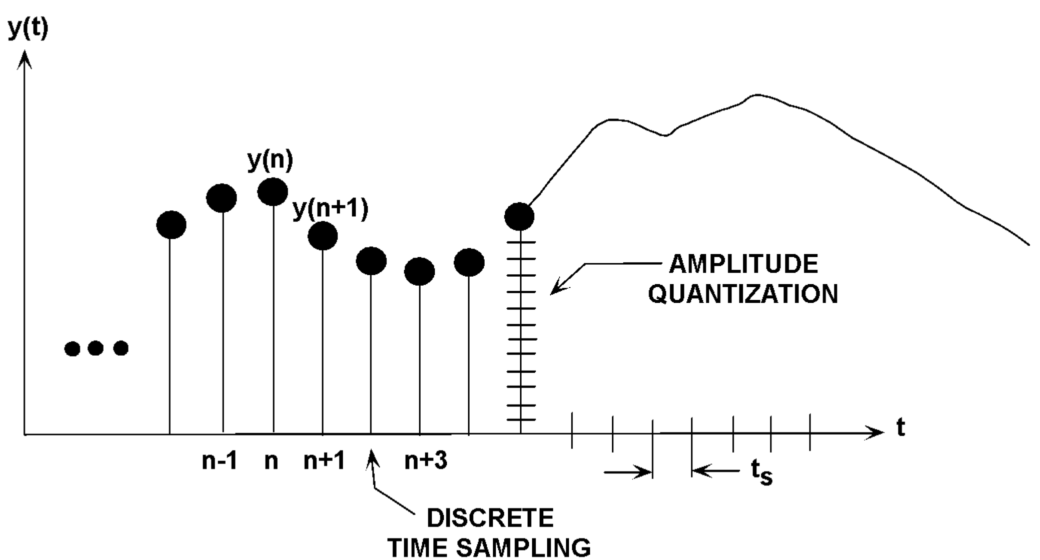
What is an Analog-Digital Converter?

$$\text{DIGITAL OUTPUT CODE} = \frac{\text{Analog Input}}{\text{Reference Input}} \times (2^N - 1)$$

- Produces a Digital Output Corresponding to the Value of the Signal Applied to Its Input Relative to a Reference Voltage
- Finite Number of Discrete Values : 2^N Resulting in Quantization Uncertainty
- Changes Continuous Time Signal into Discrete Time Sampled Representation
- Sampling and Quantization Impose Fundamental yet Predictable Limitations

Sampling Process

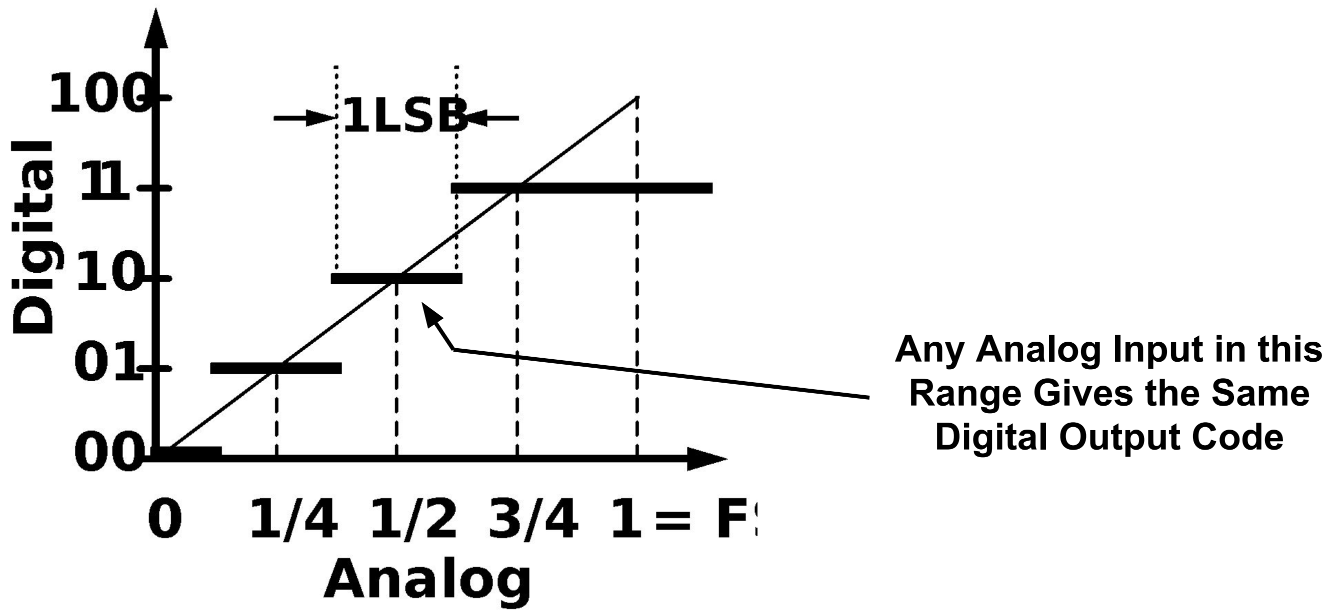
- Representing a continuous time domain signal at discrete and uniform time intervals
- Determines maximum bandwidth of sampled (ADC) or reconstructed (DAC) signal (Nyquist Criteria)
- Frequency Domain- “Aliasing” for an ADC and “Images” for a DAC



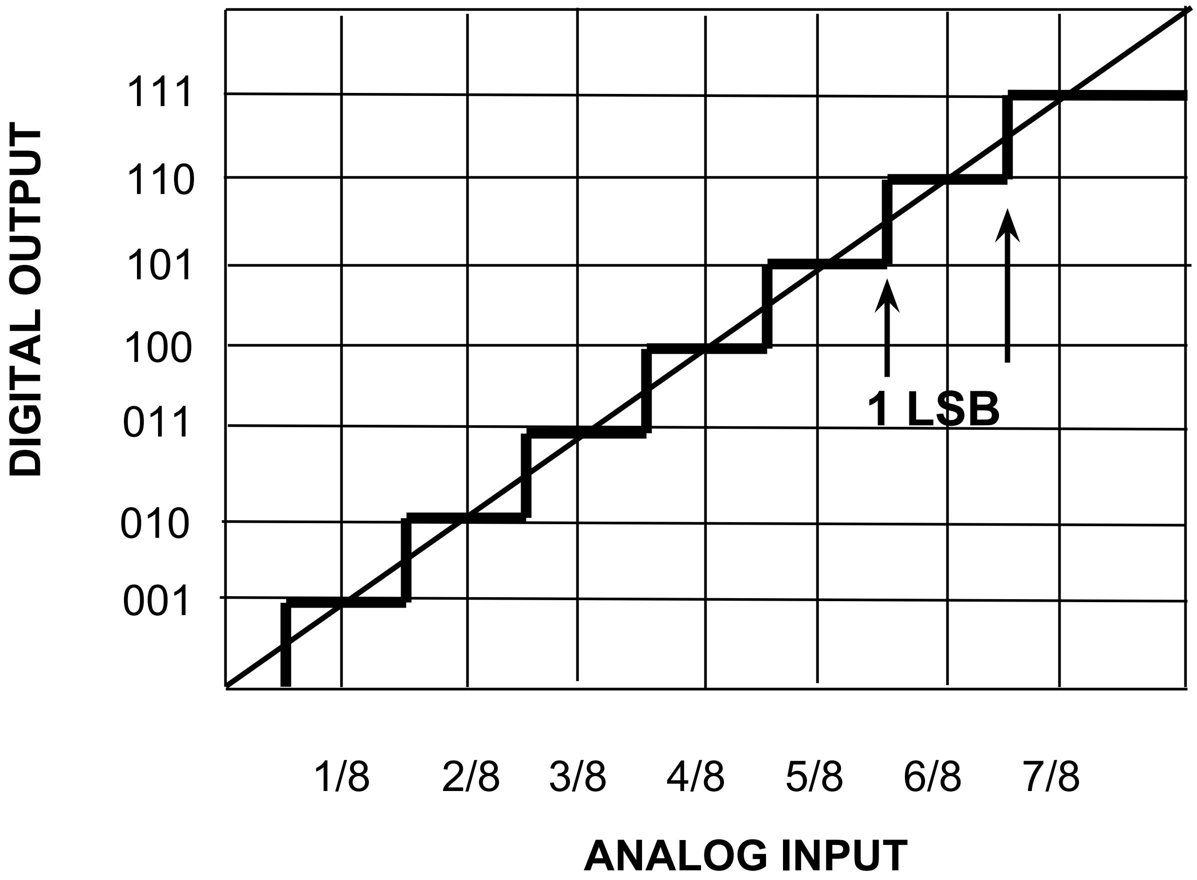
ANALOG DEVICES

Quantization Process

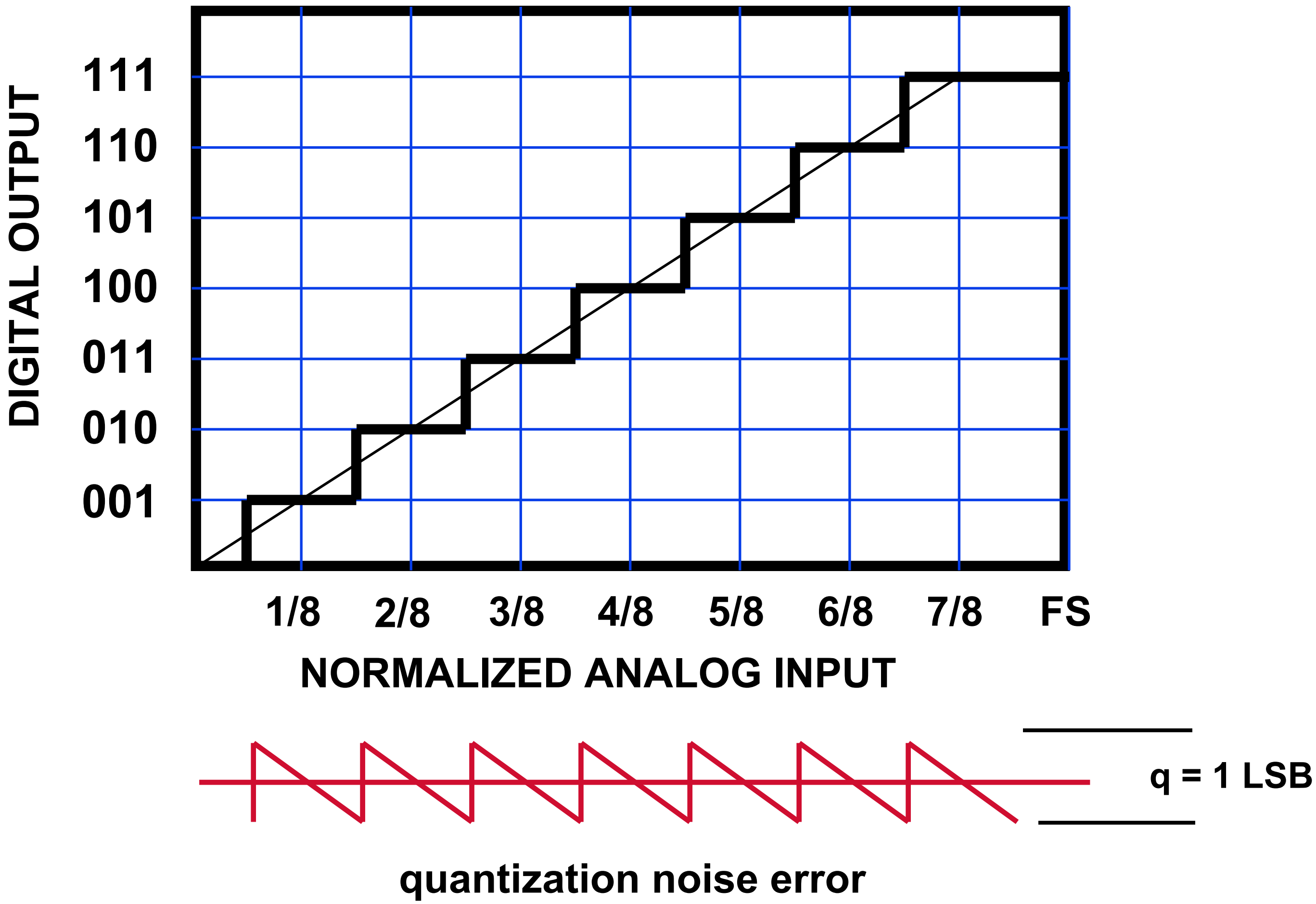
- Quantization Process
  - Representing an analog signal having infinite resolution with a digital word having finite resolution
  - Determines Maximum Achievable Dynamic Range
  - Results in Quantization Error/Noise



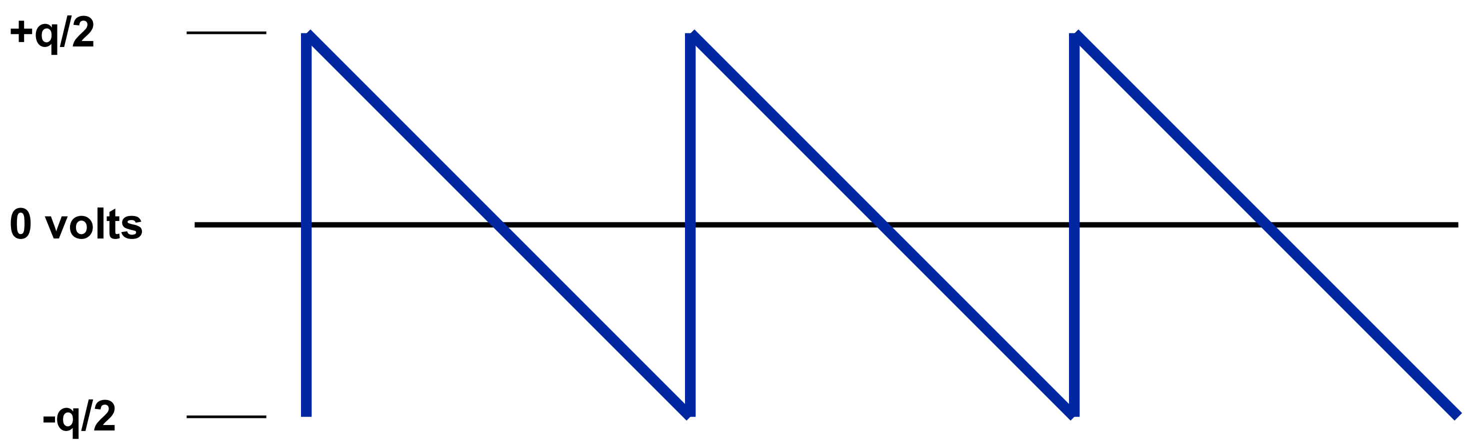
Conversion Relationship for an Ideal A/D Converter



Quantization Noise

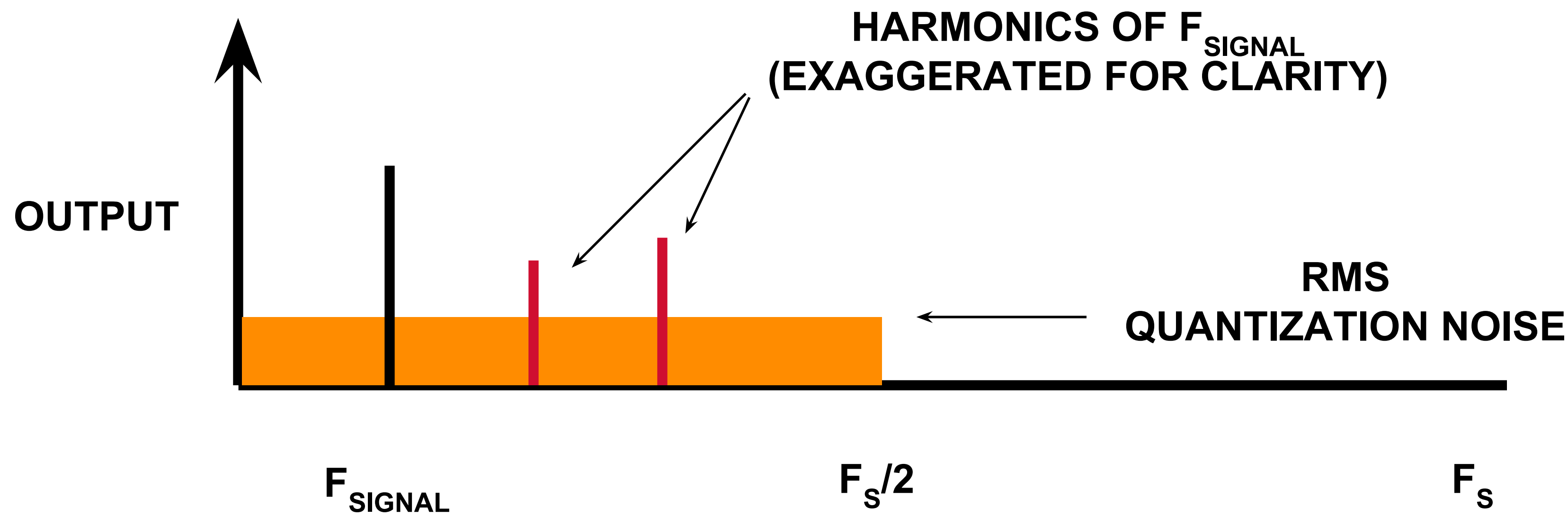


Quantization Noise (con't)



- The RMS value of the quantization noise sawtooth is its peak value, $q \div 2$, divided by $\sqrt{3}$, or $q \div \sqrt{12}$
- For Sine Wave Full Scale RMS Value is $2^{(N-1)}/\sqrt{2}$
- For Saw Tooth Quantization Error Signal RMS Value is $q/\sqrt{12}$
- Thus S/N is 1.225×2^N
- Expressed in dB as 1.76 + 6.02N, where N is the resolution of the A/D converter

Quantization Noise (con't)

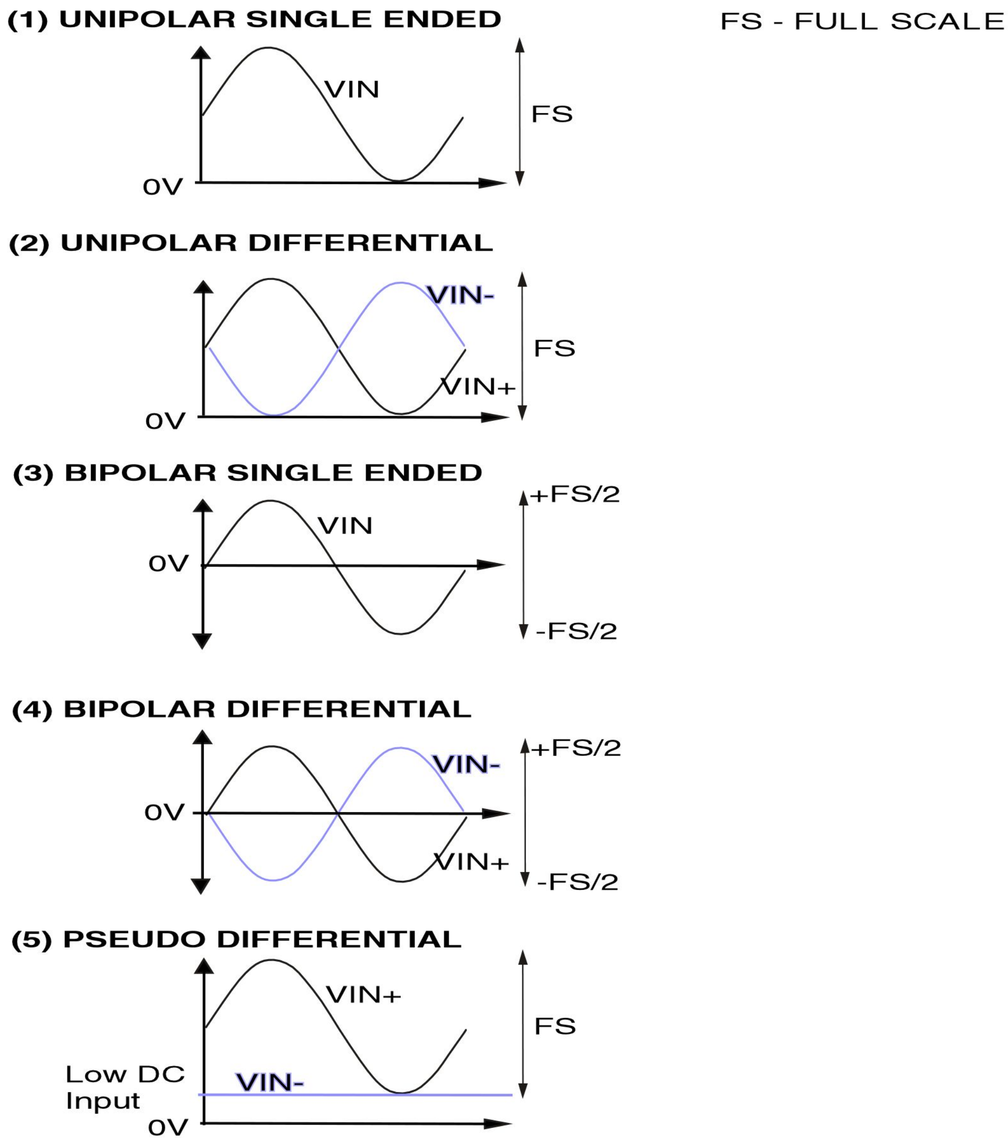


- If the quantization noise is uncorrelated with the frequency of the AC input signal, the noise will be spread evenly over the Nyquist bandwidth of $F_s/2$.
- If, however the input signal is locked to a sub-multiple of the sampling frequency, the quantization noise will no longer appear uniform, but as harmonics of the fundamental frequency

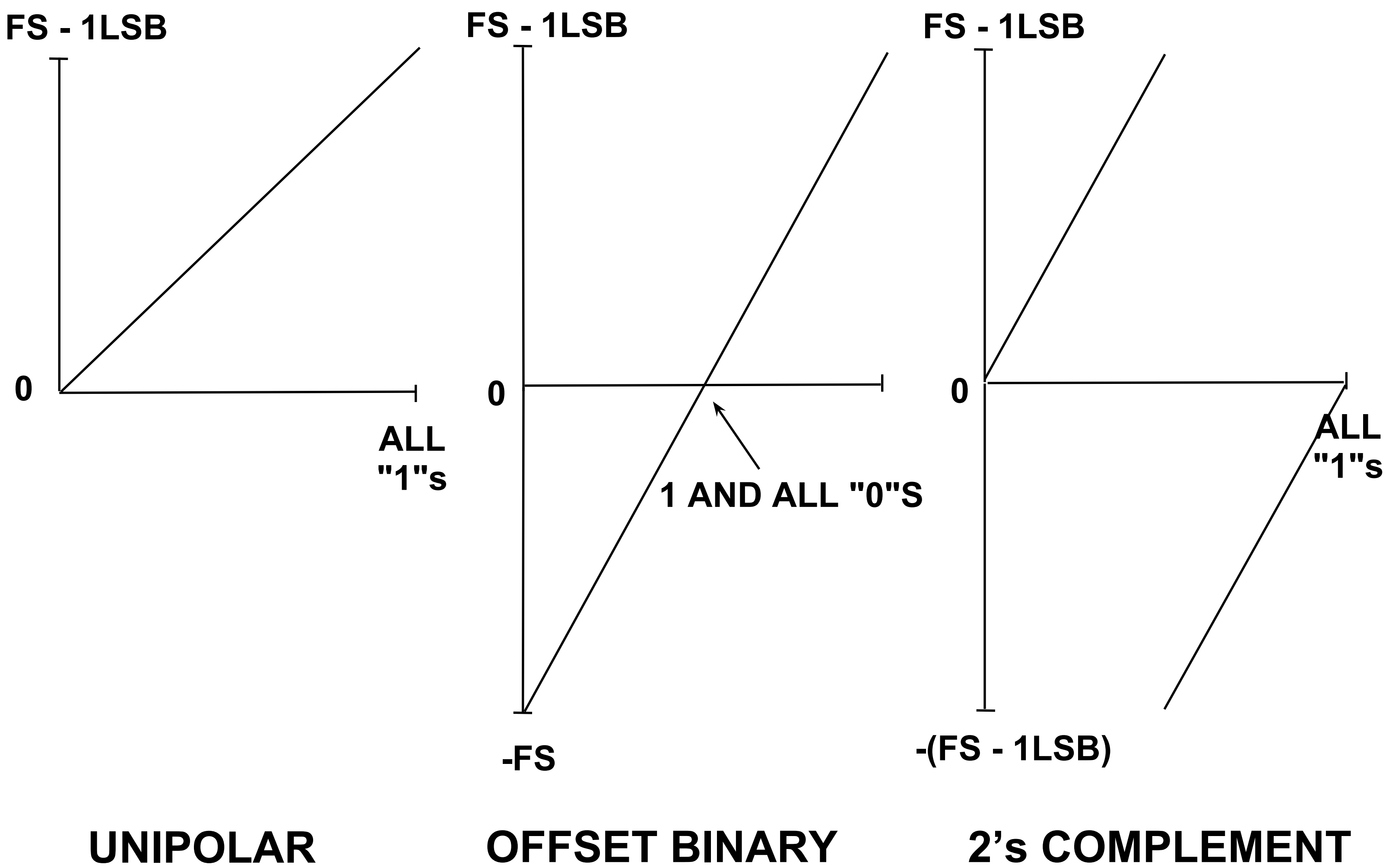
ADC Resolution vs. Quantization Parameters

Resolution, Bits (n)	2^n	LSB, mV (2.5V FS)	% Full Scale	ppm Full Scale	dB Full Scale
8	256	9.77	0.391	3906	-48.0
10	1024	2.44	0.098	977	-60.0
12	4096	0.610	0.024	244	-72.0
14	16,384	0.153	0.006	61	-84.0
16	65,536	0.038	0.0015	15	-96.0
18	262,164	0.0095	0.00038	3.8	-108.0

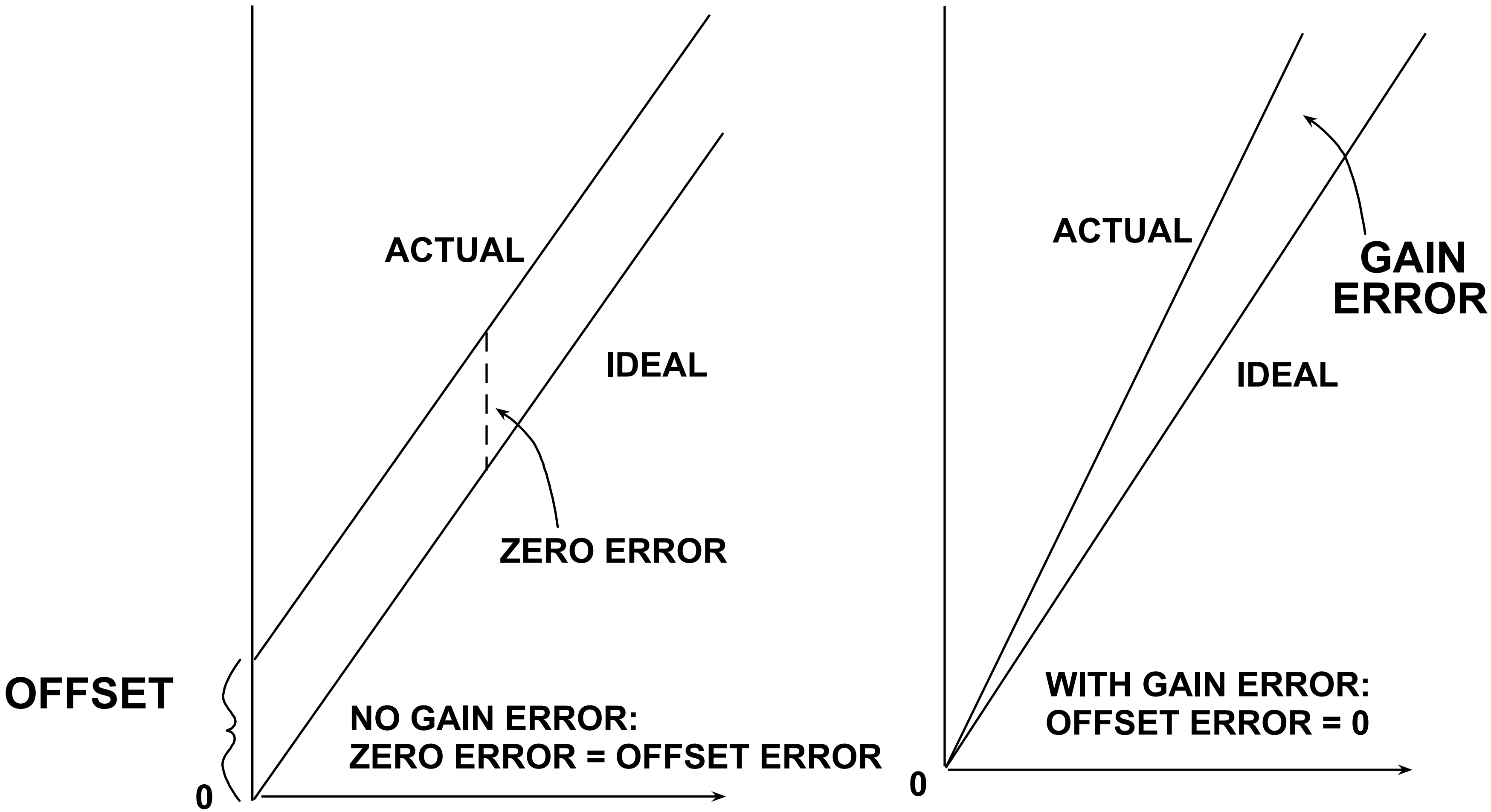
Analog Input Signal Definitions



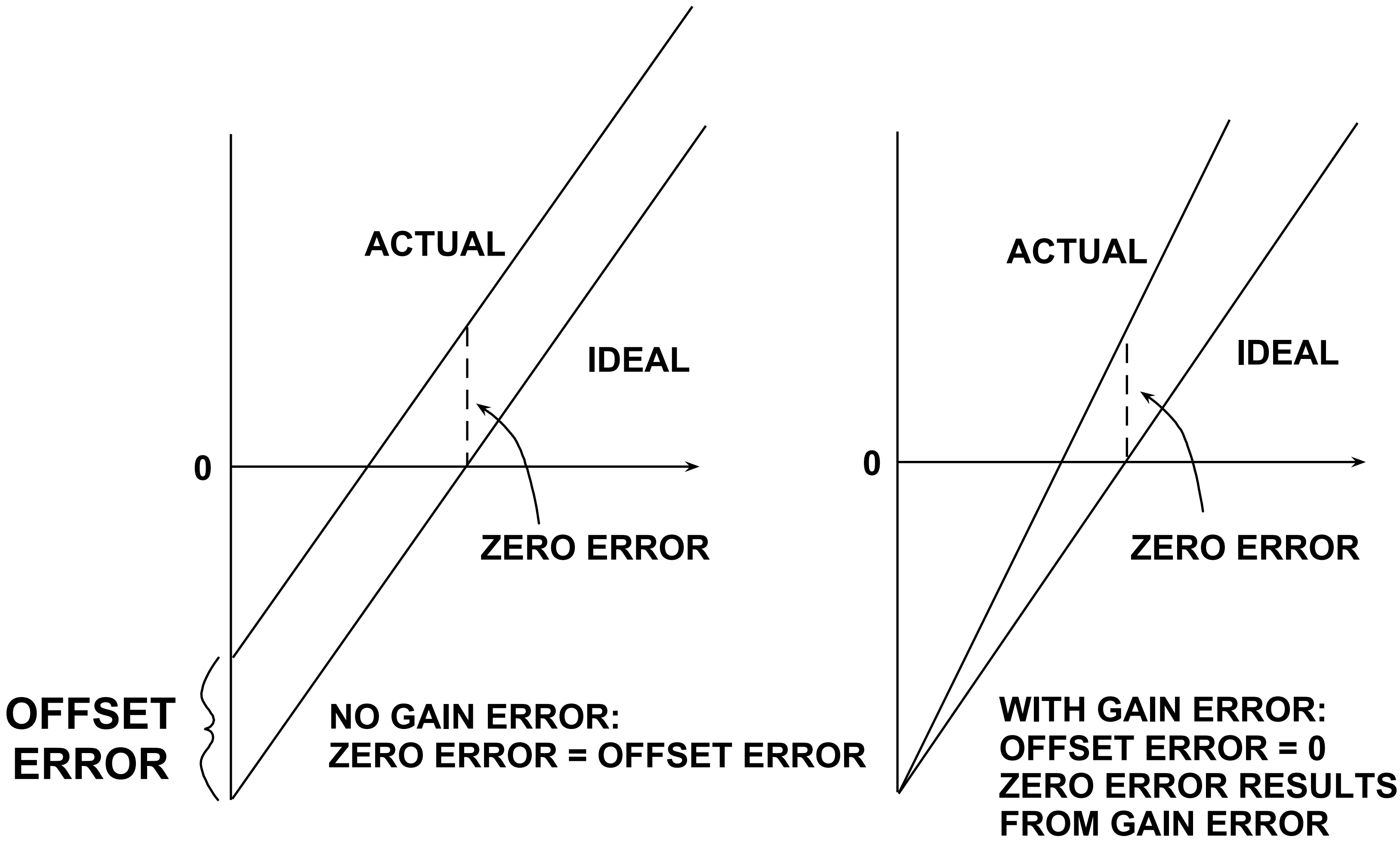
Unipolar and Bipolar Converter Codes



Factors Affecting A/D Converter Performance - Offset And Gain for Unipolar Ranges



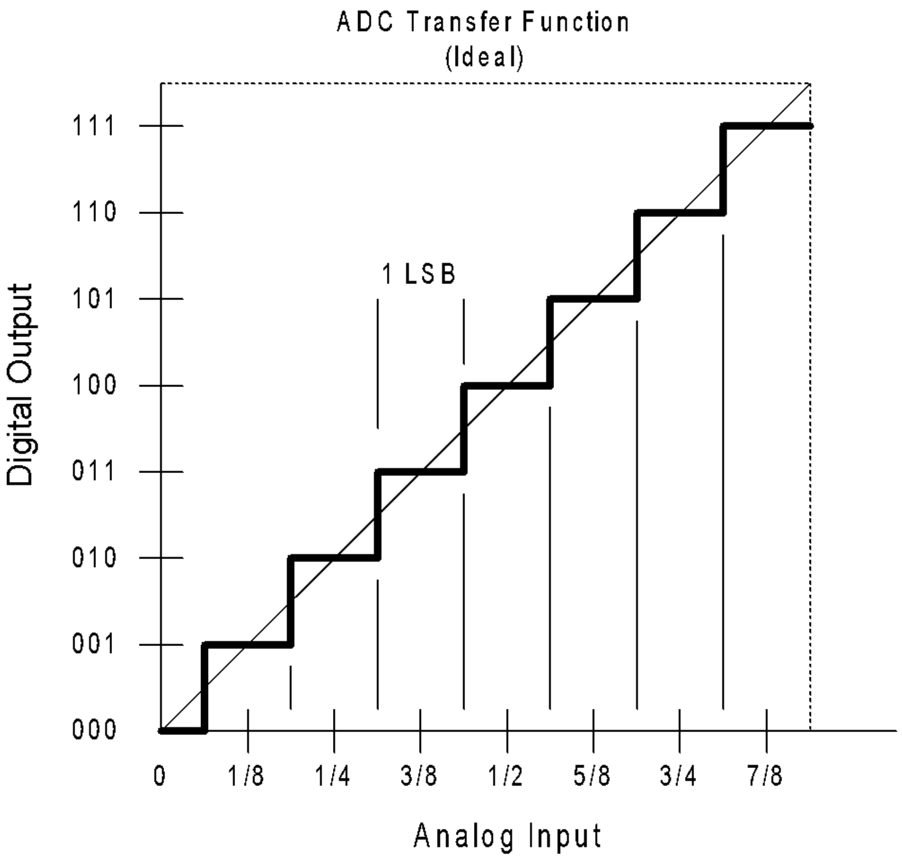
Factors Affecting A/D Converter Performance - Offset And Gain for Bipolar Ranges



ANALOG DEVICES

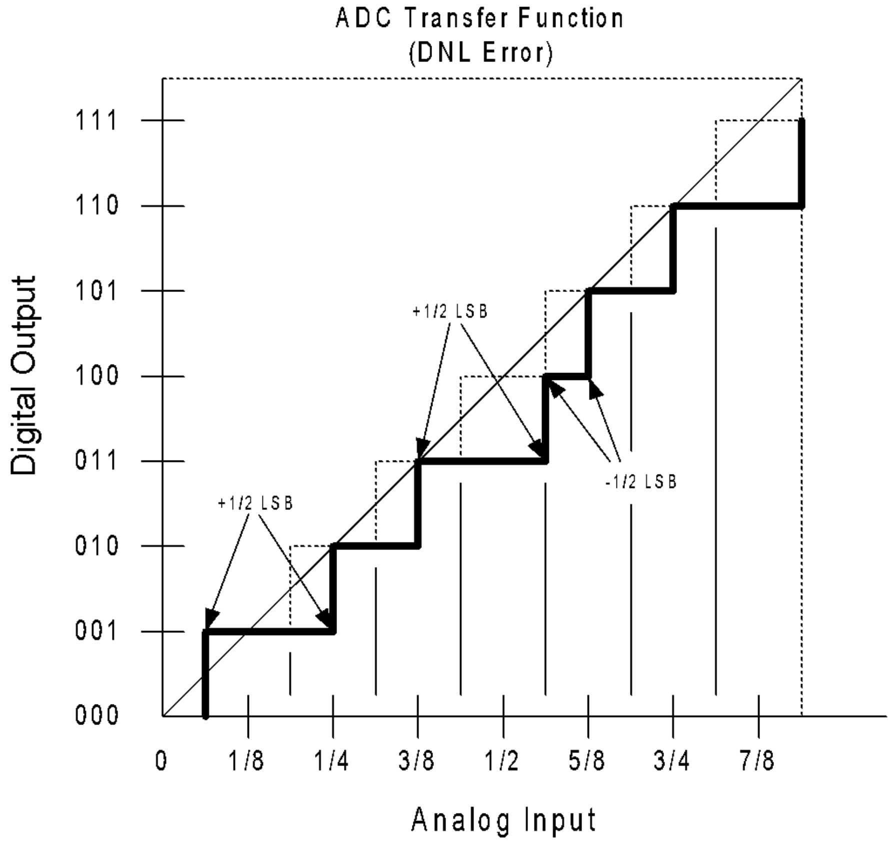
DC Specifications (Ideal)

- Ideal ADC code transitions are exactly 1 LSB apart.
- For an N-bit ADC, there are 2^N codes. (1 LSB = FS/ 2^N)
- For this 3-bit ADC, 1 LSB = ($1V/2^3$ = 1/8th)
- Each “step” is centered on an eighth of full scale



DC Specifications (DNL)

- **Differential Non-Linearity (DNL) is the deviation of an actual code width from the ideal 1 LSB code width**
- **Results in narrow or wider code widths than ideal and can result in missing codes**
- **Results in additive noise/spurs beyond the effects of quantization**



DC Specifications (DNL)

- DNL error is measured in lsbs.
- A given ADC will have a typical DNL pattern.
- These patterns will also have an element of randomness to them.

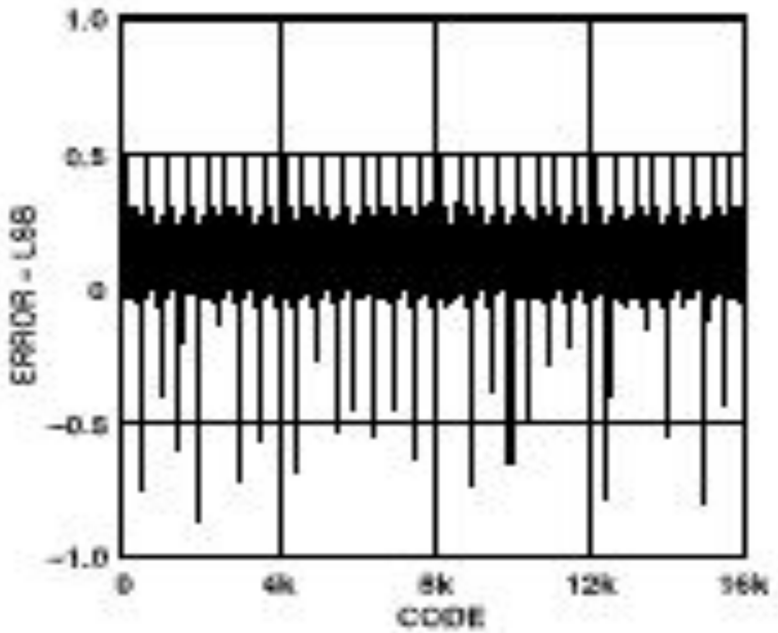
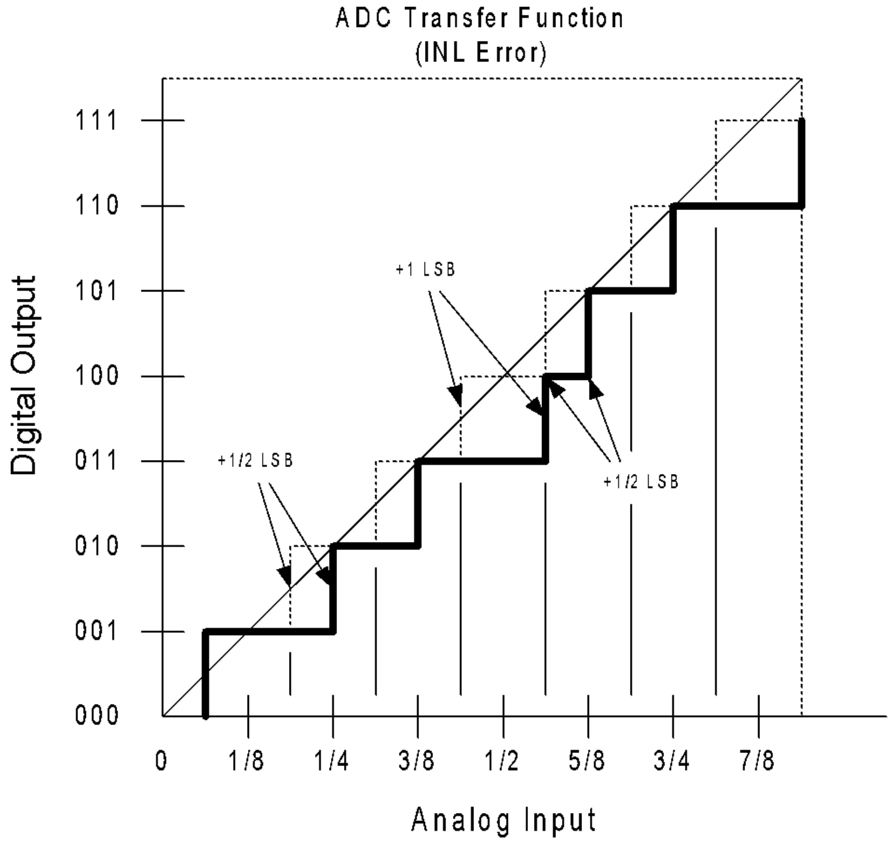


Figure 13. Typical DNL

DC Specifications (INL)

- Integral Non-Linearity (INL) is the deviation of an actual code transition point from its ideal position on a straight line drawn between the end points of the transfer function.
- INL is calculated after offset and gain errors are removed
- Results in additive harmonics and spurs



DC Specifications (INL)

- Some typical INL patterns

Bow indicates 2nd order nonlinearity

"S" indicates 3rd order nonlinearity

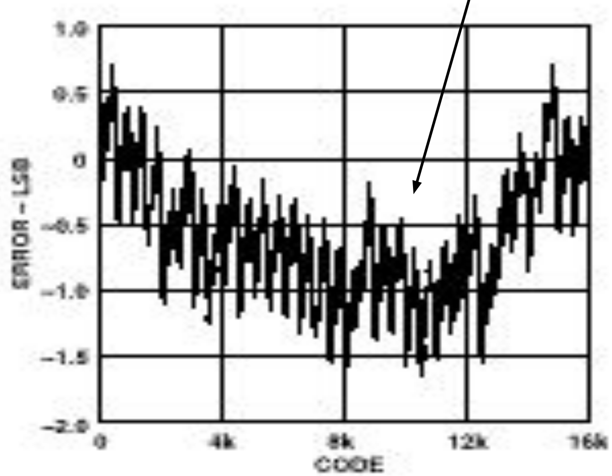


Figure 12. Typical INL

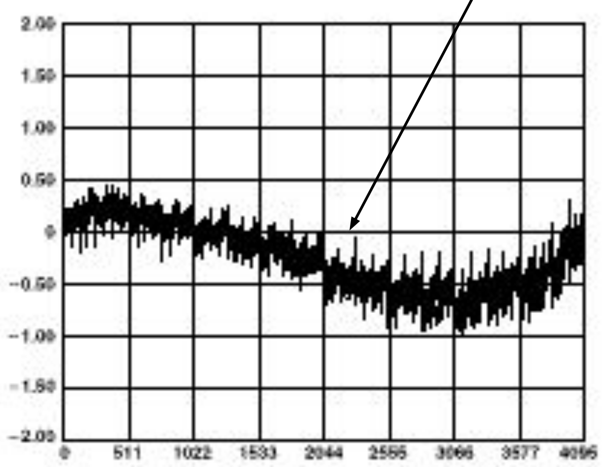
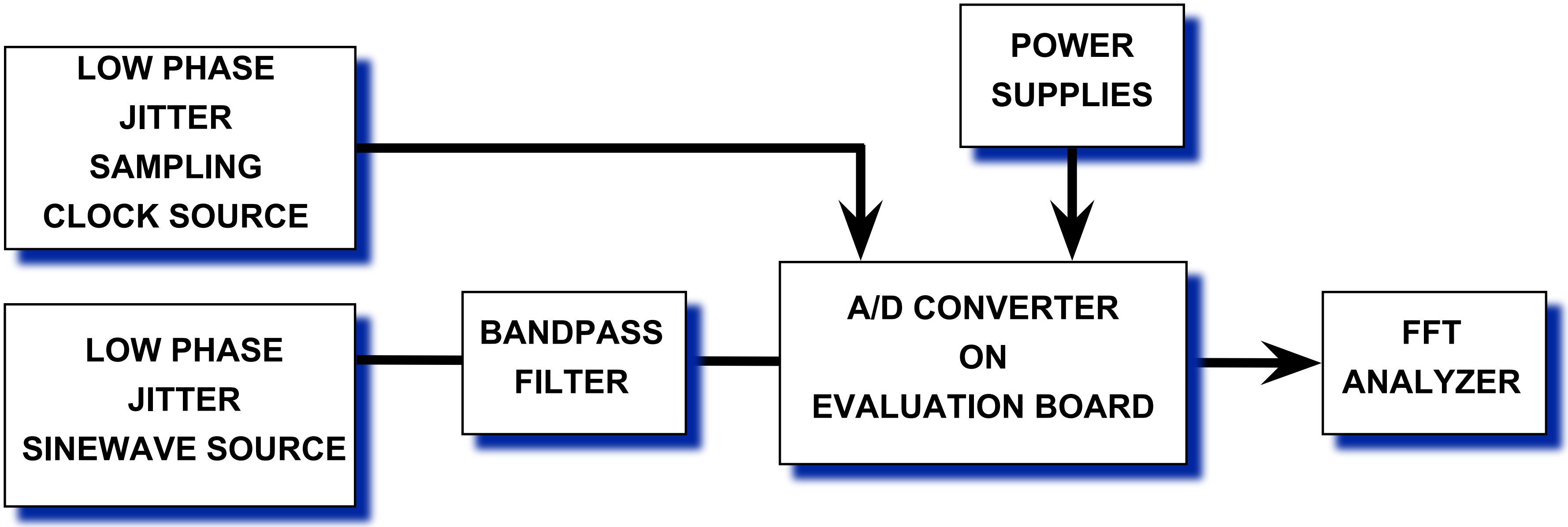


Figure 5. Typical INL

QUANTIFYING ADC DYNAMIC (AC) PERFORMANCE

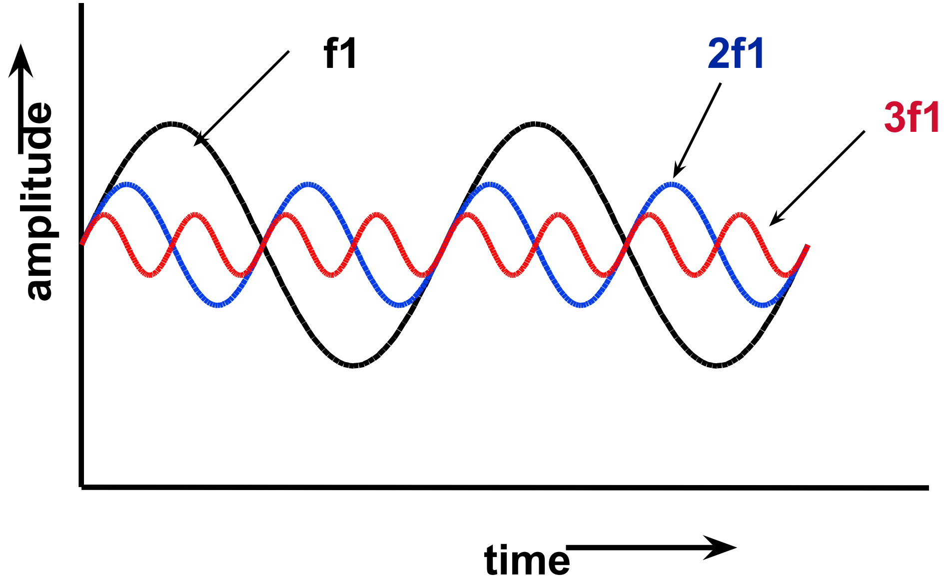
- Harmonic Distortion
- Worst Harmonic
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion Plus Noise (THD + N)
- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
- Analog Bandwidth (Full-Power, Small-Signal)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion
- Noise Power Ratio (NPR) or Multitone Power Ratio (MPR)

Dynamic Testing of A/D Converters

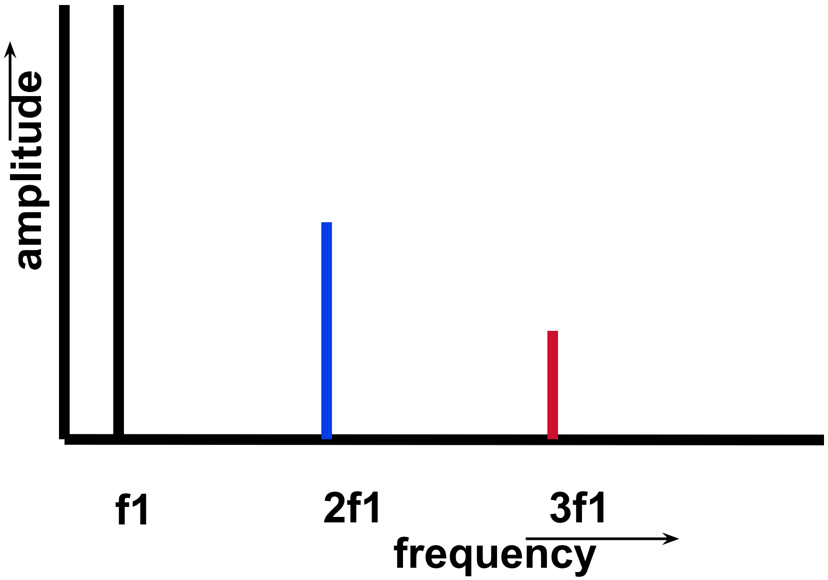


- A *Fast Fourier Transform* (FFT) Analyzer is used to measure dynamic performance

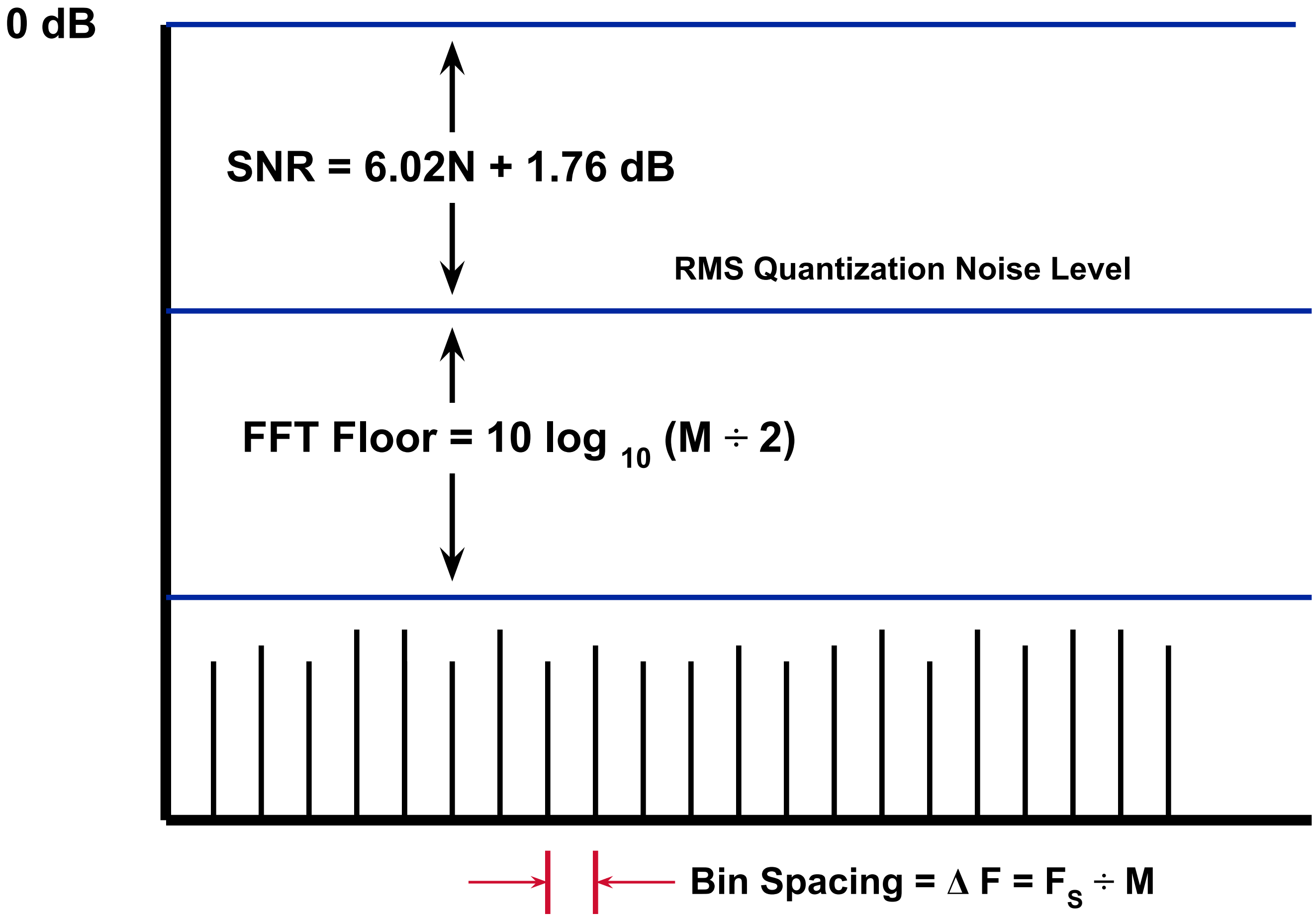
Fast Fourier Transform converts this…



…to this



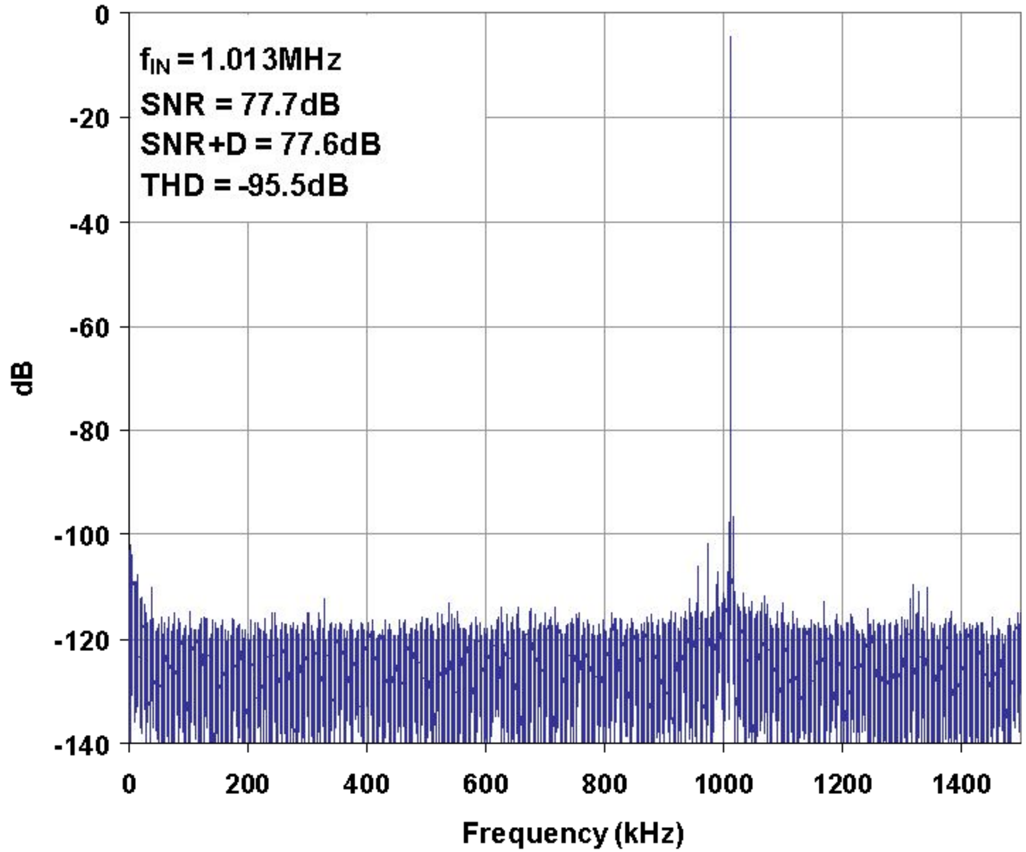
An M-Point FFT



18 dB, M = 128
21 dB, M = 256
24 dB, M = 512
27 dB, M = 1024
30 dB, M = 2048
33 dB, M = 4096

The Effective Noise Floor of an M-Point FFT Is Less Than The RMS Value of the Quantization Noise

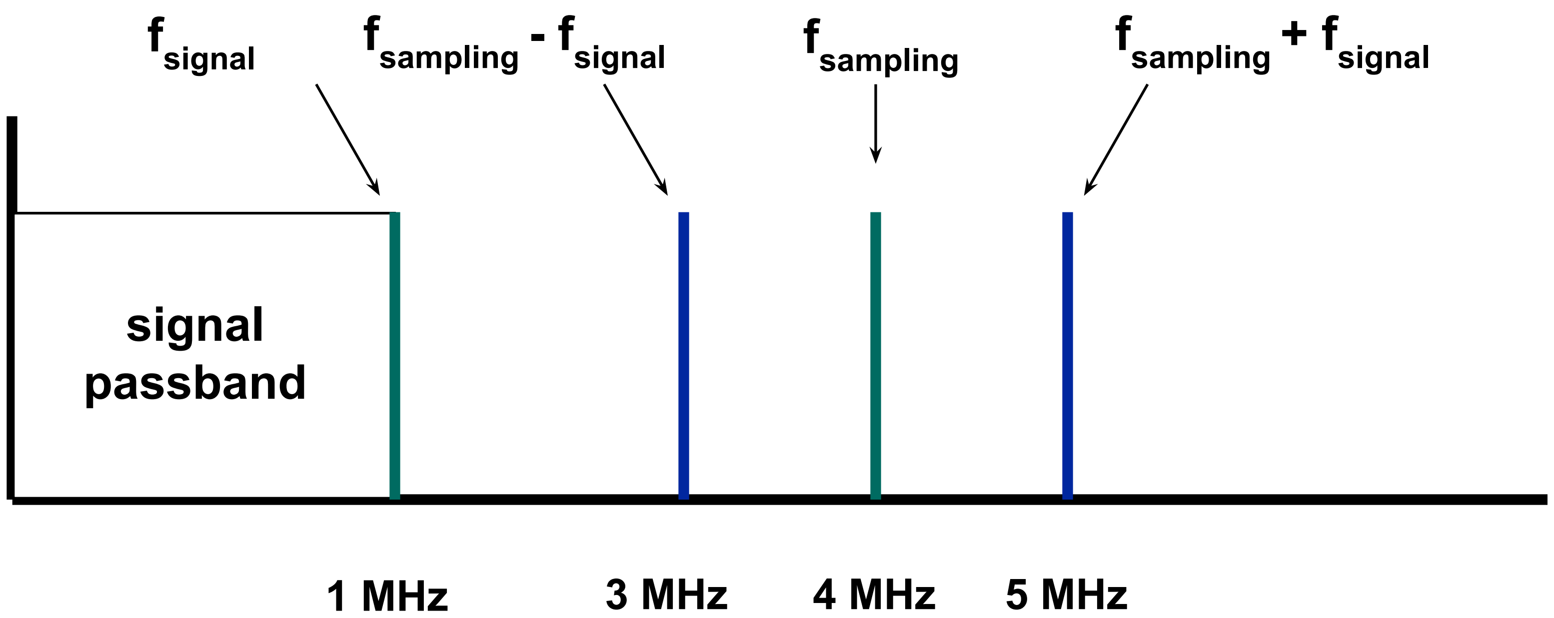
Actual FFT Plot for AD7484, 14-Bit SAR ADC Sampling at 3MHz



Nyquist Bandwidth & Aliasing

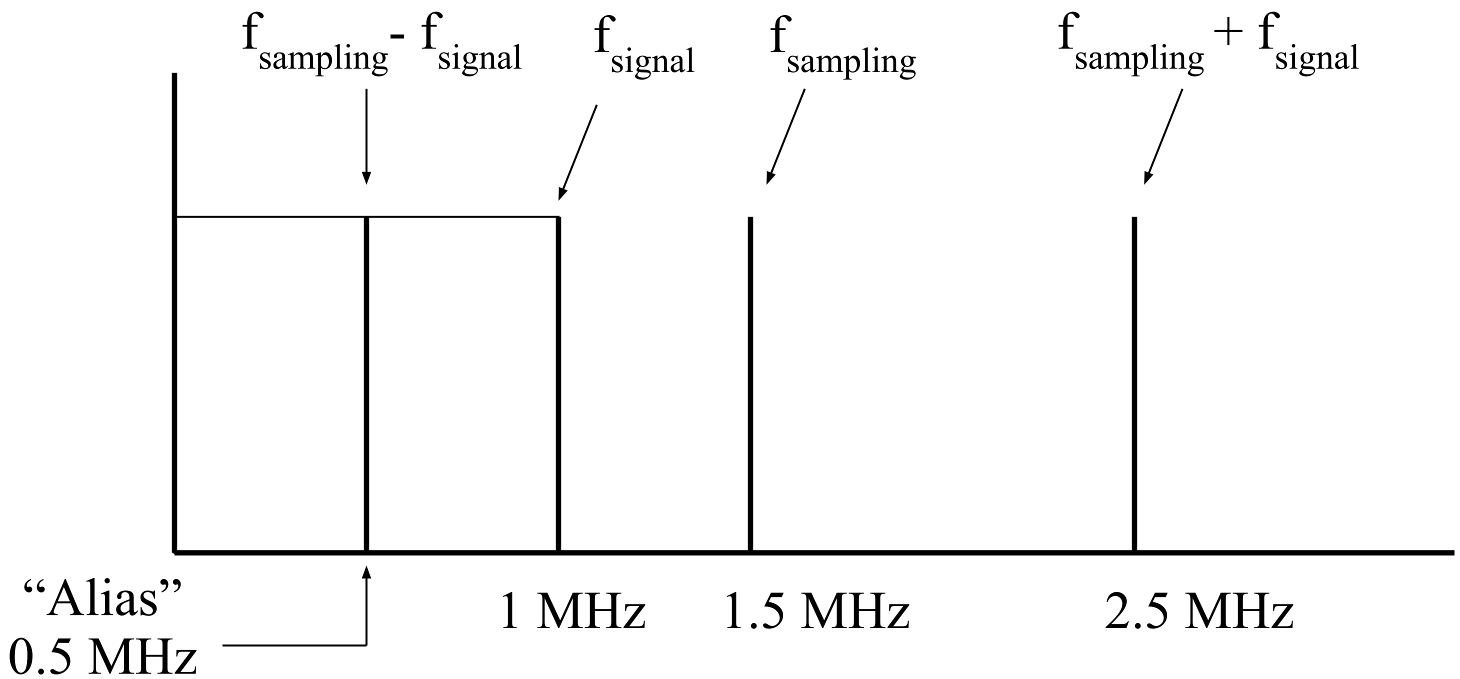
- 2 Signals that are Mixed Together Produce Sum and Difference Frequency Components
- Nyquist Theory Stipulates that the Signal Frequency, F_{SIGNAL} must be $\leq$ to ½ $F_{SAMPLING}$ to Prevent a Condition Known As “Aliasing”, in which the Difference Component Appears Within the Signal Bandwidth of Interest

The Nyquist Bandwidth & Aliasing
($F_{SIGNAL} \leq \frac{1}{2} F_{SAMPLING}$)



The Signal Frequency Is < 1/2 the Sampling Frequency and So the Sum and Difference Components Fall Outside (Beyond) the Signal Passband

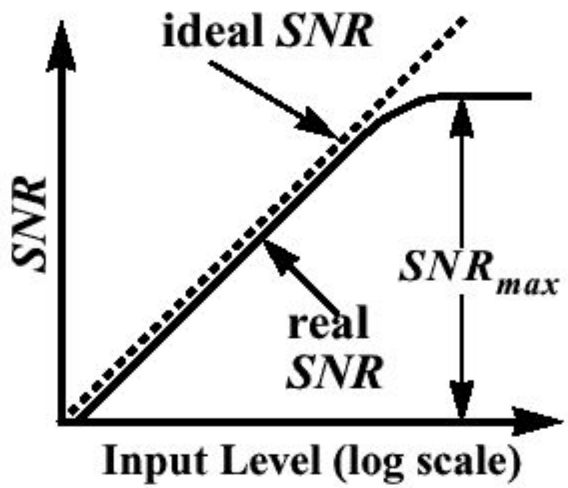
The Nyquist Bandwidth & Aliasing
$(F_{SIGNAL} \geq ½ \ F_{SAMPLING})$



The Signal Frequency Is > 1/2 (approx 2/3) the Sampling Frequency. An "Alias" or False Image is Thus Created that Falls Within the Passband of Interest.

SINAD, ENOB, and SNR

- **SINAD (Signal-to-Noise-and-Distortion Ratio)**
  - **The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding dc**
- **ENOB (Effective Number of Bits)**
  - $$ENOB = \frac{SINAD - 1.76dB}{6.02}$$
- **SNR (Signal-to-Noise Ratio, or Signal-to-Noise Ratio Without Harmonics)**
  - **The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first five harmonics and dc**

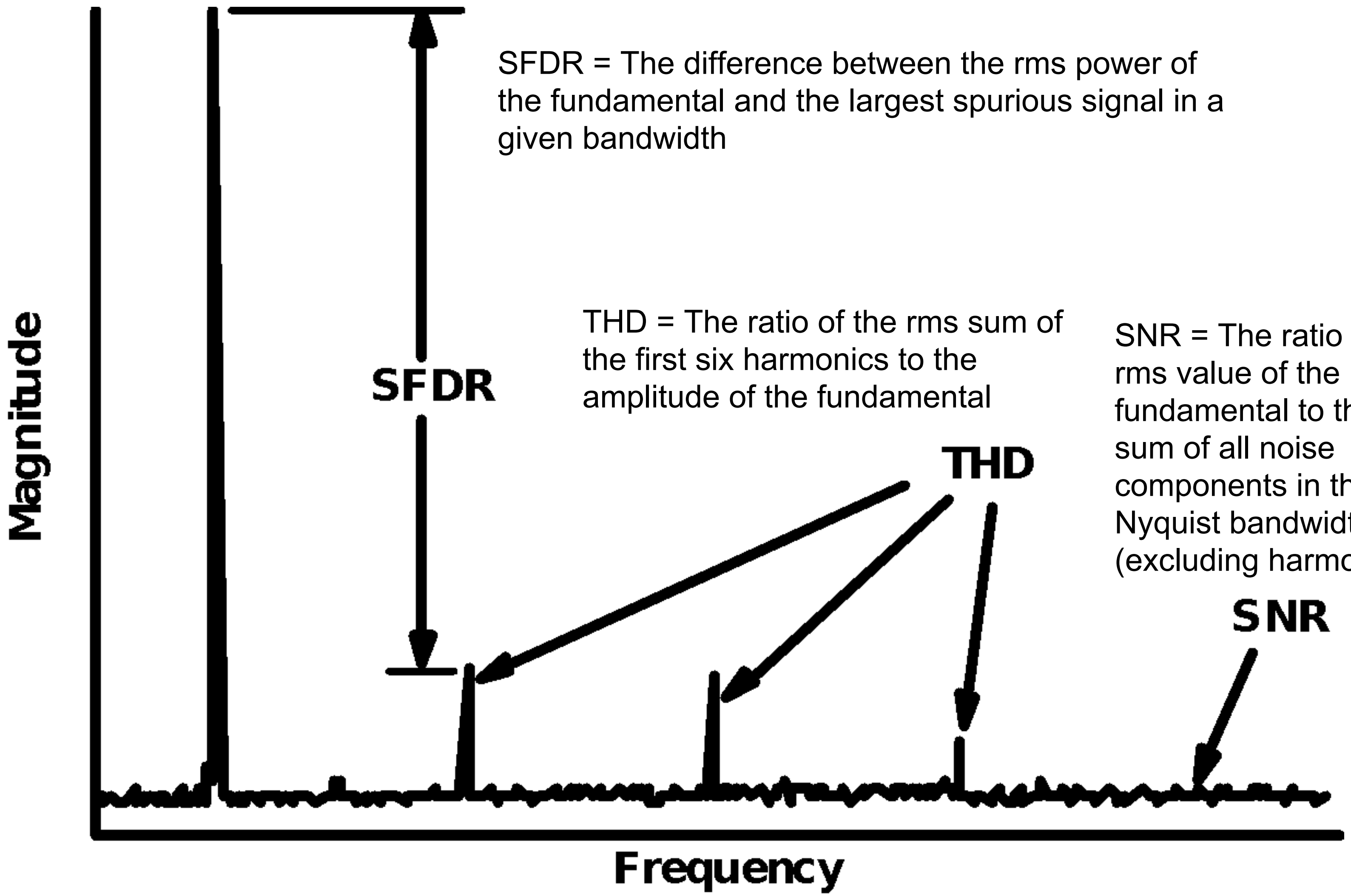


SFDR, THD, and SNR

SFDR = The difference between the rms power of the fundamental and the largest spurious signal in a given bandwidth

THD = The ratio of the rms sum of the first six harmonics to the amplitude of the fundamental

SNR = The ratio of the rms value of the fundamental to the rms sum of all noise components in the Nyquist bandwidth (excluding harmonics)



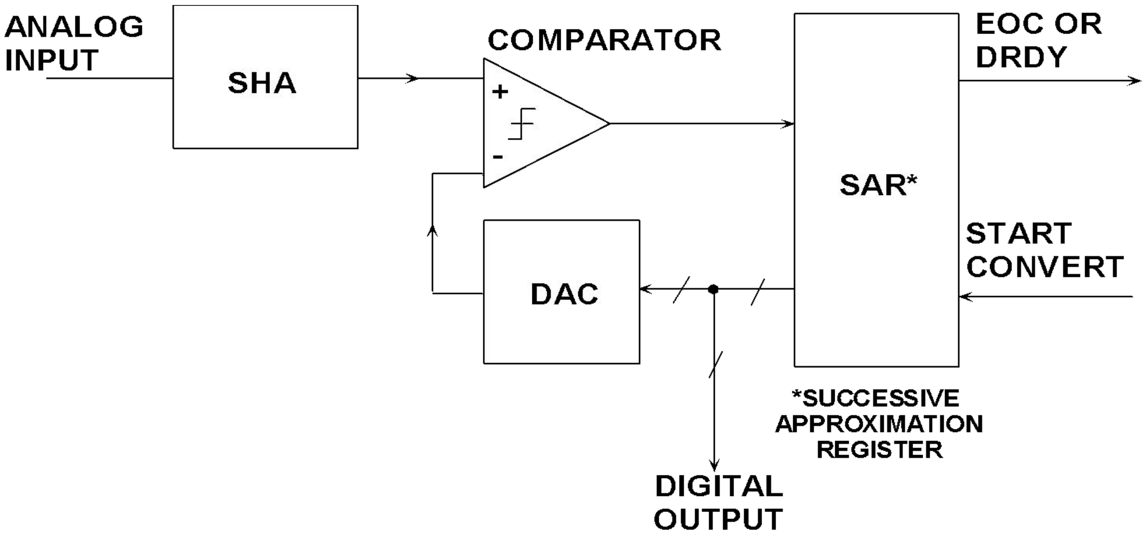
ANALOG DEVICES

ADC LARGE SIGNAL (OR FULL POWER) BANDWIDTH

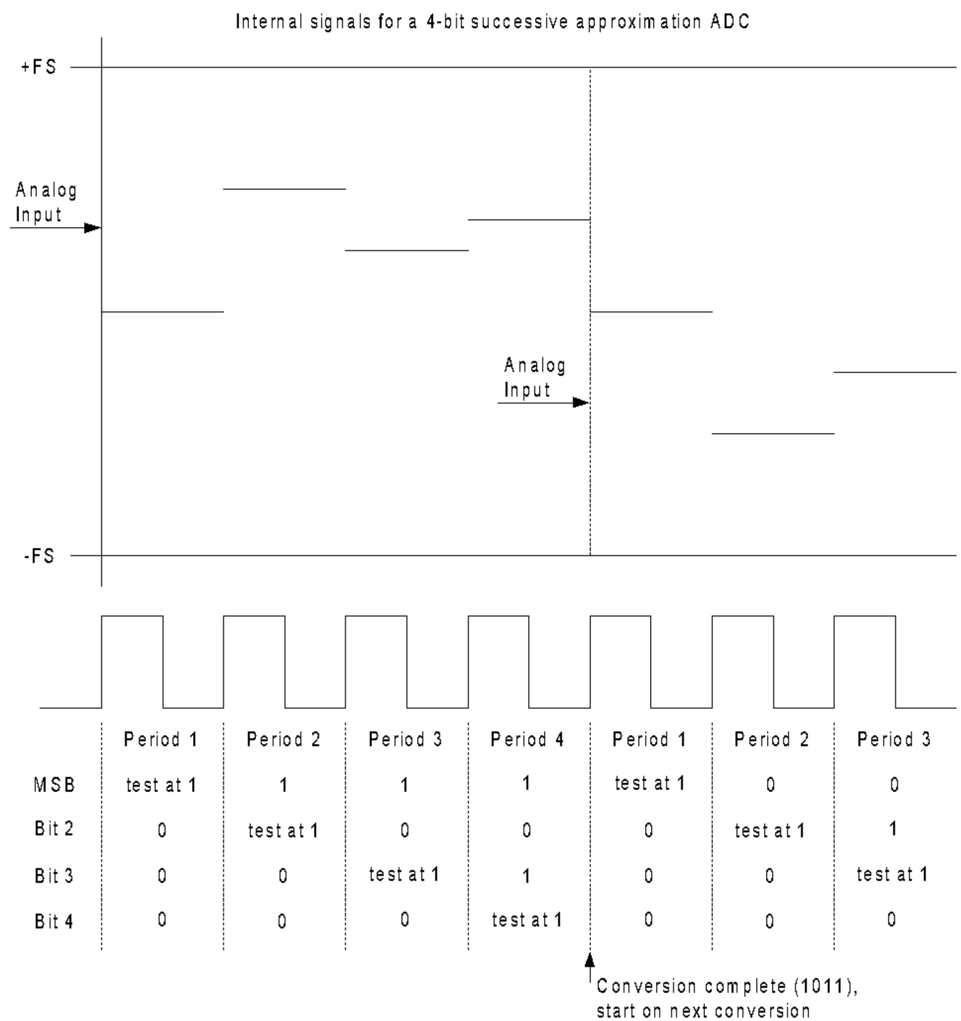
- Full-power bandwidth is defined as the input frequency where the fundamental in an FFT of the output, rolls off to its 3 dB point
- ADC's SHA generally determines the FPBW
  - FPBW often limited by slew rate of the internal circuitry.
  - May not be compatible with the converter's maximum operating rate
    - Ideally $f_{FPBW} >> f_s / 2$
    - Many High Speed Converters have $f_{FPBW} < f_s / 2$
  - Use as a "prerequisite" specification for comparing ADC's IF undersampling capabilities. But need to consider distortion as well.

Successive Approximation ADC

"Recursive" One-Bit Sub-Ranging Architecture



Successive Approximation ADC

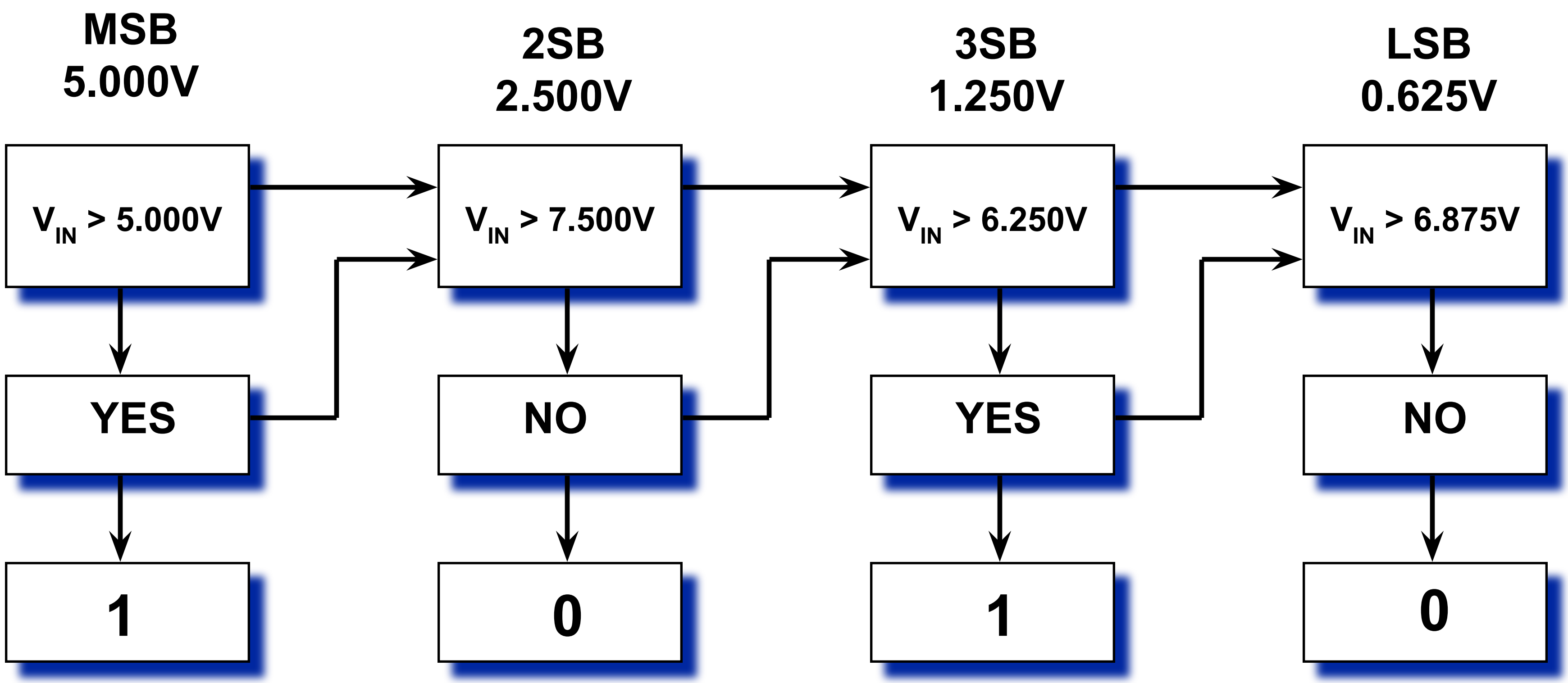


How a Successive Approximation A/D Converter Works

- Rising/Falling Edge of Convert Start Pulse Resets Logic
- Falling/Rising Edge Begins Conversion Process
- Bit Comparisons Made on Each Clock Edge
- Conversion Time Equals Number of Comparisons (Resolution) Times Clock Period
- The Accuracy of Conversion Depends on the DAC Linearity and Comparator Noise

How Successive Approximation Works

EXAMPLE : ANALOG INPUT = 6.428V, REFERENCE = 10.000V



Successive Approximation ADC

Advantages to SAR A/D converters

- Low Power (12-bit/1.5 MSPS ADC: 1.7 mW)
- Higher resolutions (16-bit/1 MSPS)
- Small Die Area and Low Cost
- No pipeline delay

Tradeoffs to SAR A/D converters

- Lower sampling rates

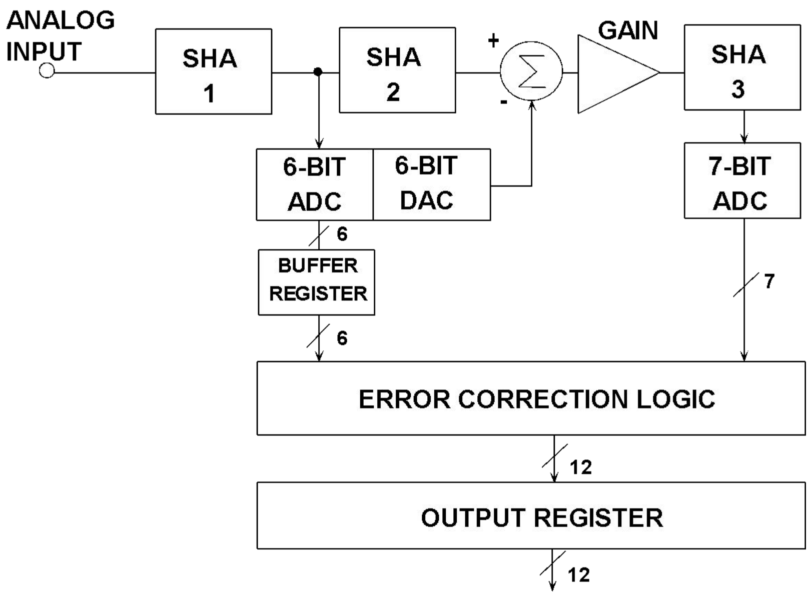
Typical Applications

- Instrumentation
- Industrial control
- Data acquisition

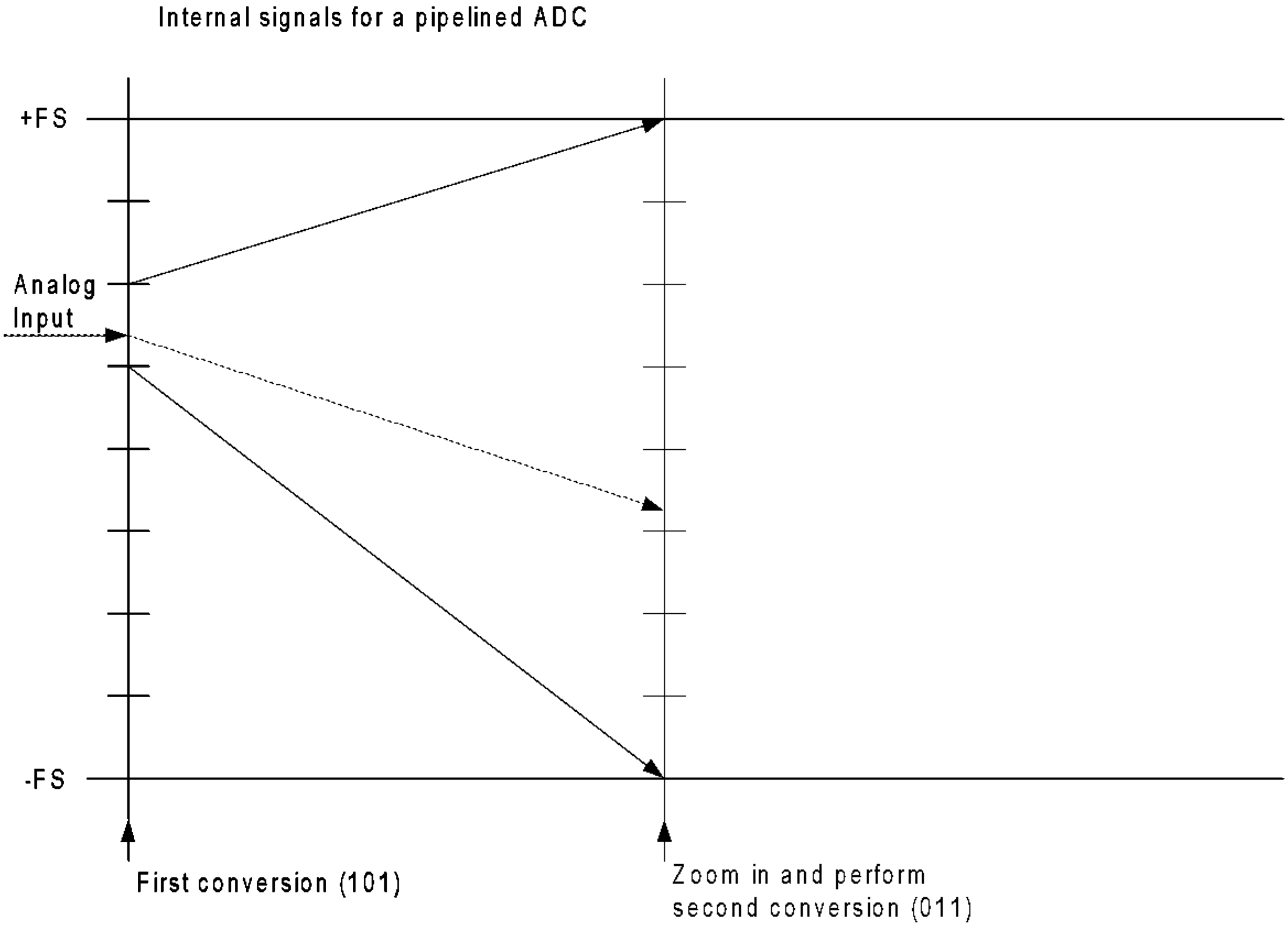
Pipelined Sub-ranging ADC

Conversion divided into discrete stages thus causing pipeline delay

- 1st Stage ADC is 6-bit FLASH
- 2nd Stage ADC is 7-bit Flash
- Total resolution is 12 bits (one bit used for error correction)



Pipelined Sub-ranging ADC



Pipelined Sub-ranging ADC

Advantages to Pipelined Sub-ranging A/D converters

- Higher resolutions at high-speeds (14-bits/105 MSPS)
- Digitize wideband inputs

- **Tradeoffs to pipelined sub-ranging A/D converters**

  - Higher power dissipation
  - Larger die size

Typical Applications

- Communications
- Medical imaging
- Radar

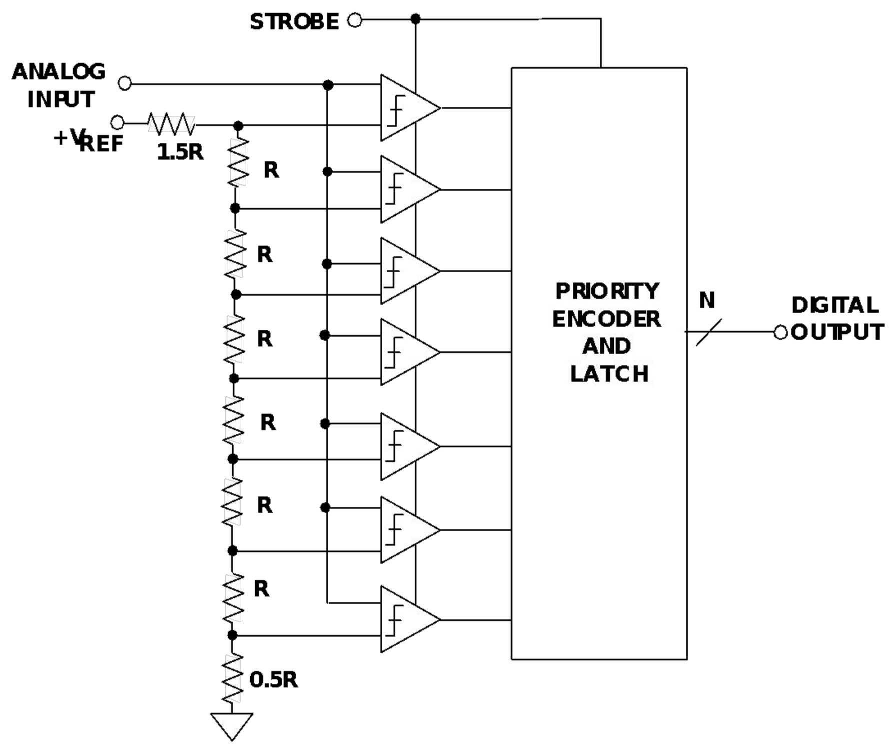
Flash or Parallel ADC

2N-1 comparators form the digitizer array, where N is the ADC resolution

Analog input is applied to one side of the comparator array, a 1 lsb reference ladder voltage is applied to the other inputs.

The comparator array is clocked simultaneously and decides in parallel.

Output logic converts from thermometer code to binary



Flash or Parallel ADC

Advantages to Flash A/D converters

- Fastest conversion times (up to 1 GSPS)
- Low data latency

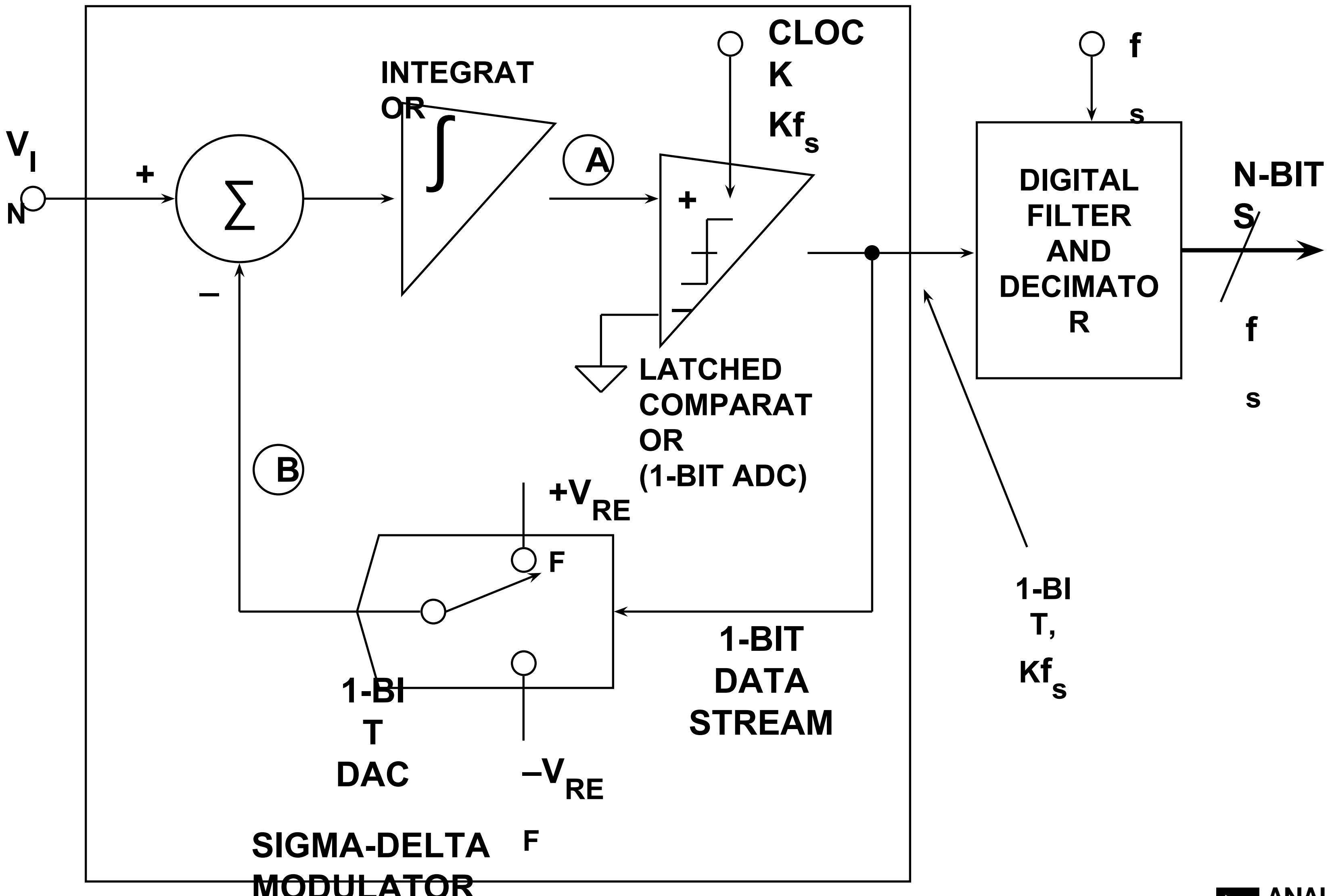
Tradeoffs to Flash A/D converters

- Higher power consumption
- High capacitive input is difficult to drive

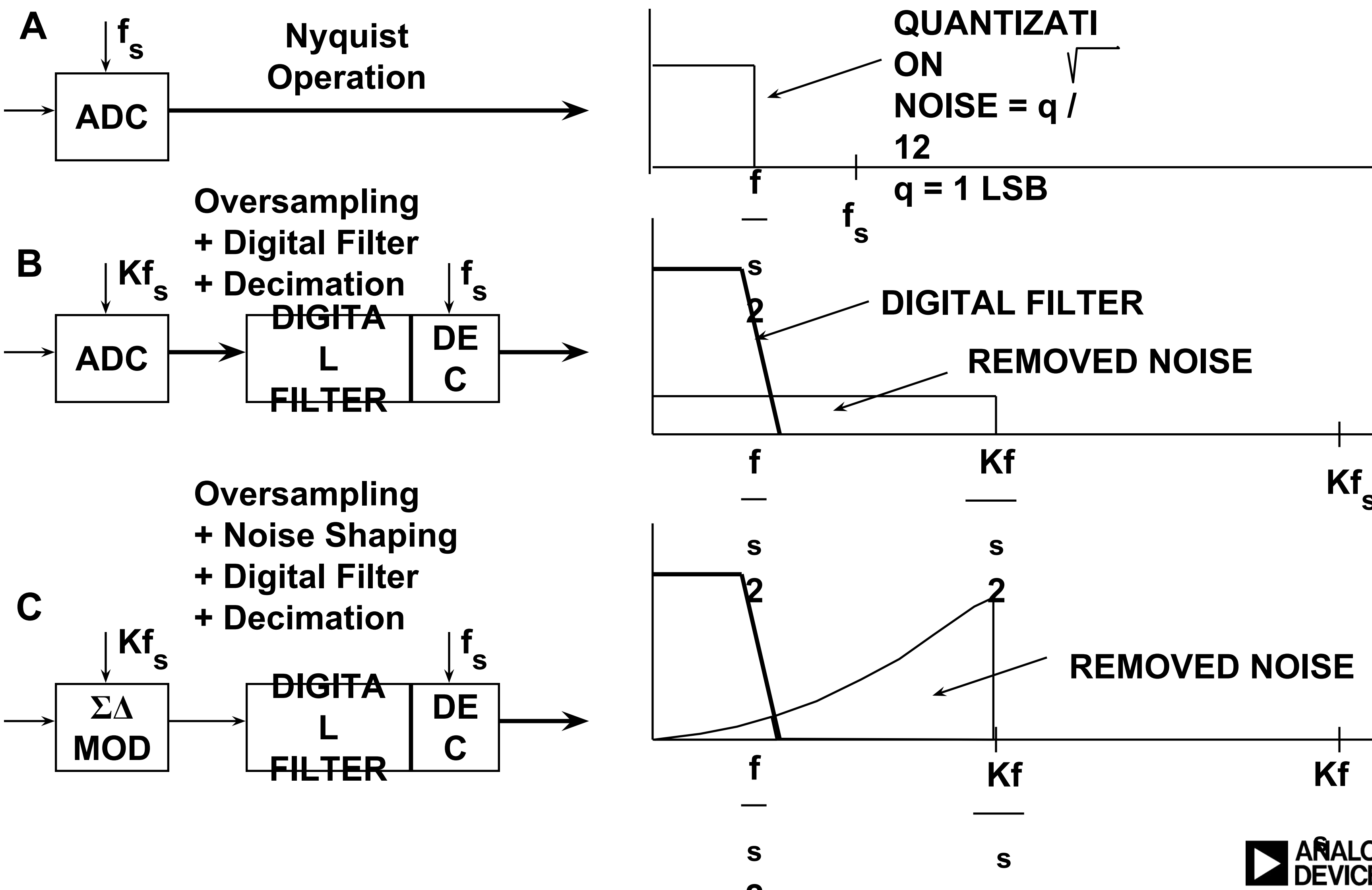
Typical Applications

- Video digitization
- High-speed data acquisition

FIRST-ORDER SIGMA-DELTA ADC



OVERSAMPLING, DIGITAL FILTERING, NOISE SHAPING, AND DECIMATION



ANALOG DEVICES

DEFINITION OF "NOISE-FREE" CODE RESOLUTION

- $$\text{EFFECTIVE RESOLUTION} = \log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{RMS NOISE}} \right] \text{BITS}$$
- $$\text{NOISE-FREE CODE RESOLUTION} = \log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{P-P NOISE}} \right] \text{BITS}$$

$$\text{P-P NOISE} = 6.6 \times \text{RMS NOISE}$$

20mV

- $$\text{NOISE-FREE CODE RESOLUTION} = \log_2 \left[\frac{\text{FULLSCALE RANGE}}{6.6 \times \text{RMS NOISE}} \right] \text{BITS}$$

16.5bits

0.4uVrms

$$= \text{EFFECTIVE RESOLUTION} - 2.72 \text{ BITS}$$

SIGMA-DELTA ADCs

Advantages to Sigma-Delta A/D converters

- High resolutions and accuracy (24-bits)
- Excellent DNL and INL performance
- Noise shaping capability

Tradeoffs in Sigma-Delta A/D converters

- Limited input bandwidth
- Slower sampling rates

Typical Applications

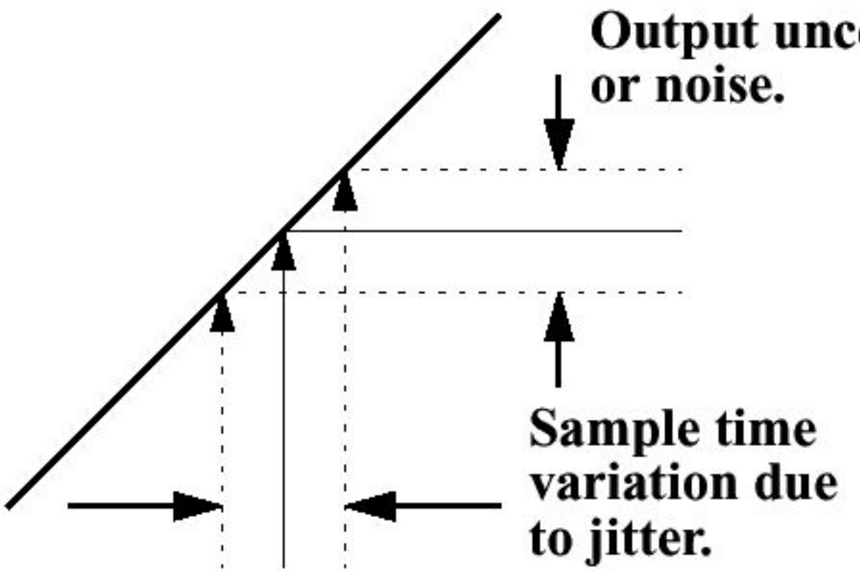
- Precision data acquisition and measurement
- Medical instrumentation

High Speed ADC Time Domain Specifications Considerations

- Aperture Jitter and Delay
- ADC Pipeline Delay
- Duty Cycle Sensitivity
- DNL Effects

EFFECTS OF APERTURE AND SAMPLING CLOCK JITTER

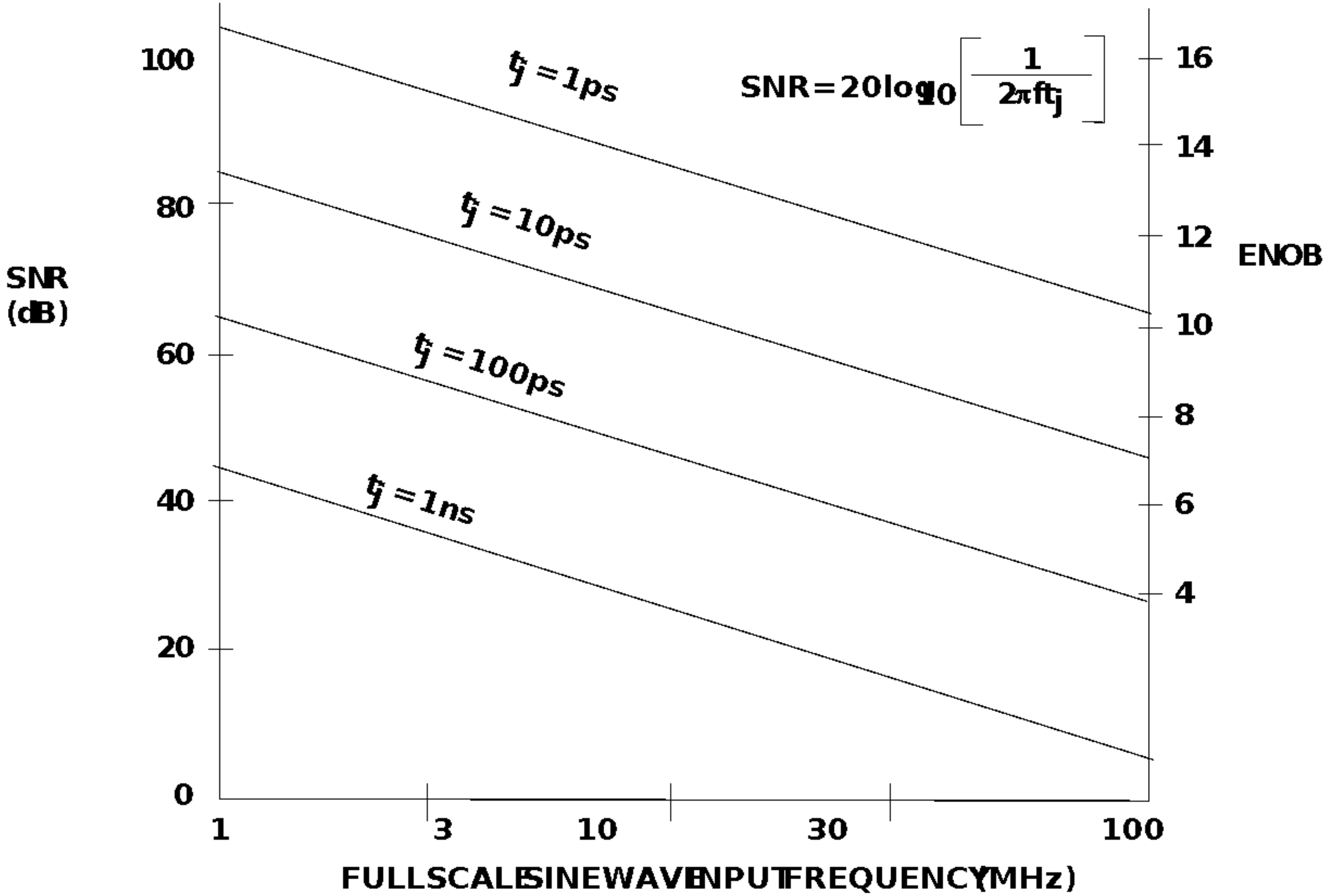
- **Jitter:**
  - **Most systems assume the signal is sampled uniformly**
  - **Clock noise leads to non-uniform sampling (*i.e.* jitter)**



  - **Jitter leads to SNR degradation for high frequency inputs:**

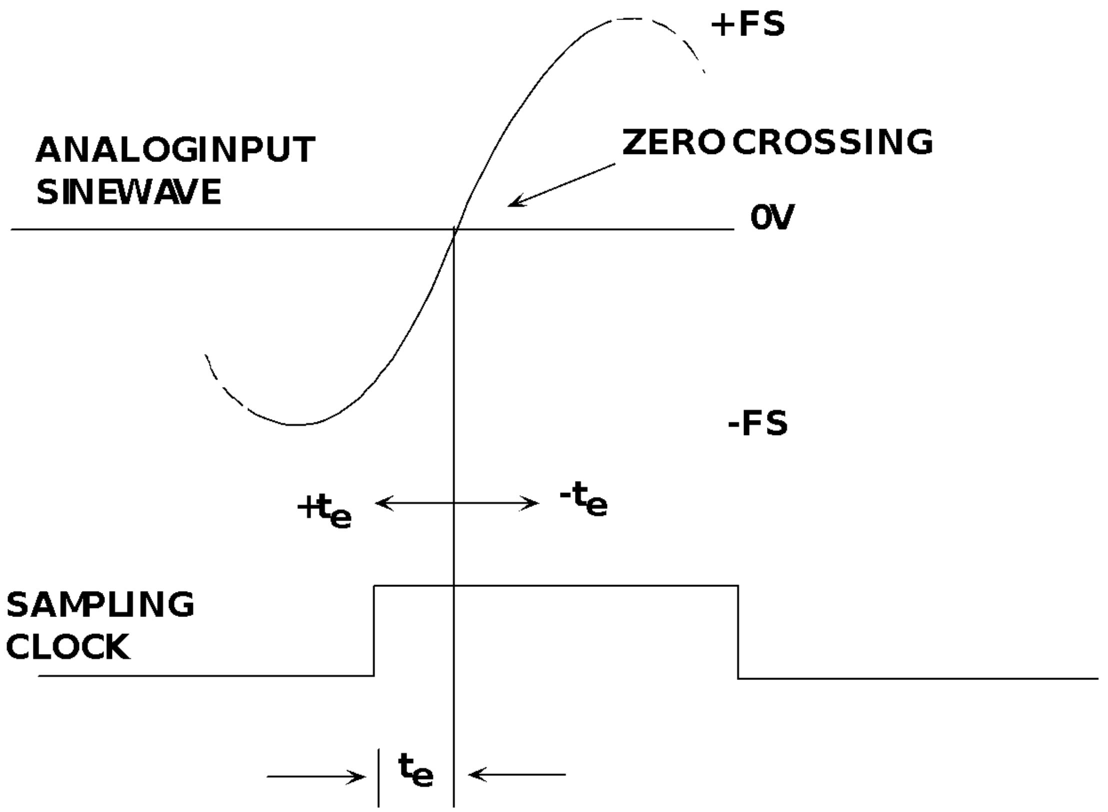
$$2\pi \; f_a T_j V_p < V_{LSB}$$

SNR DUE TO APERTURE AND SAMPLING CLOCK JITTER



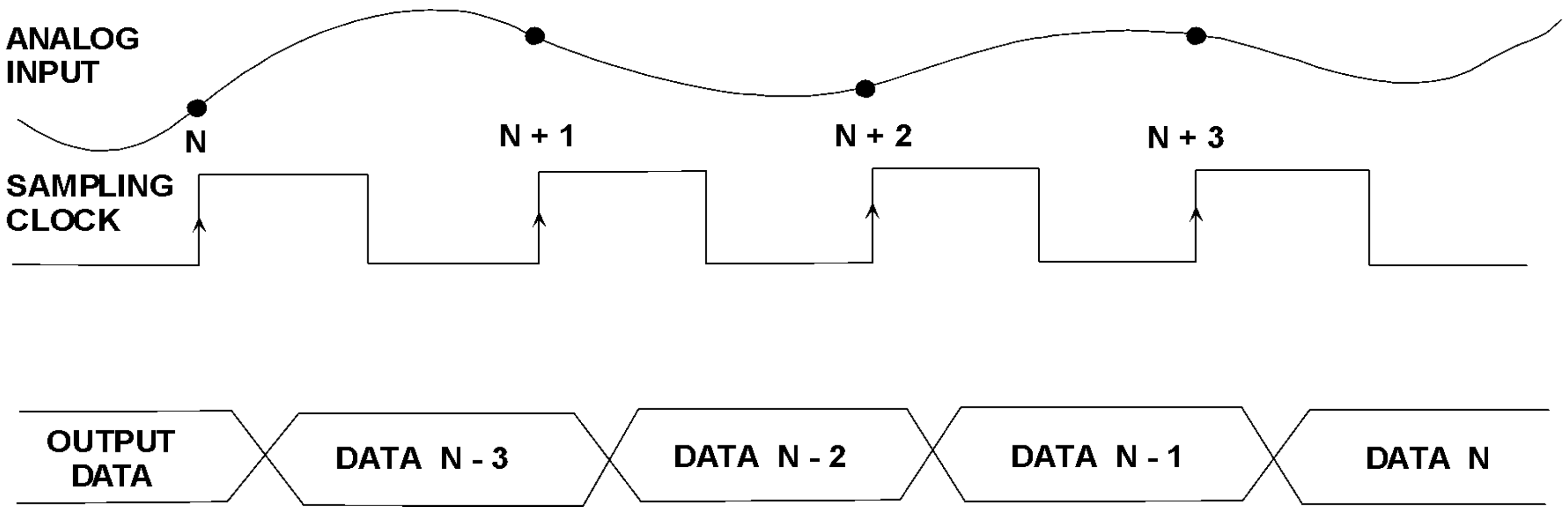
EFFECTIVE APERTURE DELAY TIME

- Typically not an issue in frequency domain applications
- May vary slightly among devices of same product due to variations in SHA bandwidth and CLK prop. delays



ADC LATENCY OR PIPELINE DELAY

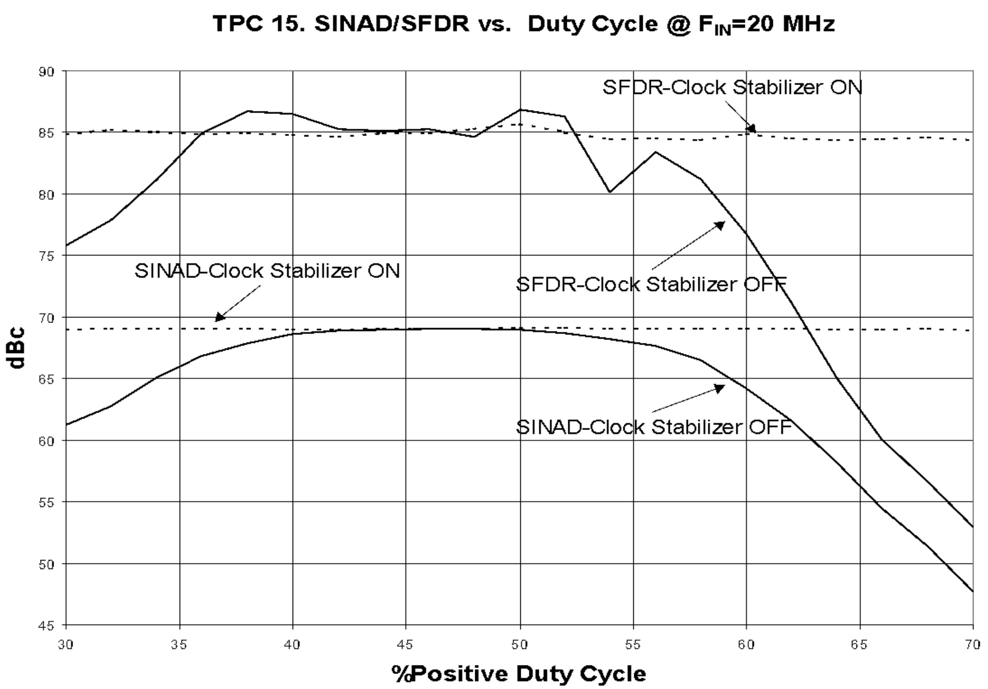
- **Many High Speed ADC's, such as subranging types, use pipeline architectures to:**
  - **Reduce chip size, and power consumption**
  - **Allows multiple samples to be converted simultaneously in ADC**
  - **Results in fixed delay between Sampled Input and corresponding digital output.**



ANALOG DEVICES

ADC DUTY CYCLE SENSITIVITY

- **High Speed ADCs are often sensitive to duty cycle of the CLK input**
  - **CLK oscillators are usually specified as 40/60 or 45/55**
  - **Digital Specifications of datasheet provide a minimum CLK HIGH/LOW period (nsec) to achieve rated performance.**
  - **Some datasheets show SNR/THD graphs as a function of duty cycle**
  - **Note, ADC also has minimum specified sample rate**



DNL ERRORS LIMIT IDEAL NOISE AND SPUR FLOOR PERFORMANCE

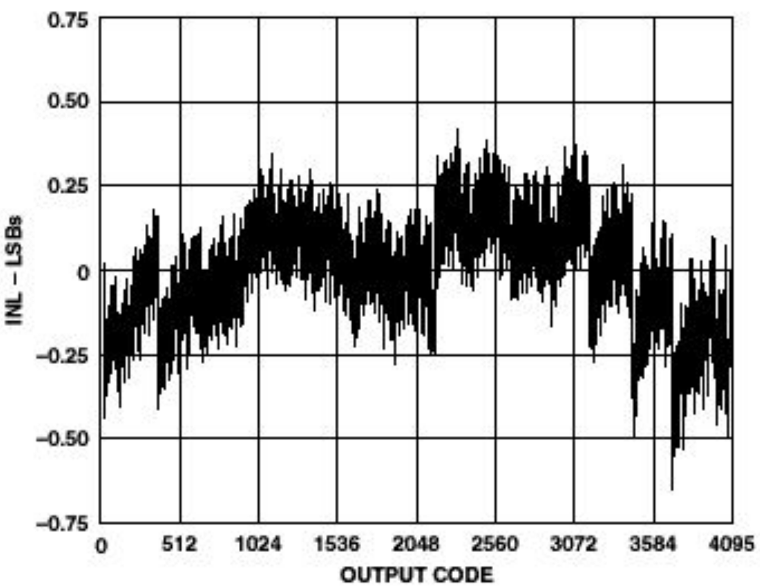
- Ideal ADC code transitions are exactly 1 LSB apart. DNL is the deviation from this value.
- Results in additive noise/spurs beyond the effects of quantization
- Limits ultimate achievable SNR and low level signal SFDR performance
  - Predictable for a given device once error transfer function is known.
  - DNL error pattern varies among devices of a given product
- Dynamic correction techniques include adding “dither” or element shuffling

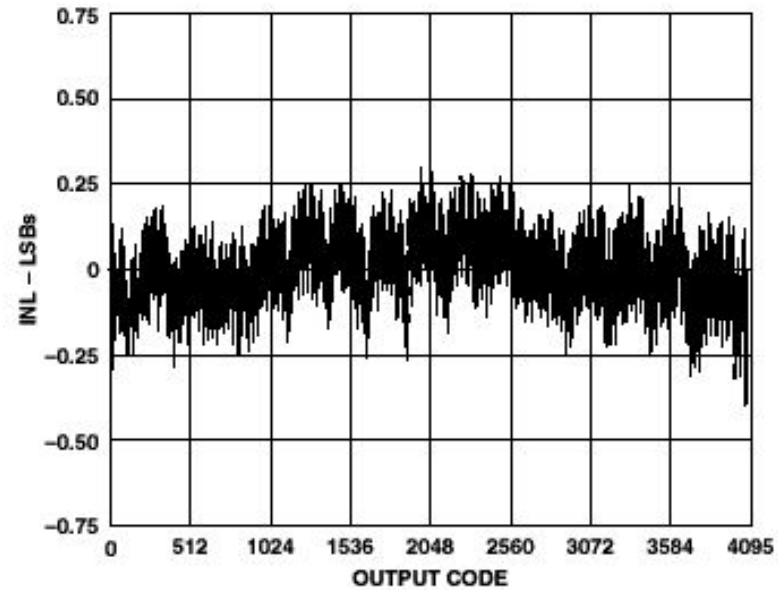
Example : AD9433 SFDR

SFDR

ENABLED

DISABLED



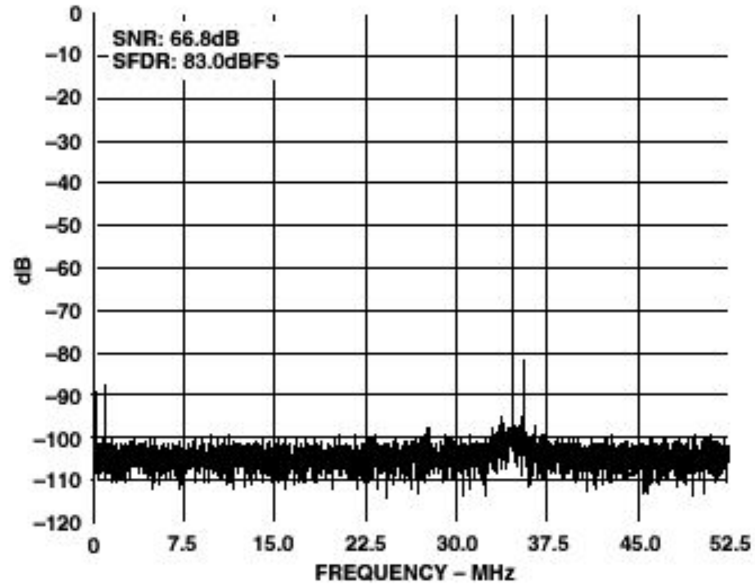


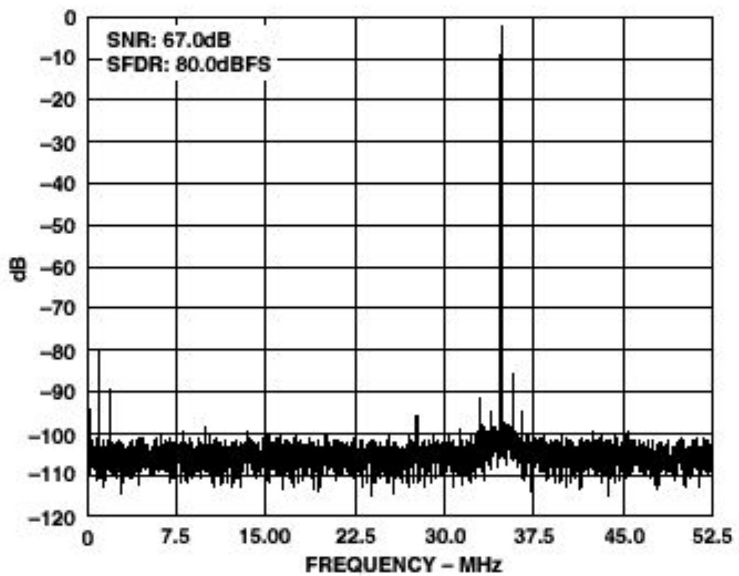
Example : AD9433 SFDR

SFDR

ENABLED

DISABLED





Encode = 105Msps
Ain = 70MHz, -0.5dBFs

ANALOG DEVICES

Example of Data Sheet Specifications for AD9430 ADC

AD9430–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = 3.3 V, DRVDD = 3.3 V; T_{MIN} = –40°C, T_{MAX} = +85°C, f_{IN} = –0.5 dBFS, Internal Reference, LVDS Output Mode, unless otherwise noted.)

Parameter	Temp	Test Level	AD9430BSV-170 Min	Typ	Max	Unit
RESOLUTION				12		Bits
ACCURACY						
No Missing Codes	Full	VI		Guaranteed		
Offset Error	25°C	I	–3		+3	mV
Gain Error	25°C	I	–5		+5	% FS
Differential Nonlinearity (DNL)	25°C	I	–1	±0.3	+1	LSB
	Full	VI	–1	±0.3	+1.5	LSB
Integral Nonlinearity (INL)	25°C	I	–1.5	±0.5	+1.5	LSB
	Full	VI	–1.5	±0.5	+2.25	LSB
TEMPERATURE DRIFT						
Offset Error	Full	V		58		µV/°C
Gain Error	Full	V		0.02		%/°C
Reference Out (VREF)	Full	V		+0.12/–0.24		mV/°C
REFERENCE						
Reference Out (VREF)	25°C	I	1.15	1.235	1.3	V
Output Current[1]	25°C	IV			3.0	mA
I_{VREF} Input Current[2]	25°C	I			20	µA
I_{SENSE} Input Current[2]	25°C	I		1.6	5.0	mA
ANALOG INPUTS (VIN+, VIN–)[3]						
Differential Input Voltage Range (S5 = GND)	Full	V		1.536		V
Differential Input Voltage Range (S5 = AVDD)	Full	V		0.766		V
Input Common-Mode Voltage	Full	VI	2.65	2.8	2.9	V
Input Resistance	Full	VI	2.2	3	3.3	kΩ
Input Capacitance	25°C	V		5		pF

ANALOG DEVICES

Example of Data Sheet Specifications for AD7476 ADC

AD7476/AD7477/AD7478

AD7476–SPECIFICATIONS[1]

(A Version: V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted; S and B Versions: V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 12 MHz, f_{SAMPLE} = 600 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1, 2]	B Version[1, 2]	S Version[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	69	70	69	dB min	
	70		70	dB min	T_A = 25°C
Signal-to-Noise Ratio (SNR)[3]	70	71	70	dB min	
Total Harmonic Distortion (THD)[3]	–80	–78	–78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	–82	–80	–80	dB typ	
Intermodulation Distortion (IMD)[3]					
Second Order Terms	–78	–78	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third Order Terms	–78	–78	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	10	10	ns typ	
Aperture Jitter	30	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY					S, B Versions, V_{DD} = (2.35 V to 3.6 V)[4]; A Version, V_{DD} = (2.7 V to 3.6 V)
Resolution	12	12	12	Bits	
Integral Nonlinearity[3]		±1.5	±1.5	LSB max	
	±1	±0.6	±0.6	LSB typ	
Differential Nonlinearity[3]		–0.9/+1.5	–0.9/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.75	±0.75	±0.75	LSB typ	
Offset Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	
Gain Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	
ANALOG INPUT					
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	±1	µA max	
Input Capacitance	30	30	30	pF typ	

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Questions

Flow of electrons is generally termed as __.

A ___is a material which offers very little resistance to theflow of current through it.

A silicon diode measures a low value of resistance with the meter leads in both positions. The trouble, if any, is

The materialswhich behave like perfect insulators at low temperatures & athigher temperatures, they behave like

Under normal conditions a diode conducts current when it is

The movement of free electrons in a conductor is called

An n-type semiconductor material

The boundary between p-type material and n-type material is called

You have an unknown type of diode in a circuit. You measure the voltage across it and find it to be 0.3 V. The diod

What type of impurities are to be added to form a P type semiconductors ?

Doping of a semiconductor material means

What occurs when a conduction-band electron loses energy and falls back into a hole in the valence band?

The term bias in electronics usually means

How many valence electrons does a silicon atom have?

Which capacitance dominates in the forward-bias region?

What is the Cut in volatage of Silicon diode?

Germanium Knee Volage is

Intrinsic Semiconductor means

Under normal conditions a diode conducts current when it is

Reverse breakdown is a condition in which a diode

There is a small amount of current across the barrier of a reverse-biased diode. This current is called

Since diodes are destroyed by excessive current, circuits must have:

Why is heat produced in a diode?

The diode schematic arrow points to the:

The voltage where current may start to flow in areverse-biased pn junction is called the

The area at the junction of p-type and n-type materials that has lost its majority carriersis called the

DC power should be connected to forward bias a diode as follows:

A diode for which you can change the reverse bias, and thus vary the capacitance is called a

Avalanche breakdown results basically due to

The varactor diode is usually

The diode in which impurities are heavily doped is

The depletion region in a Junction Diode contains

Varactor diodes are used in FM receivers to obtain:

As the forward current through a silicon diode increases, the internal resistance

Reverse breakdown is a condition in which a diode

There is a small amount of current across the barrier of a reverse-biased diode. This current is called

What is the state of an ideal diode in the region of nonconduction?

Schottky diodes are also known as

zener breakdown refers to

What kind of diode is formed by joining a doped semiconductor region with a metal?

An intrinsic semiconductor at the absolute zero temperature

A pn junction allows current flow when

The forward characteristics curve of a diode grows in _____ form.

The reverse-saturation current level is typically measured in

Varying the _____ can control the location of the Zener region.

The _____ the current through a diode, the _____ the dc resistance level.
The reverse-bias current _____ with the increase of temperature.
What is the resistor value of an ideal diode in the region of conduction?
Diodes are connected _____ to increase the current-carrying capacity
A Zener diode:
Avalanche breakdown in semiconductor diode occurs when
The varactor diode is usually
Zener diodes are:
The capacitance of a varactor diode increases when the reverse voltage across it
The diode with a forward voltage drop of approximately 0.25 V is the
Since diodes are destroyed by excessive current, circuits must have:
Drift current is influenced by
What type of diode is commonly used in electronic tuners in TVs?
Which diode employs graded doping?
A PNPN diode is a

opt1
Electric current
good conductor
the diode is open.
good conductor
reverse-biased.
voltage.
is intrinsic.
a diode.
a silicon diode.
Trivalent
that a glue-type substance is added to hold the material together.
doping
the value of ac voltage in the signal.
1
Diffusion
0.5V
0.3V
Pure Semicionductor
reverse-biased
is subjected to a large reverse voltage
forward-bias current
higher voltage sources
due to current passing through the diode
trivalent-doped material
breakdown voltage
barrier potential
– anode, + cathode
varactor diode
impact ionisation
Forward biased
Varactor diode
only charge carriers
Automatic frequency control
increases.
is subjected to a large reverse voltage.

forward-bias current.
An open circuit
PIN diodes.
Reverse bias region
laser
behaves like a metallic conductor
the p-type material is more positive than the n-type material
linear
pA
forward current

higher, lower
decreases
0
in series
Has a high forward voltage rating
Reverse bias exceeds a certain value
Forward biased
Specially doped p–n junctions
Decreases
Step-recovery diode
current limiting resistors
magnitude of voltage
varactor
zener
negative resistence device

opt2

electric shock
insulator
the diode is shorted to ground.
insulator
forward-biased.
current.
has trivalent impurity atoms added.
a reverse-biased diode.
a germanium diode.
Pentavalent
that impurities are added to increase the resistance of the material.
recombination
the condition of current through a pn junction.

Transition
0.6V
0.4V
Impure Semiconductor
forward-biased
is reverse-biased and there is a small leakage current
reverse breakdown current
current limiting resistors
due to voltage across the diode
positive axial lead
barrier potential
depletion region
– cathode, – anode
tunnel diode
strong electric field across the junction
reverse biased
PIN diode
no charge at all
Automatic gain control
decreases.
is reverse-biased and there is a small leakage current.
reverse breakdown
current.
A short circuit
hot carrier diodes.
Forward bias region
tunnel
behaves like an insulator
the n-type material is more positive than the p-type material
exponential
µA
doping levels

lower, lower
increases
5 k
in parallel-series
Is useful as an amplifier
Forward bias exceeds a certain value
Reverse biased
Normally doped p–n junctions
Increases
Schottky diode
more dopants
concentration of carriers
Schottky
LED
voltage controllable device

opt3
semiconductor
semiconductor
the diode is internally shorted.
semiconductor
avalanched.
recombination.
has pentavalent impurity atoms added.
a pn junction.
a forward-biased silicon diode.
Octavalent
that impurities are added to decrease the resistance of the material.
generation
the value of dc voltages for the device to operate properly.
3

Depletion
0.7V
0.5V
Non doped Conductor
avalanched
has no current flowing at all
conventional current
more dopants
due to the power rating of the diode
anode lead
forward voltage
n region
+ anode, – cathode
zener diode
emission of electrons
Unbiased
Tunnel diode
vacuum, and no atoms at all
Automatic volume control
remains the same.
has no current flowing at all.
conventional
current.
Unpredictable
step-recovery diodes.
no bias
pin
has a large number of holes
both the n-type and p-type materials have the same potential
logarithmic
mA
forward voltage

lower, higher
remains the same
Undefined
in parallel-series
Has a sharp breakdown at low reverse voltage
Forward current exceeds a certain value
un biased
Lightly doped p–n junctions
Breaks down
Back diode
higher voltage sources
concentration gradient of carriers
LED
tunnel
current controllable negative resistence device

opt4
none of the above
none of the above
the diode is working correctly.
none of the above
saturated.
equilibrium.
requires no doping.
a forward-biased diode.
a reverse-biased germanium diode.
Divalent
that all impurities are removed to get pure silicon.
combination
the status of the diode.
4

None of the above
0.3V
None of these
Both A & C
saturated
is heated up by large amounts of current in the forward direction
reverse leakage current
higher current sources
due to the PN junction of the diode
cathode lead
biasing voltage
p region
+ cathode, + anode
switching diode
rise in temperature
holes and electronics
Zener diode
only ions i.e., immobile charges
None of the above
increases & decreases
is heated up by large amounts of current in the forwarddirection.
reverse leakage
current.
Undefined
tunnel diodes.
depletion region
Schottky
has a large number of electrons
there is no potential on the n-type or p-type materials
sinusoidal
A
dc resistance

higher, higher
None of the above
Infinity
in parallel
None of the above
the potential barrier is reduced to zero
in the breakdown region
None of the above
Stores charges
Constant-current diode
higher current sources
forward-bias current.
Gunn
step-recovery
switching device

opt5

opt6

Answer
Electric current
good conductor
the diode is internally shorted.
semiconductor
forward-biased.
current.
has pentavalent impurity atoms added.
a pn junction.
a germanium diode.
Trivalent
that impurities are added to decrease the resistance of the material.
recombination
the value of dc voltages for the device to operate properly.
4
Diffusion
0.7V
0.3V
Both A & C
forward-biased
is subjected to a large reverse voltage
reverse leakage current
current limiting resistors
due to current passing through the diode
cathode lead
breakdown voltage
depletion region
+ anode, – cathode
varactor diode
impact ionisation
reverse biased
Tunnel diode
only ions i.e., immobile charges
Automatic frequency control
decreases.
is subjected to a large reverse voltage.

reverse leakage current.
An open circuit
hot carrier diodes.
Reverse bias region
Schottky
behaves like an insulator
the p-type material is more positive than the n-type material
exponential
µA
doping levels

lower, higher
increases
0
in parallel
Has a sharp breakdown at low reverse voltage
Reverse bias exceeds a certain value
Reverse biased
Specially doped p–n junctions
Decreases
Schottky diode
current limiting resistors
magnitude of voltage
varactor
step-recovery
switching device

Questions

When transistors are used in digital circuits they usually operate in the
A transistor has a of 250 and a base current, IB, of 20 A. The collector current, IC, equals:
A current ratio of IC/IE is usually less than one and is called:
In a C-E configuration, an emitter resistor is used for:
To operate properly,a transistor's base-emitter junction must be forward biased with reverse bias applied to which
the C-B configuration is used to
 provide which type of gain?
A transistor may be used as a switching device or as a:
If an input signal ranges from 20–40 A (microamps), with an output signal ranging from .5–1.5 mA (milliamps), wh
Which is beta's current ratio?
A collector characteristic curve is a graph showing:
With low-power transistor packages, the base terminal is usually the:
When a silicon diode is forward biased, what is V BE for a C-E configuration?
What is the current gain for a common-base configuration where IE = 4.2 mA and IC = 4.0 mA?
With a PNP circuit, the most positive voltage is probably:
If a 2 mV signal produces a 2 V output, what is the voltage gain?
The term BJT is short for
Most of the electrons in the base of an NPN transistor flow:
In a transistor, collector current is controlled by:
Total emitter current is:
Often a common-collector will be the last stage before the load; the main function(s) of this stage is to:
For a C-C configuration to operate properly, the collector-base junction should be reverse biased, while forward bi
The input/output relationship of the common-collector and common-base amplifiers is:
At saturation the value of VCE is nearly ________, and IC = ________.
In which operation region(s) does the Ebers-Moll model describe a bipolar transistor?
Transistor act as a?
The part of the transistor which is heavily doped to produce large number of majority carriers is
A BJT is a ________-controlled device.
In a transistor
The principal advantage(s) of BJTs over MOSFETs is (are) that
What is the ratio of IC to IB?
For normal operation of a pnp BJT, the base must be ________ with respect to the emitter and ________ with res
The term BJT is short for
For a silicon transistor, when a base-emitter junction is forward-biased, it has a nominal voltage drop of
What are the two types of bipolar junction transistors?
What is the order of doping, from heavily to lightly doped, for each region?
in what range of voltages is the transistor in the linear region of its operation?
What is (are) common fault(s) in a BJT-based circuit?
The dc load line on a family of collector characteristic curves of a transistor shows the
How many layers of material does a transistor have?
In which region are both the collector-base and base-emitter junctions forward-biased?
Which of the following is (are) the terminal(s) of a transistor?
Transistors are ________-terminal devices.
How many carriers participate in the injection process of a unipolar device?
In what decade was the first transistor created?
Which component of the collector current IC is called the leakage current?

Clipping is the result of
In a NPN transistors Collector is
In a NPN transistors emitter is
In a NPN transistors base is
When a transistor is used as a switch, it is stable in which two distinct regions?
At which of the following condition(s) is the depletion region uniform?
Clipping is the result of
alpha refers to
Beta refers to
gamma refers to
In a transistor, collector current is controlled by:
How much is the base-to-emitter voltage of a transistor in the "on" state?
Which of the following equipment can check the condition of a transistor?
For what kind of amplifications can the active region of the common-emitter configuration be used?
A transistor can be checked using a(n) ________.

opt1
active region
500 A
beta
stabilization
collector-emitter

voltage
fixed resistor
0.05
IC/IB
emitter current (IE) versus collector-emitter voltage (VCE) with (VBB) base bias voltage held constant
tab end
voltage-divider bias
16.8
ground
0.001
base junction transistor
out of the base lead
collector voltage
IE – IC
provide voltage gain
collector-emitter
270 degrees
zero, zero
Forward active.
conductor
emitter
current
$\beta = \alpha / (\alpha + 1)$
voltage drop across the transistor is important.
DC
positive, negative
base junction transistor
0.7 V.
npn and pnp
base, collector, emitter
0 < VCE
opens or shorts internal to the transistor
saturation region.
1
Active
Emitter
2
1
1930s
Majority

the input signal being too large
Heavily doped
Heavily doped
Heavily doped
saturation and active
No bias
the input signal being too large.
Ic/Ib
Ic/Ib
1+alfha
collector voltage
0 V
Current tracer
Voltage
curve tracer

opt2
breakdown region
5 mA
theta
ac signal bypass
base-collector

current
tuning device
20
VCC
collector current (IC) versus collector-emitter volt
middle
0.4 V
1.05
VC
0.004
binary junction transistor
into the collector
base current
IC + IE
provide phase inversion
base-emitter
180 degrees
VCC, IC(sat)
Saturation.
semi-conductor
base
voltage
$\beta = \alpha / (1 - \alpha)$
they are not as prone to ESD.
hFE
positive, positive
binary junction transistor
0.3 V.
pnn and nnp
emitter, collector, base
0.7 < VCE < VCE(max)
open bias resistor(s)
cutoff region.
2
Cutoff
Base
3
2
1940s
Independent

the transistor being driven into saturation.
moderately doped
moderately doped
moderately doped
active and cutoff
VDS > 0 V
the transistor being driven into saturation
Ic/Ie
Ic/Ie
1-alpha
base current
0.7 V
Digital display meter (DDM)
Current
digital meter

opt3
saturation and cutoff regions
50 mA
alpha
collector bias
base-emitter

resistance
rectifier
50
IB/IE
collector current (I C) versus collector-emitter voltage (VC) with (VBB) base b
right end
0.7 V
0.2
VBE
100
both junction transistor
into the emitter
collector resistance
IB + IC
provide a high-frequency path to improve the frequency response
collector-base
90 degrees
zero, I(sat)
Cut-off.
insulator
collector
-
$\alpha = \beta/(\beta-1)$
both of the above
DC
negative, positive
both junction transistor
0.2 V.
ppn and nnp
emitter, base, collector
VCE(max) > VCE
external opens and shorts on the circuit board
active region.
3
Saturation
Collector
4
3
1950s
Minority

the transistor being driven into cutoff.
lightly doped
lightly doped
lightly doped
saturation and cutoff
VDS = VP
the transistor being driven into cutoff.
Ie/Ic
Ie/Ic
1/alpha
collector resistance
0.7 mV
Ohmmeter (VOM)
Power
ohmmeter

opt4
linear region
0.208333333
omega
higher gain
collector-base

power
variable resistor
500
IE/IB
collector current (I C) versus collector-emitter voltage (VCC) with (VBB) base bias voltage held constant
stud mount
emitter voltage
0.95
VCC
1000
bipolar junction transistor
into the base supply
all of the above
IB – IC
buffer the voltage amplifiers from the low-resistance load and provide impedance matching for maximum power t
cathode-anode
0 degrees
VCC, zero
All of the above.
thermionic valve
any of the above depending upon the nature of transistor
-
α = (β+1)/β
none of the above
either DC or hFE, but not DC
negative, negative
bipolar junction transistor
VCC.
pts and stp
collector, emitter, base
none of the above
all of the above
all of the above
4
All of the above
All of the above
5
0
1960s
None of the above

all of the above
none of the these
none of the these
none of the these
none of the above
None of the above
all of the above
Ib/Ic
Ib/Ic
1/(1-alpha)
all of the above
Undefined
All of the above
All of the above
Any of the above

opt5

:ransfer

opt6

Answer
saturation and cutoff regions
5 mA
alpha
stabilization
collector-base

voltage
variable resistor
50
IC/IB
collector current (IC) versus collector-emitter voltage (V CE) with (VBB) base bias voltage held constant
middle
0.7 V
0.95
ground
1000
bipolar junction transistor
into the collector
base current
IB + IC
buffer the voltage amplifiers from the low-resistance load and provide impedance matching for maximum power t
collector-emitter
0 degrees
zero, I(sat)
All of the above.
thermionic valve
emitter
current
α = β/ (β-1)
both of the above
either DC or hFE, but not DC
negative, positive
bipolar junction transistor
0.7 V.
npn and pnp
emitter, collector, base
0.7 < VCE < VCE(max)
all of the above
all of the above
3
Saturation
All of the above
3
1
1940s
Minority

all of the above
moderately doped
Heavily doped
lightly doped
saturation and cutoff
No bias
all of the above
Ic/Ie
Ic/Ib
1+alfha
base current
0.7 V
All of the above
All of the above
Any of the above

Questions

When an input delta of 2 V produces a transconductance of 1.5 mS, what is the drain current delta?
When not in use, MOSFET pins are kept at the same potential through the use of:
D-MOSFETs are sometimes used in series to construct a cascode high-frequency amplifier to overcome the loss of:
A MOSFET has how many terminals?
IDSS can be defined as:
With the E-MOSFET, when gate input voltage is zero, drain current is:
With a 30-volt VDD, and an 8-kilohm drain resistor, what is the E-MOSFET Q point voltage, with ID = 3 mA?
When an input signal reduces the
channel size, the process is called:
When applied input voltage varies the resistance of a channel, the result is called:
When is a vertical channel E-MOSFET used?
How will a D-MOSFET input impedance change with signal frequency?
What is the transconductance of an FET when ID = 1 mA and VGS = 1 V?
Which component is considered to be an "OFF" device?
For what value of ID is gm equal to 0.5 gm0?
Where do you get the level of gm and rd for an FET transistor?
The class D amplifier uses what type of transistors?
What is (are) the function(s) of the coupling capacitors C1 and C2 in an FET circuit?
What is the typical value for the input impedance Zi for JFETs?
MOSFETs make better power switches than BJTs because they have
MOSFET digital switching is used to produce which digital gates?
Which FET amplifier(s) has (have) a phase inversion between input and output signals?
MOSFET can be used as a
What limits the signal amplitude in an analog MOSFET switch?
Input resistance of a common- drain amplifier is
E-MOSFETs are generally used in switching applications because
For an FET small-signal amplifier, one could go about troubleshooting a circuit by ________.
The E-MOSFET is quite popular in ________ applications.
Material used for design of MESFET is
Secondary breakdown occurs in
CMOS is widely used in
In the transfer characteristics of a MOSFET, the threshold voltage is the measure of the
Input impedance of MOSFET is
MOSFET uses the electric field of
In MOSFET devices the N-channel type is better the P-channel type in the following respects
In a MOSFET, the polarity of the inversion layer is the same as that of the
Which of the following is expected to have highest input impedance?
Most small - signal E - MOSFETs are found in
Which insulating layer used in Fabrication of MOSFET?
What is used to higher the speed of operation in MOSFET fabrication?
A power MOSFET has three terminals called
MESFET can be operated on
The arrow on the symbol of MOSFET indicates
The operation of CCD is
What limits the signal amplitude in an analog MOSFET switch?
Input resistance of a common- drain amplifier is

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IDSS can be defined as:
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A MOSFET has how many terminals?
IDSS can be defined as:
What is (are) the function(s) of the coupling capacitors C1 and C2 in an FET circuit?

opt1
666 mA
shipping foil
low output impedance
2 or 3
the minimum possible drain current
at saturation
6 V

enhancement
saturization
for high frequencies
As frequency increases input impedance increases.
1 kS
transistor
0 mA
from the dc biasing arrangement
JFETs
to create an open circuit for dc analysis
100 k
lower turn-off times.
inverters
common-gate
Current controlled capacitor
the switch input capacitance
RG || RIN(gate).
of their very low input capacitance.
viewing the circuit board for poor solder joints
digital circuitry
Gallium arsenide (GaAs)
MOSFET but not in BJT
Digital wrist watches
minimum voltage to induce a n-channel/p-channel for conduction
less than of FET but more than BJT.
gate capacitance to control the channel current.
it has better noise immunity.
charge on the gate electrode
MOSFET.
heavy - current applications.
Aluminium oxide
Ceramic gate
Collector, emitter and gate.
Enhancement mode (normally OFF) only
that it is a N-channel MOSFET
captures light and converts it to digital data
the switch input capacitance
RG || RIN(gate).

of their very low input capacitance.
the minimum possible drain current
at saturation
6 V

enhancement
saturization
heavy - current applications.
Aluminium oxide
Ceramic gate
666 mA
shipping foil
low output impedance
2 or 3
the minimum possible drain current
to create an open circuit for dc analysis

opt2
3 mA
nonconductive foam
capacitive reactance
3

the maximum possible current with VGS held at –4 V
zero
10 V
substrate
connecting
polarization
for high voltages
As frequency increases input impedance is constant.
1 mS
JFET
0.25 IDSS
from the specification sheet
BJTs
to isolate the dc biasing arrangement from the applied signal and load
1 M
lower on-state resistance.
NOR gates
common-drain
Voltage controlled capacitor
VGS(th)
RG + RIN(gate).
of their threshold characteristic (VGS(th)).
using a dc meter
high-frequency
Germanium
Both MOSFET and BJT
analogue circuits
minimum voltage till which temperature is constant
more than that of FET and BJT.
barrier potential of p-n junction to control the channel current.
it is faster.
minority carriers in the drain
JEFT amplifier.
discrete circuits.
Silicon Nitride
Silicon dioxide
Drain, source and gate.
Depletion mode only (normally ON) only
the direction of electrons
converts digital data
VGS(th)
RG + RIN(gate).

of their threshold characteristic (VGS(th)).
the maximum possible current with VGS held at –4 V
zero
10 V
substrate
connecting
polarization
discrete circuits.
Silicon Nitride
Silicon dioxide
3 mA
nonconductive foam
capacitive reactance
3

the maximum possible current with VGS held at –4 V
to isolate the dc biasing arrangement from the applied signal and load

opt3
0.75 mA
conductive foam
high input impedance
4
the maximum possible current with VGS held at 0 V
IDSS
24 V

gate charge
cutoff
for high currents
As frequency decreases input impedance increases.
1 k
D-MOSFET
0.5 IDSS
from the characteristics
MOSFETs
to create a short-circuit equivalent for ac analysis
10 M
a positive temperature coefficient.
NAND gates
common-source
Current controlled inductor
the switch's power handling
RG
of their high-frequency response capabilities.
applying a test ac signal
buffering
Silicon
BJT but not in MOSFET
high power circuits
minimum voltage to turn off the device
more than that of FET but less than BJT.
both (A) and (B).
it is TTL compatible.
majority carries in the substrate.
CE bipolar transistor.
disk drives.
Silicon dioxide
Silicon nitride
Drain, source and base.
Both Enhancement mode and Depletion mode
the direction of conventional current flow
project the data on screen
the switch's power handling
RG

of their high-frequency response capabilities.
the maximum possible current with VGS held at 0 V
IDSS
24 V

gate charge
cutoff
disk drives.
Silicon dioxide
Silicon nitride
0.75 mA
conductive foam
high input impedance
4

the maximum possible current with VGS held at 0 V
to create a short-circuit equivalent for ac analysis

opt4
0.5 mA
a wrist strap
inductive reactance
3 or 4
the maximum drain current with the source shorted
widening the channel
30 V

depletion
field effect
for high resistances
As frequency decreases input impedance is constant.
1 m Ω
E-MOSFET
IDSS
All of the above
any of the above
All of the above
1000 MΩ
all of the above
all of the above
all of the above
Voltage controlled inductor
VDS
RIN(gate).
of their power handling.
All of the above
All of the above
Zinc arsenide
None of these
all of the above
none of the above mentioned is true
less than that of FET and BJT.
none of these.
it has better drive capability.
majority carries in the source .
Common collector bipolar transistor
integrated circuit.
None of the mentioned
Poly silicon gate
Collector, emitter and base.
None of the above
that it is a P-channel MOSFET
Captures light
VDS
RIN(gate).

of their power handling.
the maximum drain current with the source shorted
widening the channel
30 V

depletion
field effect
integrated circuit.
None of the mentioned
Poly silicon gate
0.5 mA
a wrist strap
inductive reactance
3 or 4
the maximum drain current with the source shorted
All of the above

opt5

opt6

Answer
3 mA
conductive foam
high input impedance
3 or 4
the maximum possible current with VGS held at 0 V
zero
6 V

depletion
field effect
for high currents
As frequency decreases input impedance increases.
1 mS
E-MOSFET
0.25 IDSS
All of the above
MOSFETs
All of the above
1000 MΩ
all of the above
all of the above
common-source
Voltage controlled capacitor
VGS(th)
RG || RIN(gate).
of their threshold characteristic (VGS(th)).
All of the above
All of the above
Gallium arsenide (GaAs)
BJT but not in MOSFET
Digital wrist watches
minimum voltage to induce a n-channel/p-channel for conduction
more than that of FET and BJT.
gate capacitance to control the channel current.
it is faster.
majority carries in the source .
MOSFET.
integrated circuit.
Silicon dioxide
Poly silicon gate
Drain, source and gate.
Both Enhancement mode and Depletion mode
the direction of electrons
captures light and converts it to digital data
VGS(th)
RG || RIN(gate).

of their threshold characteristic (VGS(th)).
the maximum possible current with VGS held at 0 V
zero
6 V

depletion
field effect
integrated circuit.
Silicon dioxide
Poly silicon gate
3 mA
conductive foam
high input impedance
3 or 4
the maximum possible current with VGS held at 0 V
All of the above

Questions
A differential amplifier
When a differential amplifier is operated single-ended,
In differential-mode
In the common-mode
The common-mode gain is
The differential gain is
If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is
With zero volts on both inputs, an OPamp ideally should have an output
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
A certain OP-amp has bias currents of 50 µA and 49.3 µA. The input offset current is
The output of a particular OP-amp increases 8 V in 12 µs. The slew rate is
A common-mode signal is applied to
The common-mode voltage gain is
The input stage of an OP-amp is usually a
Current cannot flow to ground through
Which of the following electrical characteristics is not exhibited by an ideal op-amp?
An ideal op-amp requires infinite bandwidth because
Ideal op-amp has infinite voltage gain because
Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages
How will be the output voltage obtained for an ideal op-amp?
Which is not the ideal characteristic of an op-amp?
Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
Which factor determine the output voltage of an op-amp?
The opamp can amplify
In a nonlinear op-amp circuit, the
The input signal for an instrumentation amplifier usually comes from
In a differential amplifier, the CMRR is limited mostly by the
A common - mode signal is applied to
The common-mode voltage gain is
The input stage of an op amp is usually a
The common - mode rejection ratio is
A 741 C has
The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
The voltage gain of a loaded differential amp is
At the unity-gain frequency, the open-loop voltage gain is
The tail current in a differential amplifier equals
A common - mode signal is applied to
An instrumentation amplifier has a high
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The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
Current cannot flow to ground through

opt1
is a part of an OP-amp
the output is grounded
opposite polarity signals are applied to the inputs
both inputs are grounded
very high
very high
1225
equal to the positive supply voltage
1
700 nA
90 V/ µs
the non-inverting in
smaller than differential voltage gain
differential amplifier
a mechanical ground
Infinite voltage gain
Signals can be amplified without attenuation
To control the output voltage
$V_O = V_1 - V_2$
Amplifies the difference between the two input voltages
Input Resistance –> 0
8v
Both positive and negative saturation voltage
AC signals only
opamp never saturates
an inverting amplifier.
CMRR of the opamp
the non - inverting input.
smaller than the voltage gain.
differential amp.
very low.
a voltage gain of 100,000.
single - ended input and single-ended output
less than the input bias current.
input offset current.
large than the unloaded voltage gain.
1
difference between two emitter currents
the non - inverting input.
output impedance
1
Signals can be amplified without attenuation
equal to the positive supply voltage
1
700 nA

90 V/ µs
the non-inverting in
smaller than differential voltage gain
differential amplifier
a mechanical ground
Infinite voltage gain
Signals can be amplified without attenuation
very high
very high
1225
equal to the positive supply voltage
single - ended input and single-ended output
less than the input bias current.
input offset current.
a mechanical ground

opt2
has one input and one output
one input is grounded and signal is applied to the other
the gain is one
the outputs are connected together
very low
very low
10,000
equal to the negative supply voltage
2000
99.3 µA
0.67 V/ µs
the inverting input
equal to differential voltage gain
class B push-pull amplifier
an a.c. ground
Infinite bandwidth
Output common-mode noise voltage is zero
To obtain finite output voltage
V_O= A×(V_1-V_2)
Amplifies individual voltages input voltages
Output impedance –> 0
4v
Positive saturation
DC signals only.
feedback loop is never opened
resistor
gain - bandwidth product.
the inverting input.
equal to the voltage gain.
class B push-pull amplifier.
as high as possible.
an input impedance of 2 MΩ.
single - ended input and differential output.
equal to zero.
input bias current.
equal to R_C / r_e.
$A_{V(mid)}$.
sum of two emitter currents
the inverting input.
power gain.
2000
Output common-mode noise voltage is zero
equal to the negative supply voltage
2000
99.3 µA

0.67 V/ µs
the inverting input
equal to differential voltage gain
class B push-pull amplifier
an a.c. ground
Infinite bandwidth
Output common-mode noise voltage is zero
very low
very low
10,000
equal to the negative supply voltage
single - ended input and differential output.
equal to zero.
input bias current.
an a.c. ground

opt3
has two outputs
both inputs are connected together
the outputs are of different amplitudes
an identical signal appears on both inputs
always unity
dependent on input voltage
80 dB
equal to zero
80 dB
49.7 µA
1.5 V/ µs
both inputs
greater than differential voltage gain
CE amplifier
a virtual ground
Infinite output resistance
Output voltage occurs simultaneously with input voltage changes
To receive zero noise output voltage
$V_O= A\times(V_1+V_2)$
Amplifies products of two input voltage
Bandwidth –> ∞
-4v
Negative saturation
both AC and DC signals
output shape is the same as the input shape.
differential amplifier.
supply voltages
both inputs.
greater than the voltage gain.
CE amplifier.
equal to the voltage gain.
an output impedance of 75 Ω
differential input and single - ended output.
less than the input offset voltage.
input offset voltage.
smaller than the unloaded voltage gain.
zero.
collector current divided by current gain
both inputs.
CMMR.
80 dB
Output voltage occurs simultaneously with input voltage changes
equal to zero
80 dB
49.7 µA

1.5 V/ µs
both inputs
greater than differential voltage gain
CE amplifier
a virtual ground
Infinite output resistance
Output voltage occurs simultaneously with input voltage changes
always unity
dependent on input voltage
80 dB
equal to zero
differential input and single - ended output.
less than the input offset voltage.
input offset voltage.
a virtual ground

opt4
answers a and c
the output is not inverted
only one supply voltage is used
the output signals are in-phase
unpredictable
about 100
answers b and c
equal to the CMRR
100,000
none of these
none of these
top of the tail resistor
none of the above
swamped amplifier
an ordinary ground
Infinite slew rate.
Output can drive infinite number of device
None of the mentioned
$V_O = V_1 \times V_2$
None of the mentioned
Open loop voltage gain –> ∞
-2v
Supply voltage
neither AC not DC signals.
opamp may saturate.
Wheatstone bridge.
tolerance of the resistors
he top of the tail resistor
none of the above.
swamped amplifier.
equal to the common-mode voltage gain.
all of the above.
differential input and differential output
unimportant when a base resistor is used.
β.
impossible to determine.
very large
collector voltage divided by collector resistance
he top of the tail resistor
supply voltage.
100,000
Output can drive infinite number of device
equal to the CMRR
100,000
none of these

none of these
top of the tail resistor
none of the above
swamped amplifier
an ordinary ground
Infinite slew rate.
Output can drive infinite number of device
unpredictable
about 100
answers b and c
equal to the CMRR
differential input and differential output
unimportant when a base resistor is used.
β.
an ordinary ground

opt5

opt6

Answer
a and c
one input is grounded and signal is applied to the other
opposite polarity signals are applied to the inputs
an identical signal appears on both inputs
very low
very low
answers b and c
equal to zero
100,000
700 nA
0.67 V/ µs
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
To obtain finite output voltage
$V_O = A \times (V_1 - V_2)$
Amplifies the difference between the two input voltages
Input Resistance –> 0
-2v
Both positive and negative saturation voltage
both AC and DC signals
opamp may saturate.
Wheatstone bridge.
gain - bandwidth product.
both inputs.
greater than the voltage gain.
differential amp.
as high as possible.
all of the above.
differential input and single - ended output.
less than the input bias current.
input offset voltage.
equal to R_C / r_e.
1
sum of two emitter currents
both inputs.
CMMR.
100,000
Signals can be amplified without attenuation
equal to zero
100,000
700 nA

0.67 V/ µs
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
very low
very low
answers b and c
equal to zero
differential input and single - ended output.
less than the input bias current.
input offset voltage.
a virtual ground

Questions

Questions
A summing amplifier can have
An averaging amplifier has five inputs . The ratio R_f/R_i must be
In a scaling adder, the input resistors are
In an integrator , the feed back element is a
For step - in put , the out put of an integrator is a
In a differentiator , the feed back element is a
The output of the differentiator is proportional to
The voltage follower has a:
The ratio between differential gain and common-mode gain is called:
In an analog multiplier, the reference Voltage V_{ref} is internally set to ____
In one quadrant multiplier, the polarity of the input voltage V_x is _________ and V_y is__________________
If $V_s = V_s \sin(2*pi*f_s*t)$ and $V_o= V_o \sin((2*pi*f_o*t) +\theta)$ are applied to a switch type phase detector, then the output consists of a DC term and the other term is ___________
Division can be accomplished by placing the multiplier circuit in the _________ of the operational amplifier.
The input stage of Phase Locked Loop is___________
The Voltage Controlled Oscillator is also called as __________
The Voltage Controlled Oscillator is designed such that at zero voltage, it is oscillating at some initial frequency called ________ frequency.
Analog Multiplier produces an output which is a
The function of phase detector is to compare the _________ of the incoming signal to that of the output V_0 of Voltage Controlled Oscillator.
Phase detector is basically a ___________.
The output of phase detector is __________.
The signal V_c shifts the frequency in a direction to reduce the difference between f_s and f_0. Now the signal is in _____________ range.
The VCO continues to change the frequency till its output frequency is _________________the input signal frequency.
The range of frequencies over which the PLL can maintain the lock with the incoming signal is called ___________ range.
The range of frequencies over which the PLL can acquire the lock with the incoming signal is called ___________ range
The output frequency of Voltage Controlled Oscillator f_0 is ________
Voltage Controlled Oscillator is otherwise called as __________.
In PLL, the high frequency component (f_s+f_0) is removed by__________
Which of the following are the stages of PLL? i) free running ii) capture iii) tracking iv) pull in
Which of the following are the problems associated with the switch type phase detector? i) since the output voltage Ve is directly proportional to Vs, the phase detector gain and loop gain becomes dependent on the input signal amplitude. ii) output is proportional to cosΦ which makes it non linear. iii) the circuit becomes unstable iv) full wave detector
In switch type phase detector, at the locked state $(f_s = f_0)$ the phase shift should be ____________ in order to get zero error signal.
In balanced modulator type phase detector, the transistors act as _____.
In balanced modulator type phase detector, the phase angle to voltage transfer co-efficient KΦ is _________

The Voltage to Frequency conversion factor of VCO is ______.
The output from a Phase Locked Loop system is ________.
If a divide by N - network is inserted between VCO output and phase comparator input of PLL, then in the locked state f0 is ___________.
When PLL is used as AM demodulator, the AM signal is shifted in phase by _____ before being fed to the multiplier.
The other name for capture range is _____________ range.
The other name for lock in range is _____________ range.
The range of modulating input voltage applied to a VCO is __________.
Lock in range of a PLL is _______________ the capture range.
Which of the following is the drawback of variable transconductance multiplier?
The time taken for a PLL to capture the incoming signal is called ________________ time.
If the voltage at the modulation input of VCo is biased at 7/8 Vcc then the output frequency of VCO in PLL is given by f0 = _____________.
The maximum operated range of PLL 565 is_________________.
The Lock in range of Phase Locked Loop is _________________.
If the offset frequency f_1 is applied to the phase detector of frequency translator circuit, then at the locked state f0 is given by ___________.
___________ filter controls the capture range and lock in range of PLL.
The operating voltage range of IC 565 is __________________.
An external capacitor connected across IC 565 will act as ____________.
If V_c shifts the VCO frequency from the free running frequency f_0 to a frequency f, then the new frequency shift from VCO in a PLL is ______.
A _________________ is an electronic system which generates any range of frequencies from a single fixed time base or oscillator.
Phase detector is basically a ___________.
In PLL, the output of the error amplifier is equal to the ______________.
Select correct statement of PLL.
The Voltage to Frequency Converter of VCO is defined as ____
IC 566 functions as__________.
The total time taken by PLL to establish the lock is called ______.
If the frequency of the carrier wave is varied in accordance with the modulating signal, then the modulation refers to _____ modulation
The capture range of PLL is defined as __________.
The lock in range of PLL is defined as ____________.

opt1	**opt2**
only one input	only two inputs
5	0.2
all of the same value	all of different values
resistor	capacitor
pulse	triangular wave form
resistor	capacitor
the RC time constant	the rate at which the input is changing
closed-loop voltage gain of unity	small open-loop voltage gain
Amplitude	differential-mode rejection
15V	5V
positive, negative.	positive, positive
f_o	$2 * f_o$
feedback loop	inverting input terminal
Low Pass Filter	Error Amplifier
relaxation oscillator	free running multivibrator
free running	cut off
product of two input signals divided by a reference voltage.	product of two input signals and reference voltage.
phase and frequency	phase
summer	subtractor
f_s+f_0	f_s-f_0
lock-in	capture
less than	exactly the same as
tracking	capture
tracking	capture
$(V_{cc}-v_c)/(R_T*C_T*V_{cc})$	$v_c /(R_T*C_T*V_{cc})$
voltage to frequency converter	voltage to time converter
high pass filter	low pass filter
only i and ii	only ii and iv
i and ii	i,ii and iii
0^o	180^o
switch	amplifier
$(I_Q*R_L)/$ pi	$V_0/(2*\text{pi})$

f_0 / V_{CC}	8*f_0 / V_{CC}
voltage or frequency	only voltage
f_s /N	N*f_s
0º	180º
tracking	lock in
tracking	acquisition
0.5 V_{CC} to V_{CC}	0.75 V_{CC} to V_{CC}
greater than	equal to
inaccurate	costly
pull out	capture
0.25/ (R_T*C_T)	(R_T*C_T)/4
0 to 500 kHz	0.001 to 500 kHz
$\Delta f_L = 7.8 f_0/v$	$\Delta f_L = +/- (7.8 f_0/v)$
fs	fs * f_1
high pass filter	low pass filter
+/- 6V to +/-12V	+/- 10V to +/-12V
passive device	low pass filter
$f_0 + k_v$*Vc	$f_0 - k_v$*Vc
frequency multiplier	frequency synthesizer
summer	subtractor
error voltage	applied voltage
capture range is smaller than lock in range	capture range is greater than lock in range
$\Delta V_c / \Delta f_0$	Δf_0
phase detector	low pass filter
pull in time	pull out time
frequency shift keying	frequency
$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10^3))\}^{1/2}$	$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C)\}^{1/2}$
$\Delta f_L = +/- (K_v*K_\Phi)$	$\Delta f_L = +/- (K_v*K_\Phi*A$

opt3	opt4
only three inputs	any number of inputs
1	2
each proportional to the weight of its input	related by a factor of two
zener diode	voltage divider
spike	ramp
zener diode	voltage divider
the amplitude of the input	both a and b
closed-loop bandwidth of zero	large closed-loop output impedance
common-mode rejection	phase
20V	10V
negative, negative	negative positive
f_o/ 2	3* f_o
output	non inverting terminal
Voltage Controlled Oscillator	Phase Detector
monostable multivibrator	phase shift oscillator
capture	free cycle
product of three input signals.	product of two input signals.
frequency	amplitude
multiplier	divider
f_s*f_0	f_s+/ f_0
free running	unlocked
greater than	twice that of
free running	pull in
free running	pull in
2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})	1/(R_T*C_T)
voltage to current converter	frequency to voltage converter
band pass filter	band reject filter
i, ii and iii	only iv
ii,iii	only i
270º	90º
oscillator	modulator
(4*I_Q*R_L)/pi	(I_Q*R_L)/2*pi

$2*f_0$ / V_{CC}	$4*f_0$ / V_{CC}
only frequency	only phase.
f_s+N	f_s –N
270º	90º
free running	acquisition
free running	capture
0 V_{CC} to V_{CC}	0.25 V_{CC} to V_{CC}
lesser than	less than or equal to
difficult to integrate in IC	scale factor depends on temperature which affects the output
lock in	pull in
$4(R_T*C_T)$	$(R_T*C_T)/0.25$
100 to 400 kHz	10 to 400 kHz
Δf_L = +/- (8.7 f_0/v)	Δf_L = 8.7 f_0/v
fs + f_1	fs - f_1
band pass filter	band reject filter
+/- 8V to +/-12V	+/- 12V
charging device	discharging device
k_v*Vc	Vc
frequency doubler	frequncy translator
multiplier	divider
control voltage	power supply voltage
capture range is equal to lock in range	capture range is not equal to lock in range
ΔV_c	$\Delta f_0/\Delta V_c$
VCO	PLL
rise time	hold time
amplitude	phase
Δfc = +/- {(Δf_L)/ (2*pi*C*(3.6*10^3))}	Δfc = +/- {(Δf_L)/ (2*pi*C)}
Δf_L = +/- (K_v*K_Φ)/(A*(pi/2))	Δf_L = +/- $(K_v*K_\Phi$*A*(pi/2))

opt5	opt6	Answer
		any number of inputs
		0.2
		each proportional to the weight of its input
		capacitor
		ramp
		resistor
		both a and b
		closed-loop voltage gain of unity
		common-mode rejection
		10V
		positive, positive
		$2^* f_o$
		feedback loop
		Phase Detector
		free running multivibrator
		free running
		product of two input signals divided by a reference voltage.
		phase and frequency
		multiplier
		f_s+/ f_0
		capture
		exactly the same as
		tracking
		capture
		$2^*(V_{cc}-v_c)/(R_T^*C_T^*V_{cc})$
		voltage to frequency converter
		low pass filter
		i, ii and iii
		i and ii
		90º
		switch
		$(4^*I_Q^*R_L)$/pi

		$8*f_0 / V_{CC}$
		voltage or frequency
		$N*f_s$
		90º
		acquisition
		tracking
		$0.75\ V_{CC}$ to V_{CC}
		greater than
		scale factor depends on temperature which affects the output
		capture
		$0.25/ (R_T*C_T)$
		0.001 to 500 kHz
		$\Delta f_L = +/- (7.8 f_0/v)$
		$fs + f_1$
		low pass filter
		+/- 6V to +/-12V
		low pass filter
		$f_0 + k_v*Vc$
		frequency synthesizer
		multiplier
		control voltage
		capture range is smaller than lock in range
		$\Delta f_0/\Delta V_c$
		VCO
		pull in time
		frequency
		$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10^3))\}^{1/2}$
		$\Delta f_L = +/- (K_v*K_\Phi*A*(pi/2))$