16BEEC602A VLSIDESIGN L T P C
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OBJECTIVES

- To learn the basic MOS Circuits.
- To learn the MOS process technology
- To learn the concepts of modeling a digital system using Hardware Description Language.
- To learn techniques of chip design using programmable devices.
- To learn the concepts of designing V LS I subsystems.

INTENDED OUTCOMES:

- Gain knowledge in the basic MOS Technology.
- Gain knowledge in the MOS Process Technology and its second order effect.
- Gain knowledge in the concepts of modeling a digital system using Hardware Description Language.
- Gain knowledge in basic concept of V LS I implementation strategies based on CMOS and FPGA.

UNIT I-MOS TECHNOLOGY

Chip Design Hierarchy – IC Layers – Photolithography and Pattern Transfers – Basic MOS Transistors – CMOS Fabrication: n-well – p-well – twin tub – Latch up and prevention- Layout design rules, physical design- basic concepts, CAD tool sets, physical design of logic gates- Inverter, NAND, NOR.

UNIT II-MOS CIRCUIT DESIGN PROCESS

Introduction to MOSFET: Symbols, Enhancement mode-Depletion mode transistor operation – Threshold voltage derivation – body effect – Drain current Vs voltage derivation – channel length modulation. NMOS and CMOS inverter – Determination of pull up to pull down ratio –Stick diagrams – V LS I Circuit Design Flow.

UNIT III-CMOS LOGIC GATES & OTHER COMPLEX GATES

Gate delays – Logical Effort - CMOS Static Logic – Transmission Gate Logic – Tri-State Logic – Pass Transistor Logic – Dynamic CMOS Logic – Domino CMOS Logic,NORA CMOS Logic, True Single Phase Clock (TSPC) Dynamic Logic

UNIT IV-VERILOG HDL

Hierarchical modeling concepts – Basic concepts: Lexical conventions – Data types – Modules and ports. Gate level modeling – Dataflow modeling – Behavioral modeling – Design examples of Combinational and Sequential circuits – Switch level modeling – Functions – UDP concepts.

UNIT V-VLSI IMPLE MENTATION STRATEGIES

Introduction – Design of Adders: carry look ahead-carry select-carry save. Design of multiplier s: Array – Braun array – Baugh-Wooley Array. Introduction to FPGA – Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures.

TEXTBOOKS:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1	DouglasA. Pucknell	Basic VLSI Systems and Circuits	Prentice HallofIndia,3rd Edition, reprint	2008
2	JohnP.Uyemura,	Introduction to VLSI Circuits and Systems	John Wiley & Sons, Reprint	2009

REFERENCES:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1	Smith.M.J.S	Application Specific integrated circuits	Pearson Education , New York	2008
2	Weste& Eshraghian,	Principles of CMOS VLSI Design	AddisonWesley,2nd Edition	2008
3	JohnP Uyemura	Chip Design for Submicron VLSI: CMOS layout and simulation	Thomson India Edition	2010
4	SamirPalnitkar	Verilog HDL– Guide to Digital Design and Synthesis	PearsonEducation,3rd Edition	2003