17BEBME6E04 BIOSIGNAL CONDITIONING CIRCUITS 3 0 0 3 100

COURSE OBJECTIVE

- To gain in depth knowledge of fundamentals of operational amplifier circuits
- To study the various applications using operational amplifiers.

UNIT 1 INTRODUCTION TO OPAMP 9

Introduction, Signal conditioning, 741 General purpose OPAMP: ideal characteristics, offset voltages and currents. Open & Closed Loop Configuration. Inverting, Non-Inverting, Summing, Voltage Follower, Integrator, differentiators, Log & Anti-Log Amplifiers, Differential Amplifiers, CMRR.

UNIT 2 APPLICATION OF OPAMPS 9

Comparator- Zero crossing detector, Inverting and non inverting comparator, Schmitt Trigger, Precision rectifiers- Half wave and Full wave rectifiers, Peak detectors, Monostable, Astable multivibrators, Sawtooth generator, Triangular waveform generator, Sine Wave Generators-RC Phase Shift Oscillator, Wein Bridge oscillator.

UNIT 3 FILTERS

9

Introduction- Analog Filters, Active Filters and Passive Filters, First order and Second order Low Pass Filters, High Pass Filters, Band Pass Filters- Narrow Band Pass, Wide band Pass Filters,, Band Reject Filters- Notch Filter, All Pass filters and higher Order filters- Design and applications.

UNIT 4 A/D AND D/A CONVERTERS 9

Sample and Hold circuit - D/A converters: Resistive divider and R-2R ladder networks, A/D converters: Counting type, Successive approximation, parallel comparator, Voltage to Current Converter, 555 Timer and its applications- Astable multivibrators and Monostable Multivibrator.

UNIT 5 AMPLIFIERS

Instrumentation amplifiers, Bridge Amplifiers, Bioelectric Amplifiers: - Properties desired, Isolation Amplifiers:- Battery Powered, Carrier, Optically Coupled, Current Loading, Chopper Stabilized amplifier, Input Guarding.

Total : 45

TEXT / REFERENCE BOOKS

S.NO.	Author(s) Name	Title of the book	Publisher	Year of publication
1	Ramakant A Gayakwad	Operational Amplifiers & Linear Integrated Circuits	Prentice Hall	2000
2	Joseph J. Carr & John M. Brown	Introduction to Biomedical Equipment Technology	Pearson Education Pvt. Ltd, 4th edition	2001
3	Roy Choudhary	Linear Integrated Circuits	New Age International (P) Ltd,	2004
4	John P.Bentley	Principles of Measurement System	Longman Science & Technology	1995

5	Jacob Mill man	Micro Electronics	McGraw-Hill	1987
6	Robert Coughlin and Fredrer	Operational Amplifiers & Linear Integrated Circuits	Prentice Hall	2001

KARPAGAM ACADEMY OF HIGHER EDUCATION

(Established Under Section 3 of UGC Act 1956)
FACULTY OF ENGINEERING

`DEPARTMENT OF BIOMEDICAL ENGINEERING

17BEBME6E04 – BIOSIGNAL CONDITIONING CIRCUITS

LECTURE PLAN

NAME OF THE STAFF : Ms.S.JAYACHITRA

DESIGNATION : ASSISTANT PROFESSOR

CLASS : B.E-III YEAR BME

SUBJECT NAME : BIOSIGNAL CONDITIONING CIRCUITS

SUBJECT CODE : 17BEBME6E04

S.No.	TOPICS TO BE COVERED	TIME DURATION	SUPPOTING MATERIALS
UNIT I	**INTRODUCTION TO OPAMP**		
1	Introduction, Signal conditioning,	01	T3- Page.no 2-12 T1 Page.no 23-42
2	741 General purpose OPAMP: ideal characteristics	01	T3 Page.no 53-54
3	offset voltages and currents.	01	T3- Page.no.42-43
4	Open & Closed Loop Configuration	01	T3 Page.no 104-110
5	Basic op-amp circuits: Inverting & Non-Inverting Amplifier	01	T3 Page.no43-48
6	Voltage follower - Summing, scaling amplifiers	01	T3 Page.no 49
7	Integrator, differentiators	01	T3 Page.no 164-169
8	Log & Anti-Log Amplifiers	01	T3 Page.no 155-158
9	Differential Amplifiers, CMRR	01	T3 Page.no 53-60
Total Lecture Hours		**09**	
Total Hours		**09**	

UNIT II APPLICATIONS OF OPAMPS			
10	Comparator- Zero crossing detector, Inverting and non inverting comparator,	01	T3 Page.no 207-210
11	Schmitt Trigger , -	01	T3 Page.no 324,212-215
12	Precision rectifiers- Half wave and Full wave rectifiers, Peak detectors,	02	T3 Page.no 148-150
13	Monostable, Astable multivibrators,	01	T3 Page.no 216-219
14	Sawtooth generator, Triangular waveform generator	01	T3 Page.no 220
15	Sine Wave Generators	01	T3 Page.no 222-228

16	RC Phase Shift Oscillator,	01	
17	Wein Bridge oscillator.	01	
Total Lecture Hours		**09**	
Total Hours		**09**	

UNIT III FILTERS			
18	Introduction- Analog Filters, Active Filters and Passive Filters	02	T3 Page.no 262-264
19	First order and Second order Low Pass Filters	01	T3 Page.no 264-272
20	First order and Second order high Pass Filters	01	T3 Page.no 264-272
21	Band Pass Filters- Narrow Band Pass, Wide band Pass Filters,	01	T3 Page.no 272-277
22	Band Reject Filters- Notch Filter ,All Pass filters.	02	T3 Page.no 272-277
23	Higher Order filters- Design and applications	02	T3 Page.no 264-277
Total Lecture Hours		**09**	
Total Hours		**09**	

UNIT IV A/D AND D/A CONVERTERS			
24	Sample and Hold circuit	01	
25	D/A converters: Resistive divider	01	T3 Page.no 349-353
26	R-2R ladder networks,	01	T3 Page.no 353-355
27	A/D converters: Counting type	01	T3 Page.no 357-366
28	Successive approximation type A/D converters	01	T3 Page.no 361-362
29	Parallel comparator,	01	T3 Page.no356-357
30	Voltage to Current Converter	01	
31	555 Timer and its applications : Monostable operation and its applications	01	T3 Page.no 311-312
32	IC 555 Timer: Astable operation and its applications	01	T3 Page.no 318-324
Total Lecture Hours		**09**	
Total Hours		**09**	
UNIT V AMPLIFIERS			
33	Instrumentation amplifiers	01	T3 Page.no 141-144
34	Bridge Amplifiers	01	https://www.allaboutcircuits.com/technical-articles/bridge-amplifiers-for-single-supply-applications/
35	Bioelectric Amplifiers- Properties desired	01	http://www.electronicsandcommunications.c

			om/2017/07/bioelectric-amplifiers.html
36	Isolation Amplifiers	01	http://www.learningaboutelectronics.com/Articles/Isolation-amplifier
37	Battery Powered amplifiers	01	https://engineering.purdue.edu/ece40020/LectureNotes/PowerAmpClass.pdf
38	Optically Coupled amplifiers	01	https://www.alliedelec.com/m/d/70ef6270ecab8061fff13fbcd4693869.pdf
39	Current Loading	01	https://mgh-courses.ece.gatech.edu/ece4430/ECE4430/Unit2/BJTDiffAmps.pdf
40	Carrier and Chopper Stabilized amplifier	01	http://cas.ee.ic.ac.uk/people/dario/files/E302/4-amplifiers.pdf
41	Input Guarding	01	
Total Lecture Hours		**09**	
Total Hours		**09**	

Total No of Lecture Hours Planned: 45 Hours

TEXT / REFERENCE BOOKS

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4	John P.Bentley	Principles of Measurement System	Longman Science & Technology	1995
5	Jacob Mill man	Micro Electronics	McGraw-Hill	1987
6	Robert Coughlin and Fredrer	Operational Amplifiers & Linear Integrated Circuits	Prentice Hall	2001

STAFF IN-CHARGE **HOD/BME**

UNIT-1
INTRODUCTION TO OPAMP

Prepared by
S.JAYACHITRA,AP/ECE

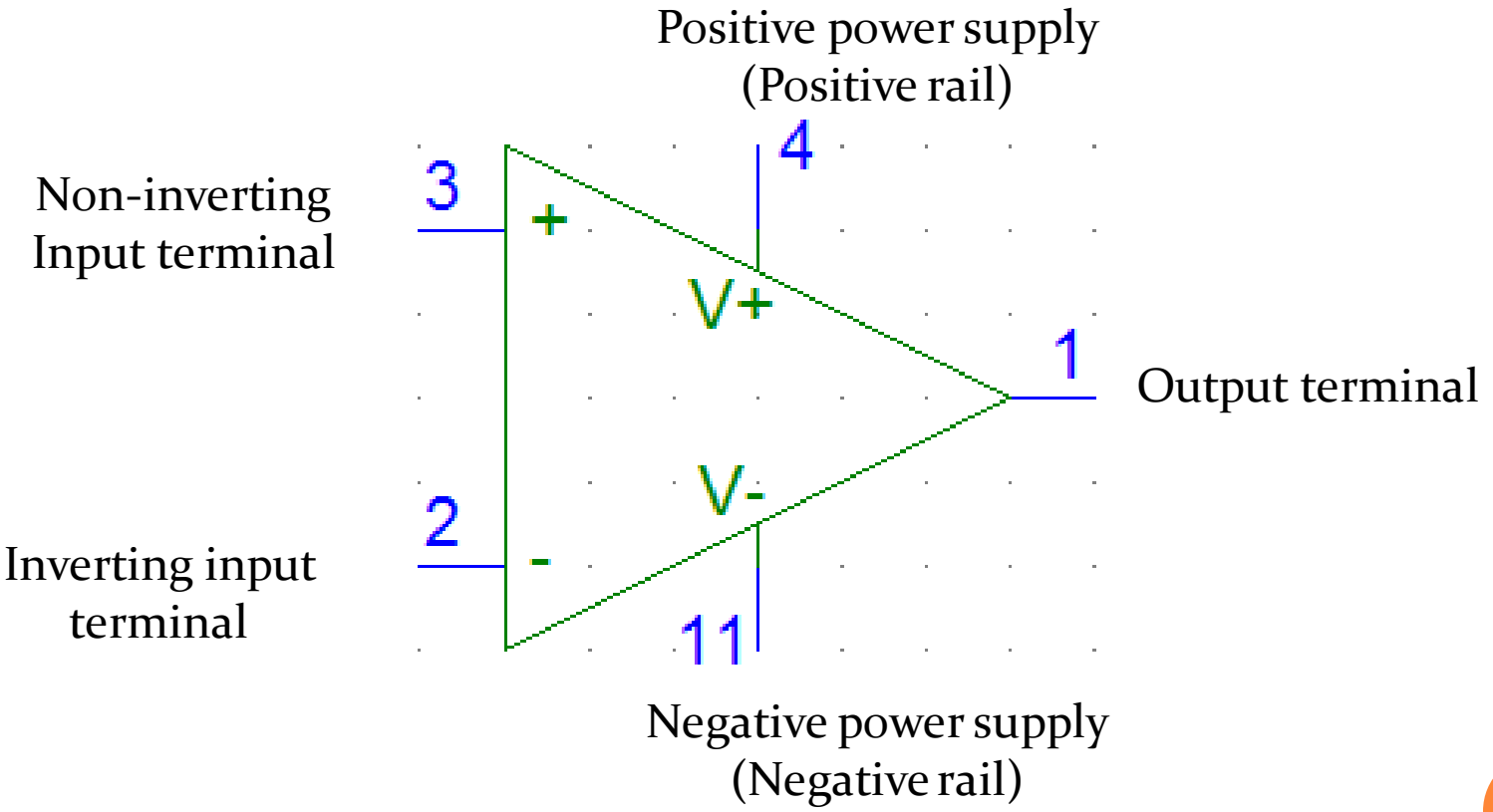
Operational Amplifier

- An operational amplifier is a direct coupled high gain
- Amplifier usually consisting of one or more differential amplifier and usually followed by a level translator and an output stage.
- An operational amplifier is available as a single
- integrated circuit package.
- The operational amplifier is versatile device that can be used to amplify DC as well as AC input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.

Op Amps Applications

- Audio amplifiers
  - Speakers and microphone circuits in cell phones, computers, mpg players, boom boxes, etc.
- Instrumentation amplifiers
  - Biomedical systems including heart monitors and oxygen sensors.
- Power amplifiers
- Analog computers
  - Combination of integrators, differentiators, summing amplifiers, and multipliers

OP AMP SYMBOL



IDEAL CHARACTERISTICS OF OP-AMP

- An IDEAL op-amp would exhibit the following
- electrical characteristics.
- – Infinite voltage gain, A
- – Infinite input resistance Ri
- – Zero output resistance Ro
- – Zero output voltage when input voltage is zero.
- – Infinite bandwidth – any signal can be amplified
- without attenuation
- – Infinite common mode rejection ratio
- – Infinite slew rate so that output voltage changes occur simultaneously with input voltage changes.

OFFSET VOLTAGE

- **Input offset voltage**: Input offset voltage Vio is
- the differential input voltage that exists
- between two input terminals of an op-amp
- with out any external inputs applied.
- **Output Offset Voltage:**
- – The output voltage caused by mismatching
- between two input terminals is called the output
- offset voltage Voo.
- – The output offset voltage Voo is a DC voltage, it
- may be +ve or –ve in polarity depending on
- whether the potential differences between the
- two input terminals is +ve or –ve.

OFFSET CURRENT

- **Input offset Current:**
- – The input offset current Iio is defined as the
- algebraic difference between two input bias
- currents Ib1 and Ib2. In equation form it is
- Iio = | Ib1 – Ib2 |
- **Input Bias Current:**
- – An input bias current Ib is defined as the average of
- the two input bias currents, Ib1 and Ib2 as shown in
- the following figure.
- Ib = (Ib1 + Ib2)/2 [Ib – DC current]
- Where Ib1= DC bias current flowing into the noninverting
- input
- Ib2 = DC bias current flowing into the inverting
- input
- - The value of input bias current Ib is very small, in the
- range of a few to few hundred nano amp.

Differences b/w Ideal and Practical Op-Amp

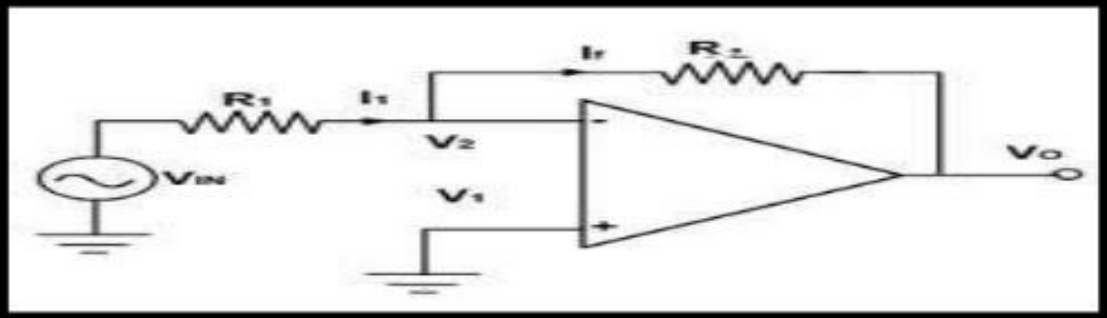
Characteristics	Ideal Op-amp	Practical Op-amp
Voltage gain	Infinite	High
Input resistance	Infinite	High
Output resistance	Zero	Low
Output voltage when input voltage is zero	Zero	Low
Band width	Infinite	High
CMRR	Infinite	High
Slew Rate	Infinite	High

Why op-amp is generally not used in open loop mode?

- As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level.
- Thus in open loop configuration, the output is at its positive saturation voltage (+Vsat) or negative saturation voltage (-Vsat) depending on which input V1 or V2 is more than the other.
- For a.c. input voltages, output may switch between positive and negative saturation voltages.
- This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode. Hence the op-amp in open loop configuration is not used for the linear applications

INVERTING OP-AMP CONFIGURATION

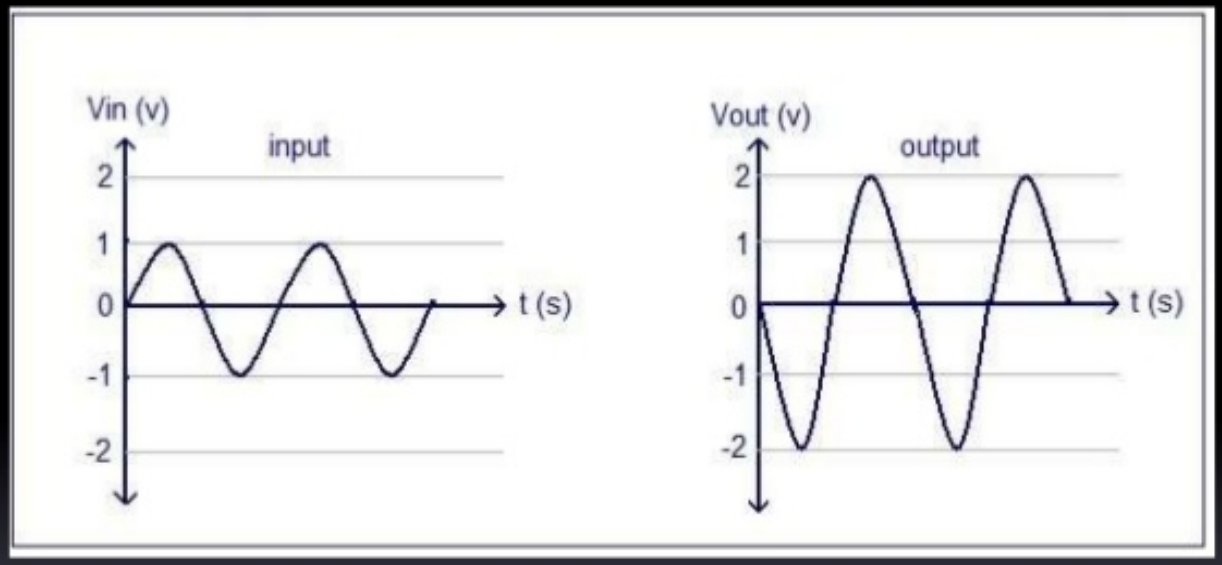
- This is a diagram of an **INVERTING OP-AMP**.



- This circuit makes use of an OP-AMP, a single resistor(R1) connected to input and a feedback resistor (R2) connected to R1.

- The Inverting Amplifier produces a 180° phase shift in voltage from input to output.

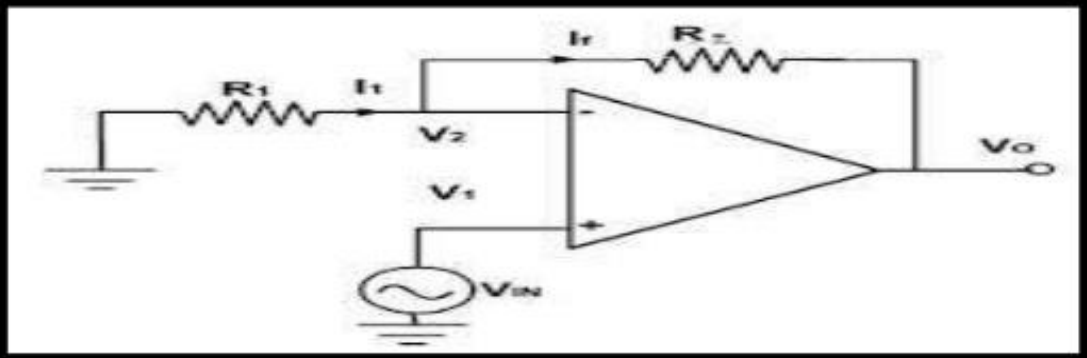
INPUT AND OUTPUT WAVEFORMS OF AN INVERTING OP-AMP (gain assumed to be 2)



- The input and output signals of the inverting amplifier are not in-phase with each other.

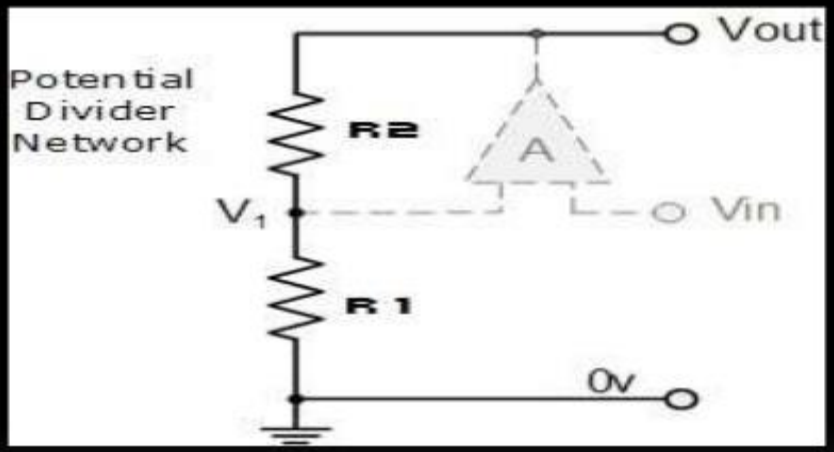
NON INVERTING OP-AMP CONFIGURATION

- This is a diagram of **NON-INVERTING OP-AMP.**



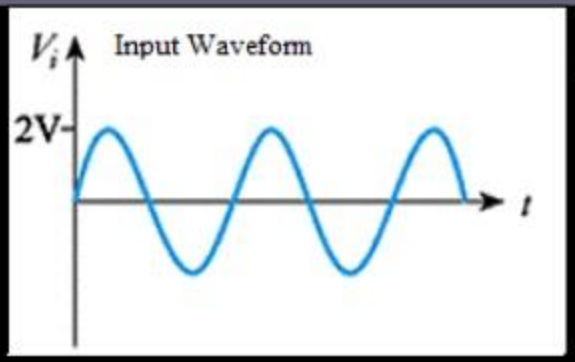
- This circuit consists of an OP-AMP, a single resistor (R1) connected to ground and feedback resistor (R2) connected to R1.
- Input Voltage is directly applied through the non-inverting terminal.

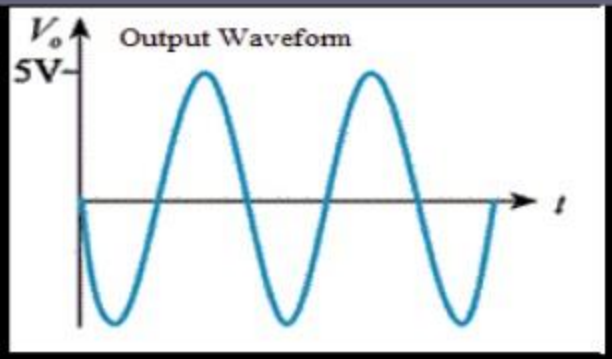
NON INVERTING OP-AMP CONFIGURATION



- R1 and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and R1

INPUT AND OUTPUT WAVEFORMS OF AN NON INVERTING OP-AMPINVERTING OP-AMP





- The input voltage signal, (Vin) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive".
- The result of this is that the output signal is "in-phase" with the input signal.

SUMMING AMPLIFIER

Besides amplification, the op amp can perform addition and subtraction.

"A summing amplifier is an op amp circuit that combines several inputs and produces an output that is the weighted sum of the inputs"

- The summing amplifier, shown in Fig.A , is a variation of the inverting amplifier. It takes advantage of the fact that the inverting configuration can handle many inputs at the same time.

- the current entering each op amp input is zero. Applying KCL at node *A* gives

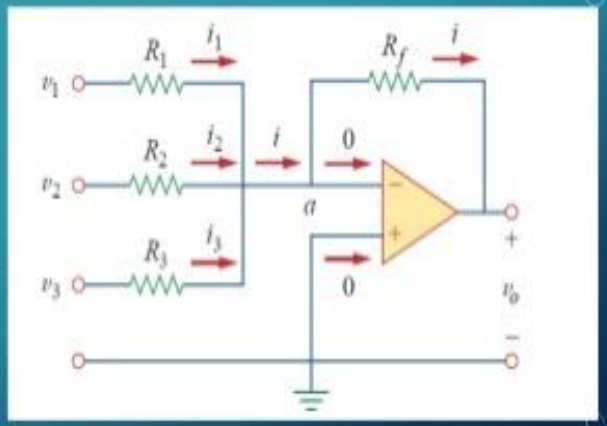
$i = i_1 + i_2 + i_3$

But

$$i_1 = (v_1 - v_a)\frac{1}{R_1}\ ,\quad i_2 = (v_2 - v_a)\frac{1}{R_2} \text{-----}(a)$$

$$i_3 = (v_3 - v_a)\frac{1}{R_3}\ ,\quad i_4 = (v_4 - v_a)\frac{1}{R_4} \text{----}$$

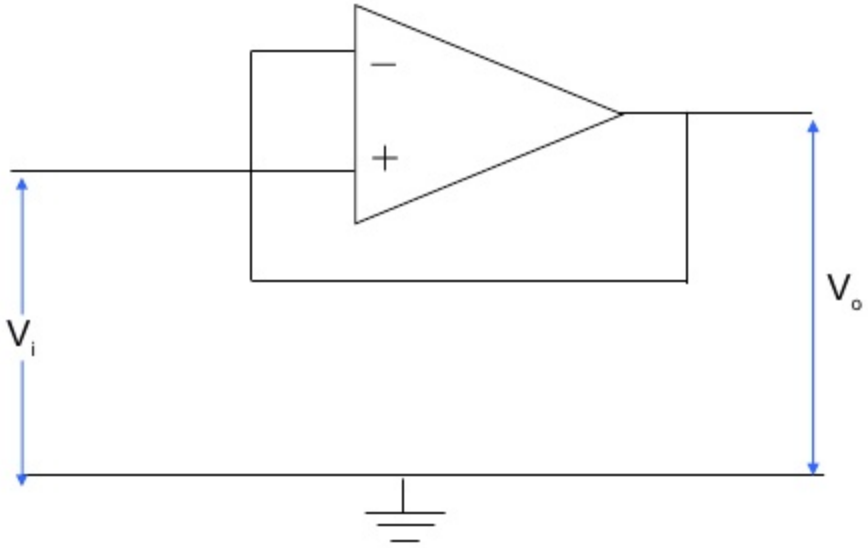
-(b)



We note that $v_a = 0$ and substitute Eq. (a) into Eq. (b). We get

$$v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right) \text{---(C)}$$

Voltage Follower



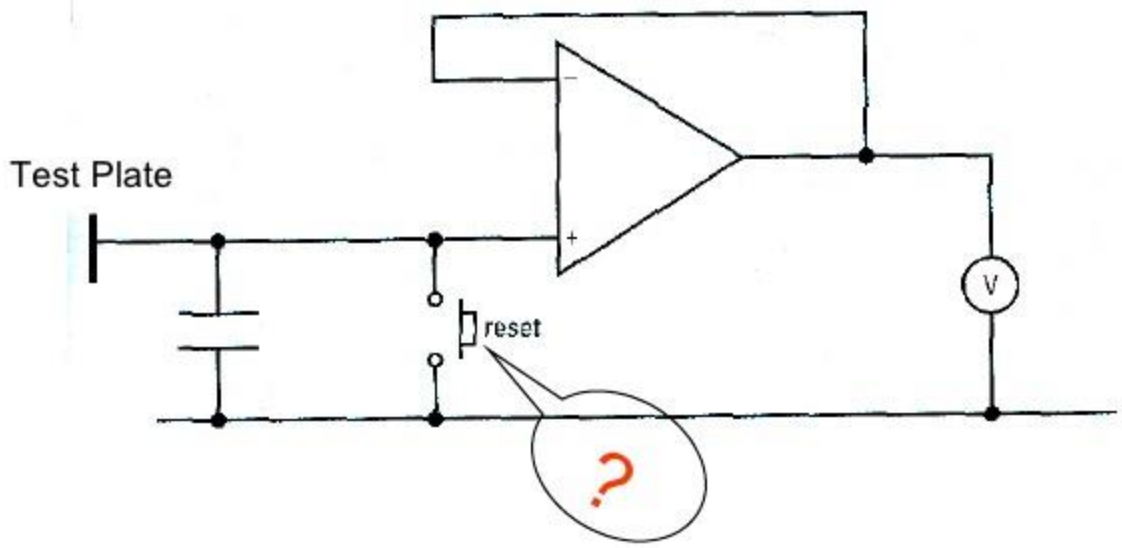
Voltage Follower

- This is a special case of the non-inverting amplifier.
- In case of non-inverting amplifier, gain
  $A = 1 + \frac{R_f}{R_i}$
  If we set $R_f = 0$, $A = 1$ (unity gain)
- This is called voltage follower because the o/p voltage is locked to the i/p voltage (both are same)
- Advantage: op amp has very high i/p impedance so it can measure V_i without drawing any current.

Characteristics of Voltage Follower

- This is a special case of the non-inverting amplifier.
- Gain A = 1
- The o/p voltage “follows” the i/p voltage
- Op amp has very high i/p impedance and very low i/p impedance

Voltage Follower used for measuring charge



Voltage Follower used for measuring charge

- This circuit uses a capacitor to make a charge-measuring device.
- If a charged object touches the test plate, it will transfer charge to the capacitor.
- The p.d. between the plates of the capacitor rises
- If the capacitor is connected directly to a voltmeter, this charge will drain away through the meter and incorrect reading would be obtained.
- Op-amp has very high i/p impedance and so practically no charge is removed from the capacitor and yet measured by the voltmeter

DIFFERENTIATOR

- A differentiator is a circuit in which the output
- waveform is the derivative of input waveform.
- A differentiator circuit is shown in the figure 4.21(a).

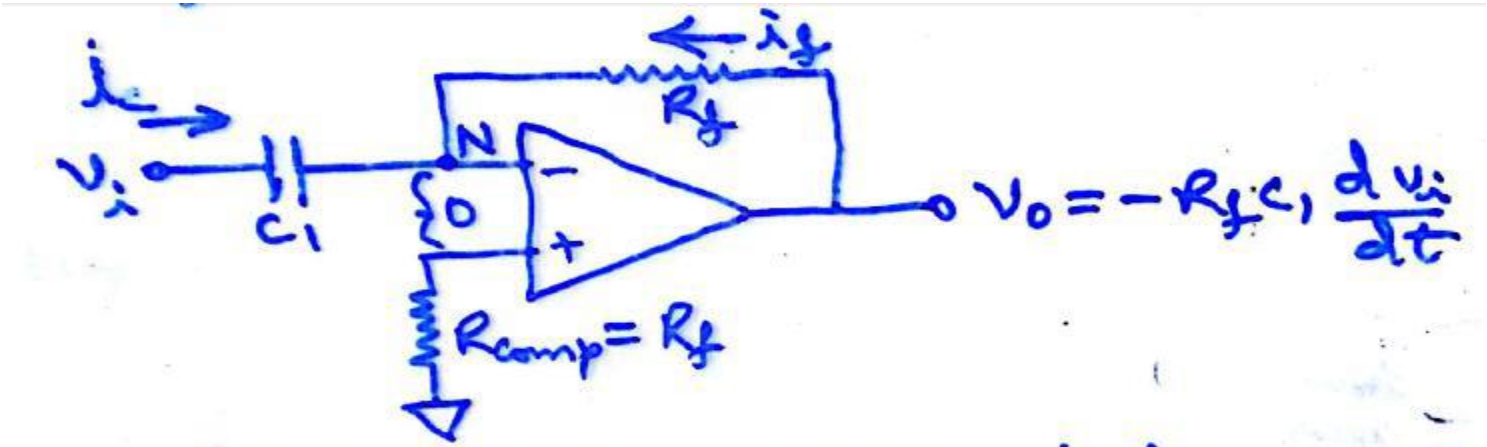


Fig 4.21(a) op-amp differentiator

Analysis:

- The node N is at virtual ground potential ie Vn=0. The current ic through the capacitor is ic= C1 d(Vi-Vn)/dt = C1

dVi/dt

- The current If(not the English word if) through the feedback resistor = Vo/Rf and there is no current into the op-amp
- Therefore nodal equation at node N is C1 dVi/dt + Vo/Rf = 0 ==> Vo= -Rf C1 dVi/dt ------ eq(1)
- The minus sign indicates a 180° phase shift of the output waveform Vo with respect to the input signal.

- The phasor equivalent of equation (1). is

Vo(s) = - Rf C1 S Vi(s) where Vo & Vi are the phasor representation of vo & vi.

- In steady state put s=jw. Now the magnitude of gain A of the differentiator is

$|A| = |Vo/Vi| = |-jw\ Rf\ C1| = w\ Rf\ C1$ ---- eq(2)

Eq (2) may be written as

- $|A| = f/fa$ where $fa = 1/2\pi\ Rf\ C1$
- At f = fa, |A| = 1 ie = 0 dB, and the gain increases at a rate of +20dB/decade.
- Thus at high frequency, a differentiator may become unstable and break into oscillations .

- There is one more problem in the
- Differentiator of figure 4.21(a).
- • The input impedance (ie 1/wC1) decreases
- with increase in frequency there by making
- the circuit sensitive to high frequency noise.

INTEGRATOR

- By interchanging the resistor and capacitor of the Differentiator, we get the circuit of an integrator which is shown in the figure 4.23(a).

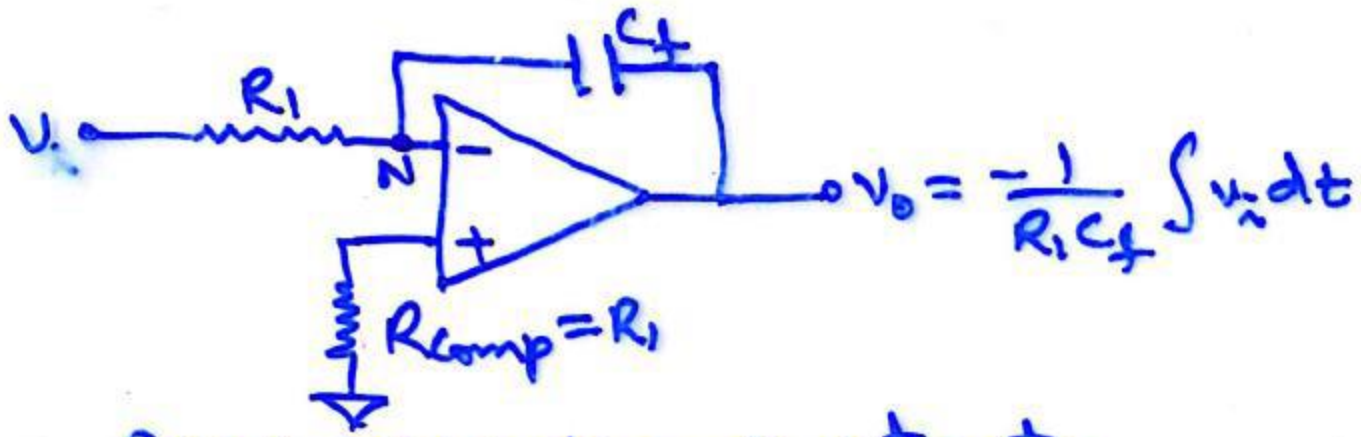


Fig 4.23(a) op-amp integrator

- The nodal equation at node N is (Vi/R1) + Cf dVo/dt = 0
- dVo/dt = -(1/R1 Cf) Vi
- $0\int t$ dVo = (-1/R1Cf) $0\int t$ Vidt
- Vo(t)= (-1/R1Cf) $0\int t$ Vi(t)dt + Vo(0) ----- eq(1) where Vo(0) is the initial o/p voltage.
- Here R1Cf is the time constant of the integrator

- Here –ve sign is present, hence it is called inverting integrator.
- Rcomp is the resistor to minimize the effect of input bias current.
- The operation of the integrator can also be studied in the frequency domain. In phasor notation the equation (1) can be written as
- $V_o(s) = -(1/sR_1C_f) V_i(s)$

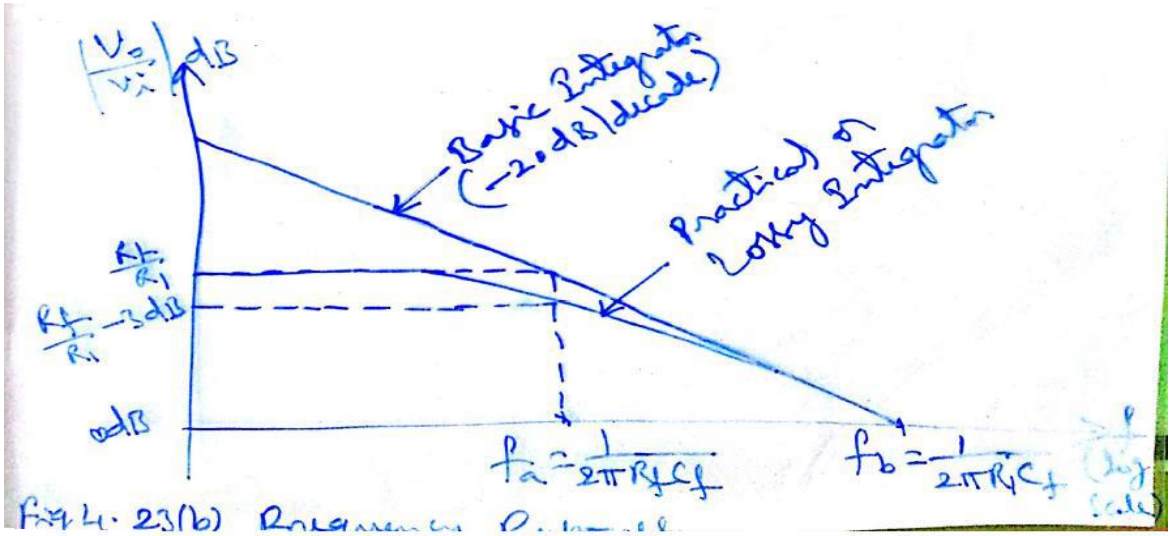
In steady state, put s=jw and we get

- $V_o(jw) = -(1/jwR_1C_f) V_i(jw)$

- So the magnitude of the gain is
- |A| = |Vo(jw)/Vi(jw)| = |-1/jwR1Cf| = 1/wR1Cf = 1/(f/fb)

Where fb = 1/2Π R1Cf

- The frequency response is shown in the figure 4.23b



- The Bode plot of basic integrator is a straight line of slope -20 dB/decade.
- • The frequency fb is the frequency at which the gain of the integrator is 0 dB and is given by

  $fb = 1/2\Pi R1Cf$
- • As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in the differentiator.
- However, at low frequencies such as DC (w=0), the gain becomes infinite (ie saturates). The solution to this problem is a practical integrator circuit.

Log and Antilog Amplifier: Log Amplifier:

Log Amplifier:

$$V_o = V_t ln\left(I_f / I_i\right)$$

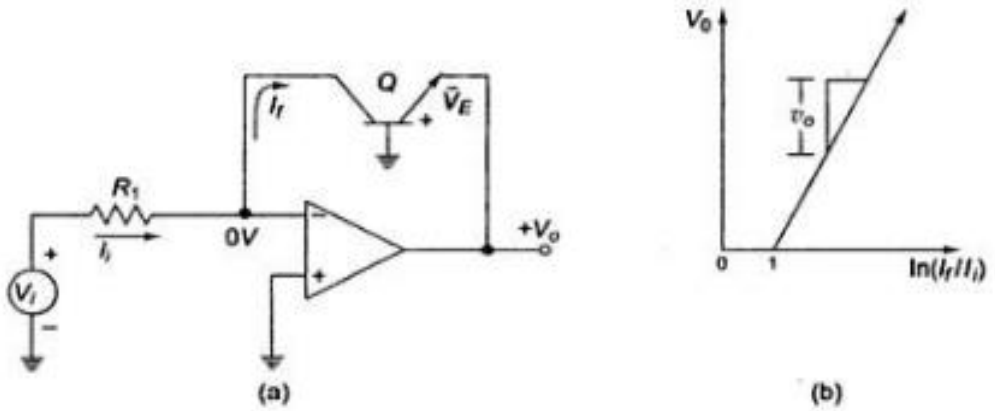


Fig 2.28 Fundamental log-amp Circuit and its characteristics

There are several applications of log and antilog amplifiers.
Antilog computation may require functions such as ln x, log x or sin hx.

- Uses: Direct dB display on a digital Voltmeter and Spectrum analyzer. Log-amp can also be used to compress the dynamic range of a signal.
- A grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor‘s voltage-current relationship becomes that of a diode and is given by, = [− 1] and since Ic =IE for a grounded base transistor IC = Is e kT Is-emitter saturation current ≈10-13A k=Boltzmann‘s constant T=absolute temperature (in o K) where Vref =R1Is
- The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find log10, by proper scaling Log10X=0.4343 ln X The circuit has one problem.
- The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtained. This is eliminated by the circuit given below

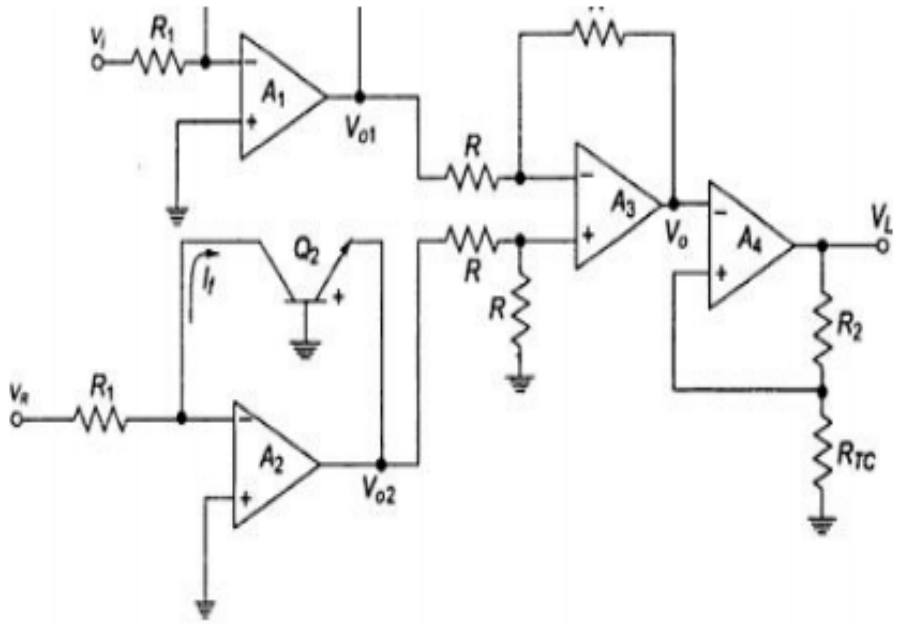


Fig. 2.29 Logarithmic amplifier with compensation of emitter saturation current

The input is applied to one log-amp, while a reference voltage is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

Assume $I_{S1}=I_{S2}=I_S$

Thus the reference level is now set with a single external voltage source. Its dependence on device

and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A4 which provides a non-inverting gain of $(1+R_2/R_{TC})$. Temperature compensated output voltage V_L

$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

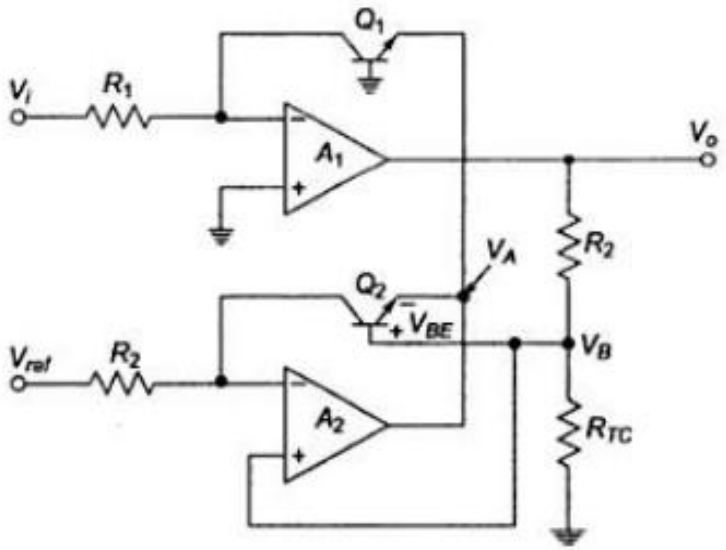


Fig.2.30 Logarithmic amplifier using two op amps

Where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensor) so that the slope of the equation becomes constant as the temperature changes.

ANTILOG AMPLIFIER

2.12 Antilog Amplifier

A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents

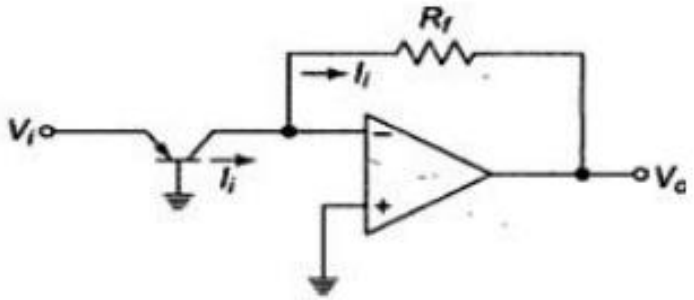


Fig. 2.31 Antilog amplifier

$$I_i = I_c = I_s\left(e^{\frac{\eta V_{BE}}{kT}}\right) \text{ and } V_0 = R_f I_s\left(e^{\frac{\eta V_{BE}}{kT}}\right)$$

The circuit is shown in figure below. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q2. The output of A2 is fed back to R1 at the inverting input of op amp A_1. The non-inverting inputs are grounded

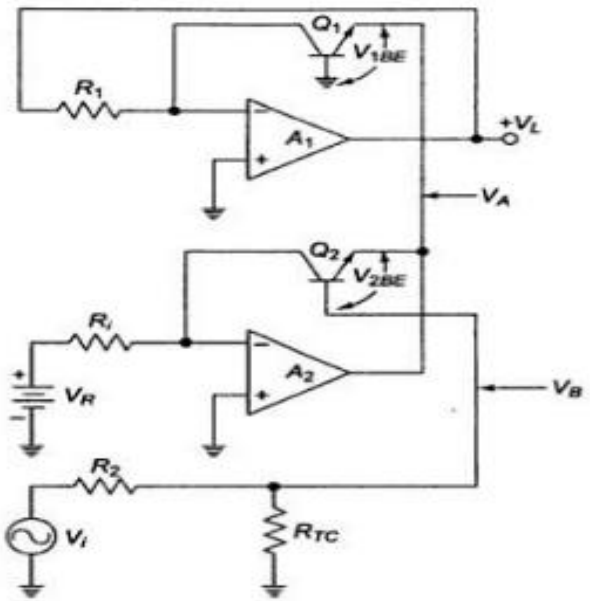


Fig 2.32 Antilog amplifier

$V_{1BE} = \frac{kT}{q} \ln[\frac{V_L}{R_1 I_S}]$ and $V_{2BE} = \frac{kT}{q} \ln[\frac{V_B}{R_1 I_S}]$ and $V_A = -V_{1BE}$ and $V_B = R_{TC}/(R_2+R_{TC})\ V_i$

$V_{Q2E} = V_B + V_{2BE} = R_{TC}/(R_2+R_{TC})\ V_i - \frac{kT}{q} \ln[\frac{V_B}{R_1 I_S}]$

$V_{Q2E} = V_A$

Therefore,

$$-\frac{kT}{q} ln\left(\frac{V_L}{R_1 I_S}\right) = \frac{R_{TC}}{R_2 + R_{TC}} V_i + \frac{kT}{q} ln\left(\frac{V_R}{R_1 I_S}\right)$$

Rearranging, we get

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q} ln\left(\frac{V_L}{R_1 I_S}\right) - \frac{kT}{q} ln\left(\frac{V_R}{R_1 I_S}\right)$$

$$= -\frac{kT}{q} ln\left(\frac{V_L}{V_R}\right)$$

We know that $\log_{10} x = 0.4343 \ln x$.

Therefore, $$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = 0.4343 \ln\left(\frac{V_L}{V_R}\right)$$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = \log_{10}\left(\frac{V_L}{V_R}\right)$$

$$-KV_i = \log\left(\frac{V_L}{V_R}\right)$$

$$K = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

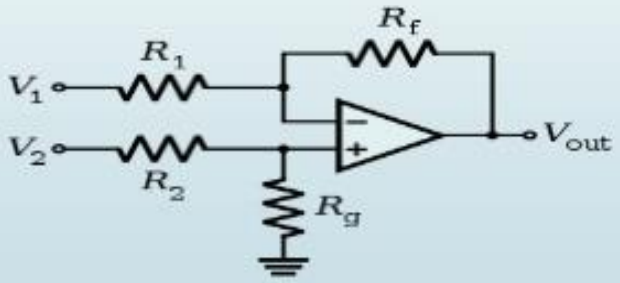
$$V_L = V_R 10^{-KV_i}$$

- The output Vo of the antilog- amp is fed back to the inverting input of A1 through the resistor R1. Hence an increase of input by one volt causes the output to decrease by a decade.

DIFFERENTIAL AMPLIFIER

What is differential amplifier?

- A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages . It is an analog circuit with two inputs and one output in which the output is ideally proportional to the difference between the two voltages.



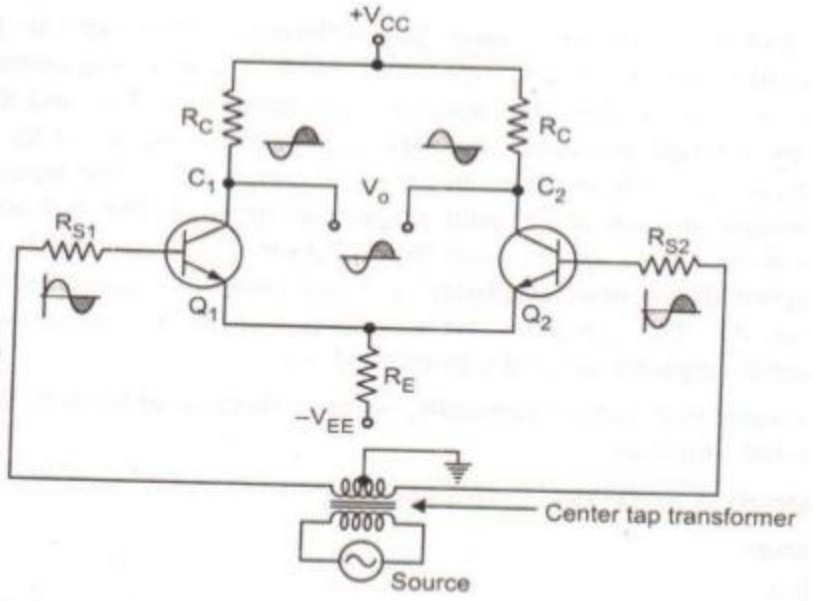
(A differential amplifier)

Modes of operation of Differential Amplifier (DA)

- There are two modes of operations of DA
  - **Differential mode**
  - **Common mode**
- **Differential mode:**
  - Two input signals are of **same magnitude** but **opposite polarity** are used (180^0 out of phase)
- **Common mode**
  - Two input signals are of **equal in magnitude** and **same phase** are used

Differential mode

- Assume sine wave on base of Q1 is +ve going signal while on the base of Q2 –ve going signal

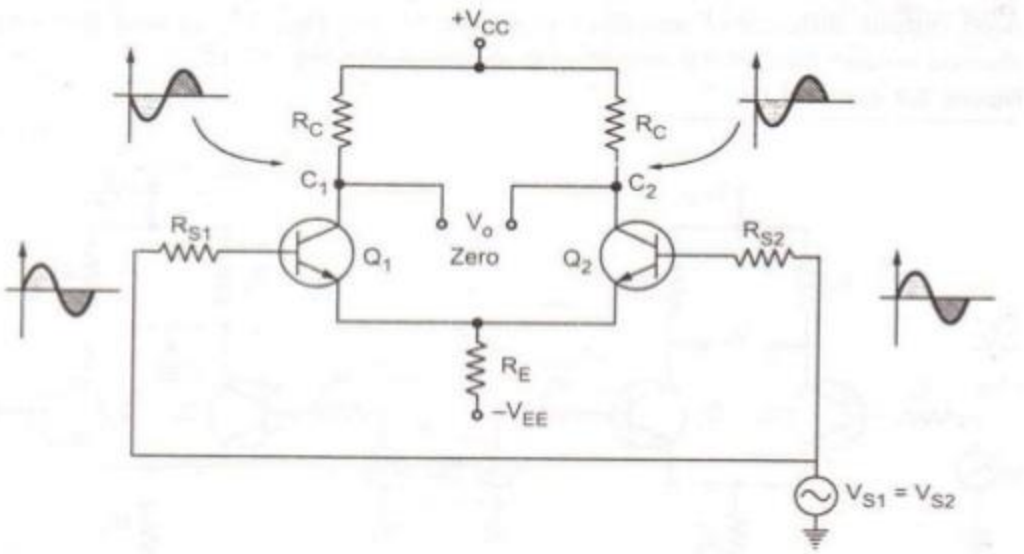


- An amplified –ve going signal will appear at collector of Q1
- An amplified +ve going signal will appear at collector of Q2
- Due to +ve going signal of base of Q1, current increases in R_E & hence a +ve going wave is developed across R_E
- Due to -ve going signal of base of Q2, -ve going wave is developed across R_E because of emitter follower action of Q2

- So, signal voltages across R_E, due to effect of Q1 &Q2 are equal in magnitude &180^0 out of phase- due to matched transistors
- Hence the two signals cancel each other & there is no signal across R_E
- No AC signal flows thro it
- V_o= +10-(-10)= 20
- V_o is difference voltage in two signals

Common Mode Operation

- Two input signals are of equal in magnitude and same phase are used
- In phase signal develops in phase signal voltages across R_E



- Hence R_E carries a signal current & provides **-ve feedback**
- This –ve f/b decreases AC
- In signal voltages of equal magnitude will appear across two collectors of Q1 &Q2
- Vo= 10-10=0 Negligibly small
- Ideally it should be zero

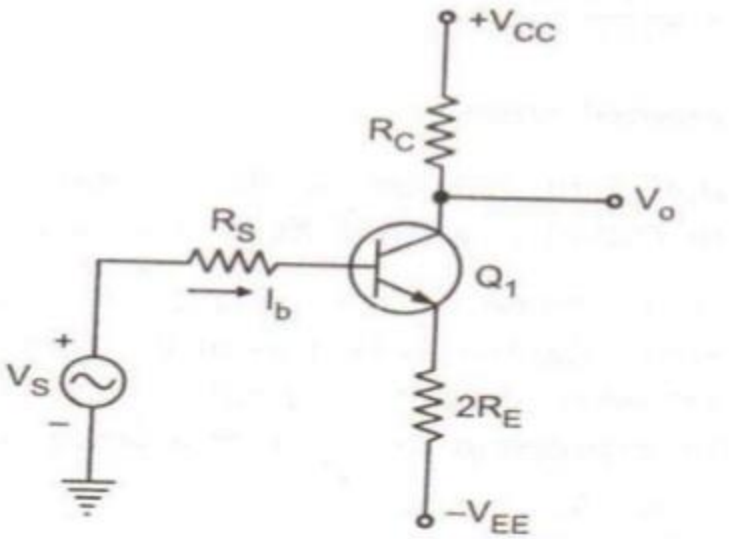
Analysis of evaluating 'A_c'

- To evaluate $\mathbf{A_c}$ we set $\mathbf{V_{S1}=V_{S2}=Vs}$
- On bisecting the Diff. amp. Ckt., we get the equivalent ckt. As shown in Fig. below
- It is nothing but **CE amplifier with un bypassed emitter resistor $\mathbf{2R_E}$**
- For calculation of $\mathbf{A_c}$ we assume that, $\mathbf{2R_E}$ connected in parallel

  ie $\mathbf{2R_E\ 2R_E / 2R_E + 2R_E = R_E}$

- Hybrid parameters equations are taken directly for **CE amplifier with un bypassed emitter resistor but value of emitter resistor can taken as "$2R_E$"**
- $A_I = (h_{oe} R_E - h_{fe}) / (1 + h_{oe}(R_C + R_E))$

  $= (h_{oe} (2R_E) - h_{fe}) / (1 + h_{oe}(R_C + 2R_E))$



- $R_i = (1 - A_I)R_E + h_{ie} + h_{re} A_I R_L$

  $= (1 - A_I)\, 2R_E + h_{ie} + h_{re} A_I R_L$

  Where $R_L = R_C + (A_I - 1/A_I)R_E$

  $R_L = R_C + (A_I - 1/A_I)\, 2R_E$

- **$A_C = A_I$ Rc/ Ri+Rs** (Since $A_V = (A_I$ Rc)/Ri)
- In Ri expression neglecting the term **hre A_I R_L** and substitute A_I and Ri we get,

A_C =((2hoe R_E - hfe)Rc)/(2 R_E(1+ hfe)+(Rs+hie)(2hoe R_E +1))

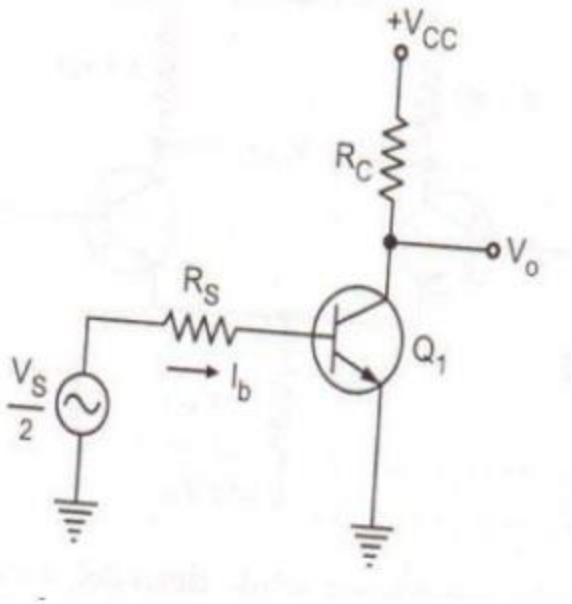
Provided that **hoe Rc<<1**

- If we use approximate model we get simpler expression
- **A_C = - hfe Rc/Rs+hie+ (1+hfe)2R_E**

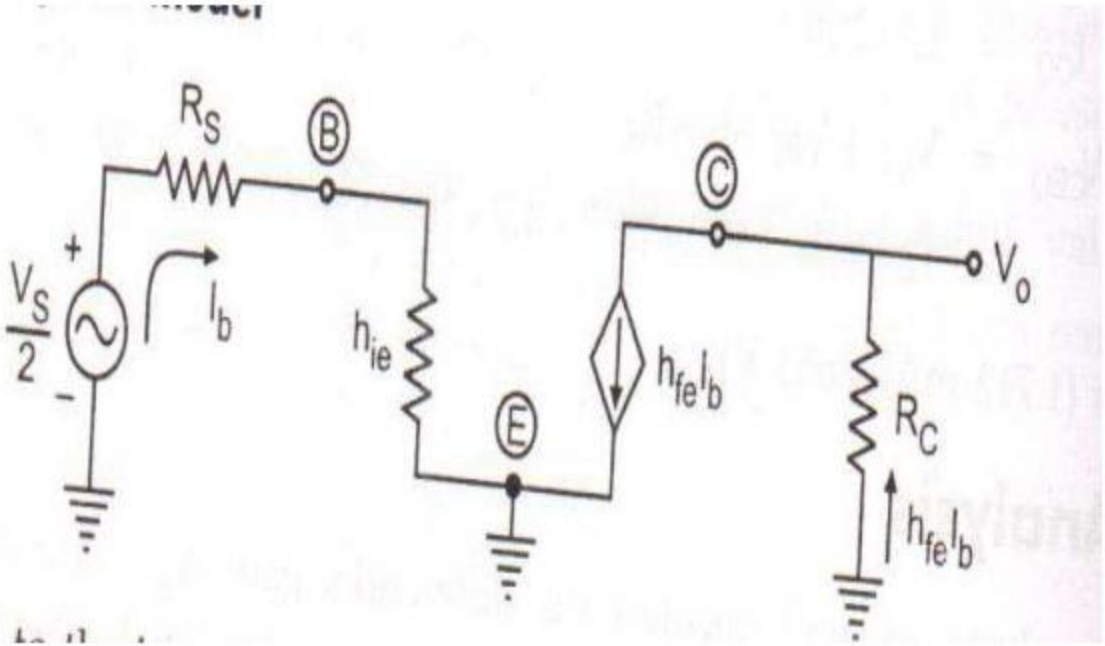
Evaluating 'A_d'

- We set $V_{S1} = -V_{S2} = Vs/2$
- ie magnitude of AC I/P voltages is set as above
- $I_{e1} = -I_{e2}$, $I_o = 0$ (They cancel each other to get resultant ac current thro R_E as I_0=o)
- **Hence for ac analysis emitter terminal can be grounded**
- Bisecting the ckt with $R_E = 0$
- We get equi. Ckt which is conventional **CE amplifier**

- Ac small signal Diff.Amp. ckt with grounded emitter is shown here
- As two trs. are matched ac equi. Ckt of the other Ckt is identical



- Approximate hybrid model for the above ckt is shown here



Applying KVL to the input loop,

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \qquad (1)$$

$$\therefore -I_b (R_S + h_{ie}) = -\frac{V_S}{2}$$

$$\therefore I_b = \frac{V_S}{2(R_S + h_{ie})} \qquad (2)$$

Applying KVL to the output loop,

$$V_o = -h_{fe} I_b R_C \qquad (3)$$

Substituting (2) in (3),

$$V_o = -h_{fe} R_C \frac{V_S}{2(R_S + h_{ie})}$$

- -ve sign indicates phase difference between I/P &O/P

$$\frac{V_o}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})}$$

- Here Vs difference I/P
- Mod of Ad is

$$A_d = \frac{V_o}{V_S} = \frac{h_{fe} R_C}{2(R_S + h_{ie})}$$

- CMRR is = $\left|\frac{Ad}{Ac}\right|$

Method of improving CMRR

Effect of R_E:

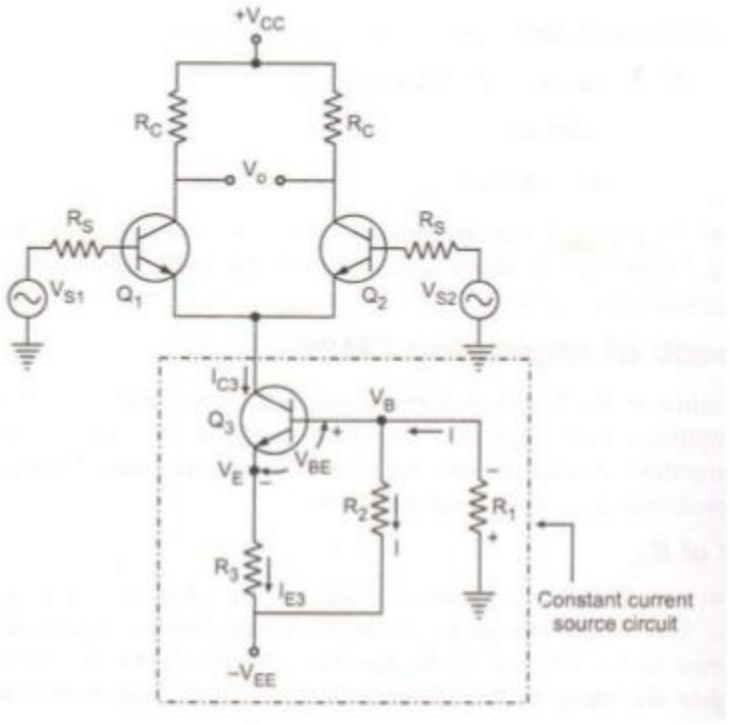
- To improve CMRR, '**Ac**' must be reduced
- "Ac" approaches **zero** as **R_E tends to infinite**
- Because R_E introduces –ve feedback which reduces 'Ac'
- **Higher value of R_E**, lesser the Ac, **higher the value of CMRR**
- 'Ad' is independent of R_E

- But practically R_E cannot be selected very high due to some limitations
  - **Large R_E needs higher biasing voltage to set Q-pt**
  - (Under Dc cond $Ic=\beta I_B$ but $I_E=I_C$ $I_B=I_E/\beta$
  - I_E depends on β
  - To make Q-pt stable I_E should be constant irrespective of β
  - For constant I_E emitter R should be very large this increases CMRR,)
  - **Increases overall chip area**

- So various methods are used which provide increased effect of R_E without any limitations
  1. **Constant current bias method**
  2. **Use of current mirror method**
- Another method to improve “Ad” to increase CMRR is **Active load**

Differential Amplifier with constant current circuit

- Here **R_E** is replaced by **constant current source circuit**
- It provides increased effect of R_E without physically increasing value of R_E



- R1, R2, R3 are selected to give the same operating point for Q1&Q2
- Let current thro **R3** is $\mathbf{I_{E3}}$ and Current **R1** is "**I**"
- Neglect base current(Because of large β)
- Assume current thro **R2** is also "I"

Applying Kirchhoff's law,

$$-IR_1 - IR_2 + V_{EE} = 0$$

$$\therefore I = \frac{V_{EE}}{R_1 + R_2} \quad \ldots(1)$$

Now $V_B = -IR_1$

Negative sign according to the direction of current .

$$\therefore V_B = -\frac{V_{EE}\, R_1}{R_1 + R_2} \quad \ldots(2)$$

Now $V_E = V_B - V_{BE}$

and $$I_{E3} = \frac{V_E - (-V_{EE})}{R_3} \quad \ldots(3)$$

Substituting expressions for V_B and V_E,

$$\therefore I_{E3} = \frac{\dfrac{-V_{EE}\, R_1}{R_1 + R_2} - V_{BE} + V_{EE}}{R_3}$$

$$\therefore I_{E3} = \frac{V_{EE}\left[\dfrac{R_2}{R_1 + R_2}\right] - V_{BE}}{R_3} \quad \ldots(4)$$

Neglecting I_{B3} we can write

$$I_{C3} = I_{E3}$$

- Thus as **V_{EE}, R1, R2, R3 & V_{BE} are constant**, Current **I_{C3} is almost equal to I_{E3}** and also constant.
- Thus ckt with Tr **Q3 acts as a constant current source.**
- **Internal Resistance of a cont. current source is very high, ideally infinite**

- Hence this ckt makes **the value of R_E ideally infinite which reduces Ac ideally to zero**

Common Mode Rejection Ratio (CMRR):

- It can be defined as the ratio of the differential
- gain AD to the common mode gain Acm, that is
- CMRR = Ad/Acm
- – It is a measure of the degree of matching between two input terminals, that is, the larger the value of CMRR, the better is the matching between the two input terminals and the smaller is the output common mode voltage Vocm.

THANK YOU

UNIT-2 APPLICATIONS OF OPAMPS

Prepared by

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Comparator

- A comparator is a circuit which compares a
- signal voltage applied at one input of an
- op-amp with a known reference voltage at the
- other input.

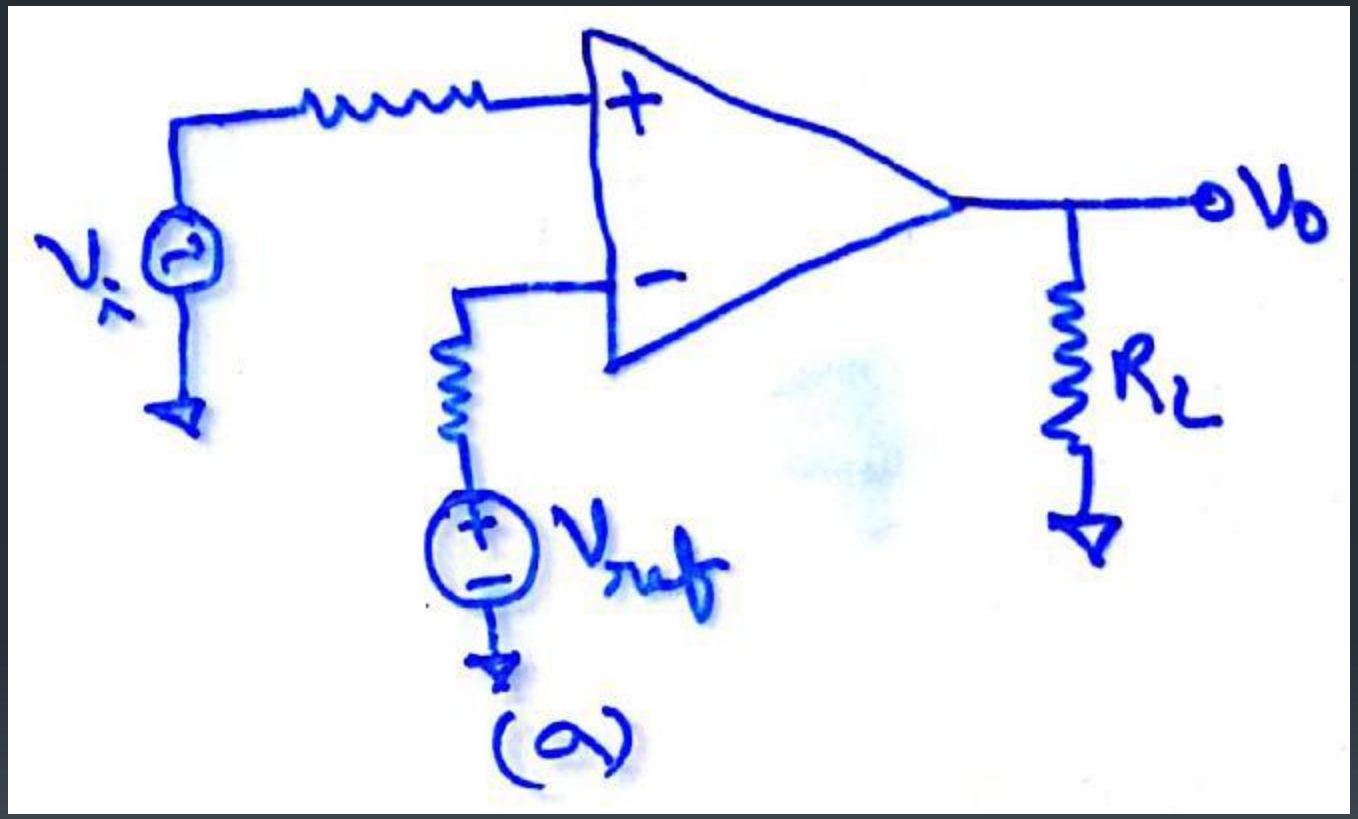
There are basically two types of comparators.

- 1. Non-inverting comparator
- 2. Inverting comparator

Non-Inverting Comparator:

- The circuit of figure 5.2a is called a non-inverting
- comparator.
- • A fixed reference voltage Vref is applied to
- – input and a time varying signal Vi is applied to
- +input.
- • There are 3 conditions for a comparator. They are
- Vi < Vref Vo = -Vsat
- Vi > Vref Vo = +Vsat
- Vi = Vref changes the state of op-amp

- The output waveform for a sinusoidal input
- signal applied to the +ve input is shown in
- figure 5.2 (b) and (c) for +ve and –ve Vref
- respectively.


+
−
V_o
V_i
R_L
V_{ref}
(a)

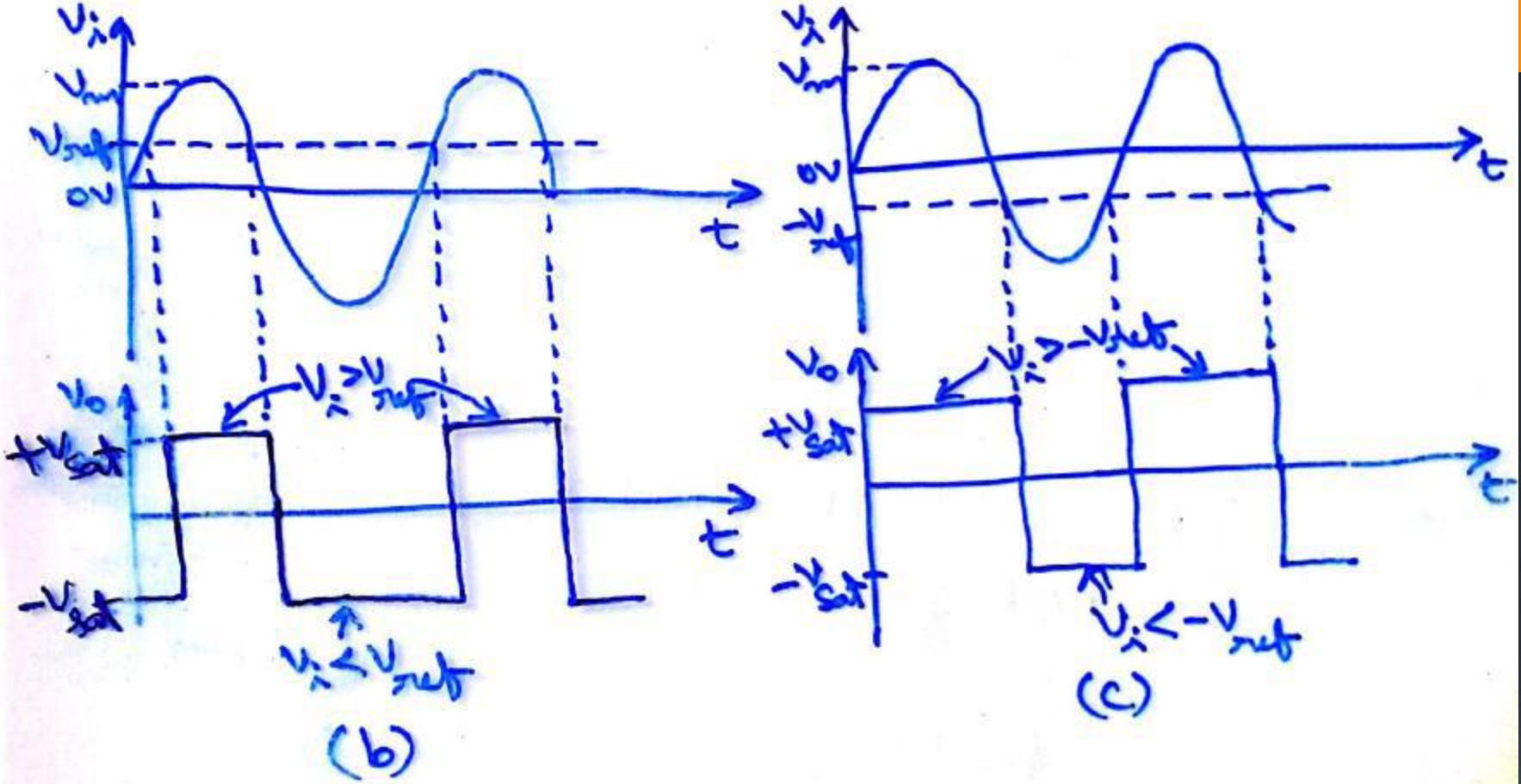
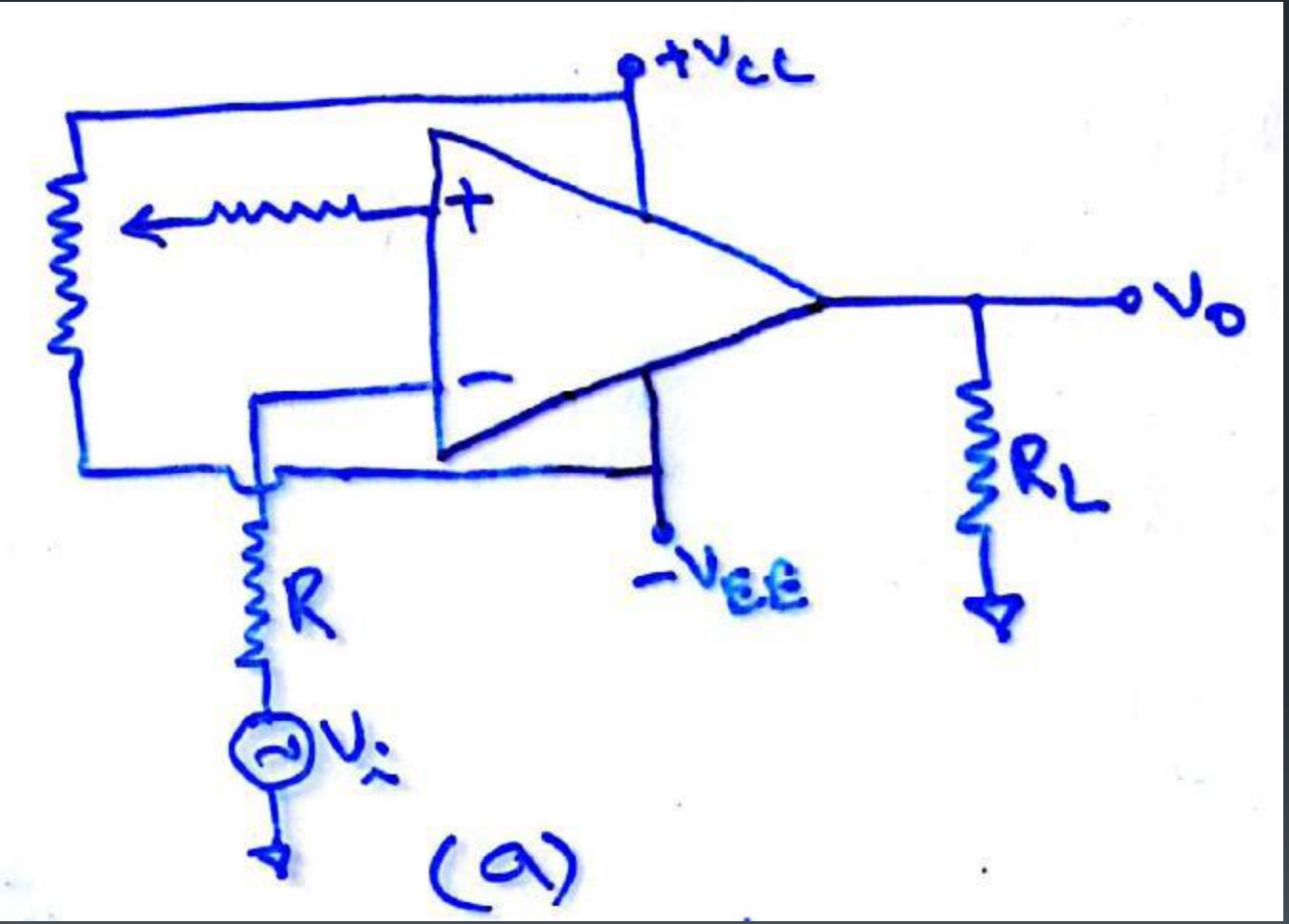


Fig 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} +ve (c) V_{ref} -ve

Inverting Comparator:

- Figure 5.3(a) shows a practical inverting
- comparator in which the reference voltage
- Vref is applied to the +input and Vi is applied
- to the –ve input.
- • For a sinusoidal input signal, the output
- waveform is shown in in figure 5.3(b) and
- 5.3(c) for Vref +ve and –ve respectively.


+Vcc
+
−
Vo
RL
R
−VEE
Vi
(a)

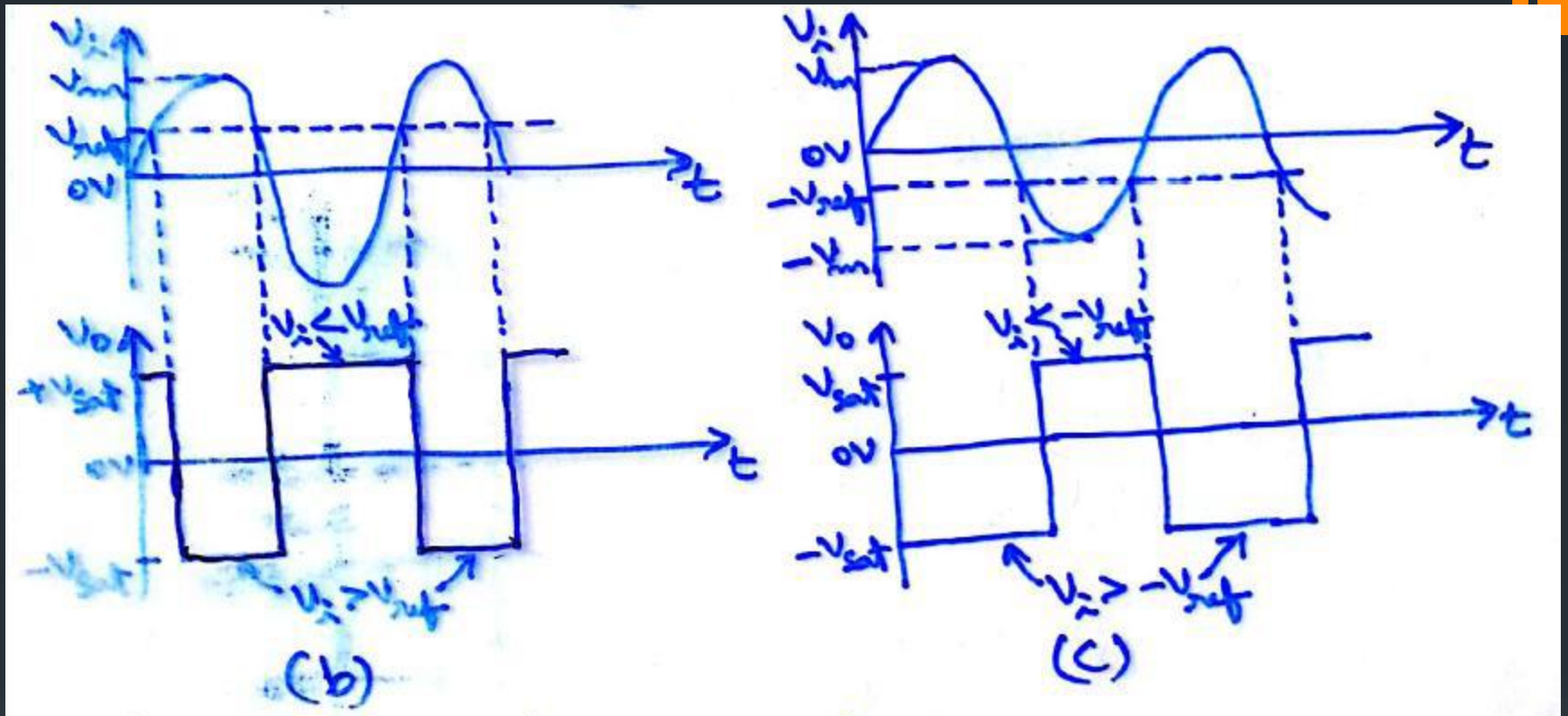
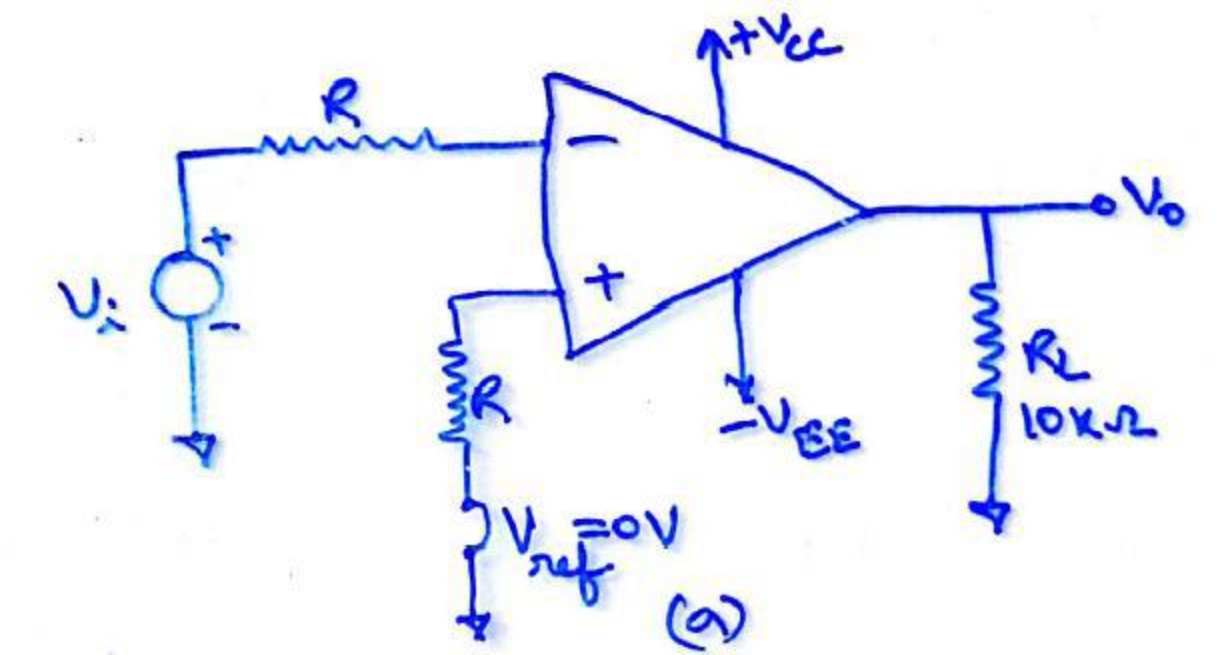


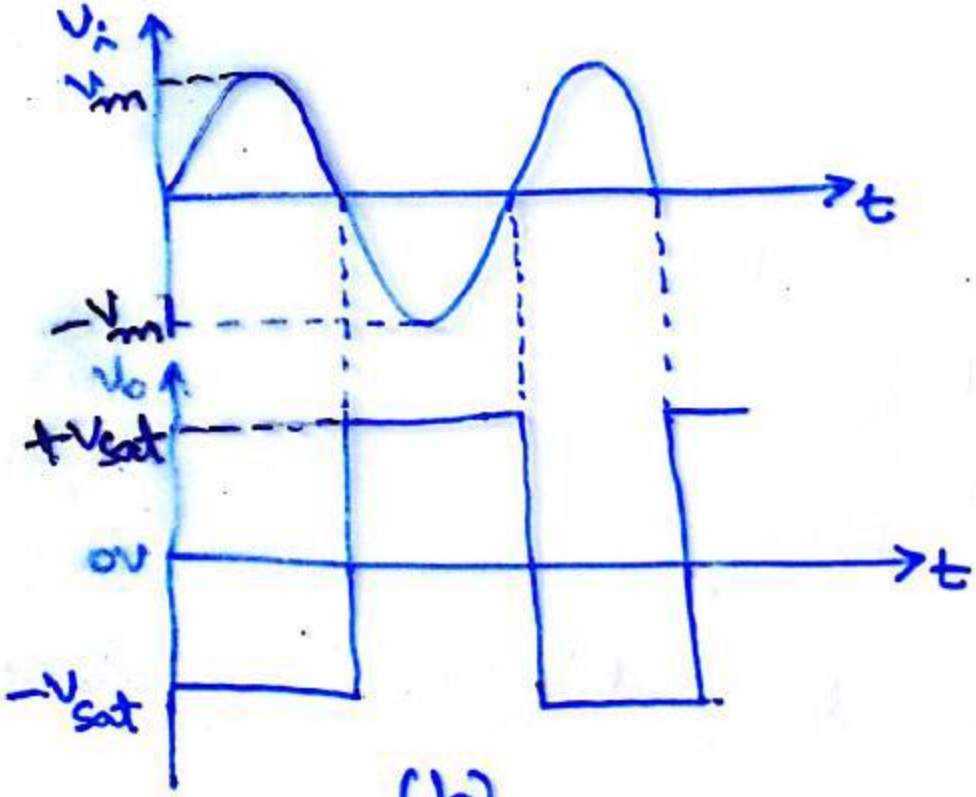
Fig 5.3(a) Inverting Comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$

Applications of Comparator

- Some important applications of comparator are
- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter.

Zero crossing detector





(b)

Fig 5.4 (a) Zero crossing detector (b) Input and o/p waveforms

- The basic comparators either non-inverting or
- inverting can be used as a zero crossing
- detector provided that Vref is set to zero. An
- inverting zero-crossing detector is shown in
- figure 5.4 (a).
- • The input and output waveforms are shown in
- Figure 5.4 (b).
- • The circuit is also called as a sine to square wave generator.

Regenerative comparator (Schmitt trigger)

- If positive feedback is added to the
- comparator circuit, gain can be increased
- greatly.
- Figure 5.8 (a) shows a regenerative
- comparator. The circuit is also known as
- Schmitt trigger

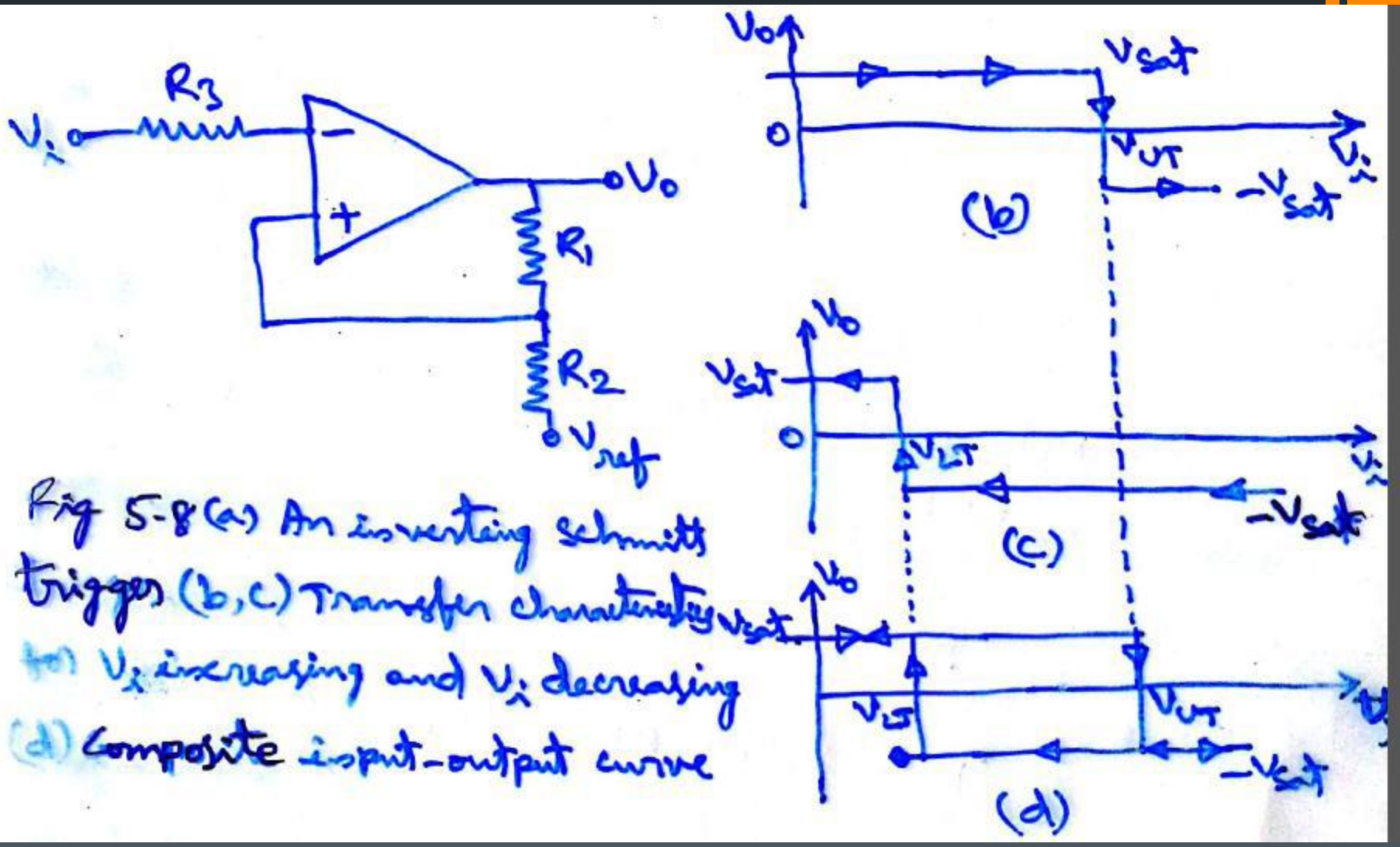


Fig 5-8 (a) An inverting Schmitt trigger (b,c) Transfer characteristics for V_i increasing and V_i decreasing (d) Composite input-output curve

- The input voltage Vi triggers the output Vo every
- time it crosses certain voltage levels. These
- voltage levels are called Upper threshold voltage
- (Vut) and Lower threshold voltage (Vlt).
- • The hysteresis width is the difference between
- these two threshold voltages ie Vut – Vlt. These
- threshold voltages are calculated as follows.
- • Suppose that the output voltage Vo is +Vsat. The
- voltage at +ve input terminal will be
- Vref + (R2/(R1+R2)) (Vsat – Vref) = Vut

- This voltage is called as Upper threshold voltage Vut
- • As long as Vi is less than Vut, the output Vo remains
- constant at +Vsat. When Vi is just greater than Vut, the
- output regeneratively switches to – Vsat and remains
- at this level as long as Vi > Vut as shown in Figure 5.8
- (b).
- • For Vo = -Vsat, the voltage at +ve input terminal is
- Vref + (R2/R1+R2) (-Vsat – Vref) = Vlt
- Vref - (R2/R1+R2) (Vsat + Vref) = Vlt
- this voltage is referred to as lower threshold voltage Vlt

- The input voltage Vi must become lesser than Vlt
- in order to cause Vo to switch from –Vsat to
- +Vsat. A regenerative transition takes place as
- shown in Figure 5.8(c) and the output Vo returns
- from –Vsat to +Vsat almost instantaneously.
- • The complete transfer characteristics are shown
- in Figure 5.8 (d).
- • Note that Vlt < Vut and the difference between
- these two voltages is the hysteresis width Vh and
- can be written as
- Vh = Vut – Vlt = 2R2 Vsat/(R1+R2)

- The resistor R3 in figure 5.8(a) is chosen equal
- to R1||R2 to compensate for the input bias
- current.
- • A non-inverting Schmitt trigger is obtained if
- Vi and Vref are interchanged in figure 5.8(a).

Wave form Generators

- There are different types of wave form
- generators which are given below.
- 1 Square wave generator
- 2 Triangular wave generator
- 3 Saw tooth wave generator
- **Square wave Generator (Astable Multivibrator)**
- A simple op-amp square wave generator is
- shown in Figure 5.10a.

Square wave generator

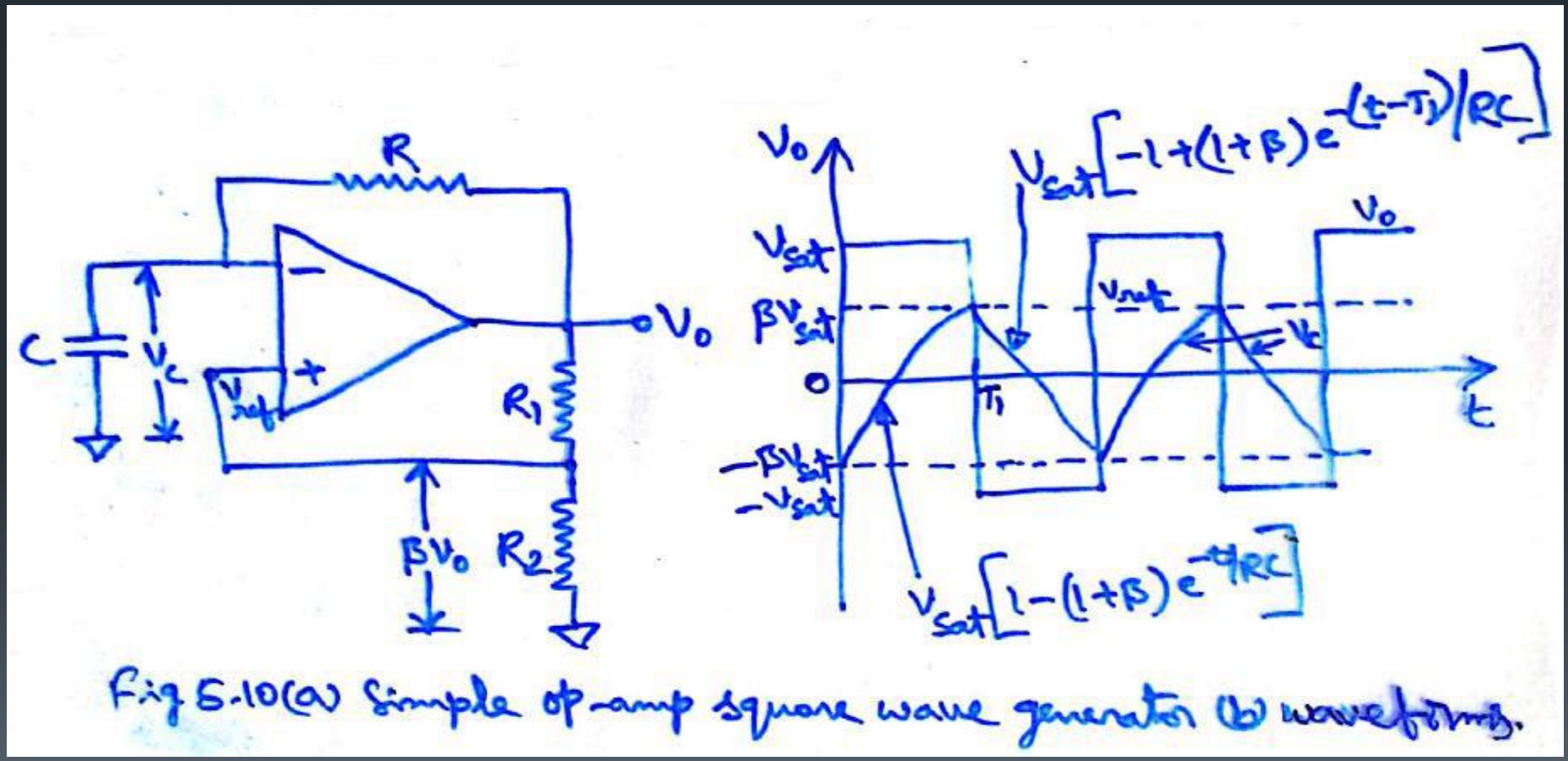


Fig 5.10(a) Simple op-amp square wave generator (b) waveforms.

- It is also called a Free running oscillator.
- • The principle of generation of square wave
- output is to force an op-amp to operate in
- saturation region.
- • In Figure 5.10(a), fraction β = R2/(R1+R2) of
- the output is fed back to the +ve input
- terminal. Thus the reference voltage Vref is
- βVo and may take values as +βVsat or – βVsat.

- The output is also fed back to the –ve input
- terminal after integrating by means of a low
- pass RC combination.
- • Whenever input at the –ve input terminal just
- exceeds Vref, switching takes place resulting in
- a square wave output.
- • In Astable multivibrator, both the states are
- quasi stable.

- **Frequency Derivation**
- The frequency is determined by the time it takes the capacitor
- to charge from –βVsat to + βVsat and vice versa.
- The voltage across the capacitor as a function of time is given
- by
- $Vc(t) = Vf + (Vi – Vf)\ e^{-t/RC}$
- where, the final value, $Vf = +Vsat$
- and the initial value, $Vi = –\beta Vsat$
- Therefore $Vc(t) = +Vsat + (–\beta Vsat – Vsat)\ e^{-t/RC}$
- $Vc(t) = Vsat – Vsat(1+\beta)\ e^{-t/RC}$
- At t = T1, voltage across the capacitor reaches βVsat and
- switching takes place.

- Therefore
- Vc(T1) = βVsat = Vsat – Vsat(1+ β) e^-T1/RC
- After algebraic manipulation, we get
- T1 = RC In (1+ β)/(1- β)
- This gives only one half of the period.
- Therefore the total time period, T
- =2*T1 = 2RC In (1+ β)/(1- β) and the output waveform
- is symmetrical.
- If R1 = R2, then β = 0.5 and T = 2RC In 3 and
- for R1=1.16 R2, it can be seen that
- T = 2RC or fo = 1/2RC

Triangular Wave Generator

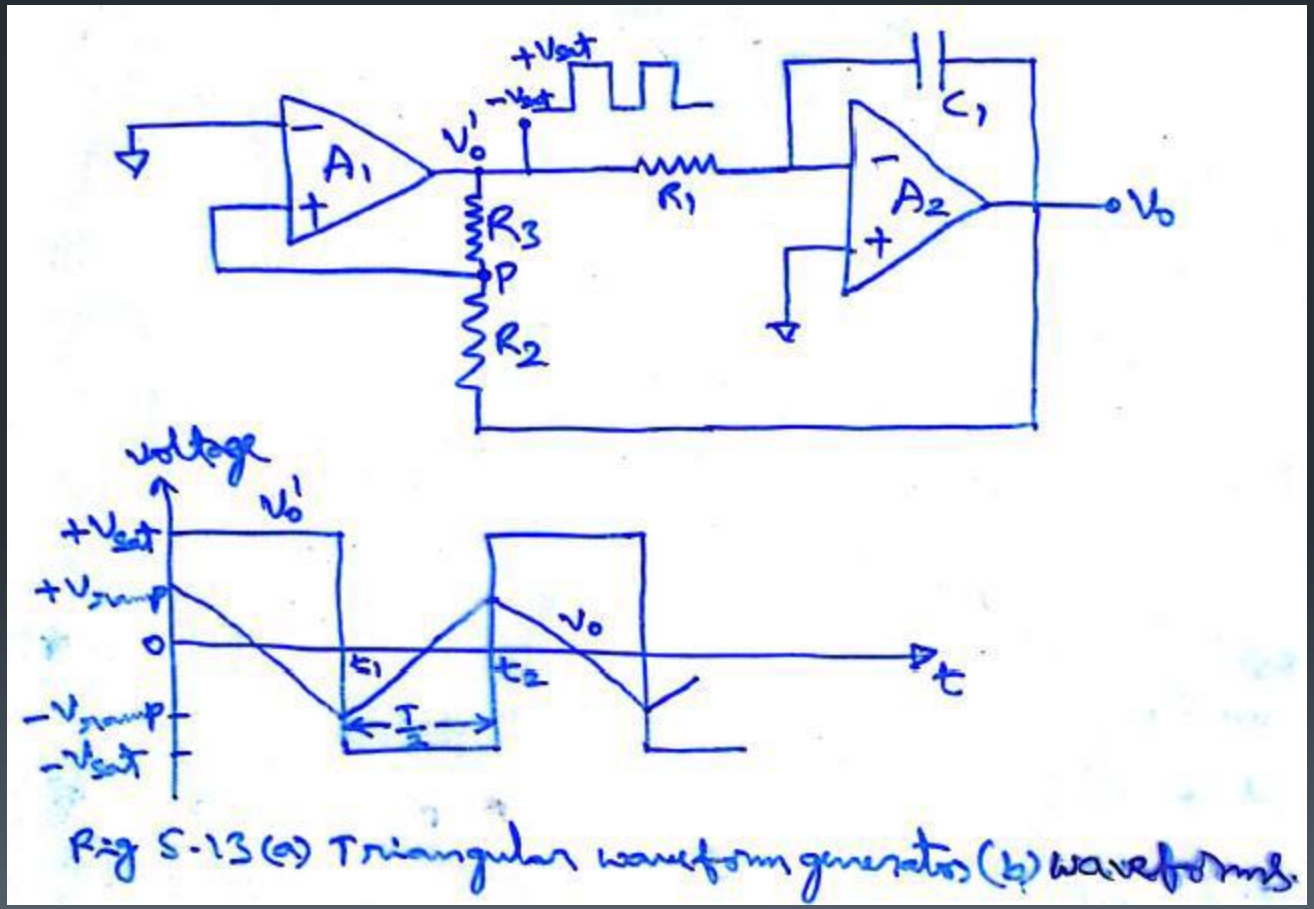


Fig 5-13 (a) Triangular waveform generator (b) waveforms.

- It basically consists of a two level comparator
- followed by an integrator.
- • The output of the comparator A1 is a square
- wave of amplitude + or – Vsat and is applied
- to the –ve input terminal of the integrator A2
- producing a triangular wave. This triangular
- wave is fed back as input to the comparator
- A1 through a voltage divider R2R3.

- Initially, let us consider that the output of the
- comparator A1 is at +Vsat. The output of the
- integrator A2 will be a –ve going ramp as shown
- in figure 5.13b. This one end of the voltage
- divider R2R3 is at a voltage +Vsat and the other at
- the –ve going ramp of A2.
- • At a time t=t1, when the –ve going ramp attains a
- value of –Vramp, the effective voltage at point p
- becomes slightly less than 0 volts. This switches
- the output of A1, from positive saturation level to
- negative saturation level – Vsat.

- During the time when the output of A1 is at -Vsat,
- the output of A2 increases in the positive direction.
- • And at the instant t=t2, the voltage at point p becomes
- just above 0 volts, thereby switching the output of A1
- from –Vsat to +Vsat. The cycle repeats and generates a
- triangular waveform.
- • It can be seen that the frequency of the square wave
- and triangular wave will be the same.
- • However, the amplitude of the triangular wave
- depends upon the RC value of the integrator A2 and
- output voltage level of A1.

- **Derivation of Frequency of Triangular Waveform**
- • The effective voltage at point p during the time
- when output of A1 is at +Vsat level is given by
- -Vramp+(R2/(R2+R3)) [+Vsat – (-Vramp)] -- Eq(1)
- At t=t1, the voltage at point p becomes
- approximately equal to zero. Therefore from
- Eq(1), we get -Vramp = (-R2/R3) (+Vsat)
- Similarly at t=t2, when the output of A1 switches
- from –Vsat to +Vsat
- Vramp = (-R2/R3) (-Vsat) = (R2/R3) Vsat

- Therefore peak to peak amplitude of the triangular wave is
- Vo (pp) = +Vramp – (-Vramp)
- Vo (pp) = 2 Vramp = 2 (R2/R3) Vsat ---- Eq(2)
- The output switches from –Vramp to +Vramp in half the time
- period T/2.
- Putting the values in the basic integrator equation Vo = -
- (1/RC) ∫Vi dt, we get
- Vo(pp)=-(1/R1C1) 0∫T/2 (-Vsat)dt =(Vsat/R1C1) (T/2)
- Therefore T=2 R1C1 Vo(pp)/Vsat
- Putting the value of Vo(pp) from Eq(2), we get
- T = 4R1 C1 R2/R3
- Hence the frequency of oscillation fo is
- fo = 1/T = R3/4 R1 C1 R2

Sawtooth Wave Generator

- The difference between the triangular and
- sawtooth waveforms is that
- rise time and fall time are equal – Triangular
- rise time and fall time are unequal – Sawtooth
- • The triangular wave generator can be converted
- into a sawtooth wave generator by injecting a
- variable DC voltage into the non-inverting
- terminal of the integrator A2.
- • This can be accomplished by using the
- potentiometer and connecting it to the +Vcc and
- -Vee as shown in Figure 8-24(a)

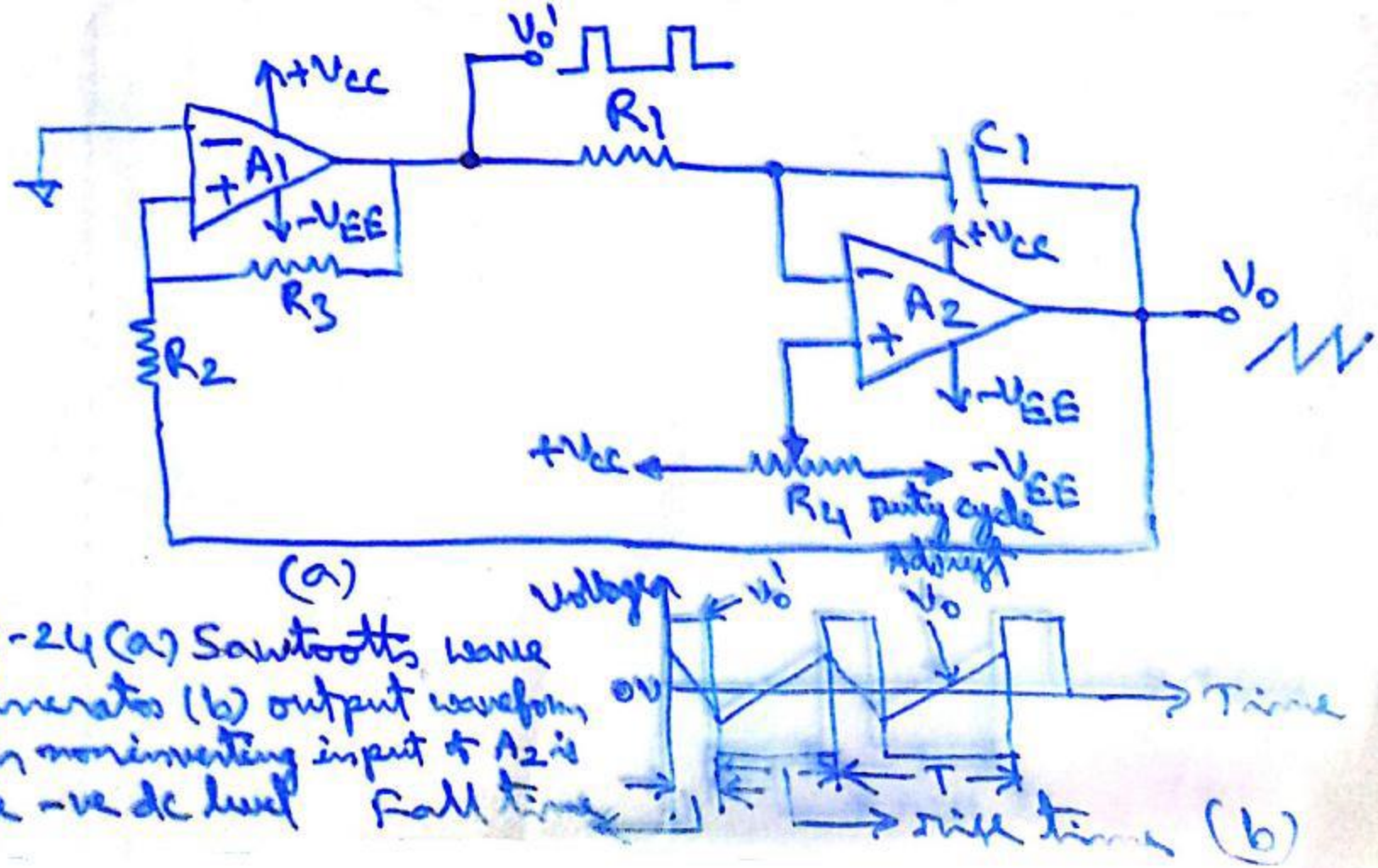


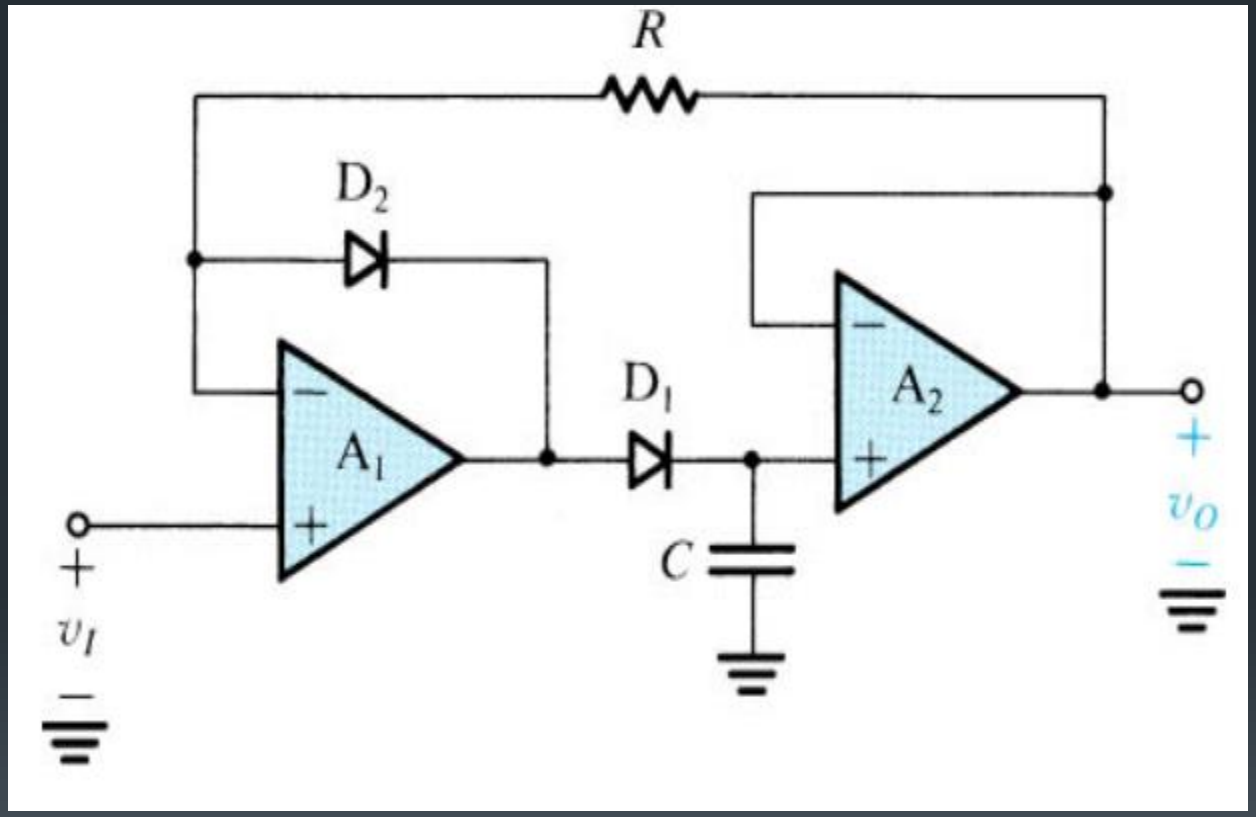
Fig 8-24 (a) Sawtooth wave generator (b) output waveform when noninverting input of A_2 is at some -ve dc level

- Depending on the R4 setting, a certain DC level is
- inserted in the output of A2.
- • Now suppose that the output of A1 is a square wave
- and the potentiometer R4 is adjusted for a certain DC
- level.
- • This means that the output of A2 will be a triangular
- wave, riding on some DC level that is a function of the
- R4 setting.
- • The duty cycle of the square wave will be determined
- by the polarity and amplitude of this DC level.
- • A duty cycle less than 50% will then cause the output
- of A2 to be a sawtooth.

- With the wiper at the center of R4, the output
- of A2 is a triangular wave. For any other
- position of R4 wiper, the output is a sawtooth
- waveform.
- R4 wiper is towards **–Vee**,the **rise time is more**
- R4 wiper is towards **+Vcc**,the **fall time is more**

Precision Peak Detector

- When the peak detector required to hold the value of the peak for a long time, the capacitor should be buffered. An op amp A 2, which should have high input impedance and low input bias current, is connected as a voltage follower.
- The rest of the circuit is similar to the half-wave rectifier. A Precision Clamping Circuit By replacing the diode in the usual clamping circuit with


R
D2
D1
A1
A2
C
+
vI
−
+
vO
−

Linear Oscillators

1. Wien Bridge Oscillators
2. RC Phase-Shift Oscillators
3. LC Oscillators
4. Stability

Wien Bridge Oscillator

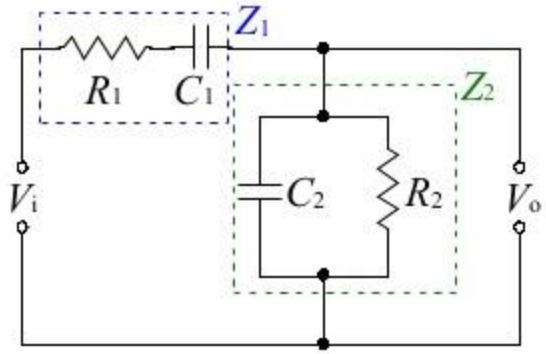
Let $X_{C1} = \frac{1}{\omega C_1}$ and $X_{C2} = \frac{1}{\omega C_2}$

$$Z_1 = R_1 - jX_{C1}$$

$$Z_2 = \left[\frac{1}{R_2} + \frac{1}{-jX_{C2}}\right]^{-1} = \frac{-jR_2X_{C2}}{R_2 - jX_{C2}}$$

Therefore, the feedback factor,

Frequency Selection Network



$$\beta = \frac{V_o}{V_i} = \frac{Z_2}{Z_1 + Z_2} = \frac{(-jR_2X_{C2}/R_2 - jX_{C2})}{(R_1 - jX_{C1}) + (-jR_2X_{C2}/R_2 - jX_{C2})}$$

$$\beta = \frac{-jR_2X_{C2}}{(R_1 - jX_{C1})(R_2 - jX_{C2}) - jR_2X_{C2}}$$

β can be rewritten as:

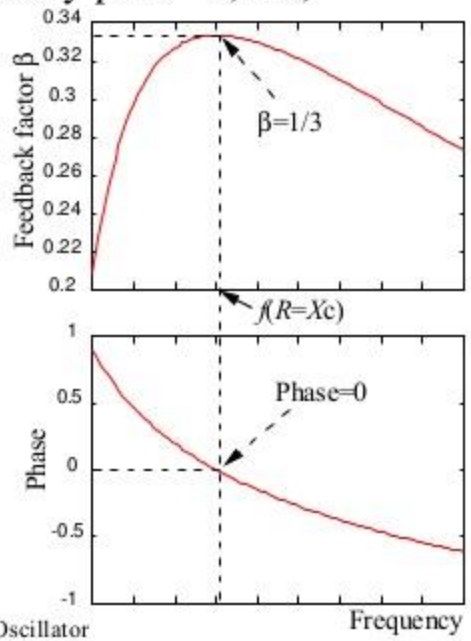
$$\beta = \frac{R_2 X_{C2}}{R_1 X_{C2} + R_2 X_{C1} + R_2 X_{C2} + j(R_1 R_2 - X_{C1} X_{C2})}$$

For ***Barkhausen Criterion***, imaginary part = 0, i.e.,

$$R_1 R_2 - X_{C1} X_{C2} = 0$$

$$\text{or} \quad R_1 R_2 = \frac{1}{\omega C_1} \frac{1}{\omega C_2}$$

$$\Rightarrow \omega = 1/\sqrt{R_1 R_2 C_1 C_2}$$



Supposing,

R_1=R_2=R and X_{C1}= X_{C2}=X_C,

$$\beta = \frac{RX_C}{3RX_C + j(R^2 - X_C^2)}$$

Example

By setting $\omega = \frac{1}{RC}$, we get

Imaginary part = 0 and $\beta = \frac{1}{3}$

Due to ***Barkhausen Criterion***,

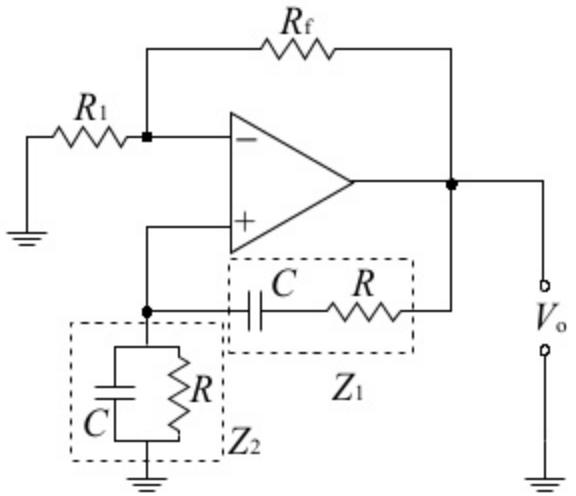
Loop gain $A_v\beta$=1

where

A_v : Gain of the amplifier

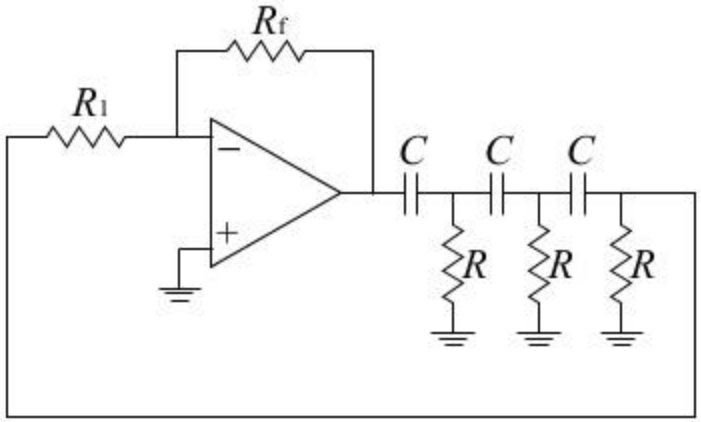
$$A_v\beta = 1 \Rightarrow A_v = 3 = 1 + \frac{R_f}{R_1}$$

Therefore, $\frac{R_f}{R_1} = 2$



Wien Bridge Oscillator

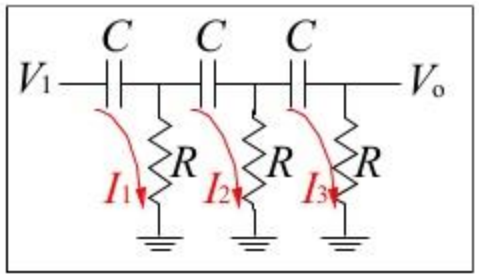
RC Phase-Shift Oscillator



- Using an inverting amplifier
- The additional 180° phase shift is provided by an RC phase-shift network

Applying KVL to the phase-shift network, we have

$$V_1 = I_1(R - jX_C) - I_2R$$
$$0 = -I_1R + I_2(2R - jX_C) - I_3R$$
$$0 = -I_2R + I_3(2R - jX_C)$$



Solve for I_3, we get

$$I_3 = \frac{\begin{vmatrix} R-jX_C & -R & V_1 \\ -R & 2R-jX_C & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} R-jX_C & -R & 0 \\ -R & 2R-jX_C & -R \\ 0 & -R & 2R-jX_C \end{vmatrix}}$$

Or
$$I_3 = \frac{V_1R^2}{(R-jX_C)[(2R-jX_C)^2 - R^2] - R^2(2R-jX_C)}$$

The output voltage,

$$V_o = I_3 R = \frac{V_1 R^3}{(R - jX_C)[(2R - jX_C)^2 - R^2] - R^2(2R - jX_C)}$$

Hence the transfer function of the phase-shift network is given by,

$$\beta = \frac{V_o}{V_1} = \frac{R^3}{(R^3 - 5RX_C^2) + j(X_C^3 - 6R^2 X_C)}$$

For 180° phase shift, the imaginary part = 0, i.e.,

$$X_C^3 - 6R^2 X_C = 0 \quad \text{or} \quad X_C = 0 \,(\text{Rejected})$$

$$\Rightarrow X_C^2 = 6R^2$$

$$\omega = \frac{1}{\sqrt{6}RC}$$

and,

$$\beta = -\frac{1}{29}$$

Note: The –ve sign mean the phase inversion from the voltage

- THANK YOU

UNIT-III
FILTERS

Prepared by
S.JAYACHITRA,AP/ECE

DEFINATION

A Filter is an electrical circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band.

It is a frequency selective circuit.

The filters are basically classified as active filters & passive filters.

They are used in circuits which require the separation of signals according to their frequencies.

They are widely use in communication & signal Processing.

GENERAL

- A Filter is an electrical circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band.
- It is a frequency selective circuit.
- The filters are basically classified as active filters & passive filters.
- They are used in circuits which require the separation of signals according to their frequencies.
- They are widely use in communication & signal processing.

ADVANTAGES OF ACTIVE FILTERS OVER PASSIVE FILTERS

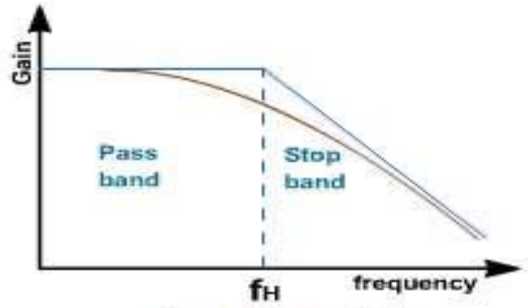
- All the elements alongwith op-amp can be used in the integrated form. Hence there is reduction in size & weight.
- The op-amp gain can be easily controlled in the closed loop fashion hence active filter I/P signals is not attenuated.
- The op-amp has high I/P impedance & low O/P impedance, hence the active filters using op-amp do not cause loading of the source or load.

LIMITATIONS OF ACTIVE FILTERS

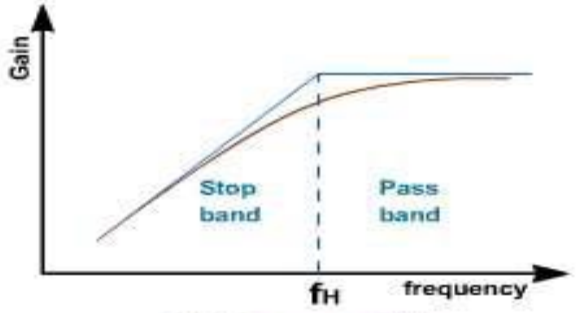
- The finite bandwidth of the active devices places a limit on the highest frequency of operation.
- A reasonably good filter performance can be achieved approximately upto 500 kHz,as against this passive filters can be used upto 500 MHz.
- The active elements are more sensitive to the temperature & environmental changes than the passive elements.
- The requirement of d.c power supply is another disadvantage of the active filters.

COMMONLY USED FILTERS

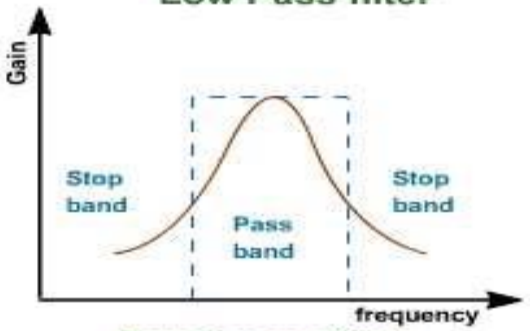
- The most commonly used filters are :-
- Low Pass Filter
- High Pass Filter
- Band Pass Filter
- Band Reject Filter
- All Pass Filter &
- Universal Filters.



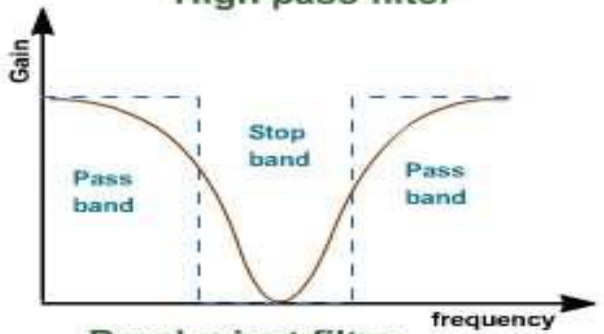
Low Pass filter



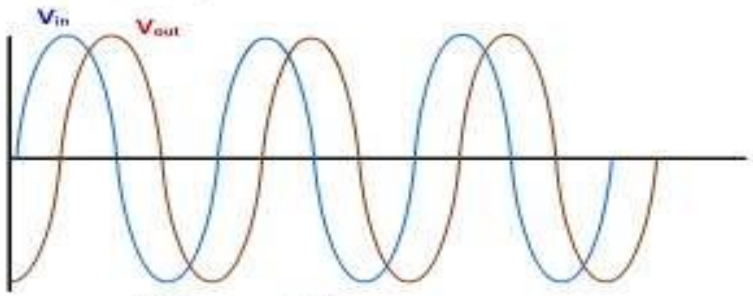
High pass filter



Band pass filter



Band reject filter



All pass filter

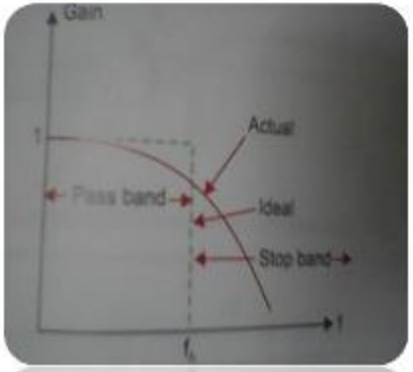
Phase shift between input and output of all pass filter

1- LOW PASS FITER

- A low-pass (LP) filter is a filter that passes low-frequency signals but attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency.
- A low-pass (LP) filter is the opposite of a high-pass (HP) filter.

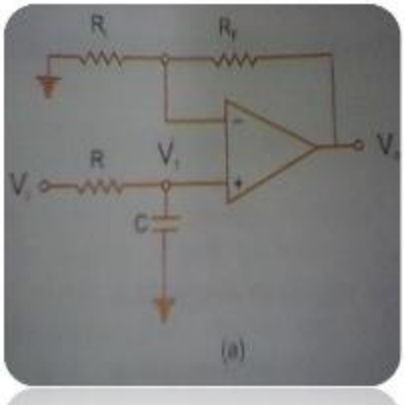
FREQUENCY RESPONSE OF LOW PASS FILTER
IDEAL & PRACTICAL RESPONSE

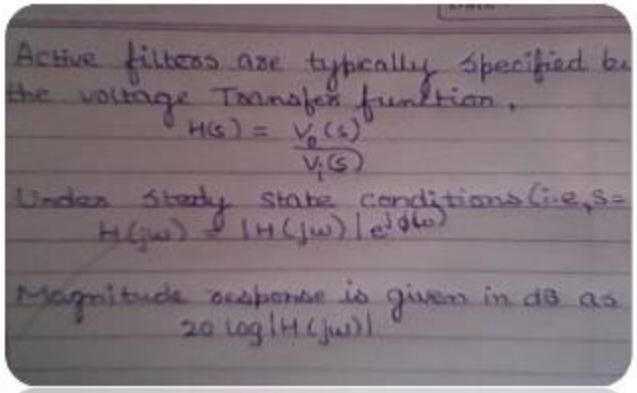
- A Low Pass Filter has a constant gain from 0 Hz to a high cut-off frequency, f_h.
- Practically, the gain decreases as the frequency increases & at $f = f_h$, the gain is down by 3 db & after f_h; it decreases at a higher rate.
- After the end of a transition band,
- the gain becomes zero.



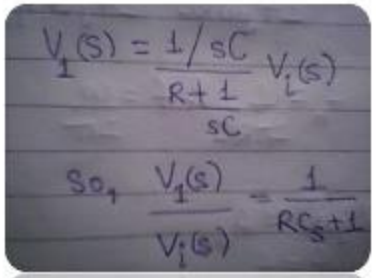
First Order LP Filter

- A first order filter consists of a single RC n/w connected to I / p terminal of a non-inverting op-amp.
- Resistors $\mathbf{R_1}$ & $\mathbf{R_f}$ determine the gain of the filter in the pass band.

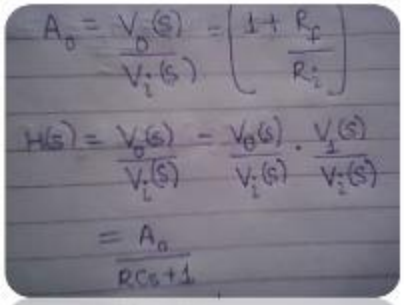




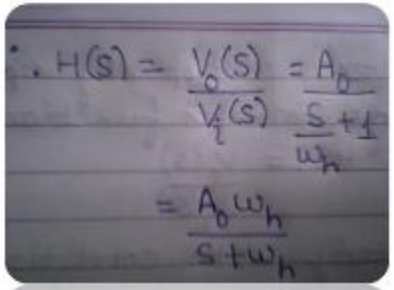
The voltage across the capacitor in the s-domain is:-



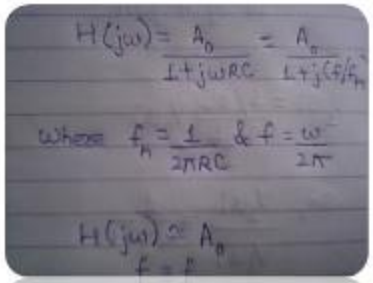
The closed loop gain of the op-amp is:-

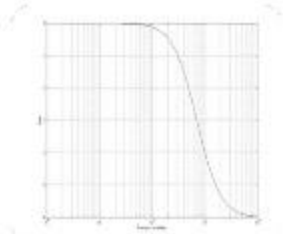


Let wh= 1/RC

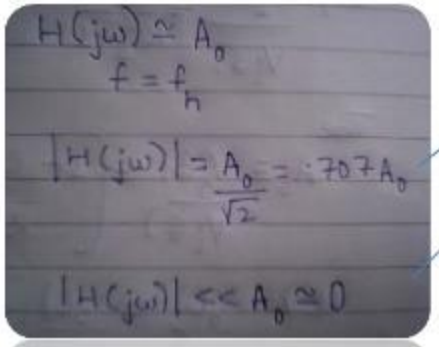


To determine the frequency response, put s=jw in above eq.





At very low frequency, i.e. f<<fh



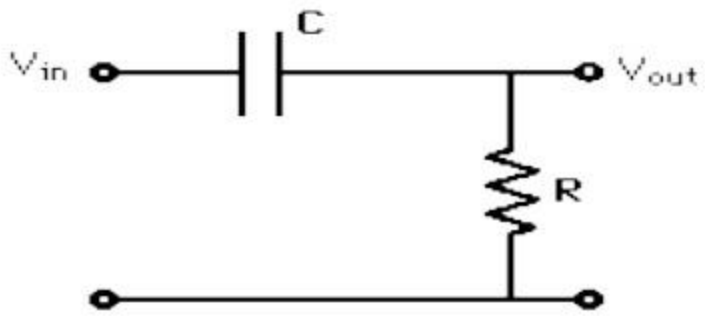
And At very High frequency i.e. f>>fh, we have

It has the max. gain at f=0 Hz. At fh the gain falls to . 707 time the max. gain.
Hence gain rolls off at the rate of 20 dB/decade.

2- A HIGH PASS FILTER

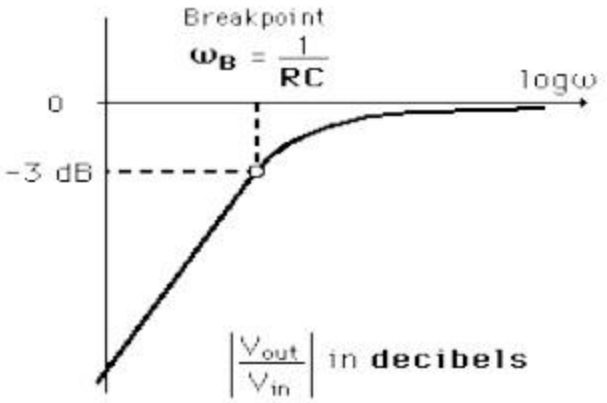
- A high-pass (HP) filter offers easy passage to high-frequency signal and attenuates the low-frequency signal.

A PASSIVE HIGH PASS FILTER:



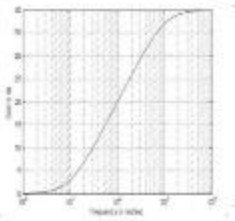
$$|V_{out}| = |V_{in}| \frac{\omega RC}{\sqrt{1 + \omega^2 R^2 C^2}}$$

Frequency response of 1st order HP Filter

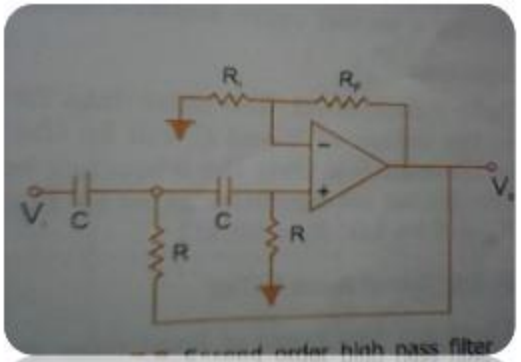


- The cutoff frequency for a high-pass filter is that frequency at which the output voltage equals 70.7% of the input voltage. Above the cutoff frequency, the output voltage is greater than 70.7% of the input, and vice versa.

2ND ORDER HP FILTER



High pass filter is the complement of the low pass filter & can be obtained simply by interchanging R & C in the low pass configuration as shown in the fig.



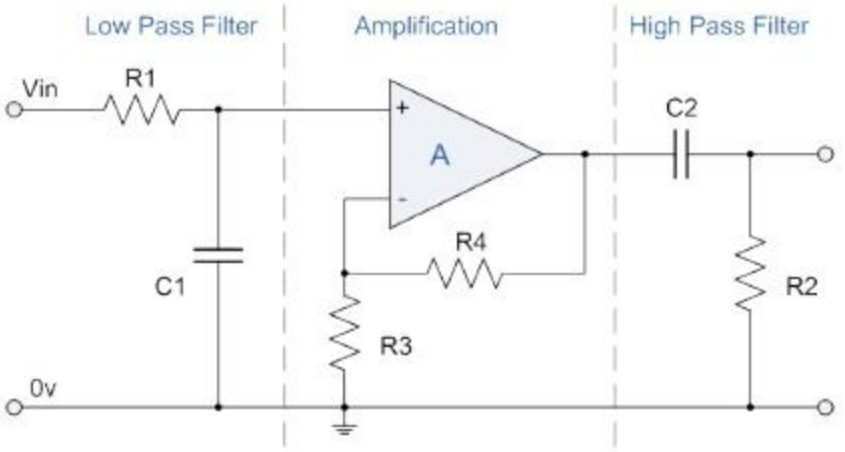
This is the transfer function:

$$H(s) = \frac{A_0 s^2}{s^2 + (3 - A_0)\omega_c s + \omega_c^2}$$

$$\omega_c = \frac{1}{RC}$$

3- BAND PASS FILTER

- The Band-Pass (BP) filter passes a selected range or band of frequencies that can be either narrow or wide while attenuating all those outside of this range.

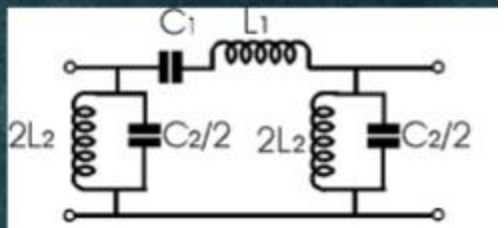


Band pass filter

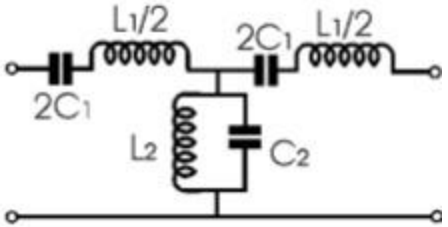
- A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range.
- These filters can also be created by combining a low-pass filter with a high-pass filter.
- The **bandwidth** of the filter is simply the difference between the upper and lower cutoff frequencies.
- **Q factor:-**
- A band-pass filter can be characterised by its Q factor. The Q-factor is the inverse of the fractional bandwidth. A high-Q filter will have a narrow passband and a low-Q filter will have a wide passband. These are respectively referred to as narrow-band and wide-band filters.

Band pass with LC components

- Like the high pass filters and the low pass filters, there are two topologies that are used for these filters, namely the Pi and the T configurations. Rather than having a single element in each leg of the filter as in the case of the low pass and high pass filters, the band pass filter has a resonant circuit in each leg. These resonant circuits are either series or parallel tuned LC circuits.



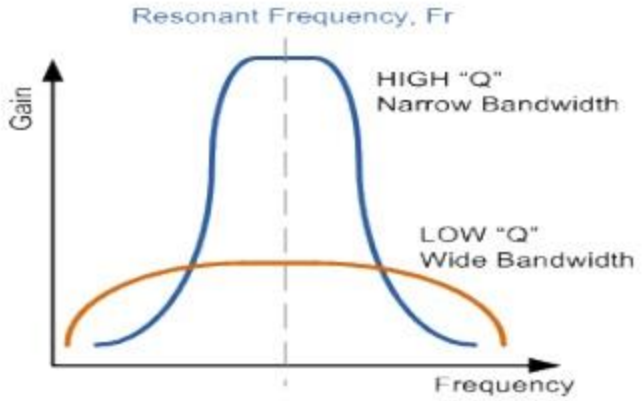
Pi section filter



T section filter

TYPES OF BP FILTER

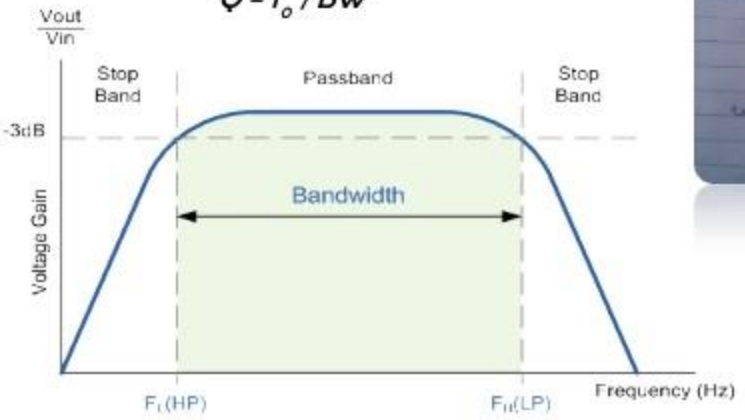
- Broad-band Band-Pass filter
- Narrow-band Band-Pass filter

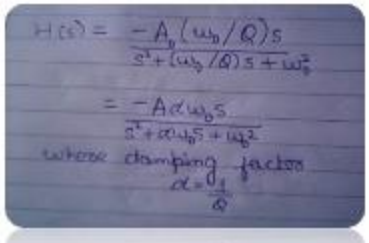


Frequency Response of a 2nd order Band-Pass (BP) FILTER:

- *The term "bandwidth" refers to the difference between the lower cut-off frequency (fc_{LOWER}) and the upper cut-off frequency (fc_{UPPER}) points.*
- A band-pass (BP) filter arrangement commonly consists of a combination of a Low-pass (LP) and a High-pass (HP) filter.

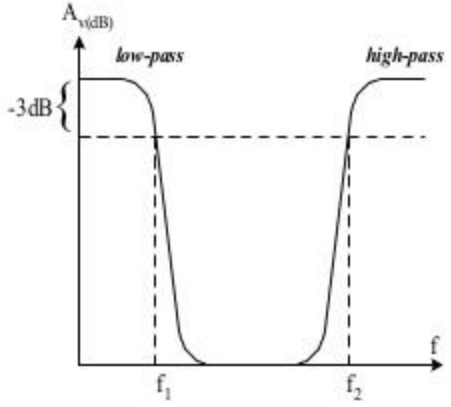
$$BW = f_2 - f_1$$
$$Q = f_o / BW$$

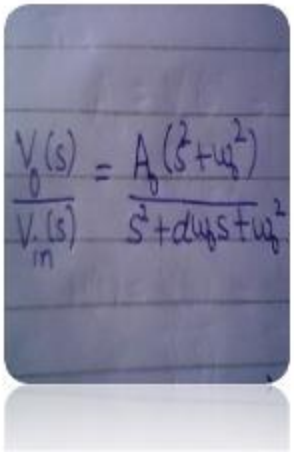


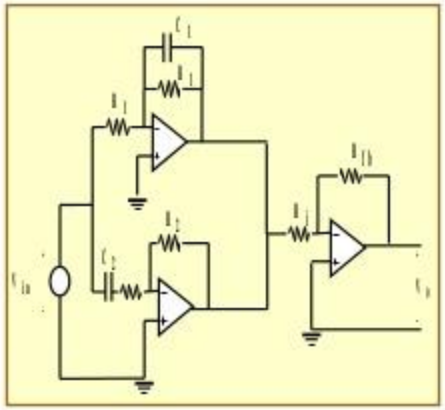


4- BAND REJECT FILTER

This can also be either as a Narrow or wide band reject filter. The narrow band reject filter is commonly called a notch filter & is useful for the rejection of a single frequency, such as 50 Hz power line frequency hum.

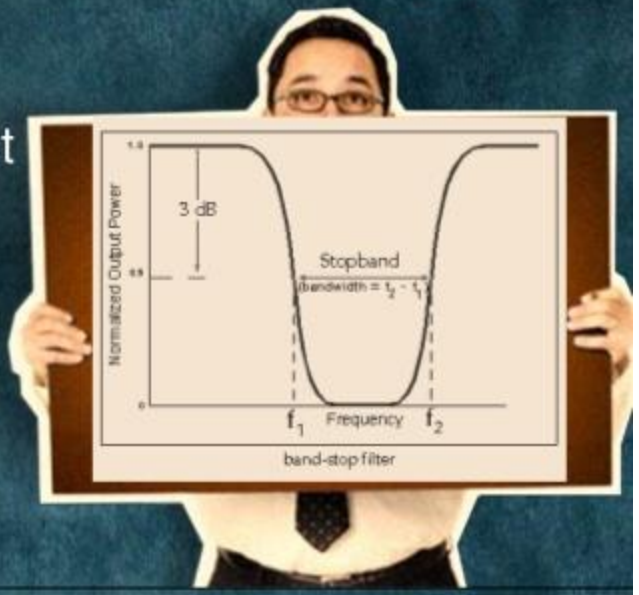


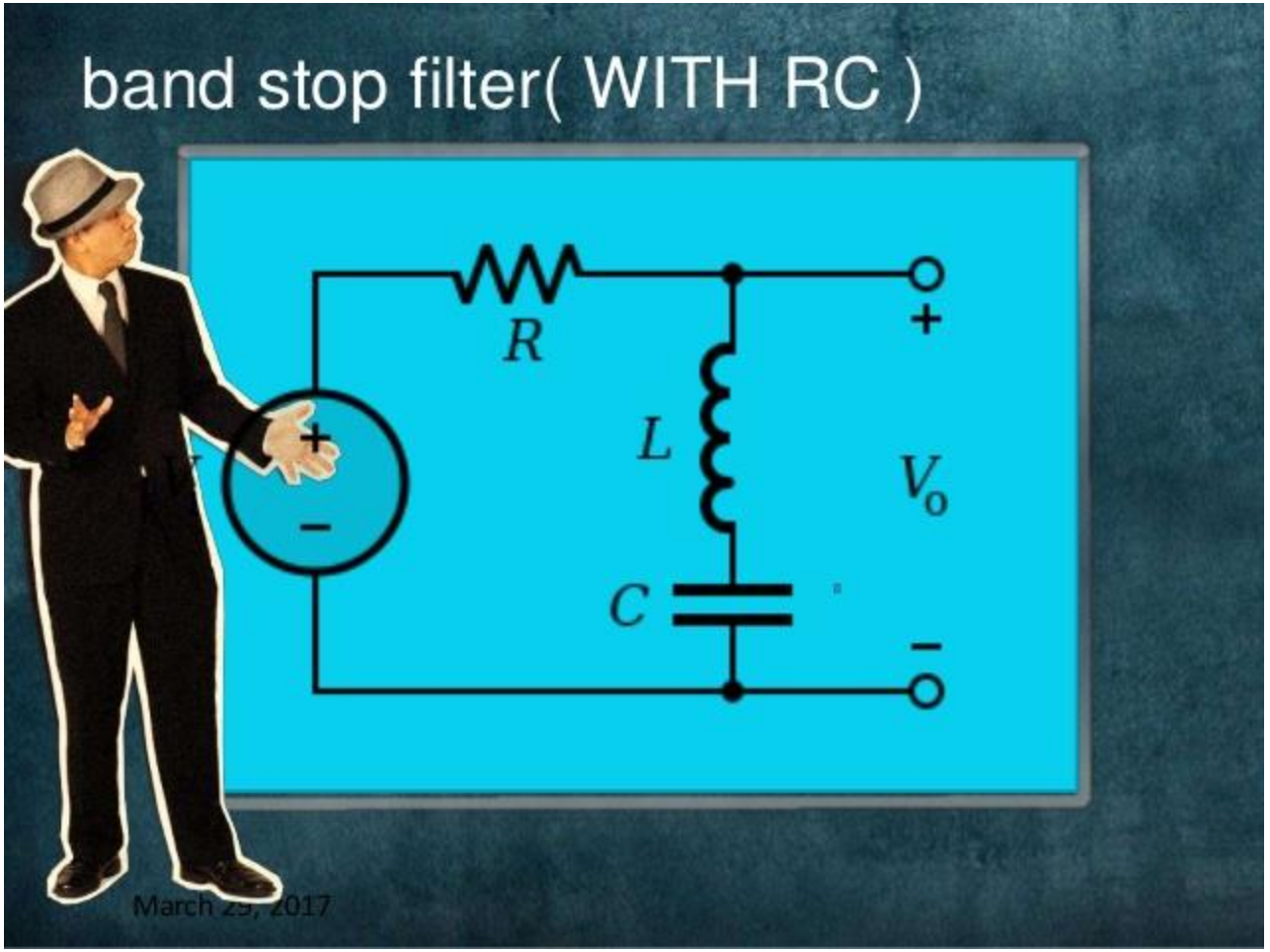




Band stop or band rejection filter

- In signal processing, a band-stop filter or band-rejection filter is a filter that passes most frequencies unaltered, but attenuates those in a specific range to very low levels.
- It is the opposite of a band-pass filter. A notch filter is a band-stop filter with a narrow stop band (high Q factor).

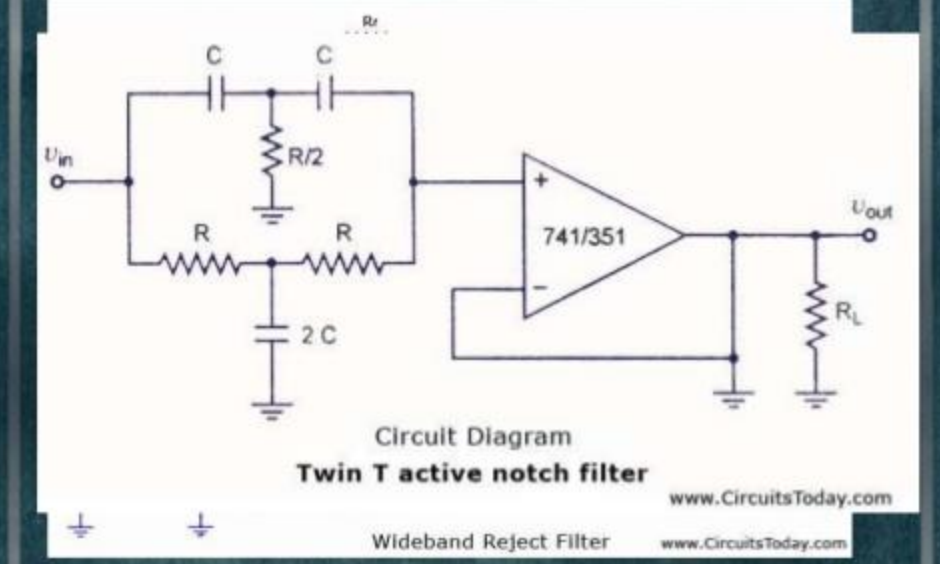



band stop filter(WITH RC)
R
L
C
+
−
+
V_o
−
March 29, 2017

Active band stop filter

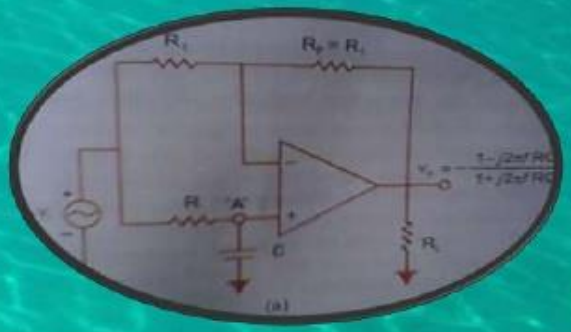
Narrow band reject filters (Notch filters).

Wide band reject filters



ALL PASS FILTER

- An all-pass filter passes all frequency components of the i/p signal without any attenuation & provides desired phase shifts at different frequencies of the I/P signal.
- When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. These phase changes can be compensated by all-pass filters.
- Thus, they are also called as delay equalizers or phase correctors



HIGH PASS FILTER DESIGN:

- The design steps of the second order filter are identical to those of the first order filter as given
- bellow:
- 1. Choose a value of high cutoff frequency fH.
- 2. To simplify the design calculations, set R2 = R3 = R and C2 = C3 = C. Then
- choose a value of c less than 1μf
- 3. Calculate the value of R using
- 4. Finally, because of the equal resistor (R2 = R3) and capacitor (C2 = C3) values,
- the pass band voltage gain AF has to be equal to 1.586. This gain is necessary to guarantee
- Butterworth response. Therefore, RF = 0.586 R1. Hence choose a value of R1= 100 kΩ and
- calculate the value of RF.

THANK YOU

UNIT-IV
A/D and D/A Converters

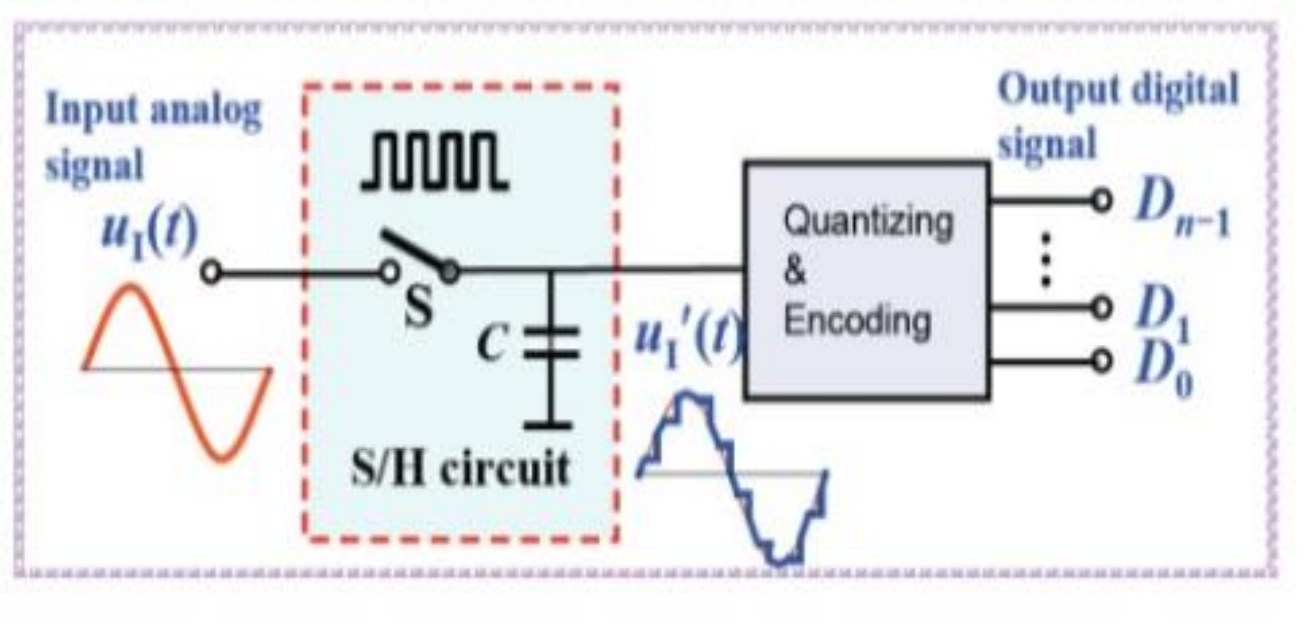
Prepared by

S.JAYACHITRA,AP/ECE

Sample and Hold Circuit

- Reduction of a continuous signal to a discrete signal
- Achieved through sampling and holding circuit
- Switch ON – sampling of signal (time to charge capacitor w/ Vin)
- Switch OFF - voltage stored in capacitor (hold operation)
- Must hold sampled value constant for digital conversion

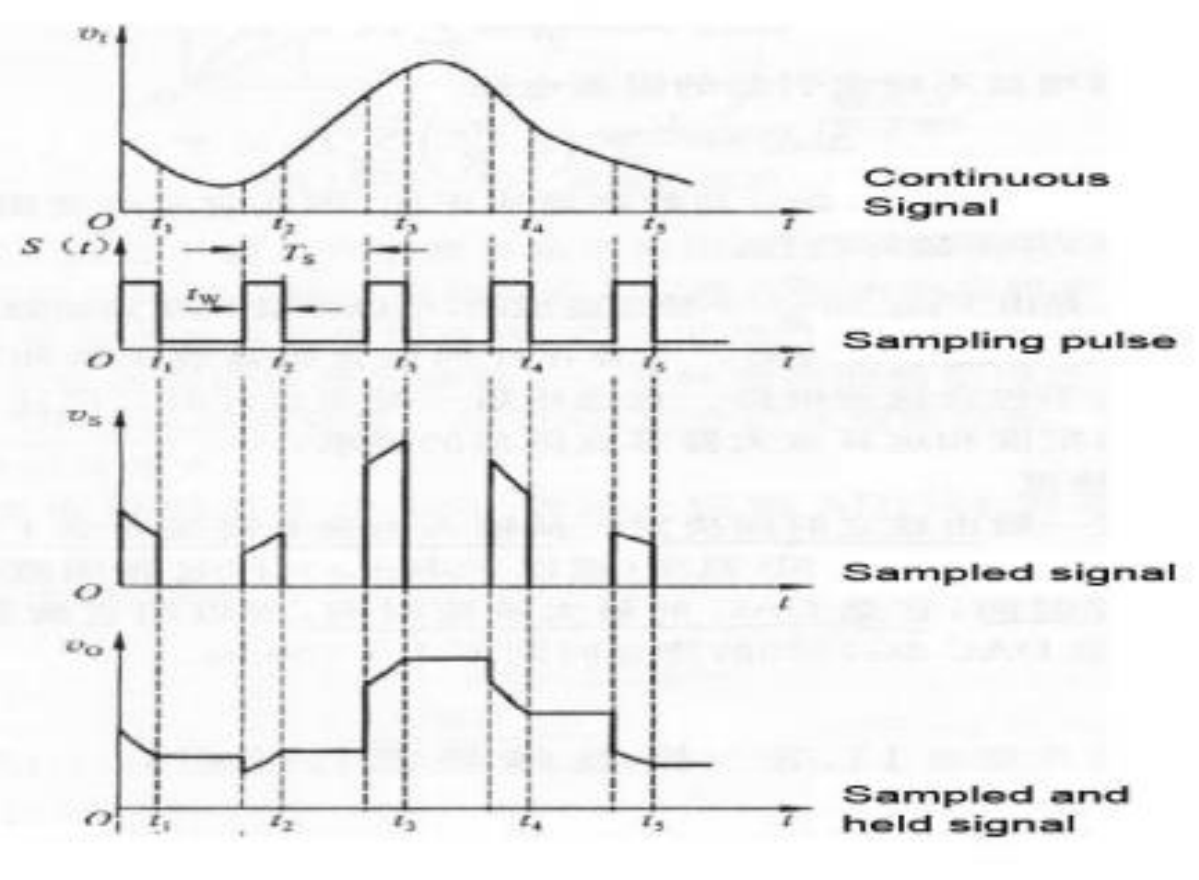
Block Diagram of Sample and Hold Circuit



Sampling and Holding

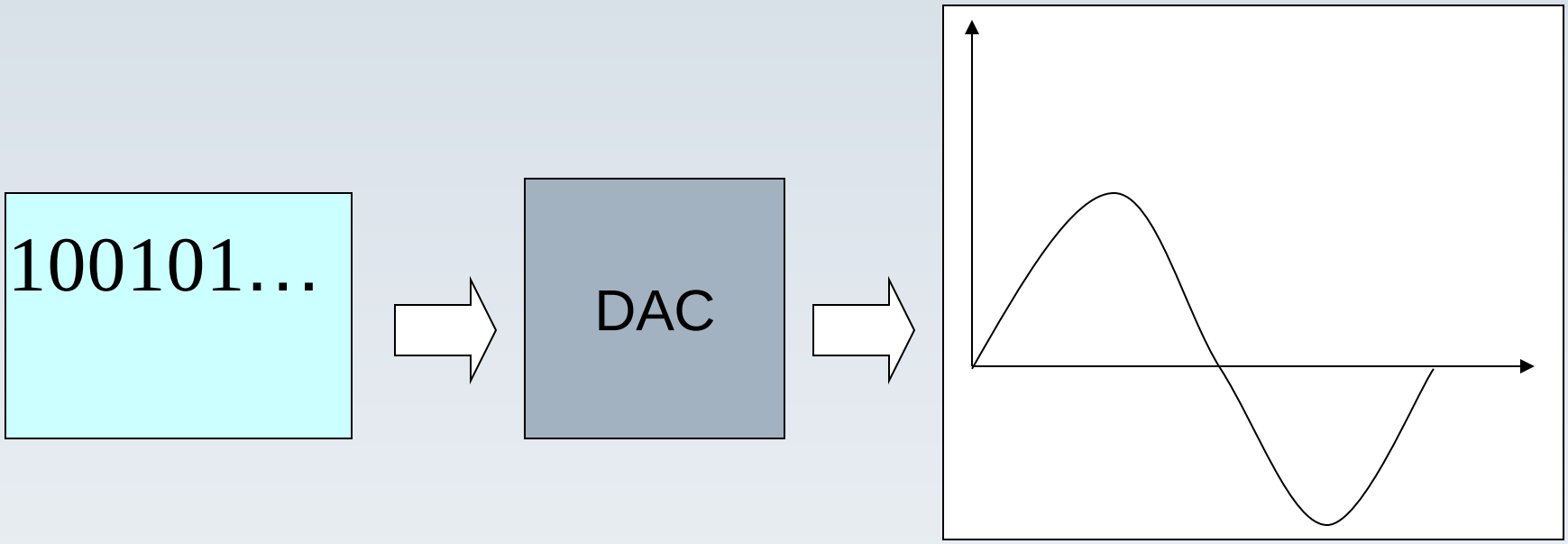
- The behavior of S/H is analogous to that of camera. its main function is "to capture picture" of the analog signal and hold its value until the adc can process the information.
- Holding signal benefits the accuracy of the A/D Conversion • Minimum sampling rate should be at least twice the highest data frequency of the analog signal.

Waveforms of Sample and Hold Circuit

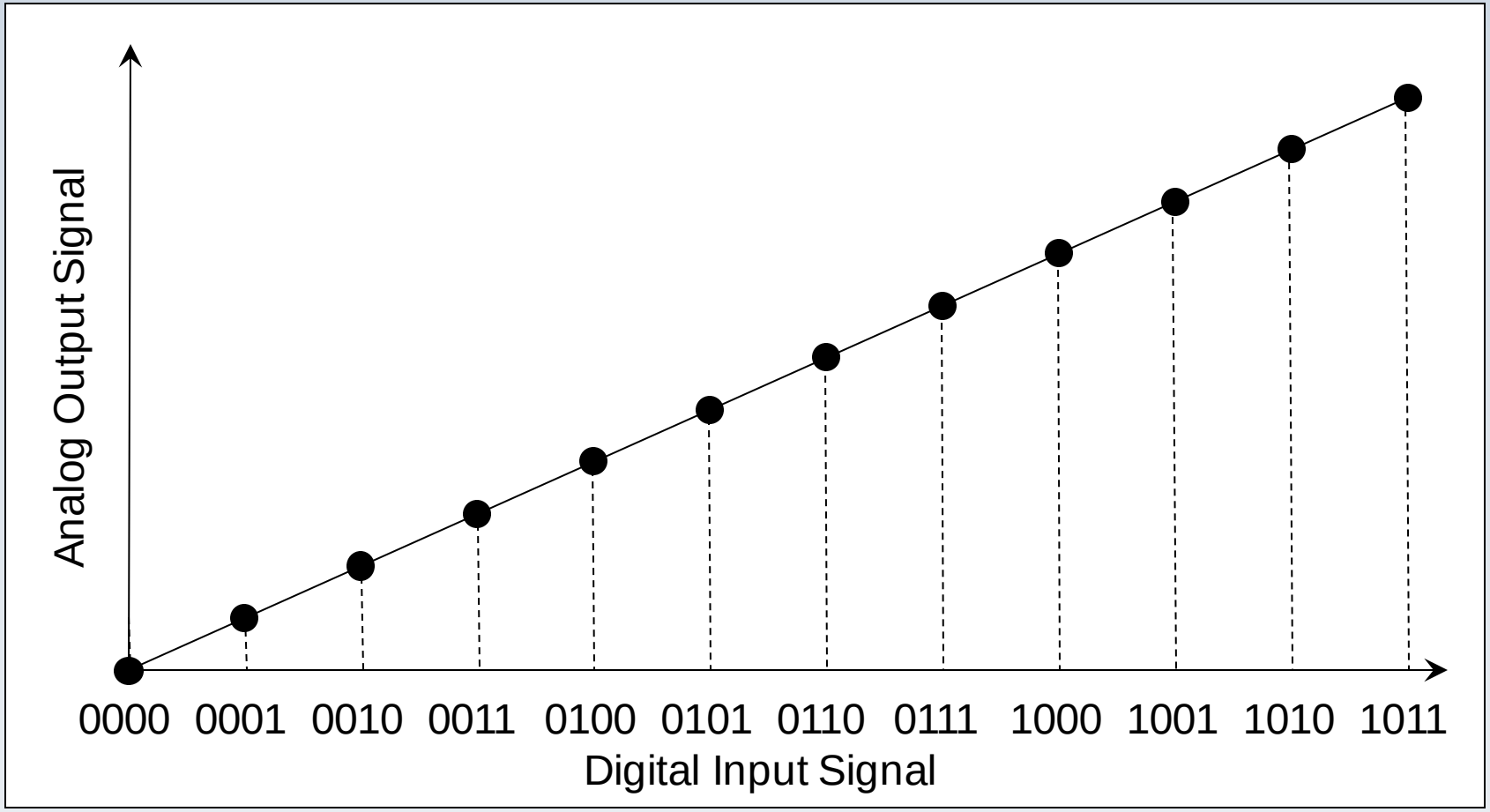


What is a DAC?

- A digital to analog converter (DAC) converts a digital signal to an analog voltage or current output.



What is a DAC?


Analog Output Signal
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011
Digital Input Signal

Types of DACs

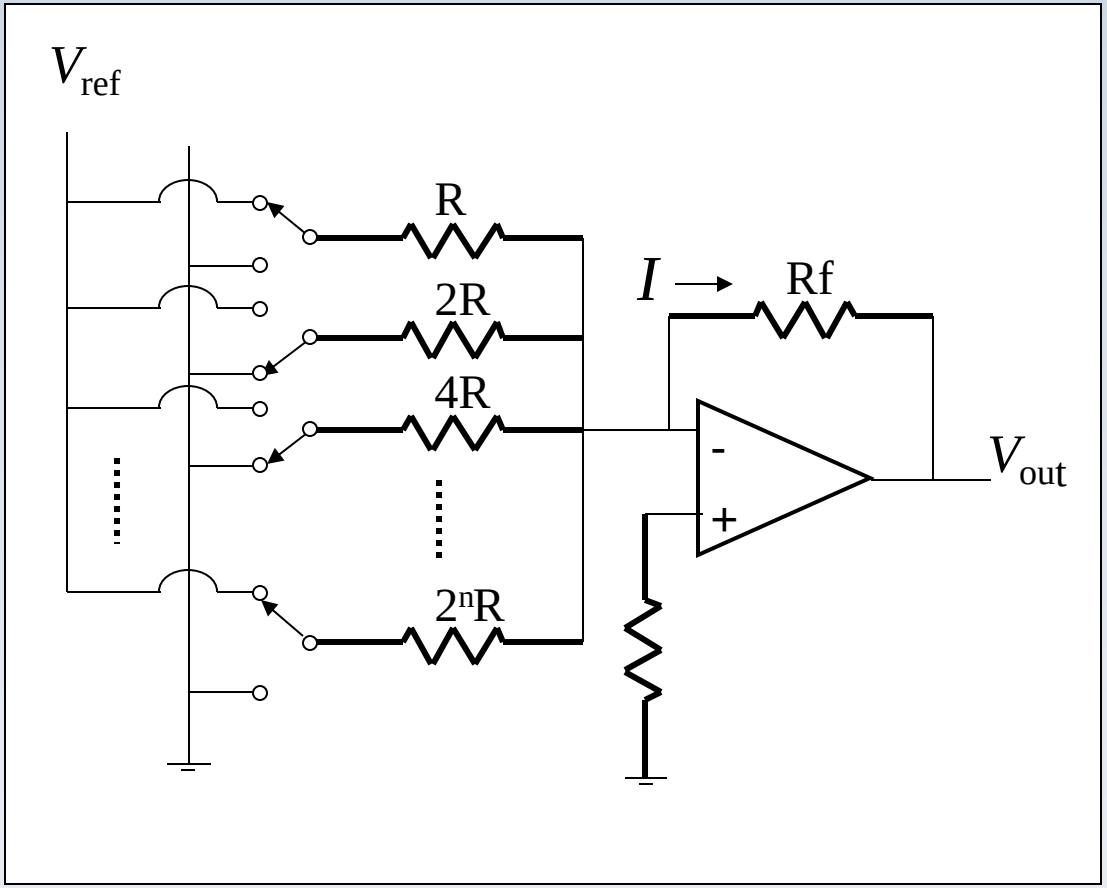
- Many types of DACs available.
- Usually switches, resistors, and op-amps used to implement conversion
- Two Types:
  - Binary Weighted Resistor/Resistive Divider
  - R-2R Ladder

Binary Weighted Resistor

- Utilizes a summing op-amp circuit
- Weighted resistors are used to distinguish each bit from the most significant to the least significant
- Transistors are used to switch between V_{ref} and ground (bit high or low)

Binary Weighted Resistor

- Assume Ideal Op-amp
- No current into op-amp
- Virtual ground at inverting input
- $V_{out} = -IR_f$

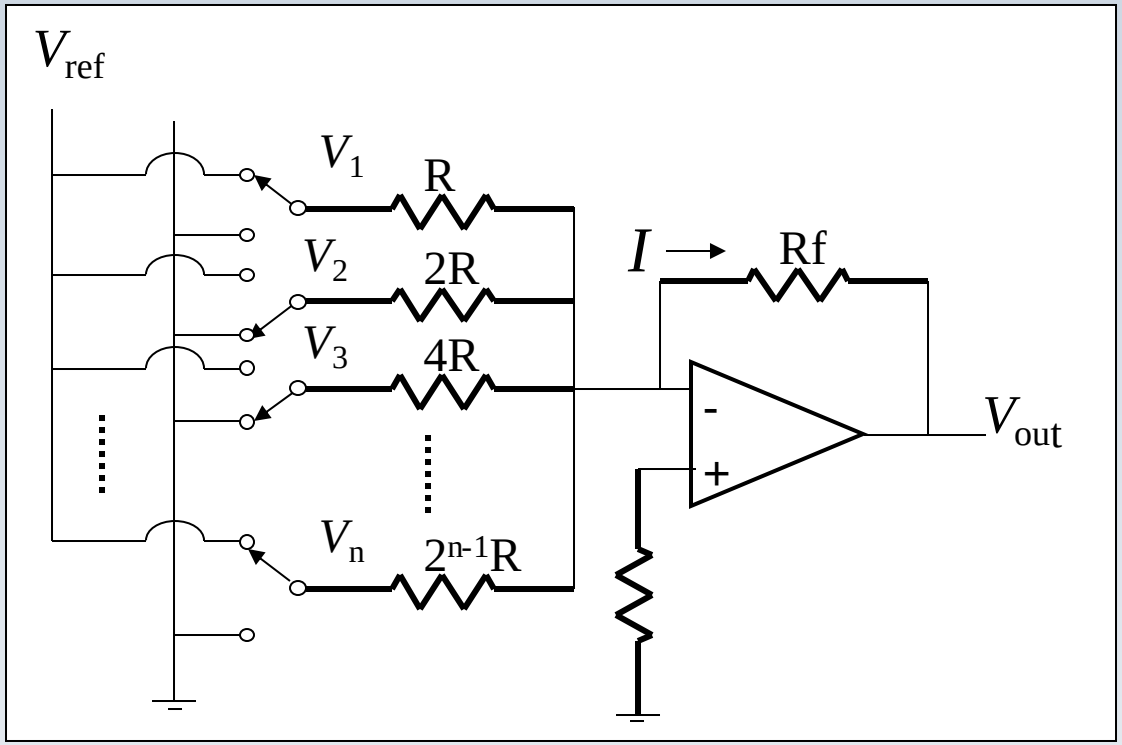


Binary Weighted Resistor

Voltages V_1 through V_n are either V_{ref} if corresponding bit is high or ground if corresponding bit is low

V_1 is most significant bit

V_n is least significant bit



MSB

LSB

$$V_{out} = -IR_f = -R_f\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \cdots \frac{V_n}{2^{n-1}R}\right)$$

Binary Weighted Resistor

If $R_f = R/2$

$$V_{out} = -IR_f = -\left(\frac{V_1}{2} + \frac{V_2}{4} + \frac{V_3}{8} + \cdots \frac{V_n}{2^n}\right)$$

For example, a 4-Bit converter yields

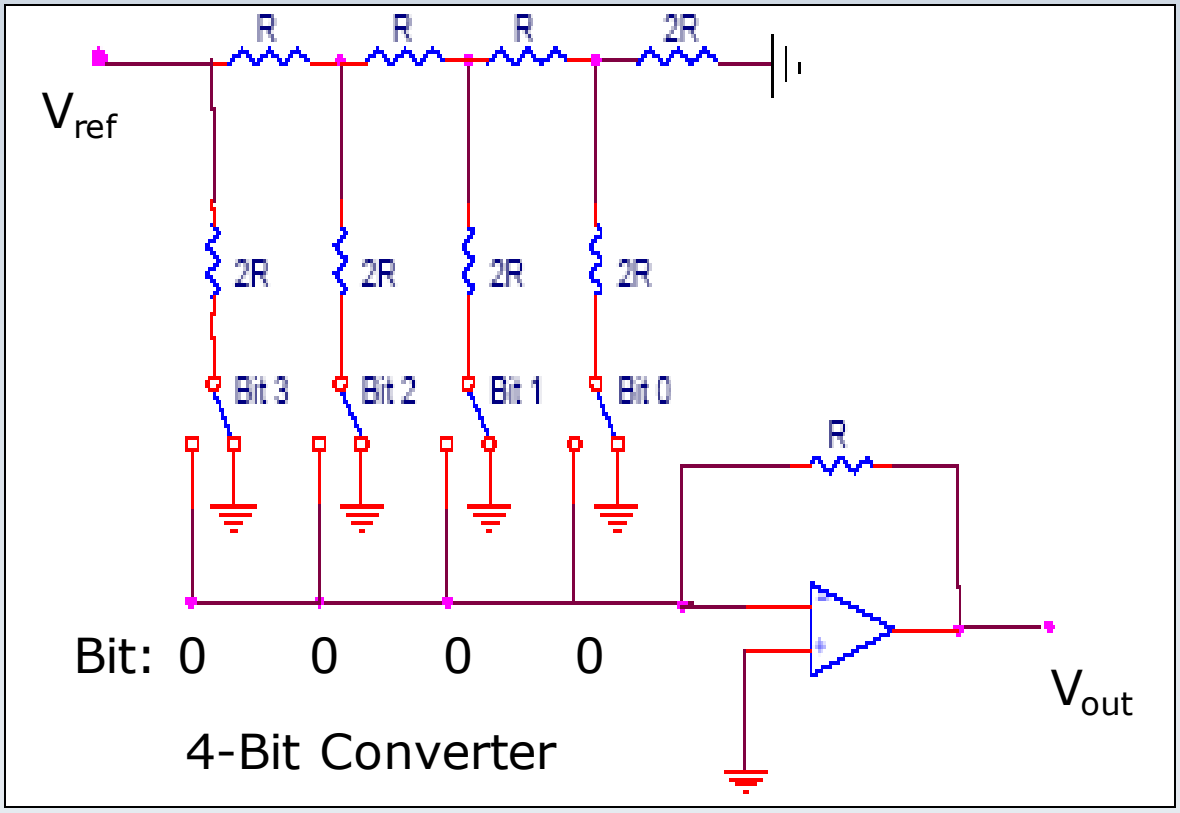
$$V_{out} = -V_{ref}\left(b_3\frac{1}{2} + b_2\frac{1}{4} + b_1\frac{1}{8} + b_0\frac{1}{16}\right)$$

Where b_3 corresponds to Bit-3, b_2 to Bit-2, etc.

Binary Weighted Resistor

- Advantages
  - Simple Construction/Analysis
  - Fast Conversion
- Disadvantages
  - Requires large range of resistors (2000:1 for 12-bit DAC) with necessary high precision for low resistors
  - Requires low switch resistances in transistors
  - Can be expensive. Therefore, usually limited to 8-bit resolution.

R-2R Ladder

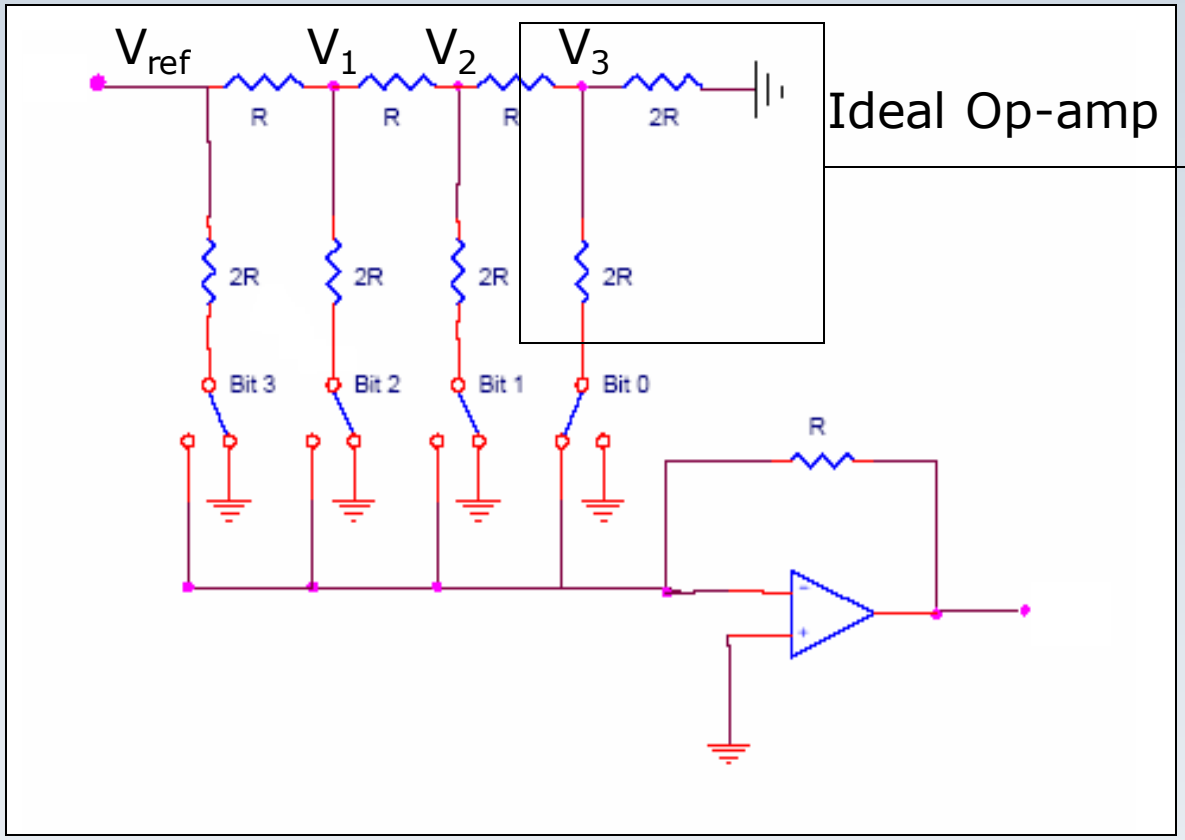


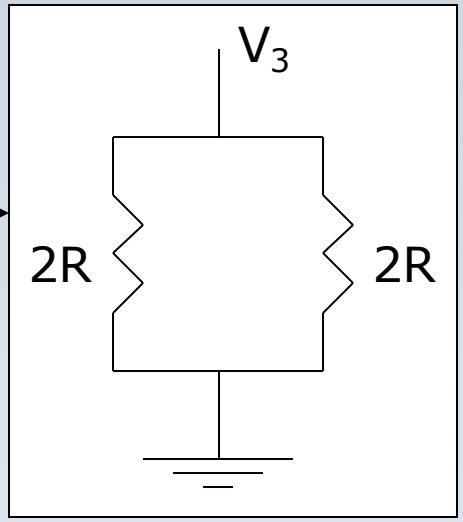
Each bit corresponds to a switch:

If the bit is high, the corresponding switch is connected to the inverting input of the op-amp.

If the bit is low, the corresponding switch is connected to ground.

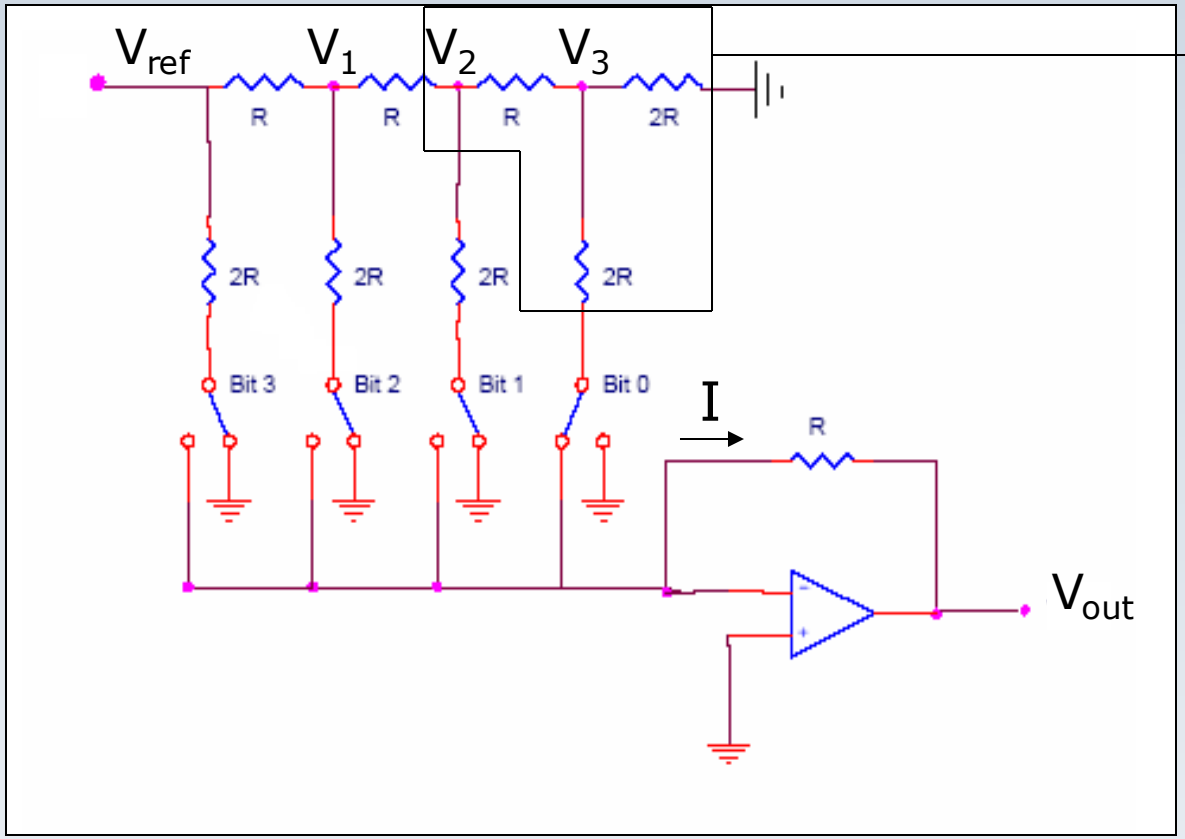
R-2R Ladder

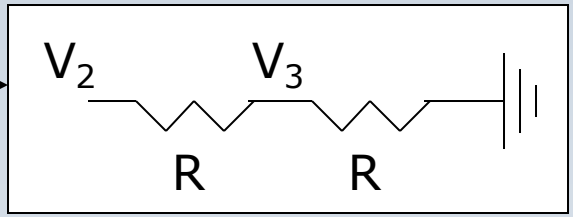




$$R_{eq} = \frac{(2R)(2R)}{(2R+2R)} = R$$

R-2R Ladder





$$V_3 = \left(\frac{R}{R+R}\right)V_2 = \frac{1}{2}V_2$$

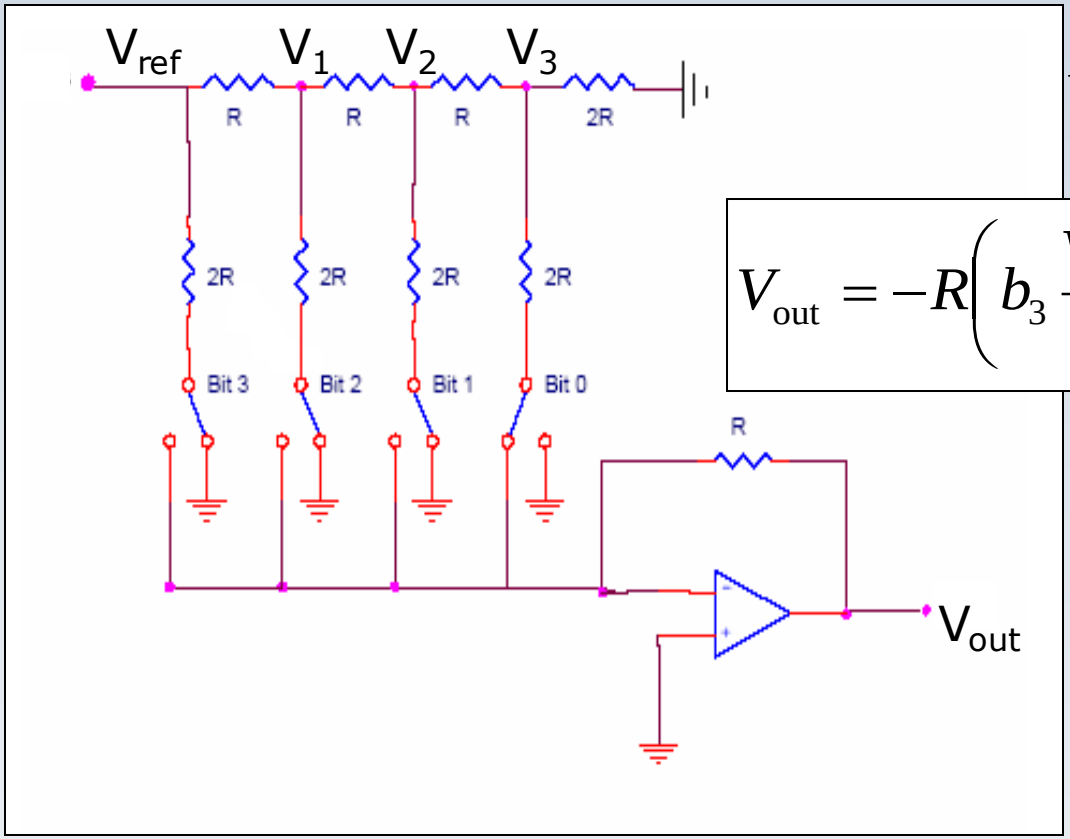
Likewise,

$$V_2 = \frac{1}{2}V_1$$

$$V_1 = \frac{1}{2}V_{\text{ref}}$$

$$V_{\text{out}} = -IR$$

R-2R Ladder



Results:

$$V_3 = \frac{1}{8}V_{\text{ref}},\ V_2 = \frac{1}{4}V_{\text{ref}},\ V_1 = \frac{1}{2}V_{\text{ref}}$$

$$V_{\text{out}} = -R\left(b_3 \frac{V_{\text{ref}}}{2R} + b_2 \frac{V_{\text{ref}}}{4R} + b_1 \frac{V_{\text{ref}}}{8R} + b_0 \frac{V_{\text{ref}}}{16R} \right)$$

Where b_3 corresponds to bit 3, b_2 to bit 2, etc.

If bit n is set, b_n=1

If bit n is clear, b_n=0

R-2R Ladder

For a 4-Bit R-2R Ladder

$$V_{\text{out}} = -V_{\text{ref}}\left(b_3\frac{1}{2}+b_2\frac{1}{4}+b_1\frac{1}{8}+b_0\frac{1}{16}\right)$$

For general n-Bit R-2R Ladder or Binary Weighted Resister DAC

$$V_{\text{out}} = -V_{\text{ref}}\sum_{i=1}^{n} b_{n-i}\frac{1}{2^i}$$

R-2R Ladder

- **Advantages**
  - Only two resistor values (R and 2R)
  - Does not require high precision resistors
- **Disadvantage**
  - Lower conversion speed than binary weighted DAC

Specifications of DACs

- Resolution
- Speed
- Linearity
- Settling Time
- Reference Voltages
- Errors

Resolution

- Smallest analog increment corresponding to 1 LSB change
- An N-bit resolution can resolve 2^N distinct analog levels
- Common DAC has a 8-16 bit resolution

$$\text{Resolution} = V_{LSB} = \frac{V_{ref}}{2^N}$$

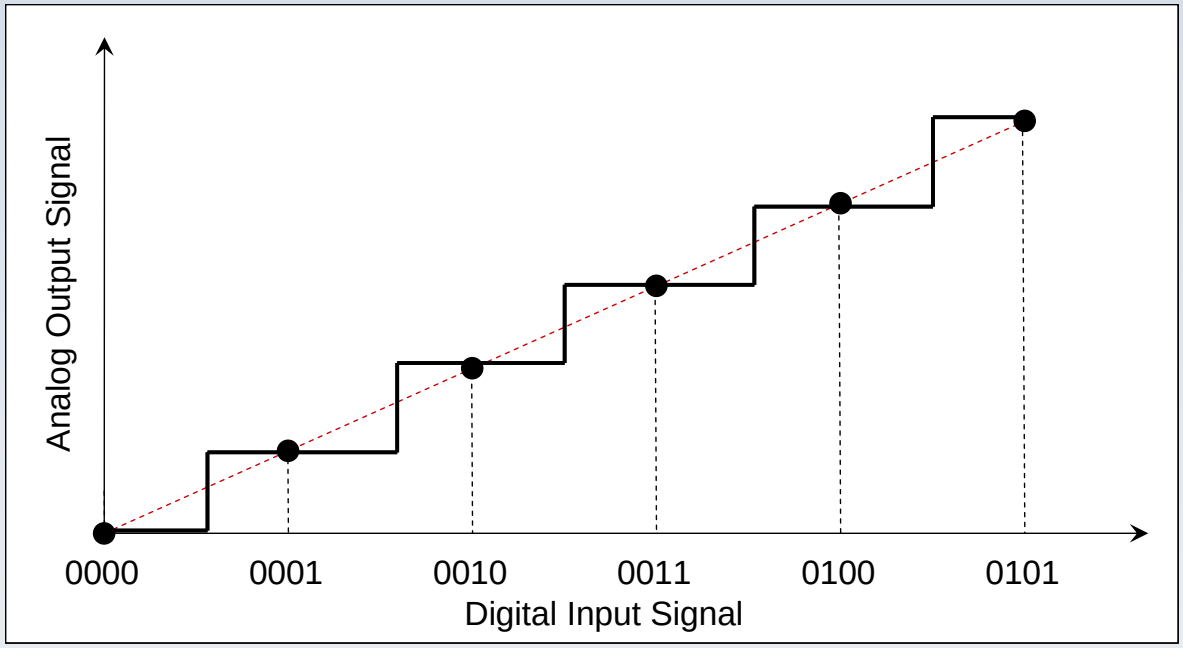
$$\text{where } N = number\ of\ bits$$

Speed

- Rate of conversion of a single digital input to its analog equivalent
- Conversion rate depends on
  - clock speed of input signal
  - settling time of converter
- When the input changes rapidly, the DAC conversion speed must be high.

Linearity

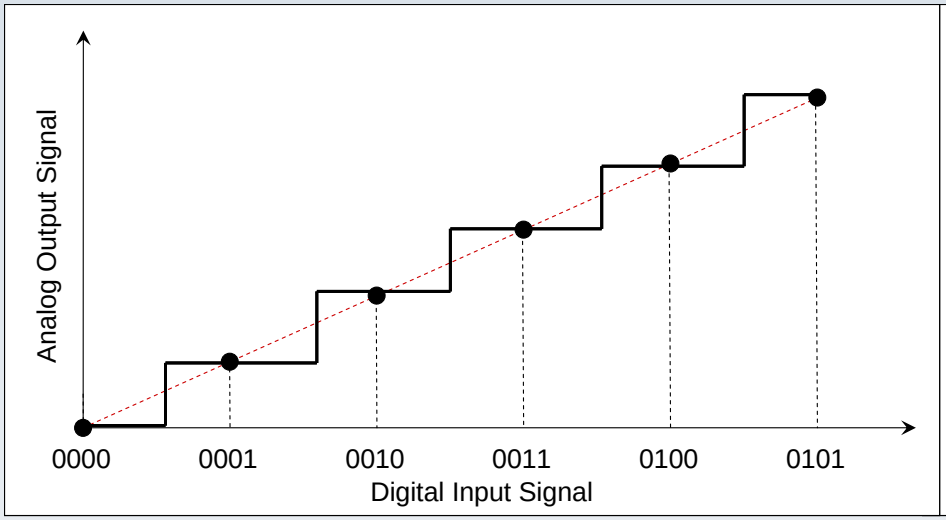
- The difference between the desired analog output and the actual output over the full range of expected values



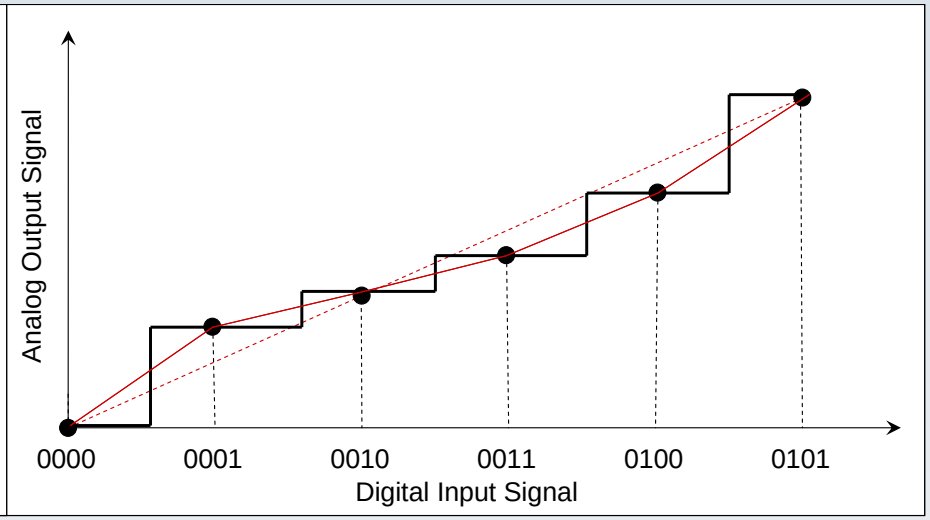
Linearity

- Ideally, a DAC should produce a linear relationship between the digital input and analog output

Linearity (Ideal)

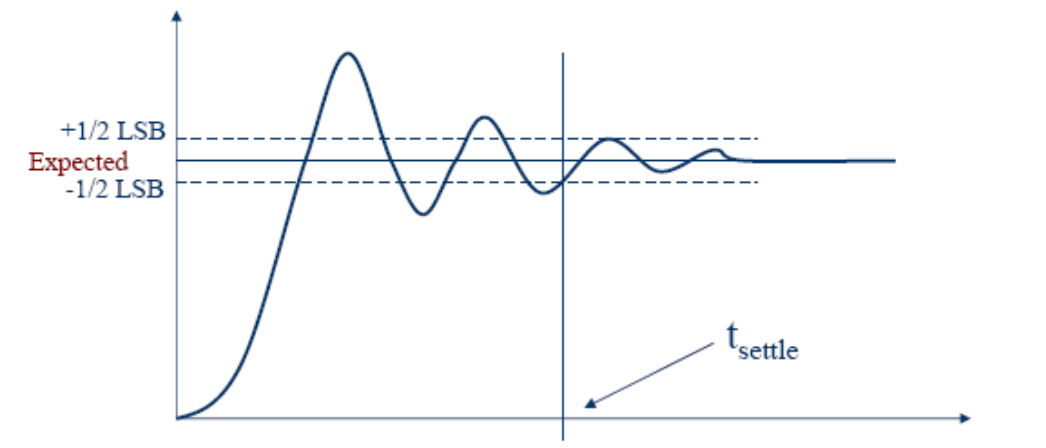


Non-Linearity



Settling Time

- Time required for the output signal to settle within +/- ½ LSB of its final value after a given change in input scale
- Limited by slew rate of output amplifier
- Ideally, an instantaneous change in analog voltage would occur when a new binary word enters into DAC



Reference Voltages

- Used to determine how each digital input will be assigned to each voltage division
- Types:
  - Non-multiplier DAC: Vref is fixed
  - Multiplier DAC: Vref provided by external source

Types of Errors Associated with DACs

- Gain
- Offset
- Full Scale
- Resolution
- Non-Linearity
- Non-Monotonic
- Settling Time and Overshoot

Applications

- Digital Motor Control
- Computer Printers
- Sound Equipment (e.g. CD/MP3 Players, etc.)
- Electronic Cruise Control
- Digital Thermostat

Types of A/D Converters

- Ramp or stair case or counter type A/D converter
- Successive Approximation A/D Converter
- Flash A/D Converter/Parallel Comparator
- Dual Slope or integrating type A/D Converter

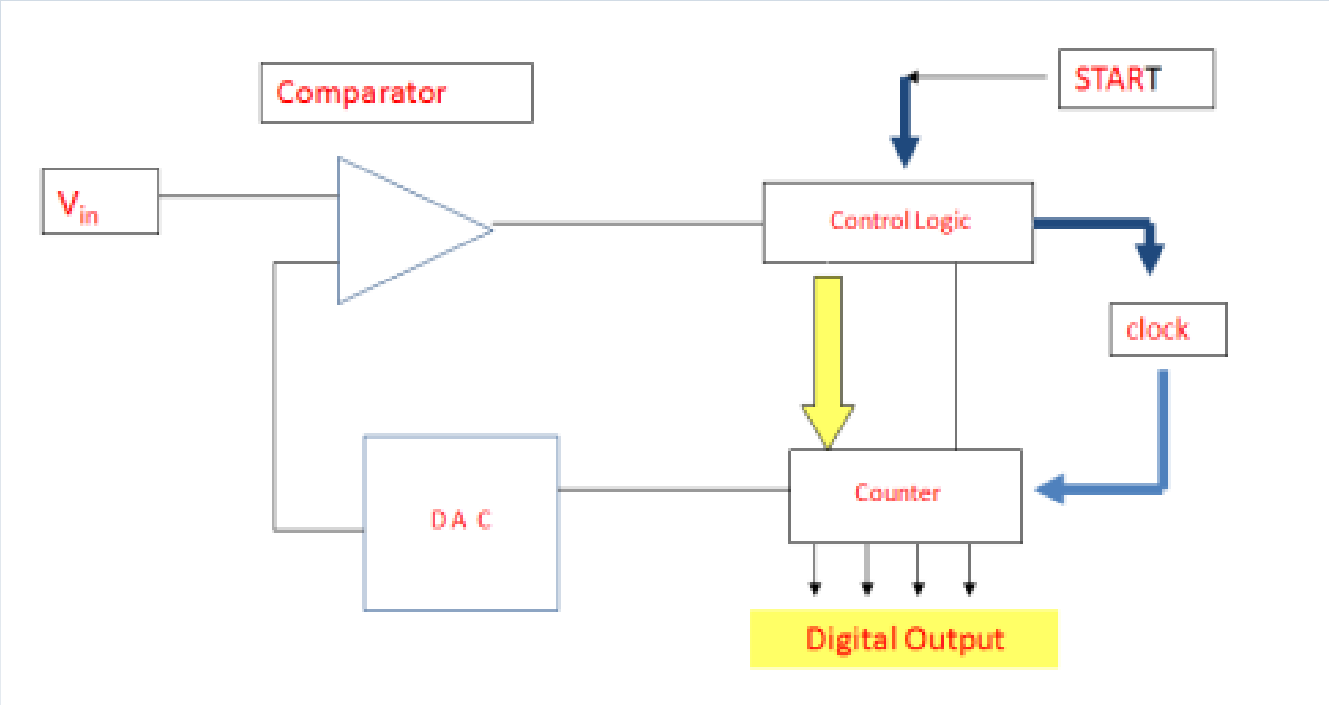
Counter type

The basic idea is to connect the output of a free-running binary counter to the input of a DAC, then compare the analog output of the DAC with the analog input signal to be digitized and use the comparator's output to tell the counter when to stop counting and reset.

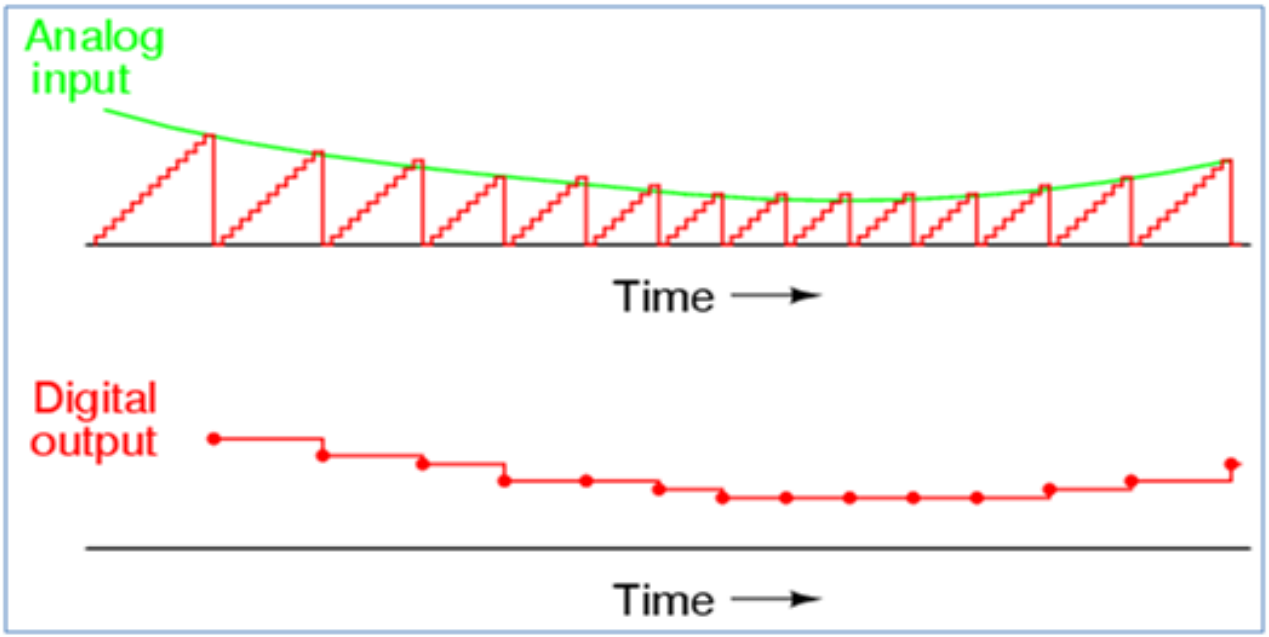
Features of counter type

- Use a clock to index the counter
- Use DAC to generate analog signal to compare against input
- Comparator is used to compare VIN and VDAC where VIN is the signal to be digitized
- The input to the DAC is from the counter

Block Diagram of Counter Type ADC



Counter Type ADC Waveforms



Counter Type ADC Waveforms

Operation

- The analog output equivalent to the digital i/p from DAC is contrasted with the i/p analog voltage with the help of an op-amp comparator.
- This Integrated Circuit evaluates the two voltages and if the produced DAC voltage is low, it gives a high pulse to the N-bit counter as a CLK pulse to raise the counter.
- The similar procedure will be continued until the output of the DAC equals to the i/p analog voltage then it produces a low CLK pulse and also gives a clear signal to the counter as well as a load signal to the storage resistor.
- Here storage resistor is used to store the corresponding digital bits. These digital values are strongly matched with the analog input values with a small error.

- For each sampling interval, the output of DAC tracks a ramp way so that it is named as a Digital ramp kind ADC. And this ramp seems like staircases for each sampling moment, so that it is also named as a staircase approximation kind ADC.
- The conversion time on the counter type is NOT fixed but depends on the actual value of the analogue input expressed as a fraction of the full scale. This can be expressed as-

$$\text{Conversion time} = \frac{Vin}{Vref} 2^N T$$

Where N is the number of bits and T is the time period of the clock pulse.

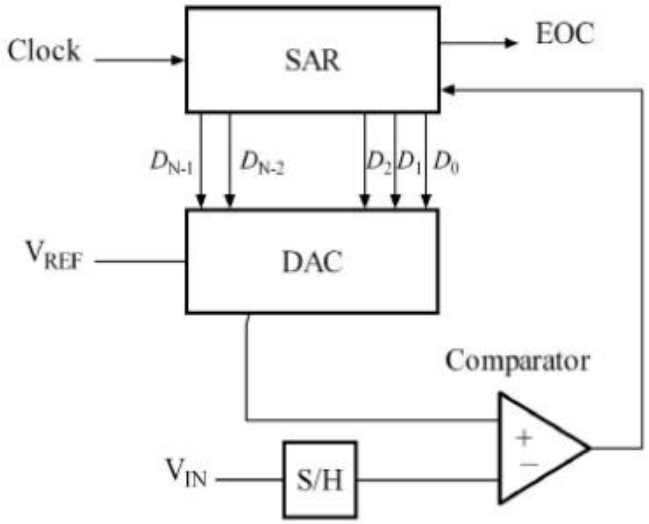
Counter type ADC Advantages

- Counter type ADC is very simple to understand and also to operate.
- Counter type ADC design is less complex, so the cost is also less

Counter type ADC Disadvantages

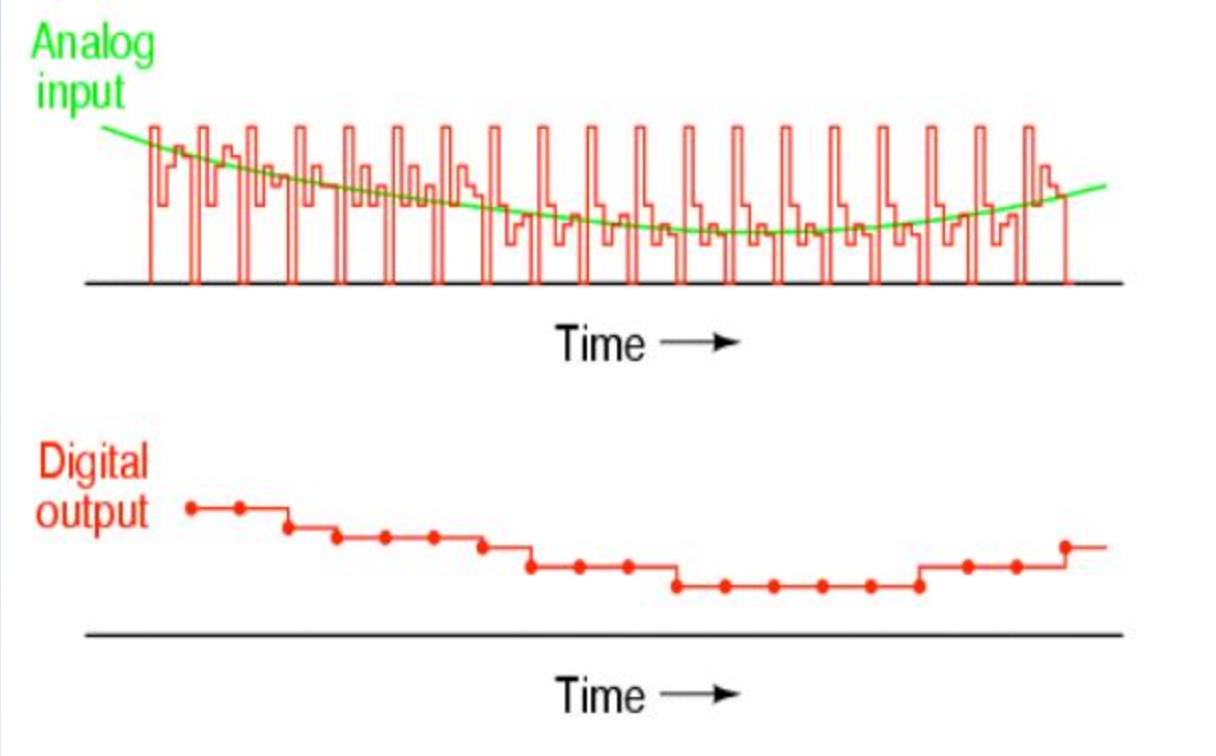
- Speed is less, since each time the counter has to begin from ZERO.
- There may be conflicts if the next i/p is sampled before completion of one process.

Successive Approximation Type ADC



- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of Vin.
- Comparison changes digital output to bring it closer to the input value.
- Uses Closed-Loop Feedback Conversion

Waveforms



- One method of addressing the digital ramp ADC's shortcomings is the so-called successive approximation ADC.
- The only change in this design is a very special counter circuit known as a successive-approximation register.
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least-significant bit.
- Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly.
- The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number.

Process

- MSB initialized as 1
- Convert digital value to analog using DAC
- Compares guess to analog input
- Is Vin>VDAC
  - Set bit 1
  - If no, bit is 0 and test next bit format.

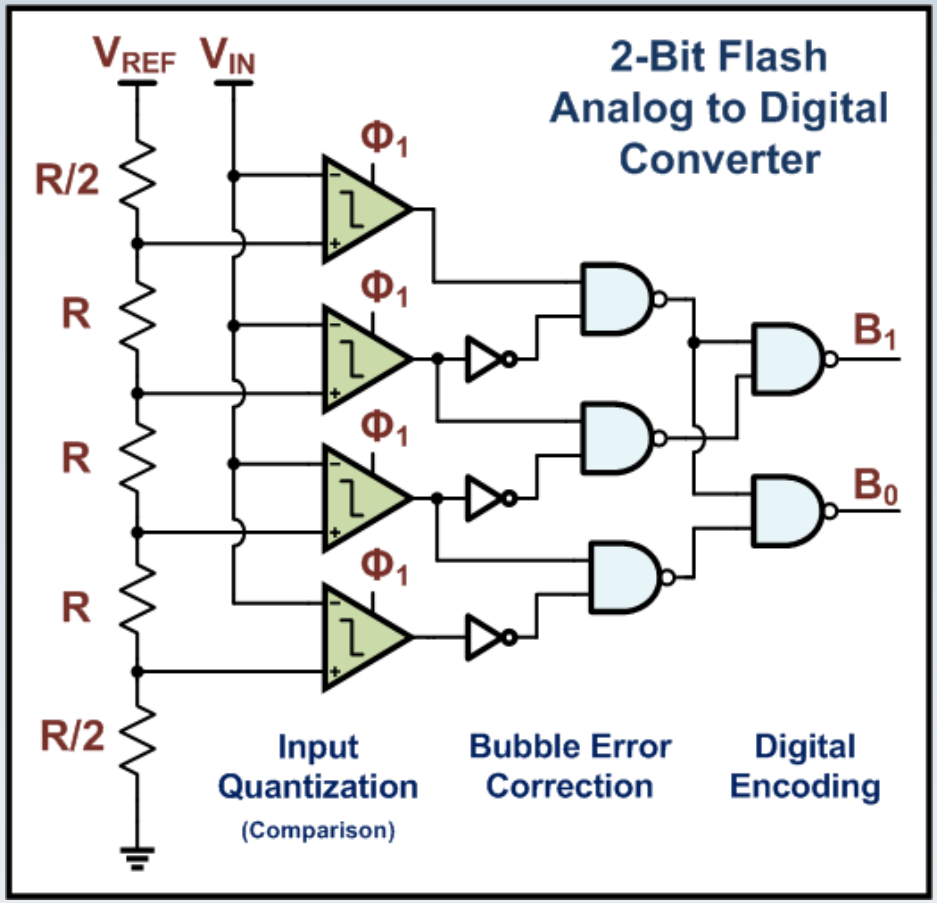
Advantage

- Capable of high speed and reliable
- Medium accuracy compared to other ADC
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time)

Disadvantages

- Higher resolution
- slower
- Speed limited to ~5Msps

Flash Type ADC /Parallel Comparator



- Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages.
- To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required.
- The three op-amps are used as comparators. The non-inverting inputs of all the three comparators are connected to the analog input voltage.

- The inverting terminals are connected to a set of reference voltages
- The output of the comparator is in positive saturation(i.e. logic 1), when voltage at non-inverting terminal is greater than voltage at inverting terminal and is in negative saturation otherwise

comparator outputs for different ranges of analog input voltages and their corresponding digital outputs.

Analog Input Conditions	Comparator Outputs			Digital output	
	C_1	C_2	C_3	B_1	B_0
$0 \leqslant V_{in} \leqslant \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \leqslant V_{in} \leqslant \frac{2V}{4}$	1	0	0	0	1
$\frac{2V}{4} \leqslant V_{in} \leqslant \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \leqslant V_{in} \leqslant V$	1	1	1	1	1

Advantages:

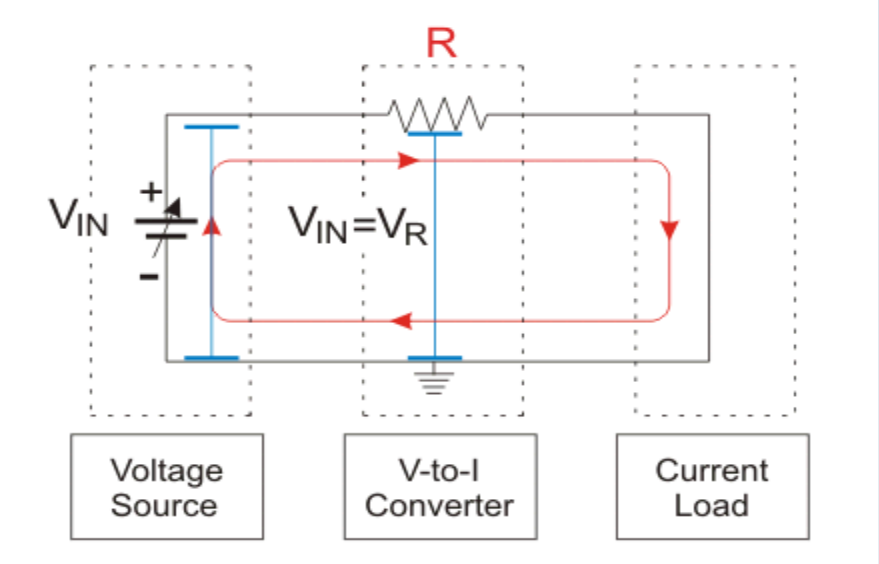
- It is the fastest type of ADC because the conversion is performed simultaneously through a set of comparators, hence referred as flash type ADC. Typical conversion time is 100ns or less.
- The construction is simple and easier to design.

Disadvantages

- It is not suitable for higher number of bits.
- To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required. The number of comparators required doubles for each added bit.

Voltage to current Converter

- The resistor decides the current flow in a voltage source circuit or it performs as a simple voltage to current converter for a linear circuit.

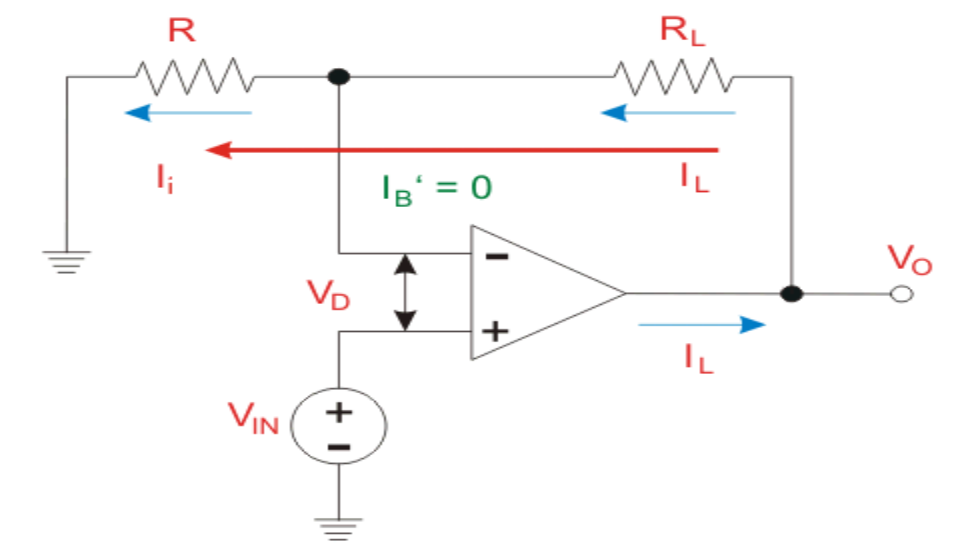


- Op-amp is implemented to simply convert the voltage signal to corresponding current signal. The Op-amp used for this purpose is IC LM741.
- This Op-amp is designed to hold the precise amount of current by applying the voltage which is essential to sustain that current through out the circuit.

Floating Load Voltage to Current Converter

- The load resistor is floating in this converter circuit. That is, the resistor R_L is not linked to ground.
- The voltage, V_{IN} which is the input voltage is given to the non-inverting input terminal.
- The inverting input terminal is driven by the feedback voltage which is across the R_L resistor.

- This feedback voltage is determined by the load current and it is in series with the V_D, which is the input difference voltage. So this circuit is also known as current series negative feedback amplifier.



For the input loop, the voltage equation is

$$V_{IN} = V_D + V_F$$

Since A is very large, $V_D = 0$

So,

$$V_{IN} = V_F$$

Since, the input to the Op-amp, $I'_B = 0$

$$V_{IN} = I_L \times R$$

$$\therefore I_I = I_L = \frac{V_{IN}}{R}$$

- It is clear that the load current depends on the input voltage and the input resistance. That is, the load current, , which is the input voltage.
- The load current is controlled by the resistor, R. Here, the proportionality constant is 1/R.
- So, this converter circuit is also known as Trans-Conductance Amplifier. Other name of this circuit is Voltage Controlled Current Source. The type of load may be resistive, capacitive or non-linear load.

Application of V-I Converter

- Zener diode tester
- Low AC and DC Voltmeters
- Testing LED
- Testing Diodes

IC 555 TIMER

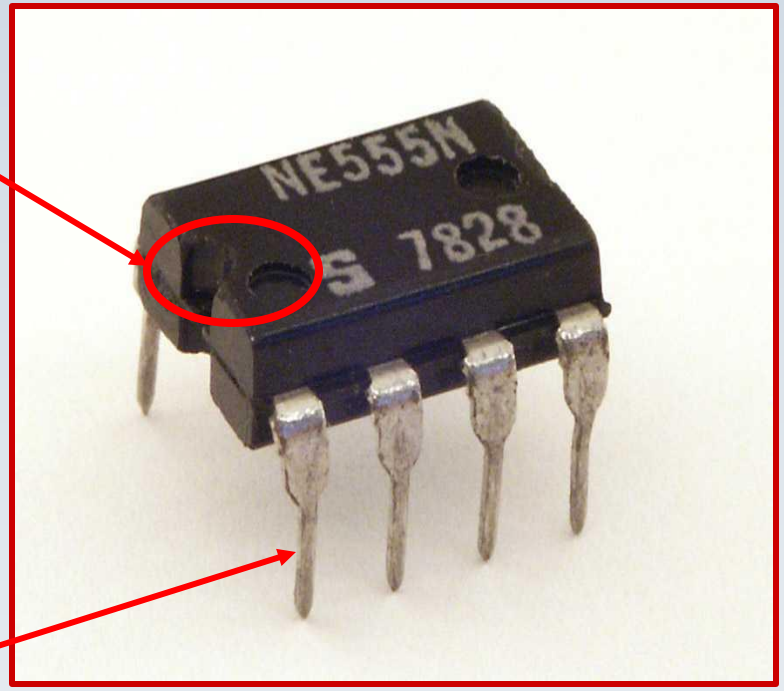
555 Timer

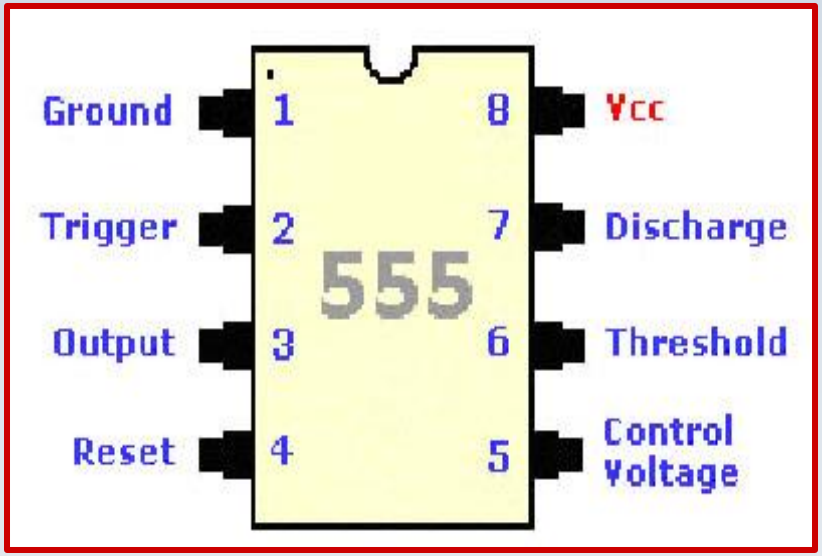
Introduction:

- "Signetics" Corporation first introduced this device as the SE/NE 555 in early 1970.
- It is a combination of digital and analog circuits.
- It is known as the "time machine" as it performs a wide variety of timing tasks.
- Applications for the 555 Timer include:
  - Ramp and Square wave generator
  - Frequency dividers
  - Voltage-controlled oscillators
  - Pulse generators and LED flashers

555 timer- Pin Diagram

The 555 timer is an 8-Pin D.I.L. Integrated Circuit or 'chip'



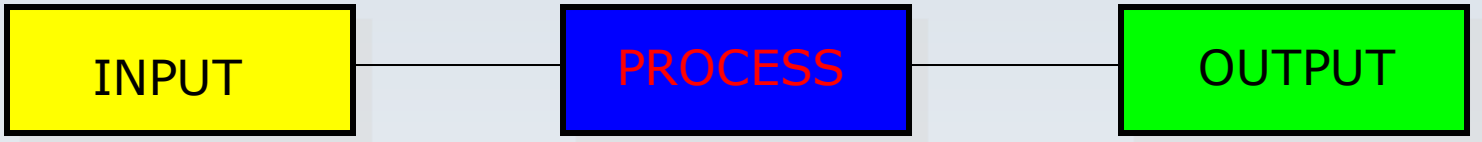


555 timer- Pin Description

Pin	Name	Purpose
1	GND	Ground, low level (0 V)
2	TRIG	OUT rises, and interval starts, when this input falls below 1/3 V_{CC}.
3	OUT	This output is driven to approximately 1.7V below $+V_{CC}$ or GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	"Control" access to the internal voltage divider (by default, 2/3 V_{CC}).
6	THR	The interval ends when the voltage at THR is greater than at CTRL.
7	DIS	Open collector output; may discharge a capacitor

Description:

- Contains 25 transistors, 2 diodes and 16 resistors
- Maximum operating voltage 16V
- Maximum output current 200mA
- Best treated as a single component with required input and output



If you input certain signals they will be processed / controlled in a certain manner and will produce a known output.

Inside the 555 Timer

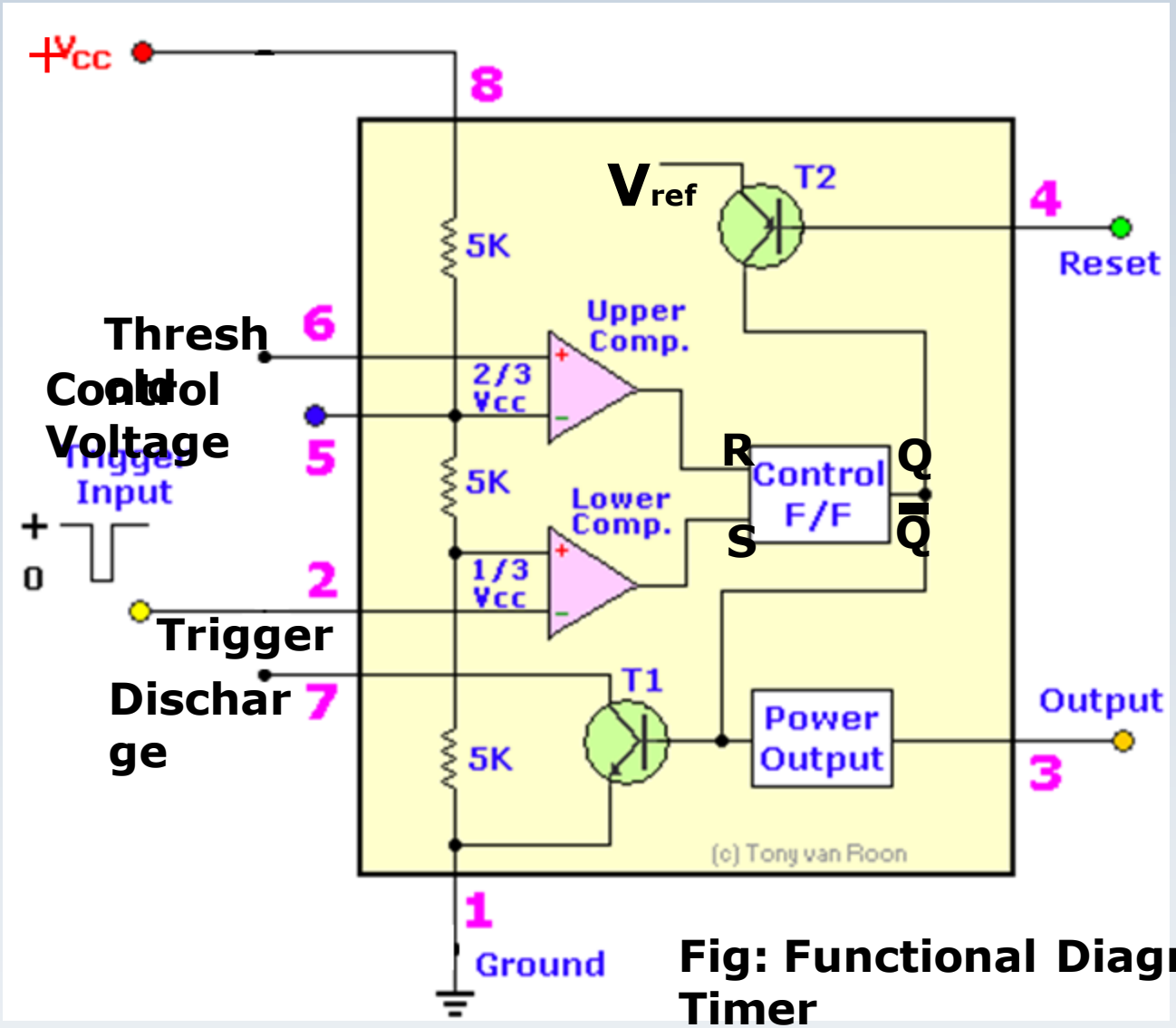


Fig: Functional Diagram of 555 Timer

Truth Table

S	R	Q	Q
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	X	X

OPERATION

- The voltage divider has three equal 5K resistors. It divides the input voltage (V_{cc}) into three equal parts.
- The two comparators are op-amps that compare the voltages at their inputs and saturate depending upon which is greater.
- The Threshold Comparator saturates when the voltage at the Threshold pin (pin 6) is greater than (2/3)V_{cc}.
- The Trigger Comparator saturates when the voltage at the Trigger pin (pin 2)[62]is

Features of IC 555 Timer

The Features of IC 555 Timer are:

1. The 555 is a monolithic timer device which can be used to produce accurate and highly stable time delays or oscillation. It can be used to produce time delays ranging from few microseconds to several hours.

2. It has two basic operating modes: monostable and astable.

3. It is available in three packages: 8-pin metal can, 8-pin mini DIP or a 14-pin. A 14-pin package is IC 556 which consists of two 555 times.

Features of IC 555 Timer

4. The NE 555(signetics) can operate with a supply voltage in the range of 4.5v to 18v and output currents of 200mA.

5. It has a very high temperature stability, as it is designed to operate in the temperature range of -55^{o}c to 125^{o}c.

6. Its output is compatible with TTL, CMOS and Op-Amp circuits.

Application of IC 555 Timer

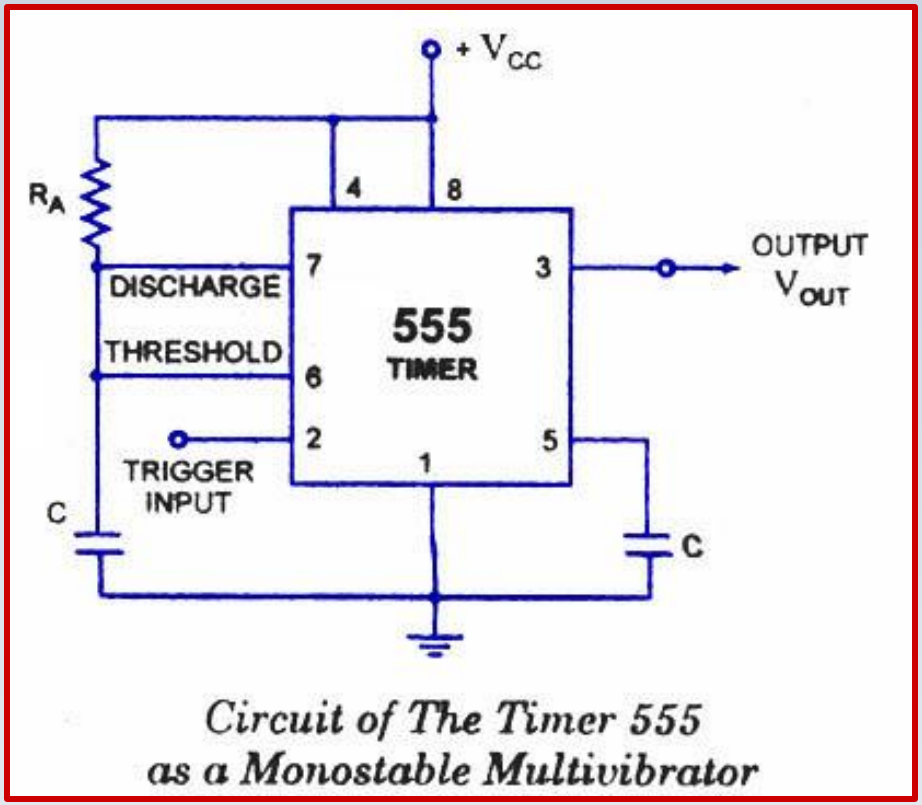
- Pulse Generation
- Time Delay Generation
- Precision Timing
- Sequential Timing
- Pulse Width Modulation (PWM)

555 Timer operating modes

- The 555 has three operating modes:

  1. Monostable Multivibrator
  2. Astable Multivibrator
  3. Bistable Multivibratior

555 Timer as Monostable Multivibrator

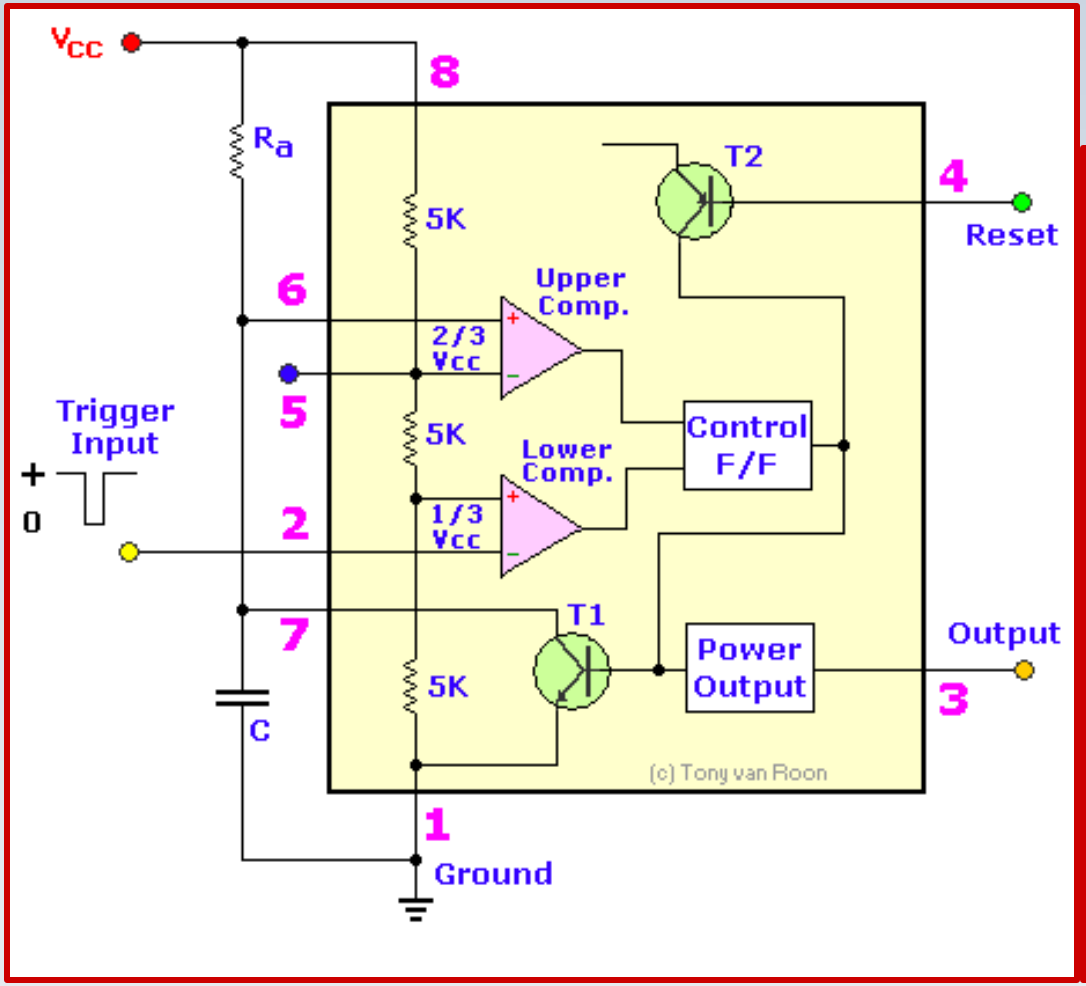


Circuit of The Timer 555 as a Monostable Multivibrator

Description:

- In the standby state, FF holds transistor Q_1 ON, thus clamping the external timing capacitor C to ground. The output remains at ground potential. i.e. $V_{cc}/3$, the FF is set, i.e. Low.
- As the trigger passes through Q bar=0, then the transistor Q_1 OFF and the short circuit across the timing capacitor C is released. As Q

555 Timer as Monostable Multivibrator



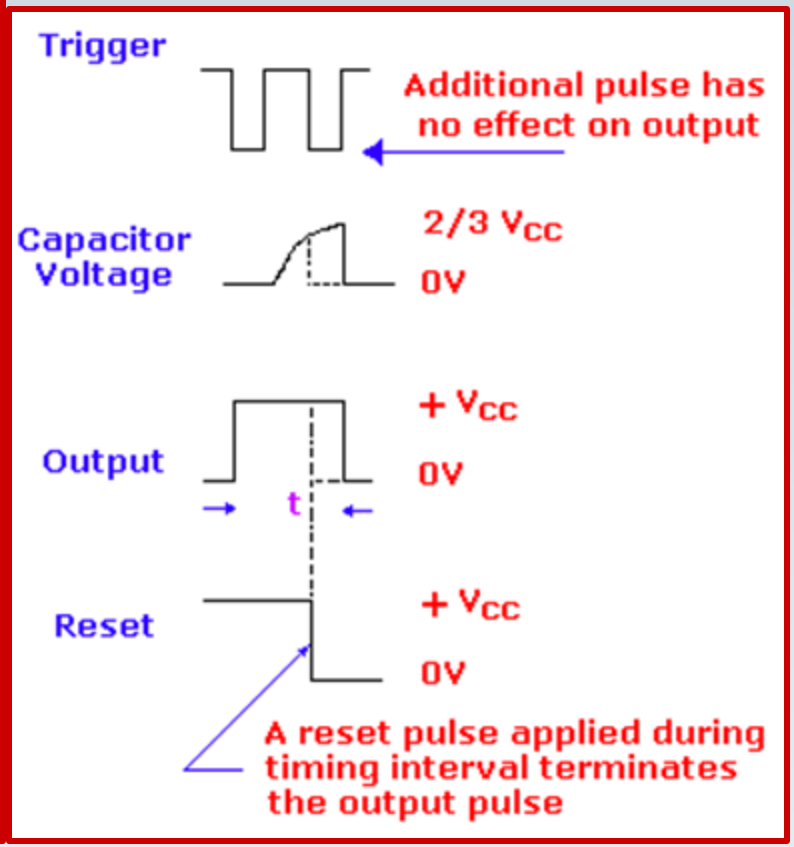


Fig (a): Timer in Monostable Operation with Functional Diagram

Fig (b): Output wave Form of Monostable

Monostable Multivibrator-Description

- Voltage across it rises exponentially through R towards V_{cc} with a time constant RC.
- After Time Period T, the capacitor voltage is just greater than $2V_{cc}/3$ and the upper comparator resets the FF, i.e. R=1, S=0. This makes Q bar =1, C rapidly to ground potential.
- The voltage across the capacitor as given by,

$$v_C = V_{CC}(1 - e^{-t/RC})$$

at $t = T, v_C = \frac{2}{3}V_{CC}$

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-T/RC})$$

$$T = RC\ln(\frac{1}{3}) \Rightarrow T = 1.1RC\,\text{sec}$$

- If –ve going reset pulse terminal (pin 4) is applied, then transistor Q_2-> OFF, Q_1-> ON & the external timing capacitor C is immediately discharged.

Behavior of the Monostable Multivibrator

- The monostable multivibrator is constructed by adding an external capacitor and resistor to a 555 timer.
- The circuit generates a single pulse of desired duration when it receives a trigger signal, hence it is also called a one-shot.
- The time constant of the resistor-capacitor

  combination determines the length of the pulse.

Uses of the Monostable Multivibrator

- Used to generate a clean pulse of the correct height and duration for a digital system
- Used to turn circuits or external components on or off for a specific length of time.
- Used to generate delays.
- Can be cascaded to create a variety of sequential timing pulses. These pulses can allow you to time and sequence a number of related operations.

Applications in Monostable Mode

1. Missing Pulse Detector.
2. Linear Ramp Generator.
3. Frequency Divider.
4. Pulse Width Modulation.

1.Missing Pulse Detector

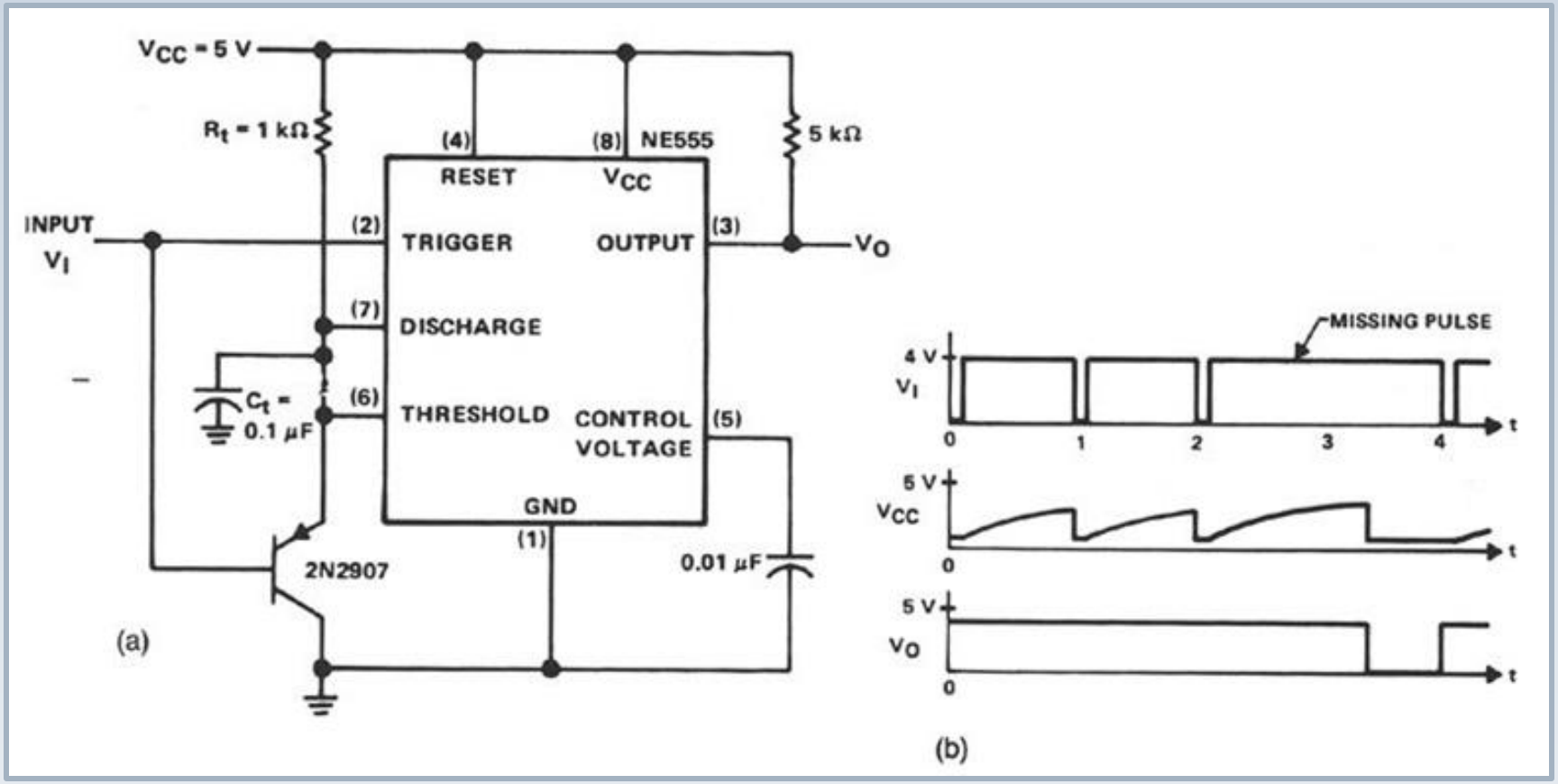


Fig (a) : A missing Pulse Detector Monostable Circuit
Fig (b) : Output of Missing Pulse Detector

Missing Pulse Detector-Description

- When input trigger is Low, emitter-base diode of Q is forwarded biased capacitor is clamped to 0.7v(of diode), output of timer is HIGH width of T o/p of timer > trigger pulse width.
- T=1.1RC select R & C such that T > trigger pulse.
- Output will be high during successive coming of input trigger pulse. If one of the input trigger pulse missing trigger i/p is HIGH, Q is cut off, timer acts as normal monostable state.
- It can be used for speed control and measurement.

3.Frequency Divider

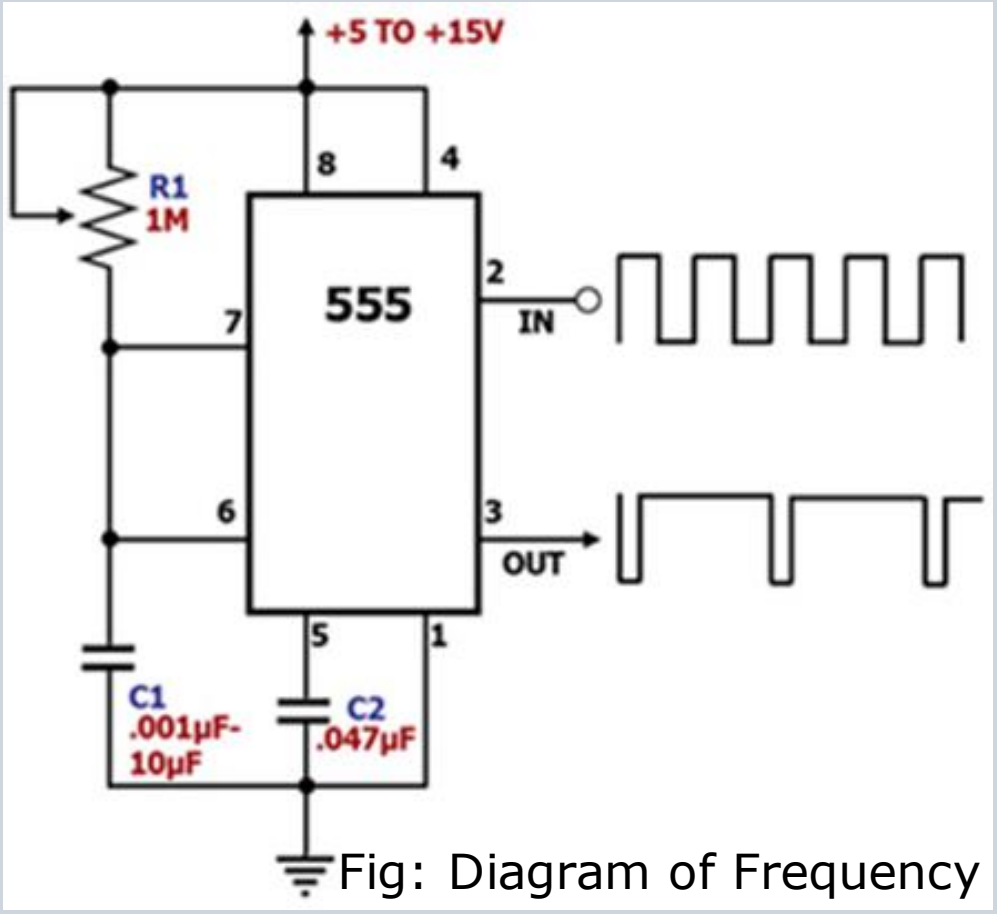


Fig: Diagram of Frequency Divider

Description:

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal.

The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH(because of greater timing interval) for next

Astable Multivibrator

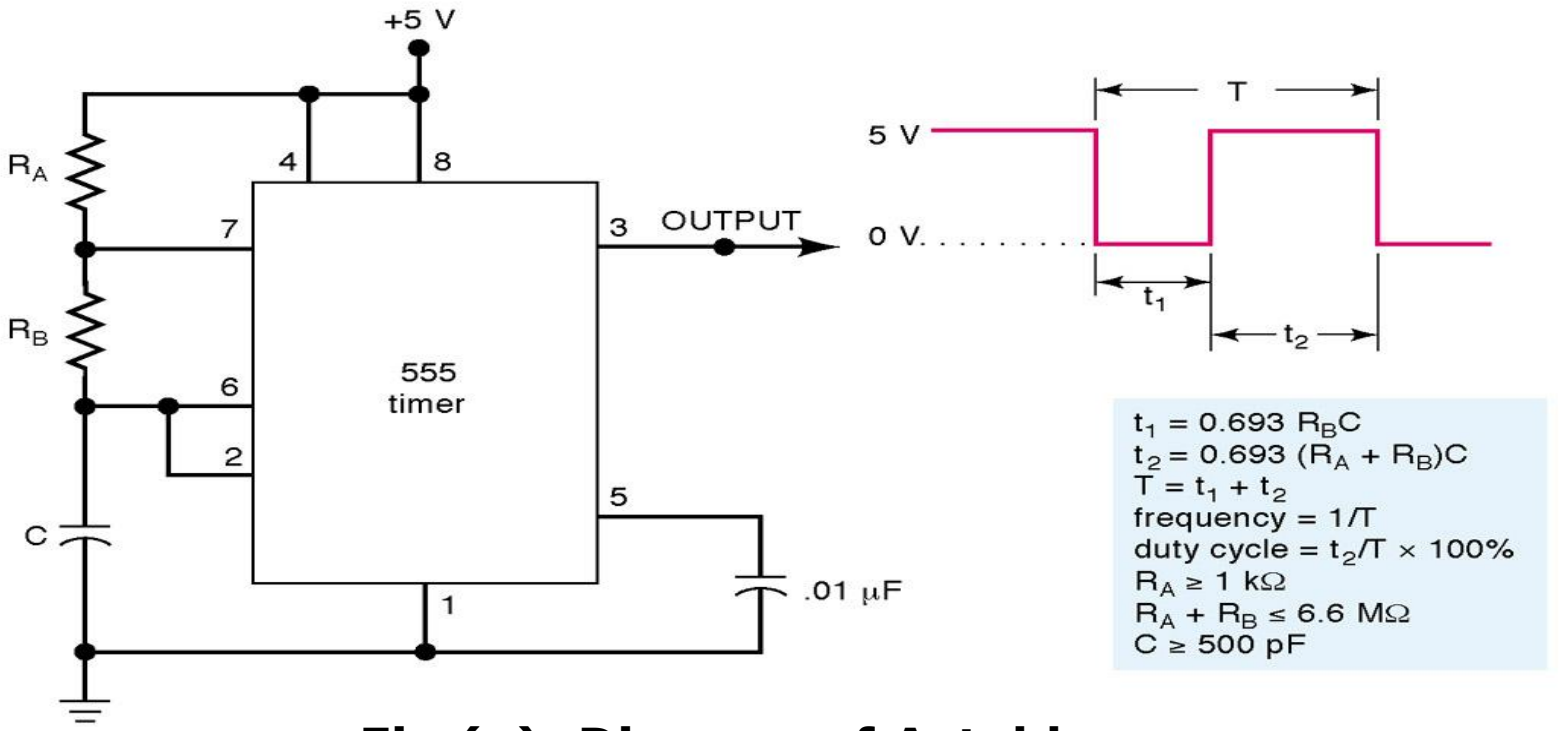


Fig (a): Diagram of Astable Multvibrator

1 – Ground
2 – Trigger
3 – Output
4 – Reset (Set HIGH for normal operation)
5 – FM Input (Tie to gnd via bypass cap)
6 – Threshold
7 – Discharge
8 – Voltage Supply (+5 to +15 V)

Astable Multivibrator

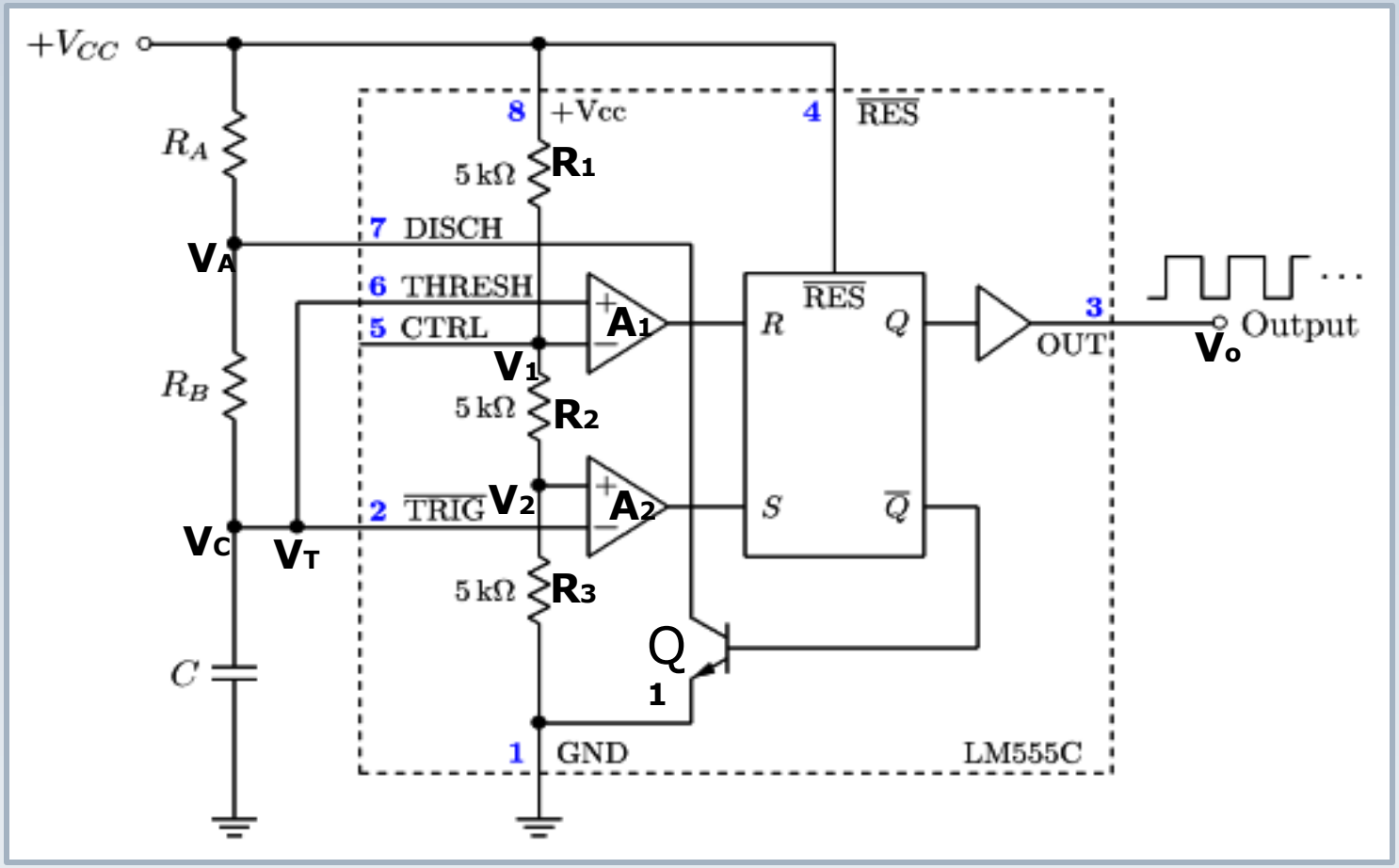


Fig (b): Functional Diagram of Astable Multivibrator using 555 Timer

Astable Multivibrator- Description

- Connect external timing capacitor between trigger point (pin 2) and Ground.
- Split external timing resistor R into R_A & R_B, and connect their junction to discharge terminal (pin 7).
- Remove trigger input, monostable is converted to Astable multivibrator.
- This circuit has no stable state. The circuits changes its state alternately. Hence the operation is also called free running oscillator.

Astable 555 Timer Block Diagram Contents

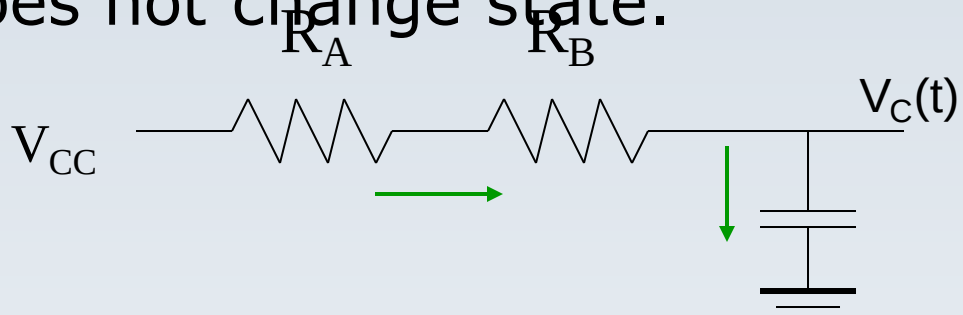
- Resistive voltage divider (equal resistors) sets threshold voltages for comparators

  $V_1 = V_{TH} = 2/3\ V_{CC}$ $V_2 = V_{TL} = 1/3\ V_{CC}$

- Two Voltage Comparators
  - For A_1, if $V_+ > V_{TH}$ then R =HIGH
  - For A_2, if $V_- < V_{TL}$ then S = HIGH
- RS FF
  - If S = HIGH, then FF is SET, $\bar{Q}$ = LOW, Q_1 OFF, V_{OUT} = HIGH
  - If R = HIGH, then FF is RESET, $\bar{Q}$ = HIGH, Q_1 ON, V_{OUT} = LOW
- Transistor Q_1 is used as a Switch

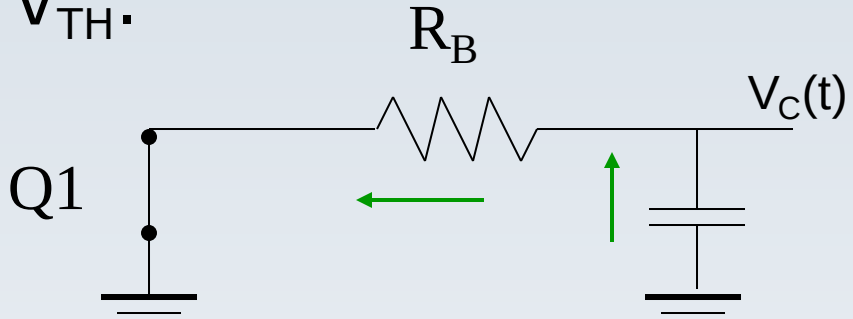
Operation of a 555 Astable

1) Assume initially that the capacitor is discharged.
   a) For A_1, $V_+ = V_C = 0V$ and for A_2, $V_- = V_C = 0V$, so R=LOW, S=HIGH, = LOW , Q1 OFF, $V_{OUT} = V_{CC}$
   b) Now as the capacitor charges through R_A & R_B, eventully $V_C > V_{TL}$ so R=LOW & S=LOW. FF does not change state.



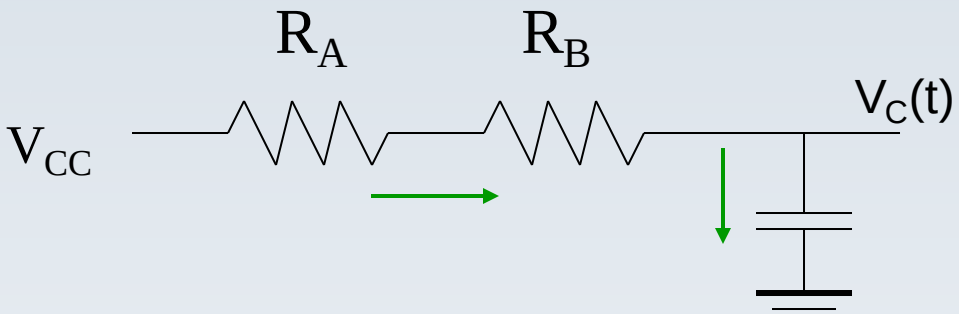
Operation of a 555 Astable Continued……

2) Once $V_C \geq V_{TH}$
   a) R=HIGH, S=LOW, $\bar{Q}$ = HIGH ,Q1 ON, V_{OUT} = 0
   b) Capacitor is now discharging through R_B and Q_1 to ground.
   c) Meanwhile at FF, R=LOW & S=LOW since $V_C < V_{TH}$.

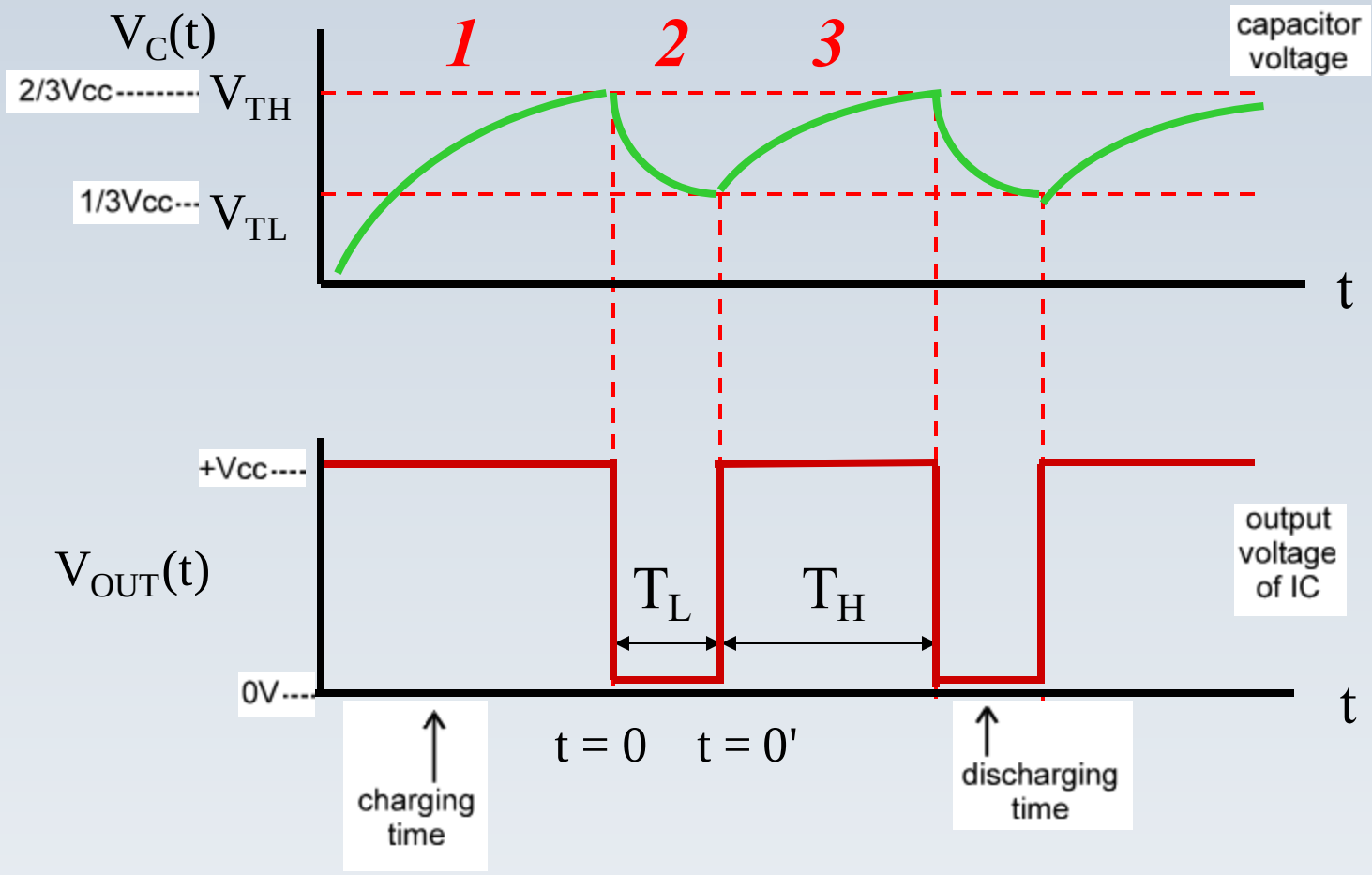


Operation of a 555 Astable Continued.....

3) Once $V_C < V_{TL}$
   a) R=LOW, S=HIGH, $\bar{Q}$ = LOW , Q1 OFF, $V_{OUT} = V_{CC}$
   b) Capacitor is now charging through R_A & R_B again.



Timing Diagram of a 555 Astable



Astable Multivibrator- Analysis

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by,

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to change from 0 to $2V_{cc}/3$ is, $V_C = \frac{2}{3}V_{CC}$

$$\frac{2V_{CC}}{3} = V_{CC}(1 - e^{-t_1/RC}) \Rightarrow t_1 = 1.09RC$$

The time t_2 to charge from 0 to $V_{cc}/3$ is $V_C = \frac{1}{3}V_{CC}$

$$\frac{V_{CC}}{3} = V_{CC}(1 - e^{-t_2/RC}) \Rightarrow t_2 = 0.405RC$$

So the time to change from $V_{cc}/3$ to $2V_{cc}/3$ is, $t_{HIGH} = t_1 - t_2 = 1.09RC - 0.405RC = 0.69RC$

So, for the given circuit, $t_{HIGH} = 0.69(R_A + R_B)C$ ..... Charging time

The output is low while the capacitor discharges from $2V_{cc}/3$ to $V_{cc}/3$ and the voltage across the capacitor is given by,

$$\frac{V_{CC}}{3} = \frac{2}{3}V_{CC}e^{-t/RC}$$

Contd...

Astable Multivibrator- Analysis

After solving, we get, t=0.69RC

For the given circuit, $t_{LOW} = 0.69 R_B C$ …… Discharging time

Both R_A and R_B are in the charge path, but only R_B is in the discharge path.

∴ The total time period, $T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C + 0.69 R_B C$

$$\Rightarrow T = 0.69[(R_A + R_B)C + R_B C] = 0.69(R_A + R_B + R_B)C = 0.69(R_A + 2R_B)C$$

Frequency, $f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C} = \frac{1.45}{(R_A + 2R_B)C}$ …….1.45 is Error Constant

Duty Cycle,

$$\%D = \frac{t_{HIGH}}{T} X100 = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} X100 = \frac{(R_A + R_B)}{(R_A + 2R_B)} X100$$

$$\%D = \frac{t_{LOW}}{T} X100 = \frac{0.69 R_B C}{0.69(R_A + 2R_B)C} X100 = \frac{R_B}{(R_A + 2R_B)} X100$$

Behavior of the Astable Multivibrator

- The astable multivibrator is simply an oscillator. The astable multivibrator generates a continuous stream of rectangular off-on pulses that switch between two voltage levels.
- The frequency of the pulses and their duty cycle are dependent upon the RC network values.
- The capacitor C charges through the series resistors R_A and R_B with a time constant $(R_A + R_B)C$.
- The capacitor discharges through R_B with a

Uses of the Astable Multivibrator

- Flashing LED's
- Pulse Width Modulation
- Pulse Position Modulation
- Periodic Timers
- Uses include LEDs, pulse generation, logic clocks, security alarms and so on.

Applications in Astable Mode

1. Square Generator
2. FSK Generator
3. Pulse Position Modulator

1. FSK Generator

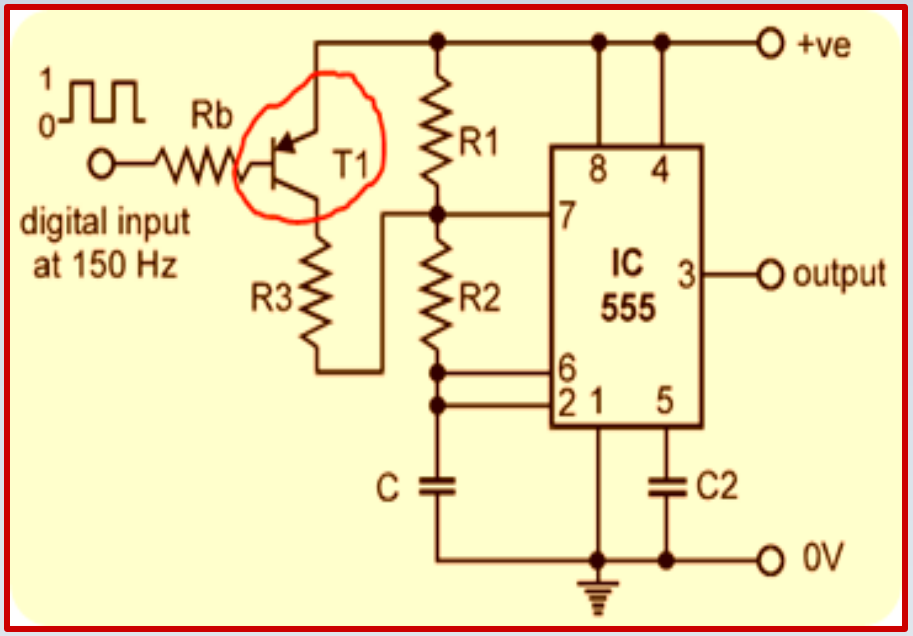


Fig: FSK Generator

Description:

- In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called Frequency Shift

Contd....

FSK Generator

- A 555 timer is astable mode can be used to generate FSK signal.
- When input digital data is HIGH, T_1 is OFF & 555 timer works as normal astable multivibrator.

The frequency of the output wave form given by,

$$f_o = \frac{1.45}{(R_1 + 2R_2)C}$$

When input digital is LOW, Q_1 is ON then R_3 parallel R_1

$$\therefore f_o = \frac{1.45}{(R_3 \| R_1 + 2R_2)C}$$

2. Pulse Position Modulator

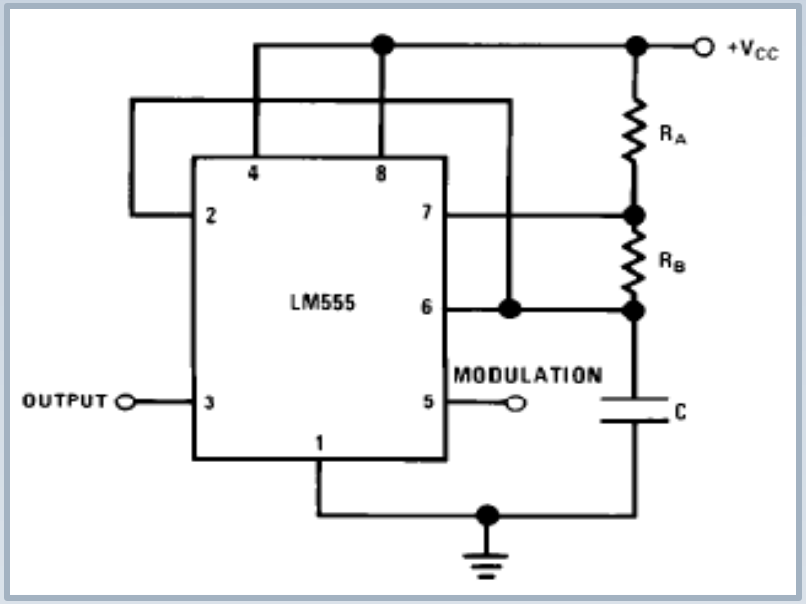


Fig (a): Pulse position

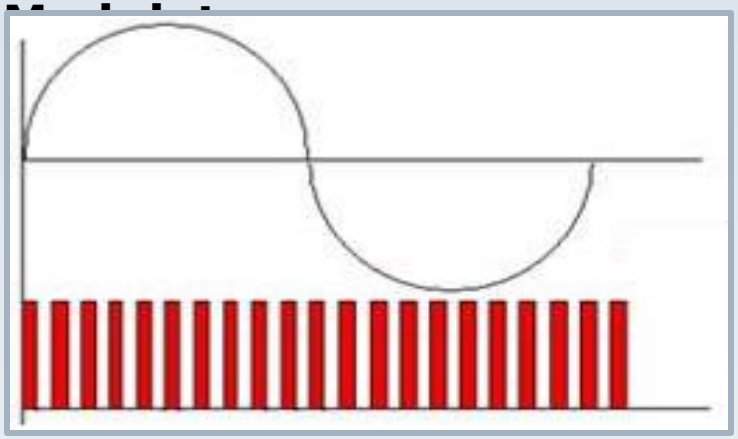


Fig (b): Output Wave Form of PPM

Description:

- The pulse position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation.
- The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.
- The output waveform that the

Comparison of Multivibrator Circuits

Monostable Multivibrator	Astable Multivibrator
1. It has only one stable state	1. There is no stable state.
2. Trigger is required for the operation to change the state.	2. Trigger is not required to change the state hence called free running.
3. Two comparators R and C are necessary with IC 555 to obtain the circuit.	3. Three components R_A, R_B and C are necessary with IC 555 to obtain the circuit. $f_o = \frac{1}{T} = \frac{1.45}{(R_A+2R_B)C}$
4. The pulse width is given by T=1.1RC Seconds	4. The frequency is given by,
5. The frequency of operation is controlled by frequency of	5. The frequency of operation is controlled by R_A, R_B & C.

Thank You

UNIT-V AMPLIFIERS

Prepared by

S.JAYACHITRA,AP/ECE

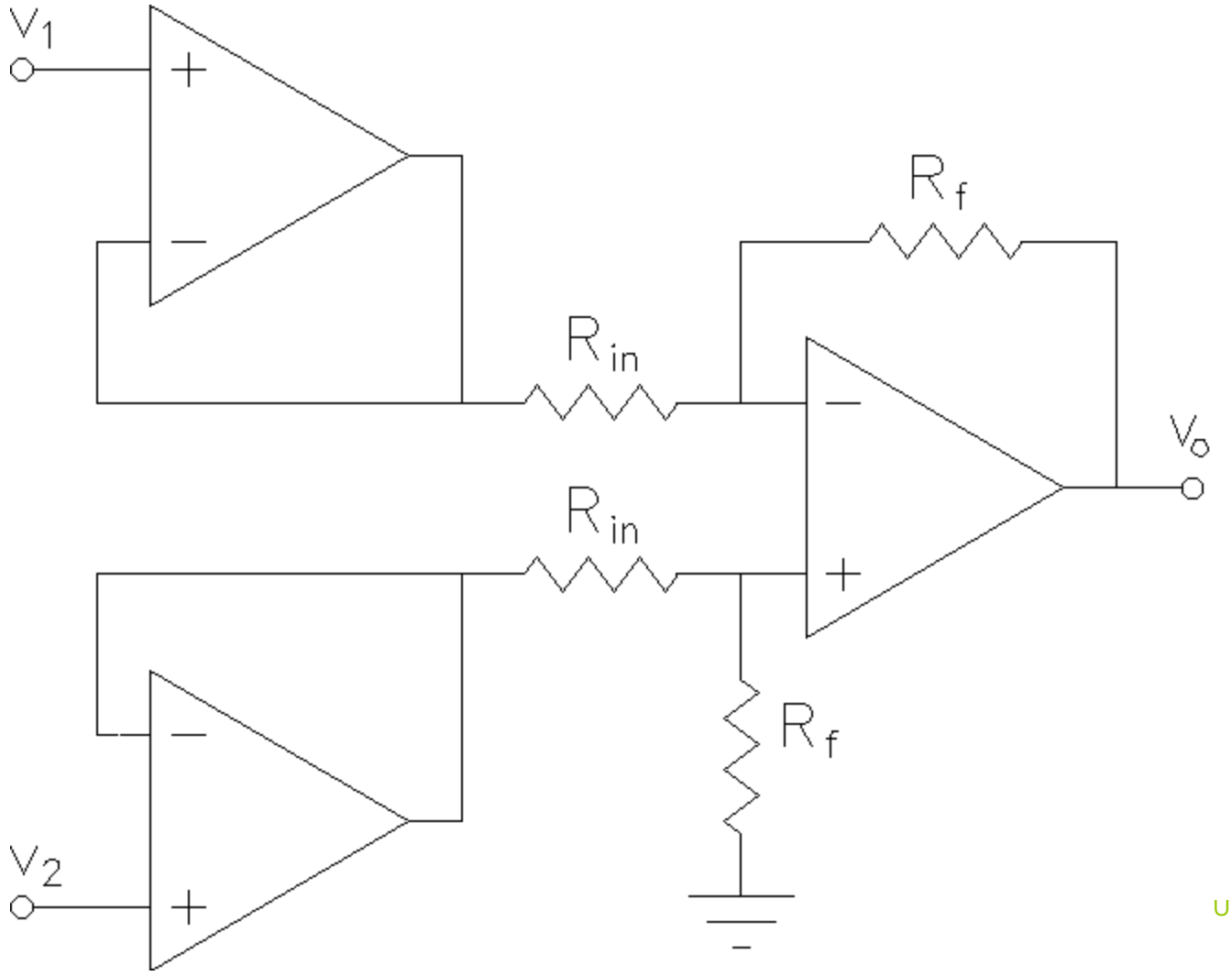
Instrumentation Amplifier

- An instrumentation amplifier is used to amplify very low-level signals, rejecting noise and interference signals. Examples can be heartbeats, blood pressure, temperature, earthquakes and so on.
- In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

Features of instrumentation amplifier

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

Instrumentation Amplifier



- Current flowing in resistor R is I= (V1-V2)/R and it flow through R’ in the direction shown, Voltage.
- at non-inverting terminal op-amp A3 is R2V1’/(R1+R2). By superposition theorem, Vo= (R2/R1)V1+(1+R2/R1)(R2V2/(R1+R2)=R2/R1(V1’-V2’); V1’= R’I+V1=R’/R(V1-V2)+V1 V2’= R’I+V1=R’/R(V1-V2)+V2; V0= (R2/R1)[(2R’/R(V2-V1)+ (V2-V1)]= (R2/R1)[(1+2R’/R)(V2-V1) In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

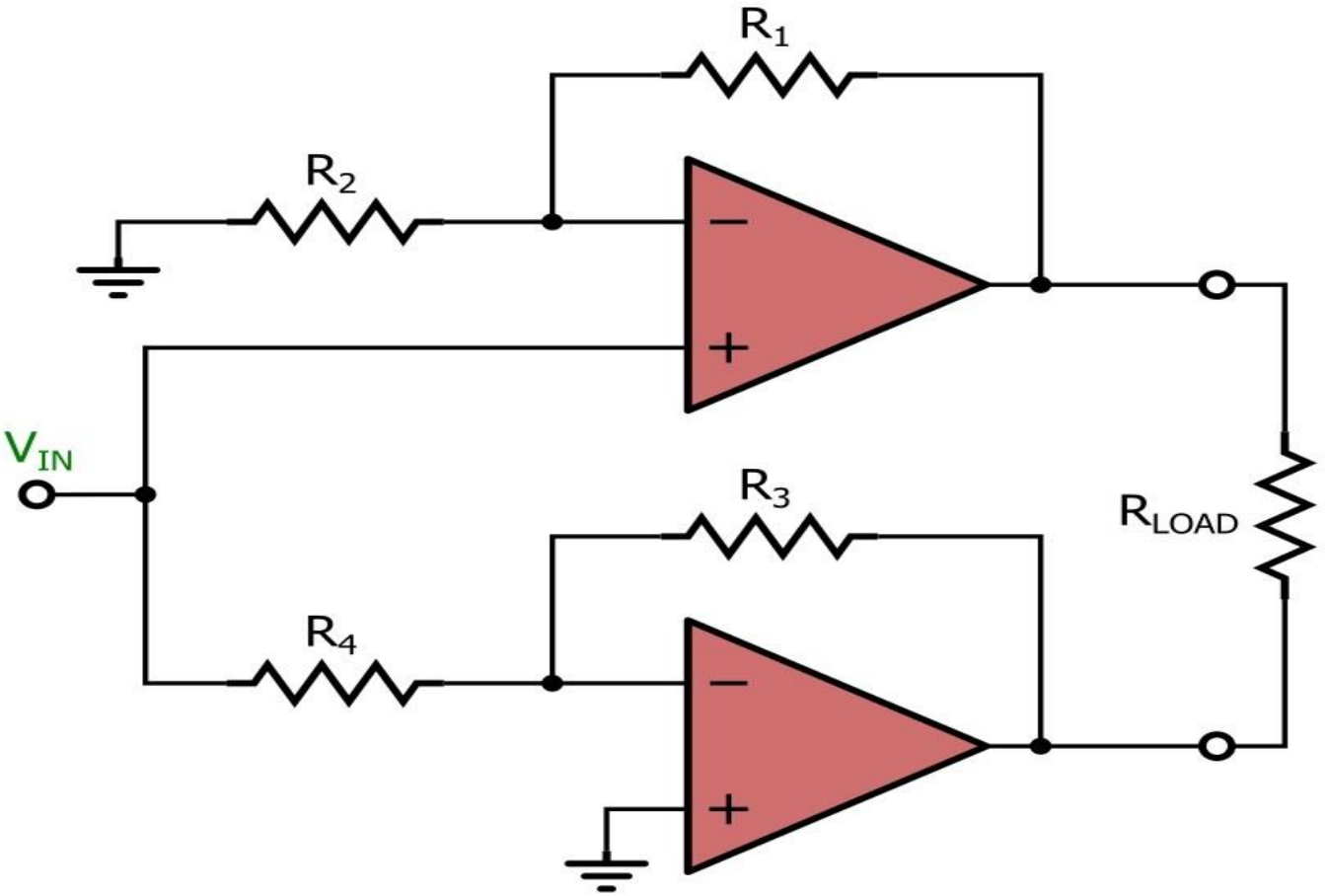
- The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.
- **Applications of instrumentation amplifier with the transducer bridge:**

a) Temperature indicator,
b) Temperature controller and
c) Light intensity meter .

Advantages of Instrumentation Amplifier

- The input impedance is very high due to the emitter follower configurations of amplifiers 1 and 2
- The output impedance of the instrumentation amplifier is very low due to the difference amplifier3.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

Bridge Amplifier



- The input signal is fed to two op-amp circuits, one noninverting, the other inverting; the resistors are chosen so that both amplifiers have the same gain magnitude.
- The load is connected between the outputs of the two amplifiers; note that the load is “floating,” i.e., it has no direct connection to the ground node. As you have probably figured out by now, the bridge amplifier results in a factor-of-two increase in the voltage across the load.

- The standard bridge amplifier shown here is not a single-supply circuit.
- Both op-amps have an input terminal that is referenced to ground; thus, a ground-referenced sinusoidal input signal would require both op-amps to generate negative output voltages, and this of course, is quite impossible when the op-amp's negative-supply pin is connected to ground.

Bioelectric Amplifiers

- The bioelectric amplifiers are used to amplify the bioelectric signals. The bioelectric signals measured from various body parts are having an amplitude ranging from mVs to µVs.

- So it is necessary to amplify the extremely low amplitude signals for the analysis of the biological data. It is for this purpose that the bioelectric amplifiers are used. Usually we use operational amplifiers as bioelectric amplifiers due to its high gain and other versatile features.

- 1. The gain of the bioelectric amplifier may be low, medium or high depending on the type of amplifier and the signal to be amplified.
- For example the low gain amplifiers are used for the measurement of action potential, medium gain amplifiers are used for the amplification of ECG waveform and the high gain amplifiers are used for EEG signal amplification.

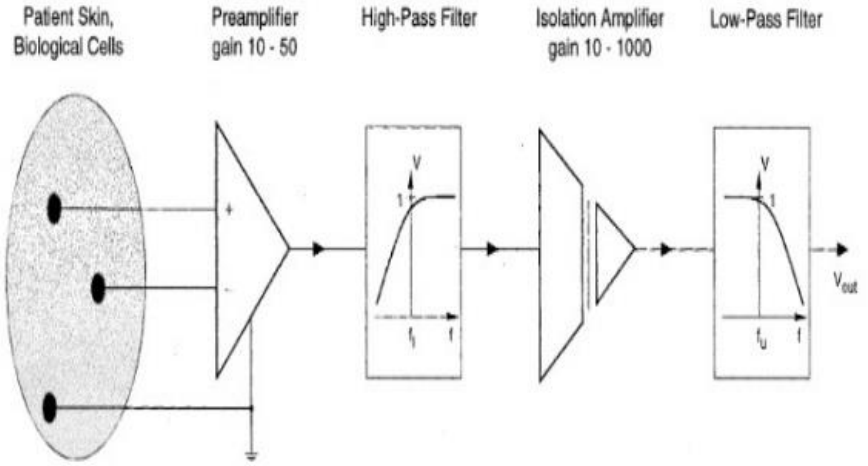
2. The bioelectric amplifiers may be ac coupled or dc coupled.

3. The frequency response of a bioelectric amplifier range from very low frequency to high frequency range.

4. Bioelectric amplifiers have differential input and single ended output.

5. High CMRR and extremely high input impedance.

Bio Electric Amplifiers



- Two important parameters of bioelectric amplifiers are noise and drift. We have to avoid the effect of both these parameters on bioelectric amplifiers.
- Drift is the change in output due to the change in temperature. Noise is the thermal noise generated in electronic devices.
- Both these problems can be avoided by proper design to make the bioelectric amplifier more effective.

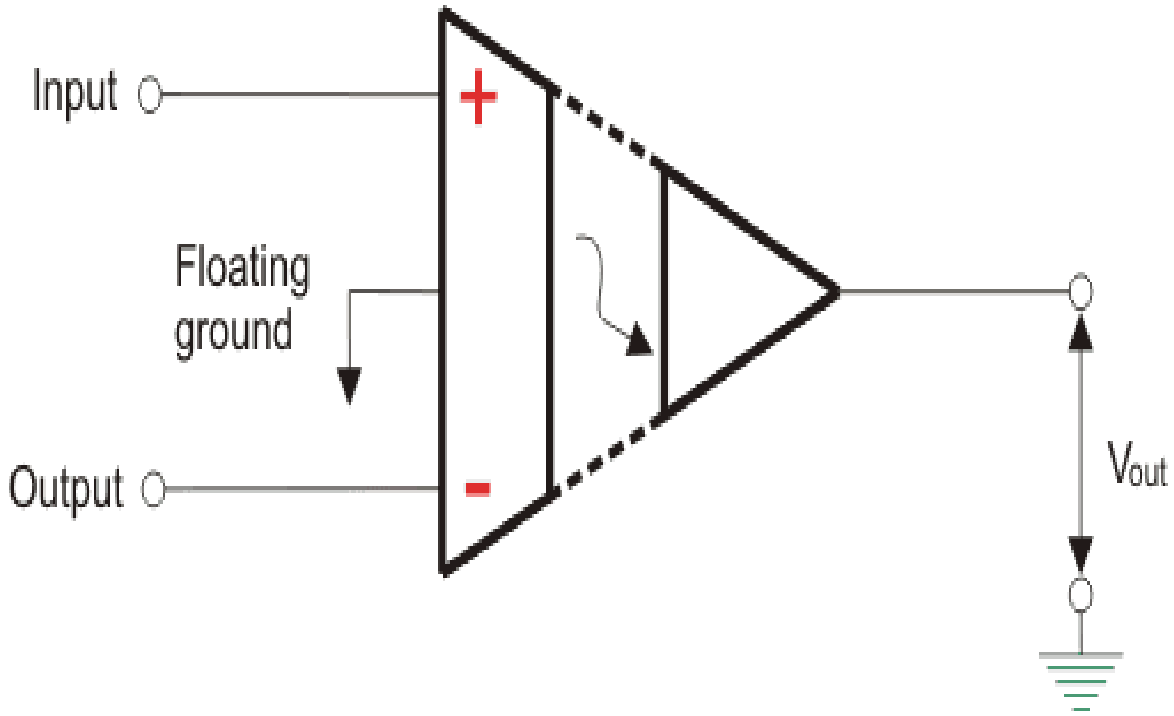
Isolation Amplifier

- Isolation amplifiers are known as Pre-amplifier isolation circuits. An isolation amplifier increases the input impedance of a patient monitoring system.
- Provides a way to link a fixed ground to a floating ground.
- Isolates the DSP from the high voltage associated with the power amplifier.
- It also helps to isolate the patient from the device. Using the isolation amplifier prevents accidental internal cardiac shock. It provides up to 1012 Ω insulation between the patient and the power line in the hospital.

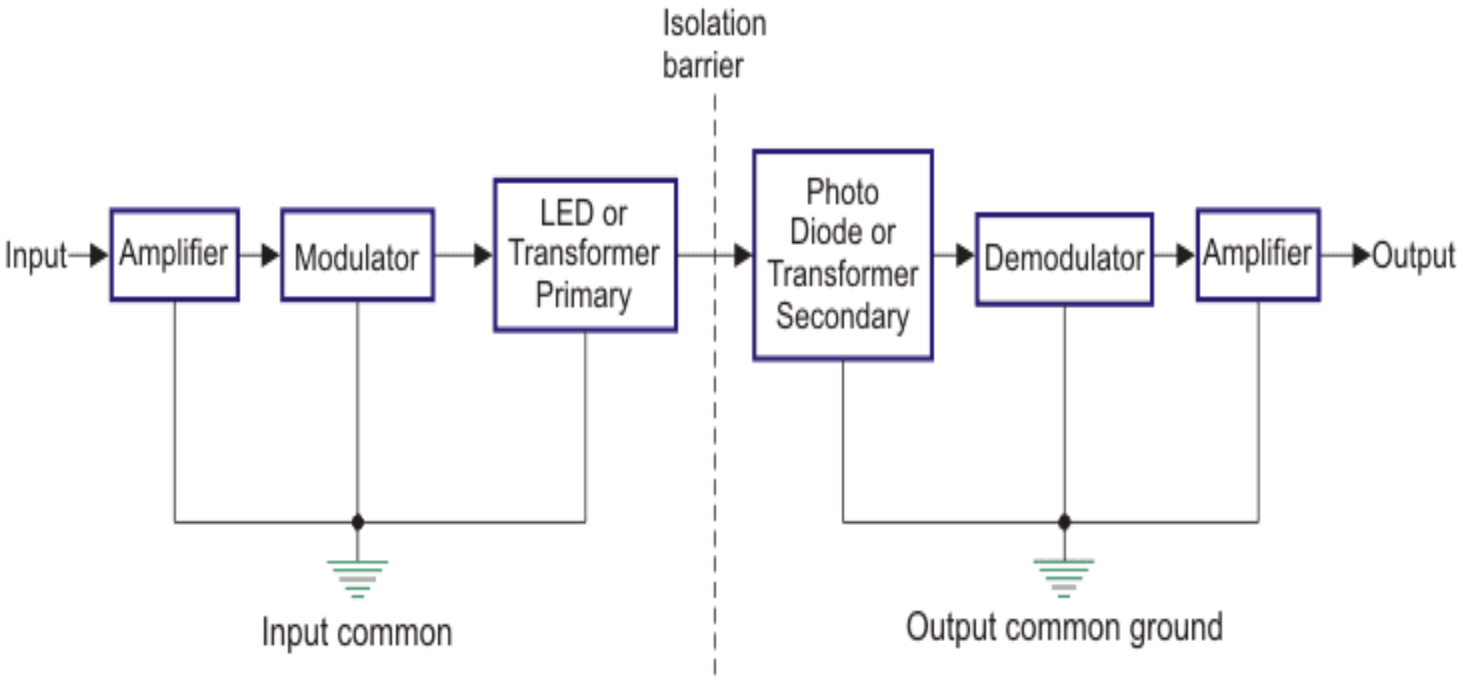
ISOLATION AMPLIFIER

Purposes

- To break ground to permit incompatible circuits
- to be interfaced together while reducing noise
- To amplify signals while passing only low leakage current to prevent shock to people or damage to equipment
- To withstand high voltage to protect people, circuits, and equipment



Symbol of Isolation Amplifier



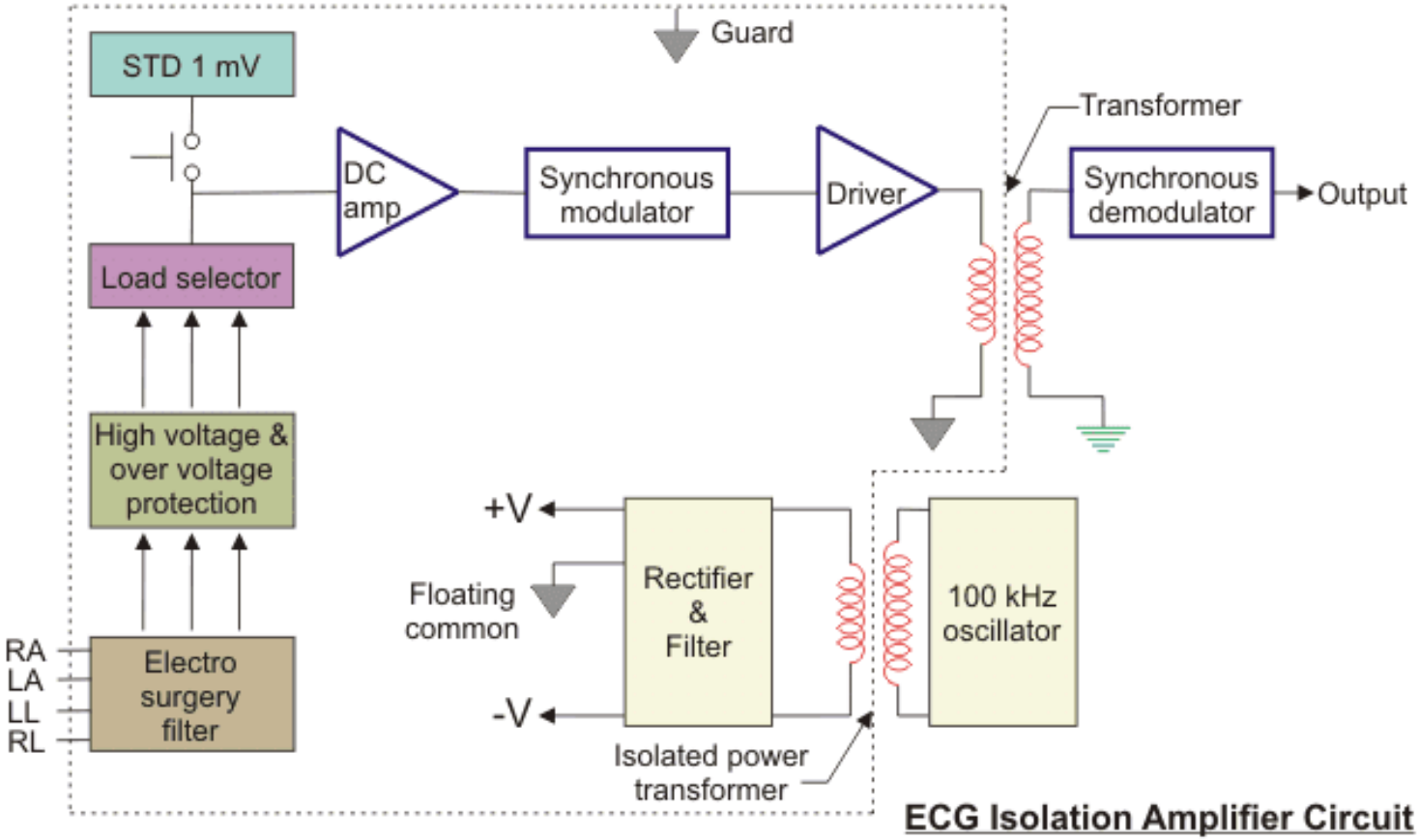
Block Diagram of Isolation Amplifier

- The electrical signals are obtained with electrodes. The signals received goes to the amplifier block, where signals amplification occurs. After amplification, the signal enters the modulation block.
- When either it goes to the isolation barrier, optical cable or transformer can be used. If in case of optical cable, modulator output travels to LED.
- The LED converts electrical signals into light energy. If the transformer acts an isolation barrier, modulator output connects the primary winding of the transformer.

- Energy from primary transfers to the secondary winding based on the mutual induction principle. At the next stage, secondary output enters the demodulation block. Finally, the amplified demodulated signal is obtained.

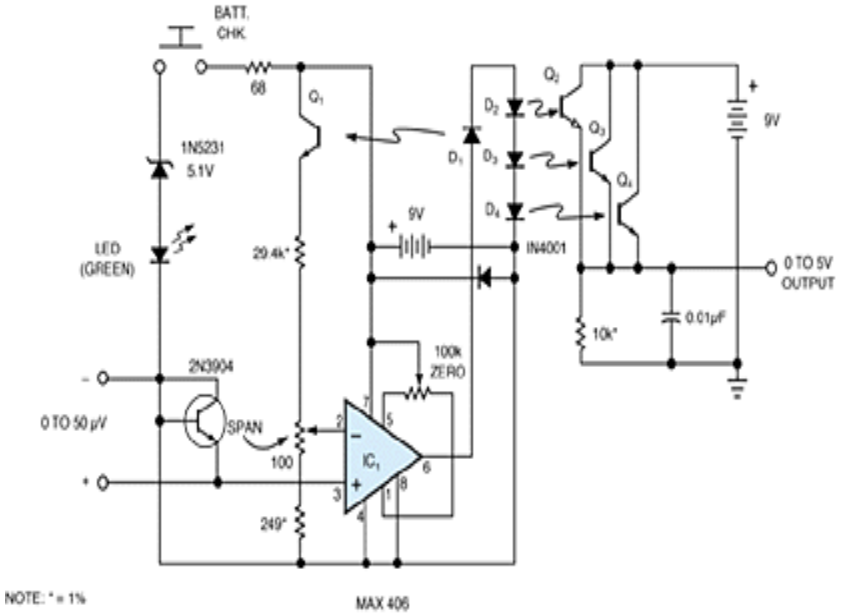
ECG Isolation Amplifier

- During ECG measurement, signals generated from all leads are sent to the low pass filter.
- This filter is named as Electro surgery filters because it decreases the interference between electrosurgery and radio frequency.
- Next block is the high voltage and overvoltage protection that can withstand large voltage during defibrillation.
- Proceeding further, it goes to Lead Selector Switch block, which selects the required configuration.
- Lead selection output goes to the DC amplifier. We have a transformer, whose primary winding is connected to the oscillator and secondary to rectifier and filter.
- ECG signal is modulated with the Synchronous modulator. The second transformer delivers the output from the synchronous modulator to the synchronous demodulator.
- The output from the demodulator is fed as input to the power amplifier.



ECG Isolation Amplifier Circuit

Battery Powered amplifiers

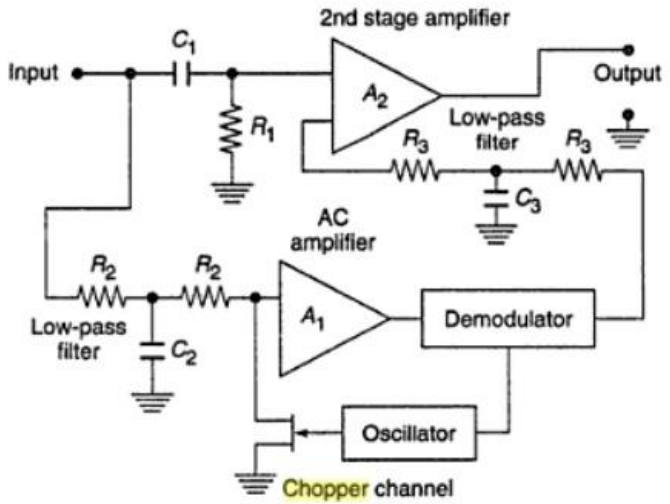


Chopper Stabilized amplifier

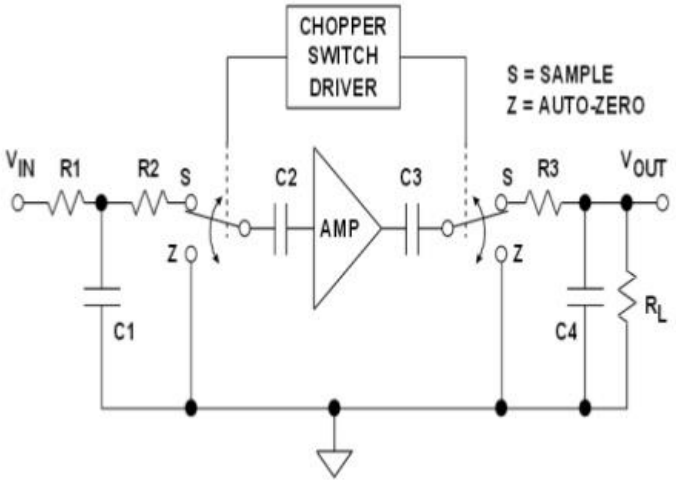
Chopper Stabilized amplifiers

- Chopper stabilization constantly corrects input offset voltage errors, including both errors in the initial input offset voltage and errors in input offset voltage due to time, temperature, and common-mode input voltage.
- A chopper-stabilized amplifier is actually two amplification paths in parallel.
- A high-accuracy, low-frequency path (A2) incorporates high gain and chopping, while high-frequency signals are amplified by the parallel wideband amplifier A1.
- The outputs of both stages are subtracted in a summer amplifier, whose output is fed back to the inputs of both amplifiers through a feedback resistor.

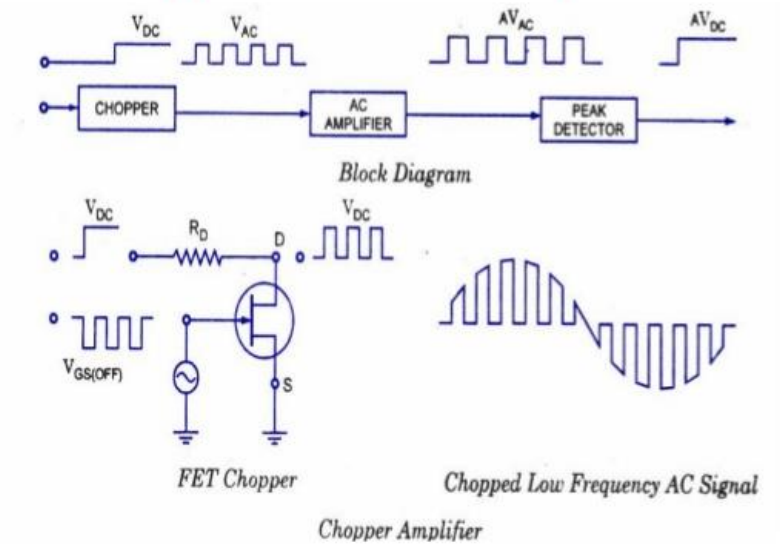
Chopper Stabilized Amplifiers



Chopper Stabilized amplifiers



Chopper Stabilized amplifiers



Chopper Stabilized amplifiers

- Two problems arise when we tries to record low level bio-potentials.
- Noise
- DC Drift
- These are worse , if we are using high gain amplifiers to amplify the weak bio-potentials.
- Noises produced in amplifier circuit and human body makes the problem worse.
- Drift is the change in gain or dc offset caused by thermal effects on amplifier components.

Chopper Stabilized amplifiers

- Drift can be minimized with the use of negative feedback.
- This can be avoid by convert a DC (or near dc, low frequency analog) signal to an AC signal that will pass through the amplifier.
- The solution is to chop or sample the analog signal at a frequency that will pass through the AC coupled amplifier.

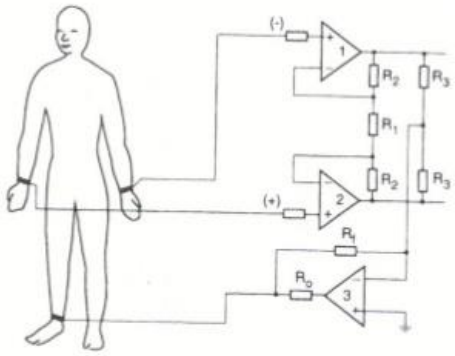
Input Guarding

Input Guarding

- Physiological signals are low amplitude signals.
- In most cases physiological signals accompanied by large CM signals.
- If Op Amps are used, both differential (E)and common mode (Ecm) signals are present.
- The op amp cannot distinguish artifact from real signal and C.M signal.
- To avoid these problem, input guarding is used.
- Here , we are placing a shield at the CM signals.
- Input cable is shielded to avoid CM signals.

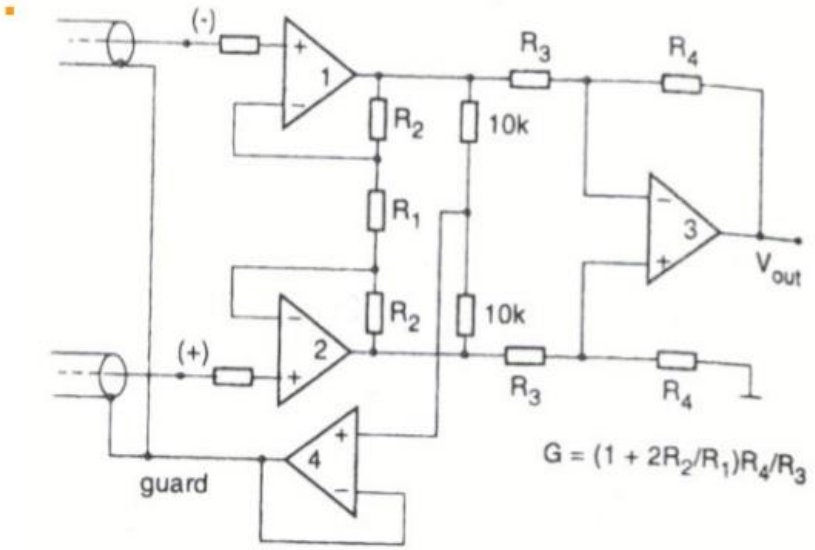
Input Guarding

- Technique for increase both the input impedance of the amplifier of bio-potentials and the CMRR.
- Instrumentation amplifier providing input guarding
-



Driven-right-leg circuit reducing common-mode interference.

Input Guarding



Questions
A differential amplifier
When a differential amplifier is operated single-ended,
In differential-mode
In the common-mode
The common-mode gain is
The differential gain is
If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is
With zero volts on both inputs, an OPamp ideally should have an output
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is
The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is
For an OP-amp with negative feedback,the output is
The use of negative feedback
Negative feedback
A certain non-inverting amplifier has R_i of 1 kΩ and R f of 100 kΩ. The closed-loop voltage gain is
A certain non-inverting amplifier has R_i of 1 kΩ and R f of 100 kΩ. If feedback resistor is open, the voltage gain
A certain inverting amplifier has a closed loop voltage gain of 25. The OP-amp has an open-loop voltage gain of 100,000. If an OP-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain
A voltage follower
The OP-amp can amplify
The input offset current equals the

The tail current of a differential amplifier is
The node voltage at the top of the tail resistor is closest to.
The tail current in a differential amplifier equals
A common-mode signal is applied to
The common-mode voltage gain is
The input stage of an OP-amp is usually a
Current cannot flow to ground through
Which of the following electrical characteristics is not exhibited by an ideal op-amp?
An ideal op-amp requires infinite bandwidth because
Ideal op-amp has infinite voltage gain because
Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages
How will be the output voltage obtained for an ideal op-amp?
Which is not the ideal characteristic of an op-amp?
Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
Which factor determine the output voltage of an op-amp?
The opamp can amplify
In a nonlinear op-amp circuit, the
The input signal for an instrumentation amplifier usually comes from
In a differential amplifier, the CMRR is limited mostly by the
An instrumentation amplifier has a high
The input offset electric current equals the
When the two input terminals of a differential amplifier are grounded

A common - mode signal is applied to
The common-mode voltage gain is
The input stage of an op amp is usually a
The common - mode rejection ratio is
A 741 C has
The voltage follower has a
An opamp has a voltage gain of 200,000. If the output voltage is 1 V, the input voltage is
The 741 C has a unity - gain frequency of
The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
The voltage gain of a loaded differential amp is
At the unity-gain frequency, the open-loop voltage gain is
The tail current in a differential amplifier equals
A common - mode signal is applied to
An instrumentation amplifier has a high
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
An ideal op-amp requires infinite bandwidth because
How many leads does the TO-5 metal can package of an operational amplifier have?

Op1	Op2	Op3
is a part of an OP-amp	has one input and one output	has two outputs
the output is grounded	one input is grounded and signal is applied to the other	both inputs are connected together
opposite polarity signals are applied to the inputs	the gain is one	the outputs are of different amplitudes
both inputs are grounded	the outputs are connected together	an identical signal appears on both inputs
very high	very low	always unity
very high	very low	dependent on input voltage
1225	10,000	80 dB
equal to the positive supply voltage	equal to the negative supply voltage	equal to zero
1	2000	80 dB
700 nA	99.3 µA	49.7 µA
90 V/ µs	0.67 V/ µs	1.5 V/ µs
increased	fed back to the inverting input	fed back to the noninverting input
reduces the voltage gain of an OP-amp	makes the OP-amp oscillate	makes linear operation possible
increases the input and output impedances	increases the input impedance and bandwidth	decreases the output impedance and bandwidth
100,000	1000	101
is not affected	increases	decreases
doubles	drops to 12.5	remains at 25
has a voltage gain of 1	in non-inverting	has no feedback resistor
a.c. signals only	d.c. signals only	both a.c. and d.c. signals
difference between two base currents	average of two base currents	collector current divided by current gain

half of either collector current	equal to either collector current	two times either collector current
collector supply voltage	zero	emitter supply voltage
difference between two emitter currents	sum of two emitter currents	collector current divided by current gain
the non-inverting in	the inverting input	both inputs
smaller than differential voltage gain	equal to differential voltage gain	greater than differential voltage gain
differential amplifier	class B push-pull amplifier	CE amplifier
a mechanical ground	an a.c. ground	a virtual ground
Infinite voltage gain	Infinite bandwidth	Infinite output resistance
Signals can be amplified without attenuation	Output common-mode noise voltage is zero	Output voltage occurs simultaneously with input voltage changes
To control the output voltage	To obtain finite output voltage	To receive zero noise output voltage
$V_O = V_1 - V_2$	$V_O = A \times (V_1 - V_2)$	$V_O = A \times (V_1 + V_2)$
Amplifies the difference between the two input voltages	Amplifies individual voltages input voltages	Amplifies products of two input voltage
Input Resistance –> 0	Output impedance –> 0	Bandwidth –> ∞
8v	4v	-4v
Both positive and negative saturation voltage	Positive saturation	Negative saturation
AC signals only	DC signals only.	both AC and DC signals
opamp never saturates	feedback loop is never opened	output shape is the same as the input shape.
an inverting amplifier.	resistor	differential amplifier.
CMRR of the opamp	gain - bandwidth product.	supply voltages
output impedance	power gain.	CMMR.
average of the two base currents	collector electric current divided by electric current gain.	difference between the two base-emitter voltages
the base currents are equal.	the collector currents are equal.	an output error voltage usually exists.

the non - inverting input.	the inverting input.	both inputs.
smaller than the voltage gain.	equal to the voltage gain.	greater than the voltage gain.
differential amp.	class B push-pull amplifier.	CE amplifier.
very low.	as high as possible.	equal to the voltage gain.
a voltage gain of 100,000.	an input impedance of 2 MΩ.	an output impedance of 75 Ω
closed - loop voltage gain of unity.	small open - loop voltage gain	closed - loop bandwidth of zero.
2 micro V.	5 micro V.	10 V.
10 Hz.	20 Hz.	1 MHz.
single - ended input and single-ended output	single - ended input and differential output.	differential input and single - ended output.
less than the input bias current.	equal to zero.	less than the input offset voltage.
input offset current.	input bias current.	input offset voltage.
large than the unloaded voltage gain.	equal to R_C / r_e.	smaller than the unloaded voltage gain.
1	$A_{V(mid)}$.	zero.
difference between two emitter currents	sum of two emitter currents	collector current divided by current gain
the non - inverting input.	the inverting input.	both inputs.
output impedance	power gain.	CMMR.
1	2000	80 dB
Signals can be amplified without attenuation	Output common-mode noise voltage is zero	Output voltage occurs simultaneously with input voltage changes
8, 10, or 12	6, 8, or 10	8 or 14

Op4	Op5	Op6
answers a and c		
the output is not inverted		
only one supply voltage is used		
the output signals are in-phase		
unpredictable		
about 100		
answers b and c		
equal to the CMRR		
100,000		
none of these		
none of these		
equal to the input		
answers a and c		
does not affect impedance or bandwidth		
100		
depends on R_i		
increases slightly		
has all of these		
neither d.c. nor a.c. signals		
none of these		

equal to the difference in base currents		
tail current times base resistance		
collector voltage divided by collector resistance		
top of the tail resistor		
none of the above		
swamped amplifier		
an ordinary ground		
Infinite slew rate.		
Output can drive infinite number of device		
None of the mentioned		
$V_O = V_1 \times V_2$		
None of the mentioned		
Open loop voltage gain –> ∞		
-2v		
Supply voltage		
neither AC not DC signals.		
opamp may saturate.		
Wheatstone bridge.		
tolerance of the resistors		
supply voltage.		
difference between the two base currents.		
the ac output voltage is zero.		

he top of the tail resistor		
none of the above.		
swamped amplifier.		
equal to the common-mode voltage gain.		
all of the above.		
large closed - loop output impedance.		
1 V.		
15 MHz.		
differential input and differential output		
unimportant when a base resistor is used.		
β.		
impossible to determine.		
very large		
collector voltage divided by collector resistance		
he top of the tail resistor		
supply voltage.		
100,000		
Output can drive infinite number of device		
8 or 16		

Answer
answers a and c
one input is grounded and signal is applied to the other
opposite polarity signals are applied to the inputs
an identical signal appears on both inputs
very low
very low
answers b and c
equal to zero
100,000
700 nA
0.67 V/ µs
fed back to the inverting input
makes the OP-amp oscillate
increases the input impedance and bandwidth
101
increases
remains at 25
has all of these
both a.c. and d.c. signals
difference between two base currents

two times either collector current
zero
sum of two emitter currents
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
To obtain finite output voltage
$V_O = A \times (V_1 - V_2)$
Amplifies the difference between the two input voltages
Open loop voltage gain –> ∞
-2v
Both positive and negative saturation voltage
both AC and DC signals
opamp may saturate.
Wheatstone bridge.
gain - bandwidth product.
CMMR.
collector electric current divided by electric current gain.
the base currents are equal.

both inputs.
greater than the voltage gain.
differential amp.
as high as possible.
all of the above.
closed - loop bandwidth of zero.
5 micro V.
1 MHz.
differential input and single - ended output.
less than the input bias current.
input offset voltage.
equal to R_C / r_e.
1
sum of two emitter currents
both inputs.
CMMR.
100,000
Signals can be amplified without attenuation
8, 10, or 12

Questions
A certain non - inverting amplifier has an R_i of 1.0 kΩ and an R_f of 100 kΩ. The closed loop gain is
The bandwidth of an ac amplifier having a lower critical frequency of 1 kHz and an upper critical frequency of 10 kHz is
The bandwidth of a d c amplifier having an upper critical frequency of 100 kHz is
At the unity gain frequency, the open – loop gain is
The cutoff frequency of an op - amp equals the unity - gain frequency divided by
The initial slope of a sine wave is directly proportional to
The 741C has a unity gain frequency of
When slew rate distortion of a sine wave occurs, the output
The 741C has
When negative feed back is used , the gain-band width product of an op - amp
A summing amplifier can have
An averaging amplifier has five inputs . The ratio R_f/R_i must be
In a scaling adder, the input resistors are
In an integrator , the feed back element is a
For step - in put , the out put of an integrator is a
In a differentiator , the feed back element is a
The output of the differentiator is proportional to
Current cannot flow to the ground through
In an averaging circuit, the input resistances are
When a large sine wave drives a Schmitt trigger, the output is a
A comparator with a trip point of zero is some times called a
To work properly, many IC comparators need an external
A Schmitt trigger uses
A Schmitt trigger
.An ideal operational amplifier has
Another name for a unity gain amplifier is:
The open-loop voltage gain (A_{ol}) of an op-amp is the
A series dissipative regulator is an example of a:
A noninverting closed-loop op-amp circuit generally has a gain factor:
. In order for an output to swing above and below a zero reference, the op-amp circuit requires:
Op-amps used as high- and low-pass filter circuits employ which configuration?
If ground is applied to the (+) terminal of an inverting op-amp, the (–) terminal will:
An astable multivibrator is also known as a:
With negative feedback, the returning signal:
. What starts a free-running multivibrator?

A portion of the output that provides circuit stabilization is considered to be:

If a noninverting amplifier has an R_{IN} of 1000 ohms and an R_{FB} of 2.5 kilohms, what is the R_{IN} voltage when 1.42 mV is applied to the correct input?
Input impedance [Z_{in} (I)] of an inverting amplifier is approximately equal to:
The closed-loop voltage gain of an inverting amplifier equals
All of the following are basic op-amp input modes of operation EXCEPT
A circuit whose output is proportional to the difference between the input signals is considered to be which type of amplifier?
With negative feedback, the returning signal
The voltage follower has a:
The ratio between differential gain and common-mode gain is called:
If the gain of a closed-loop inverting amplifier is 3.9, with an input resistor value of 1.6 kilohms, what value of feedback resistor is necessary?
In an open-loop op-amp circuit, whenever the inverting input (–) is negative relative to the noninverting input (+), the output will:
With a differential gain of 50,000 and a common-mode gain of 2, what is the common-mode rejection ratio?
If the input to a comparator is a sine wave, the output is a:
What three subcircuits does a phase locked loop (PLL) consist of?
The major difference between ground and virtual ground is that virtual ground is only a:
If an op-amp has one input grounded and the other input has a signal feed to it, then it is operating as what?
If the feedback/input resistor ratio of a feedback amplifier is 4.6 with 1.7 V applied to the noninverting input, what is the output voltage value?
The Schmitt trigger is a two-state device that is used for:
. When a capacitor is used in place of a resistor in an op-amp network, its placement determines:
. The common-mode voltage gain is
How many logic states does an S-R flip-flop have?
An output that is proportional to the addition of two or more inputs is from which type of amplifier?
In a PLL, to obtain lock, the signal frequency must:
An ideal amplifier should have:
In an analog multiplier, the reference Voltage V_{ref} is internally set to ____
In one quadrant multiplier, the polarity of the input voltage V_x is _____ and V_y is_____.

If $V_s = V_s \sin(2*pi*f_s*t)$ and $V_o = V_o \sin((2*pi*f_o*t) + \theta)$ are applied to a switch type phase detector, then the output consists of a DC term and the other term is _____
Division can be accomplished by placing the multiplier circuit in the _____ of the operational amplifier.
Analog Multiplier produces an output which is a

Op1	Op2	Op3
100,000	1000	101
1 kHz	9 kHz	10 kHz
100 kHz	unknown	infinity
1	Amid	zero
the cut off frequency	closed - loop voltage gain	unity
slew rate	frequency	voltage gain
10 Hz	20 kHz	1 MHz
is larger	appears triangular	is normal
an input impedance of 2 MΩ	an out put impedance of 75 Ω	all of the above
increases	decreases	stays the same
only one input	only two inputs	only three inputs
5	0.2	1
all of the same value	all of different values	each proportional to the weight of its input
resistor	capacitor	zener diode
pulse	triangular wave form	spike
resistor	capacitor	zener diode
the RC time constant	the rate at which the input is changing	the amplitude of the input
mechanical ground	an ac ground	a virtual ground
equal to the feedback resistor	less than the feedback resistor	greater than the feedback resistor
rectangular wave	triangular wave	rectified sine wave
threshold detector	zero - crossing detector	positive limit detector
pull - up resistor	compensating capacitor	by pass capacitor
positive feed back	negative feedback	compensating capacitors
is a zero - crossing detector has two trip points	has two trip points	produces triangular output waves
infinite output impedance	zero input impedance	infinite bandwidth
difference amplifier	comparator	single ended
external voltage gain the device is capable of	internal voltage gain the device is capable of	most controlled parameter
linear regulator	switching regulator	shunt regulator
less than one	greater than one	of zero
a resistive feedback network	zero offset	a wide bandwidth.
Noninverting	Comparator	open-loop
not need an input resistor	be virtual ground	have high reverse current
one-shot multivibrator	free-running multivibrator	bistable multivibrator
aids the input signal	is proportional to output current	opposes the input signal
a trigger	an input signal	an external circuit

negative feedback	distortion	open-loop

3.5 mV	Ground	1.42 mV
R_i	$R_f + R_i$	∞
the ratio of the input resistance to the feedback resistance	the open-loop voltage gain	the feedback resistance divided by the input resistance
inverting mode	common-mode	double-ended
common-mode	darlington	differential
is proportional to the output current	is proportional to the differential voltage gain	differential
closed-loop voltage gain of unity	small open-loop voltage gain	closed-loop bandwidth of zero
Amplitude	differential-mode rejection	common-mode rejection
6240 ohms	2.4 kilohms	410 ohms
swing negative	close the loop	be balanced
–87.9 dB	–43.9 dB	43.9 dB
ramp voltage	sine wave	rectangular wave
phase comparator, comparator, and VCO	phase comparator, bandpass filter, and VCO	phase comparator, bandpass filter, and demodulator
voltage reference	current reference	power reference
Common-mode	Single-ended	Double-ended
a) 7.82 V	Saturation	Cutoff
pulse shaping	peak detection	input noise rejection
open- or closed-loop gain	integration or differentiation	saturation or cutoff
smaller than differential voltage gain	equal to voltage gain	greater than differential voltage gain
2	3	4
Differentiator	Difference	Summing
come within the lock range	be less than the capture frequency	come within the capture range
high input current	zero set	high output impedance
15V	5V	20V
positive, negative.	positive, positive	negative, negative

f_o	$2* f_o$	$f_o/ 2$
feedback loop	inverting input terminal	output
product of two input signals divided by a reference voltage.	product of two input signals and reference voltage.	product of three input signals.

Op4	Op5	Op6
100		
11 kHz		
0 H z		
very large		
common - mode voltage gain		
capacitance		
15 MHz		
has no effect		
voltage gain of 100,000		
fluctuates		
any number of inputs		
2		
related by a factor of two		
voltage divider		
ramp		
voltage divider		
answers a and b		
an ordinary ground		
unequal		
series of ramps		
half - wave detector		
compensating resistor		
pull - up resistors		
is designed to trigger on noise voltage		
All of the above		
voltage follower		
same as A_{cl}		
dc-to-dc converter		
equal to one		
a negative and positive supply		
inverting		
not invert the signal		
monostable multivibrator.		
is proportional to differential voltage gain		
nothing		

positive feedback		

0.56 mV		
$R_f - R_i$		
the input resistance		
single-ended		
operational		
aids the input signal		
large closed-loop output impedance		
phase		
0.62 kilohms		
swing positive		
87.9 dB		
sawtooth wave		
phase comparator, low-pass filter, and VCO		
difference reference		
Noninverting mode		
9.52 V		
filtering		
addition or subtraction		
None of the above		
5		
analog subtractor		
be greater than the capture frequency		
moderate gain		
10V		
negative positive		

3* f_o		
non inverting terminal		
product of two input signals.		

Answer
101
9 kHz
100 kHz
1
closed - loop voltage gain
slew rate
1 **MHz**
appears triangular
voltage gain of 100,001
stays the same
any number of inputs
0.2
each proportional to the weight of its input
capacitor
ramp
capacitor
answers a and b
a virtual ground
greater than the feedback resistor
triangular wave
positive limit detector
by pass capacitor
compensating capacitors

has two trip points

infinite bandwidth
voltage follower
internal voltage gain the device is capable of
dc-to-dc converter
greater than one
a negative and positive supply
inverting
be virtual ground
free-running multivibrator
opposes the input signal
nothing

negative feedback

1.42 mV
R_i
the feedback resistance divided by the input resistance
inverting mode
differential
differential
closed-loop voltage gain of unity
common-mode rejection
6240 ohms
swing positive
87.9 dB
rectangular wave
phase comparator, low-pass filter, and VCO
voltage reference
Single-ended
9.52 V
pulse shaping
integration or differentiation
smaller than differential voltage gain
2
Summing
come within the capture range
zero set
10V
positive, positive

2* f_o
feedback loop
product of two input signals divided by a reference voltage.

Questions	Op1
The input stage of Phase Locked Loop is_____	Low Pass Filter
The Voltage Controlled Oscillator is also called as _____	relaxation oscillator
The function of phase detector is to compare the _____ of the incoming signal to that of the output V_0 of Voltage Controlled Oscillator.	phase and frequency
Phase detector is basically a _____.	summer
The output of phase detector is _____.	f_s+f_0
The signal V_c shifts the frequency in a direction to reduce the difference between f_s and f_0. Now the signal is in _____ range.	lock-in
The VCO continues to change the frequency till its output frequency is _____the input signal frequency.	less than
The range of frequencies over which the PLL can maintain the lock with the incoming signal is called _____ range.	tracking
The range of frequencies over which the PLL can acquire the lock with the incoming signal is called _____ range	tracking
The output frequency of Voltage Controlled Oscillator f_0 is _____	$(V_{cc}-v_c)/(R_T*C_T*V_{cc})$
Voltage Controlled Oscillator is otherwise called as _____.	voltage to frequency converter
In PLL, the high frequency component (f_s+f_0) is removed by_____	high pass filter
Which of the following are the stages of PLL? i) free running ii) capture iii) tracking iv) pull in	only i and ii
Which of the following are the problems associated with the switch type phase detector? i) since the output voltage Ve is directly proportional to Vs, the phase detector gain and loop gain becomes dependent on the input signal amplitude. ii) output is proportional to cosΦ which makes it non linear. iii) the circuit becomes unstable iv) full wave detector	i and ii
In switch type phase detector, at the locked state ($f_s = f_0$) the phase shift should be _____ in order to get zero error signal.	0^o
In balanced modulator type phase detector, the transistors act as _____.	switch
In balanced modulator type phase detector, the phase angle to voltage transfer co-efficient KΦ is _____	(I_Q*R_L)/ pi

In digital type phase detector, the phase angle to voltage transfer co-efficient KΦ is _____	V_{CC}/(2*pi)
In EX-OR type digital phase detector, the maximum dc output voltage occurs when the phase difference is _____ degrees.	0
The EX-OR type phase detector is used only when the input waves are _____.	square and sine
The output wave of Voltage Controlled Oscillator is _____.	square, triangular
The Voltage to Frequency conversion factor of VCO is _____.	f_0 / V_{CC}
The output from a Phase Locked Loop system is _____.	voltage or frequency
If a divide by N - network is inserted between VCO output and phase comparator input of PLL, then in the locked state f0 is _____.	f_s /N
When PLL is used as AM demodulator, the AM signal is shifted in phase by _____ before being fed to the multiplier.	0º
The other name for capture range is _____ range.	tracking
The other name for lock in range is _____ range.	tracking
The range of modulating input voltage applied to a VCO is _____.	0.5 V_{CC} to V_{CC}
Lock in range of a PLL is _____ the capture range.	greater than
Which of the following is the drawback of variable transconductance multiplier?	inaccurate
The time taken for a PLL to capture the incoming signal is called _____ time.	pull out
If the voltage at the modulation input of VCo is biased at 7/8 Vcc then the output frequency of VCO in PLL is given by f0 = _____.	0.25/ (R_T*C_T)
The maximum operated range of PLL 565 is_____.	0 to 500 kHz
The Lock in range of Phase Locked Loop is _____.	$\Delta f_L = 7.8 f_0/v$
If the offset frequency f_1 is applied to the phase detector of frequency translator circuit, then at the locked state f0 is given by _____.	fs
_____ filter controls the capture range and lock in range of PLL.	high pass filter
The operating voltage range of IC 565 is _____.	+/- 6V to +/-12V
An external capacitor connected across IC 565 will act as _____.	passive device

If V_c shifts the VCO frequency from the free running frequency f_0 to a frequency f, then the new frequency shift from VCO in a PLL is _____.	$f_0 + k_v*Vc$
A _____ is an electronic system which generates any range of frequencies from a single fixed time base or oscillator.	frequency multiplier
Phase detector is basically a _____.	summer
In PLL, the output of the error amplifier is equal to the _____.	error voltage
Select correct statement of PLL.	capture range is smaller than lock in range
The following gate can be used as phase detector.	NAND
The output of divider circuit with input signals V_x as divisor and V_y as dividend using opamp ____.	$V_o= (V_{ref}*V_y)/V_x$
If $V_x=V_x*\sin wt$, $V_y= V_y*\sin(wt+\theta)$ are the inputs to the four quadrant Multiplier, then the output voltage is _____.	V_x*V_y
The Voltage to Frequency Converter of VCO is defined as ____	$\Delta V_c / \Delta f_0$
IC 566 functions as_____.	phase detector
The total time taken by PLL to establish the lock is called _____.	pull in time
If the frequency of the carrier wave is varied in accordance with the modulating signal, then the modulation refers to _____ modulation	frequency shift keying
The capture range of PLL is defined as _____.	$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10\text{^}3))\}^{1/2}$
The lock in range of PLL is defined as _____.	$\Delta f_L = +/- (K_v*K_\Phi)$
Which of the following is the drawback of variable transconductance multiplier?	inaccurate
The basic blocks in Voltage Controlled Oscillator are _____	constant current source, buffer, astable multivibrator, inverter
The pulsewidth T of IC 555 as a monostable multivibrator is _____.	$RC* \ln(V_{cc}/(V_{cc} -V_{TH})$
A single 555 timer can provide time delay ranging from _____.	microseconds to minutes
The pulse width of monostable Multivibrator using 555 timer is _____.	0.693 *RC
IC 555 Timer is used in astable mode. The total time taken by the capacitor to charge and discharge is _____.	$T= 1.1*(2R_A+R_B)*C$
Which of the following are the applications of Monostable Multivibrator using 555 timer? i) missing pulse detector ii) pulse position modulator iii) pulse width modulator iv) frequency divider.	only ii

. For R_A =6.8k ohm, R_B = 3.3kohm and C=0.1microfarad, Calculate t_{HIGH} of astable multivibrator using 555 timer.	0.23ms
Which of the following are the applications of astable Multivibrator using 555 timer? i) missing pulse detector ii) pulse position modulator iii) pulse width modulator iv) FSK Generator	only ii
Match the following. i) pulse position modulator - A) Monostable Multivibrator ii) pulse width modulator - B) Class A iii) full cycle amplification - C) Class B iv) half cycle amplification - D) astable Multivibrator	i-D, ii-A, iii-B, iv-C
Which of the following is the application of astable multivibrator using 555 timer?	pulse position modulation
The duty cycle D of astable operation using 555 timer is defined as _____.	R_B *(R_A+R_B)
The efficiency of switching regulators compared to series voltage regulators is _____.	high
. Which of the following is one-shot application of IC 555 timer?	frequency divider
Which of the following are the operating modes of 555 timer? i) free running operation ii) one-shot operation. iii) bistable operation	only I
The value of output voltage of IC 555 timer in the off state is _____.	0V
When IC 555 timer is operated as one shot multivibrator, the output switches high due to _____.	negative going trigger pulse to the timer
The lower threshold voltage VLT and upper threshold voltage VUT for IC 555 timer is _____.	Vcc/3, 2Vcc/3
Thigh and Tlow for astable mode multivibrator of IC 555 are _____.	t_{high} = 0.69(R_A+R_B)*C, t_{low}= 0.69(R_A+2R_B)*C
When R_A = R_B in IC 555 timer circuit, then the total time for output waveform T= 0.69(R_A + R_B)*C. Duty cycle for the circuit is _____.	80%

If R_A =10k, C=0.1microfarad, calculate the timing interval for IC 555 monostable operation.	2 millisecond
The frequency of oscillation of astable multivibrator using IC 555 timer is _____.	$1.45 / ((R_A+2R_B)*C)$

Op2	Op3
Error Amplifier	Voltage Controlled Oscillator
free running multivibrator	monostable multivibrator
phase	frequency
subtractor	multiplier
f_s-f_0	f_s*f_0
capture	free running
exactly the same as	greater than
capture	free running
capture	free running
v_c /(R_T*C_T*V_{cc})	2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})
voltage to time converter	voltage to current converter
low pass filter	band pass filter
only ii and iv	i, ii and iii
i,ii and iii	ii,iii
180º	270º
amplifier	oscillator
V_0/(2*pi)	(4*I_Q*R_L)/pi

V_{CC}/(pi)	V_0/(2*pi)
90	180
square and cosine	square and triangular
square	triangular
$8*f_0 / V_{CC}$	$2*f_0 / V_{CC}$
only voltage	only frequency
$N*f_s$	f_s+N
180º	270º
lock in	free running
acquisition	free running
0.75 V_{CC} to V_{CC}	0 V_{CC} to V_{CC}
equal to	lesser than
costly	difficult to integrate in IC
capture	lock in
$(R_T*C_T)/4$	$4(R_T*C_T)$
0.001 to 500 kHz	100 to 400 kHz
$\Delta f_L = +/- (7.8 f_0/v)$	$\Delta f_L = +/- (8.7 f_0/v)$
fs * f_1	fs + f_1
low pass filter	band pass filter
+/- 10V to +/-12V	+/- 8V to +/-12V
low pass filter	charging device

$f_0 - k_v*Vc$	k_v*Vc
frequency synthesizer	frequency doubler
subtractor	multiplier
applied voltage	control voltage
capture range is greater than lock in range	capture range is equal to lock in range
AND	EX-OR
$V_o = - (V_{ref}*V_y)/V_x$	$V_o = (V_y)/V_x$
$\{(V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}/Vref$	$\{V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}$
Δf_0	ΔV_c
low pass filter	VCO
pull out time	rise time
frequency	amplitude
$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C)\}^{1/2}$	$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C*(3.6*10\text{^}3))\}$
$\Delta f_L = +/- (K_v*K_\Phi*A$	$\Delta f_L = +/- (K_v*K_\Phi)/(A*(pi/2))$
costly	difficult to integrate in IC
constant current source, astable multivibrator, triangular wave generator, inverter.	constant current source, buffer, Schmitt trigger, inverter
$RC* \ln(Vcc - V_{TH}/(Vcc)$	$RC* \ln(Vcc - V_{TH})$
microseconds to milliseconds	microseconds to seconds
1.1*RC	0.3*RC
$T= 0.69*(R_A+R*C)$	$T= 0.69*(R_A+2R_B)*C$
a) i, iii and iv	i and ii only

0.7ms	0.5ms
ii and iii only	ii and iv only
i-D, ii-A, iii-C, iv-B	i-A, ii-D, iii-B, iv-C
pulse width modulation	) pulse code modulation
c) $R_B / (R_A+2R_B)$	$R_B / (1+R_B)$
low	same
pulse position modulator	FSK generator
only i and ii	i,ii and iii
0.1V	1V
positive going trigger pulse to the timer	positive voltage
2Vcc/3, Vcc/3	Vcc, 2Vcc/3
$t_{high} = 0.69(R_A)*C$, $t_{low}=$ 0.69(R*C	$t_{high} = 0.69(R_A+R_B)*C$, $t_{low}= 0.69(R_B)*C$
50%	25%

1.1 millisecond	2.2 millisecond
$1.45((R_A+2R_B)*C)$	$((R_A+2R_B)*C)/ 1.45$

Op4	Op5
Phase Detector	
phase shift oscillator	
amplitude	
divider	
f_s+/ f_0	
unlocked	
twice that of	
pull in	
pull in	
$1/(R_T*C_T)$	
frequency to voltage converter	
band reject filter	
only iv	
only i	
90^o	
modulator	
$(I_Q*R_L)/2*pi$	

V_0/(pi)	
360	
square.	
sine	
$4*f_0 / V_{CC}$	
only phase.	
f_s –N	
90º	
acquisition	
capture	
0.25 V_{CC} to V_{CC}	
less than or equal to	
scale factor depends on temperature which affects the output	
pull in	
$(R_T*C_T)/0.25$	
10 to 400 kHz	
$\Delta f_L = 8.7 f_0/v$	
fs - f_1	
band reject filter	
+/- 12V	
discharging device	

Vc	
frequncy translator	
divider	
power supply voltage	
capture range is not equal to lock in range	
OR	
$V_o = V_{ref}/(V_x * V_y)$	
$(V_x * \sin * (wt+\theta)) * V_y$	
$\Delta f_0/\Delta V_c$	
PLL	
hold time	
phase	
$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C)\}$	
$\Delta f_L = +/- (K_v * K_\Phi * A * (pi/2))$	
scale factor depends on temperature which affects the output	
constant current source, buffer, Schmitt trigger	
$RC * \ln(V_{TH} - Vcc /(V_{TH})$	
microseconds to hours	
0.2*RC	
T= 1.1*RC	
only iv	

0.4ms	
i and ii only	
i-A, ii-D, iii-C, iv-B	
pulse amplitude modulation	
d) R_B / (1+R_B)	
halved	
FM demodulator	
only iii	
0.7V	
negative voltage	
Vcc, Vcc/3	
t_{high} = 0.69(R_B)*C, t_{low}= 0.69 (R_A+R_B)*C	
100%	

2.3 millisecond	
1.45/ $((R_A+R_B)*C)$	

Op6	Answer
	Phase Detector
	free running multivibrator
	phase and frequency
	multiplier
	f_s+/ f_0
	capture
	exactly the same as
	tracking
	capture
	$2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})$
	voltage to frequency converter
	low pass filter
	i, ii and iii
	i and ii
	90º
	switch
	$(4*I_Q*R_L)/pi$

	V_{CC}/(pi)
	180
	square.
	square, triangular
	$8*f_0 / V_{CC}$
	voltage or frequency
	$N*f_s$
	90º
	acquisition
	tracking
	0.75 V_{CC} to V_{CC}
	greater than
	scale factor depends on temperature which affects the output
	capture
	$0.25/ (R_T*C_T)$
	0.001 to 500 kHz
	$\Delta f_L = +/- (7.8 f_0/v)$
	$fs + f_1$
	low pass filter
	+/- 6V to +/-12V
	low pass filter

	$f_0 + k_v*Vc$
	frequency synthesizer
	multiplier
	control voltage
	capture range is smaller than lock in range
	EX-OR
	$V_o = -(V_{ref}*V_y)/V_x$
	$\{(V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}/Vref$
	$\Delta f_0/\Delta V_c$
	VCO
	pull in time
	frequency
	$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C*(3.6*10\text{^}3))\}^{1/2}$
	$\Delta f_L = +/- (K_v*K_\Phi*A*(pi/2))$
	scale factor depends on temperature which affects the output
	constant current source, buffer, Schmitt trigger, inverter
	$RC*\ln(Vcc/(Vcc - V_{TH})$
	microseconds to hours
	1.1*RC
	$T = 0.69*(R_A+2R_B)*C$
	a) i, iii and iv

	0.7ms
	ii and iv only
	i-D, ii-A, iii-B, iv-C
	pulse position modulation
	R_B / (1+R_B)
	high
	frequency divider
	only i and ii
	0.1V
	negative going trigger pulse to the timer
	Vcc/3, 2Vcc/3
	$t_{high} = 0.69(R_A+R_B)*C$, $t_{low} = 0.69(R_B)*C$
	50%

	1.1 millisecond
	$1.45 / ((R_A+2R_B)*C)$

Questions
_____ is a highly stable device for generating accurate time delay or oscillation.
In the switched capacitor filter, the value of resistor is determined by _____.
For the given value of input voltage, if the time period is constant then the output voltage of switching regulator is _____.
A Regulated power supply provides a dc voltage independent of _____.) load current variations ii) temperature variations iii) load current and ac line voltage variations
_____ is defined as the change in the output voltage for a change in the load current.
The duty cycle of a switching regulator is
The output voltage of switching regulator is a function of _____.
The basic elements of switching regulators are _____.
To improve the efficiency of a switching regulator, which of the following device is used? .
The resonance frequency of the tuned circuit is _____.
The selectivity of tuned circuit is high when _____.
Video Amplifiers are called as wide band amplifiers because they have ____.
Small signal tuned amplifiers are operated in the mode of _____.
Tuned class-C amplifier are also called as _____.
In Class B tuned amplifier the efficiency increases linearly with the output amplitude V1 and it reaches its maximum when V1 is equal to _____.
The Class-B mode of operation means that the collector current flows in a transistor only for _____.
If the tuned amplifier bursts into oscillation instead of amplification then it is said to be _____.
The tuned amplifiers cannot be used at low frequency because _____.
The separation in Isolation amplifier is achieved by _____.
The large signal amplifiers are otherwise known as _____.
In which type of Power amplifier, the signal is amplified for full cycle?
Which of the following power amplifier has high efficiency?
Which of the following power amplifier is never used in audio amplifiers?
The output is obtained for more than 180° but less than 360° in _____.
Which of the following are the important sections of a voltage regulator IC?) reference voltage circuit ii) error amplifier iii) series pass transistor

The output voltage of linear regulator using op-amp is _____.
The name linear regulator is due to _____.
A voltage regulator is a circuit that provides _____.
Which of the following IC is a variable voltage regulator IC?
The fold back current limiting is employed in a _____.
Switching regulator has advantage over series regulator because of _____.
Which of the following is the limitation of a three terminal regulator?
Which of the following statement is incorrect?
The IC regulators use reference voltage source, error op-amp and pass transistor with _____. i) short-circuit current limiting ii) current foldback iii) thermal overload protection
A duty cycle of 50% (half the frequency) of timer will give _____.
The pass transistor used in regulators has switching frequency
In switching regulator, the series pass transistor is switched
In the voltage regulators, if the output is shorted or load current exceeds the set value, then the current through the series transistor _____.
Which of the following are the limitations of IC 723?
The constant output voltage and current from IC regulator is due to ____.

Op1	Op2	Op3
555 timer	VCO	Voltage to Time converter
$R = 1/(C*f_{clk})$	$R= Vin/I_{avg}$	$R= 1/(C*T_{clk})$
directly proportional to OFF time	directly proportional to ON time	inversely proportional to OFF time
only I	only i and ii	only iii
line regulation	load regulation	input regulation
t_{on} / f_s	$t_{off} * f_s$	$t_{on} / (t_{on} + t_{off})$
input voltage and frequency	ON and OFF time	On time and input voltage
switch, pulse generator, voltage source and filter	control element and voltage source	switch, pulse generator and control element
step-up transformer	series pass transistor	variable resistor
1/((2*pi*(sqrt(RC))	1/((2*pi*(sqrt(LC))	1/((2*pi*(sqrt(RL))
bandwidth is high	bandwidth is small	resonant frequency is high
high selectivity	small bandwidth	bandwidth from dc to high frequency
Class A	Class B	Class C
small signal tuned amplifiers	large signal tuned amplifiers	linear circuit amplifiers
Vcc	2*Vcc	Vcc/2
half the period of ac input cycle	one fourth of the period of ac input cycle	full period of ac input cycle
oscillator	open circuit	short circuit
the required gain is low	the size of L and C are large	the size of L and C are small
transistor	transformer	SCR
tuned amplifiers	voltage amplifiers	current amplifiers
Class B	Class A	Class C
Class B	Class A	Class C
Class B	Class A	Class C
Class B	Class A	Class C
only i and ii	i,ii and iii	only ii and iii

$V_0 = \{1+(R_2/R_1)\} * V_{ref}$	$V_0 = -\{1+(R_2/R_1)\} * V_{ref}$	$V_0 = -(R_2/R_1) * V_{ref}$
transistor in regulator conducts in cut-off region	transistor in regulator conducts in linear region	transistor conduction in cut-off and saturation region
stable dc voltage	stable dc voltage independent of load current	stable ac voltage
IC 723	LM 320	LM 340
low voltage current regulator circuits	high voltage current regulator circuits	low current voltage regulator circuits
improved efficiency	improved efficiency and high switching frequency	high switching frequency
no short-circuit protection	output voltage is fixed	no short-circuit protection and output voltage is fixed
switching regulators use switching speed of 20kHz and above	The output voltage of a switching regulator is controlled by altering the switching	both Bipolar transistors and FETs have very good switching characteristics
only I	only ii	i and iii
rectangular waveform	square waveform	sawtooth waveform
Below 20 kHz	20 kHz	Above 20 kHz
in saturation region	in active region	between active and saturation region
increases	folds back	remains same
no Short circuit protection	no in-built thermal protection	no Short circuit protection and no in-built thermal protection
constant current source	reference amplifier	constant current source and reference amplifier

Op4	Op5	Op6
Voltage to Frequency converter		
R= V_{sense}/I_{limit}		
inversely proportional to ON time		
only iv		
ripple rejection		
$t_{off}/ (t_{on} + t_{off})$		
input voltage and duty cycle		
control element and switch		
variable inductor.		
(2*pi*(sqrt(RC))		
resonant frequency is low		
bandwidth from zero to infinity		
Class AB		
stagger tuned amplifiers		
infinity		
dc input		
unstable		
the required bandwidth is high		
inverter		
power amplifiers		
Class AB		
Class AB		
Class AB		
Class AB		
nly i and iii		

$V_0 = (R_2/R_1) * V_{ref}$		
transistor conduction in saturation region		
stable ac voltage with no load current variations		
IC7805		
high current voltage regulator circuits		
less number of components needed		
more number of components needed		
switching regulator is that their power consumption is very low		
only iii		
ramp waveform		
10 kHz		
between cutoff and saturation		
gets doubled		
output voltage is fixed		
constant voltage source		

Answer
555 timer
$R = 1/(C*f_{clk})$
directly proportional to ON time
only iv
load regulation
$t_{on} / (t_{on} + t_{off})$
input voltage and duty cycle
switch, pulse generator, voltage source and filter
series pass transistor
1/((2*pi*(sqrt(LC))
bandwidth is small
bandwidth from dc to high frequency
Class A
large signal tuned amplifiers
Vcc/2
half the period of ac input cycle
unstable
the size of L and C are large
transformer
power amplifiers
Class A
Class C
Class C
Class AB
i,ii and iii

$V_0 = \{1+(R_2/R_1)\} * V_{ref}$
transistor in regulator conducts in linear region
stable dc voltage independent of load current
IC 723
high current voltage regulator circuits
improved efficiency and high switching frequency
no short-circuit protection and output voltage is fixed
The output voltage of a switching regulator is controlled by altering the switching frequency
i and iii
square waveform
Above 20 kHz
between cutoff and saturation
folds back
no Short circuit protection and no in-built thermal protection
constant current source and reference amplifier

Questions
JFET is used as an analog switch. If V_{GS} is less than or equal to V_{GS} (OFF), JFET operates in _____ region and it acts as _____ switch.
Which of the following are the drawbacks in weighted resistor DAC? i) wide range of resistors are required. ii) for better resolution the binary word length has to be increased. The fabrication of large resistance in IC is impractical. iii) voltage across the resistor due to bias current will affect the accuracy.
What is the drawback of R-2R ladder type DAC?
The time required for the conversion of analog signal into a digital equivalent is called _____ time.
Which of the following is the fastest ADC?
Which of the following are the advantages of R-2R ladder DAC? i) easier to build accurately as only resistors of two values are required. ii) number of bits can be expanded by adding more sections of R-2R values. iii) conversion time is less
Which of the following are the drawbacks of flash type ADC? i) slowest ADC ii) number of comparator almost doubles for each added bit iii) most expensive iv) for larger value of bits, more complex is the priority encoder
Which of the following is a direct type ADC?
JFET is used as an analog switch. If V_{GS} = 0v,JFET operates in _____ region and it acts as _____ switch.
10. The other name for flash type comparator is _____comparator ADC.
Which of the following is integrating type ADC?
The conversion time for flash type converter is in the order of _____.
The number of comparators required for a 3-bit flash type ADC is _____.
Which of the following ADC uses trial and error method to find the digital output?
In successive approximation ADC, with the arrival of START command, the SAR register sets _____.
ADC and DAC are otherwise called as _____.
Digital to Analog conversion can be done by _____.
The only two values of resistor required for DAC is _____.

The main disadvantage of binary weighted resistor method is _____
The R-2R ladder DAC has a drawback of _____.
ADC can be classified as _____.
The resolution of DAC for 8-bit length is _____. i) 8-bit resolution ii) resolution of 0.392 of full scale iii) resolution of 1 part in 255
The property of DAC in which analog output increases with digital input is called _____.
The linearity error of DAC should be _____.
The accuracy of Data converters can be specified in _____.
Which of the following components are required by DAC? i) resistors ii) op-amp iii) electronic switches
ADC 0800/0801/0802 is _____.
The amount by which the actual output of a DAC differs from the ideal straight line characteristics is _____
Which of the following ADC is low speed ADC?
JFET is used as a shunt switch. When V_{GS}=0, JFET acts as _____ switch and the output V0= _____.
For D/A converter, analog output voltage for MSB is _____.
The Sample and Hold circuit is not needed for _____ ADC.
The main drawback of dual slope ADC is _____
The advantage of dual slope ADC is _____.
A V/F Converter circuit is used in _____.
_____ of ADC gives error when an analog signal changes rapidly.
For D/A converter, analog output voltage for LSB is _____.
The conversion time of 10-bit successive approximation A/D converter is ____, if the input clock is 5MHz.
The smallest possible change in the analog output voltage is referred to as _____.

The time required for the holding capacitor C to charge upto a level close to the input voltage during sampling is _____
_____ indicates how close the analog output voltage is to its theoretical value.
The non- zero level of analog output when all the digital inputs are zero is called _____.
To obtain close approximation of input waveform, the sampling frequency should be atleast _____ that of the input frequency.
What would be the output voltage produced by a D/A Converter, if output range is 0 to 10V and binary number is 102 (2 bit DAC)?
The input stage of any data acquisition system will be _____.
The total number of clock pulses required for 8-bit successive approximation ADC is _____.
What is the expression for analog voltage Va of dual slope ADC? (N=digital count, V_R= reference voltage)
The maximum deviation between actual converter output and ideal converter output is _____
The maximum deviation between actual converter output and ideal converter output after gain and offset errors have been removed is _____
The main drawback of single slope ADC is _____.
_____ ADC is suitable for accurate measurement of slowly varying signals such as thermocouples.
An analog voltage can be converted into digital form by producing pulses whose frequency is proportional to analog voltage _____.
The converter that converts an analog input signal into a linear function of time or frequency and then to a digital code is _____
Which of the following electronic switches are used in DAC? i) SPDT ii) totem pole MOSFET switches iii) CMOS inverter switch
What is the main difference between n-JFET and n-MOSFET when V_{GS}=0?

In ADC, the control line used to indicate the start and end of conversion is _____
Match the following. i) R-2R ladder type - A) fastest ADC ii) successive approximation - B) current flow through the resistor is not constant iii) inverted R-2R type - C) slowest ADC iv) flash type - D) current flow through the resistor is constant
In dual slope ADC, the unknown voltage and the reference voltages are converted into an equivalent _____using an integrator.
DAC 0800/0801/0802 is _____.
Inverted R-2R ladder DAC works on the principle of _____.

Op1	Op2
cut-off, closed	cut-off, open
i only	i, ii and iii
current is not constant in all branches	The fabrication of large resistance in IC is impractical.
aperture	acquisition
flash	successive approximation
only I	only i and ii
only I	only iv
successive approximation	single slope
cut-off, closed	cut-off, open
successive approximation	single slope
successive approximation	single slope
nanosecond	millisecond
3	6
successive approximation	single slope
LSB = 1 and all other bits to 0	MSB = 0 and all other bits to 1
amplifiers	data converters
weighted resistor method	successive approximation method
weighted resistor method	binary weighted method

word length of binary word is small	temperature variations
direct type, comparator type	indirect type, comparator type
only i	only i and ii
linearity	stability
+/- (1/2) LSB	+/- (1/2) MSB
LSB level	MSB level
only i and ii	i,ii and iii
1 bit ADC	2 bit ADC
offset error	linearity error
successive approximation	parallel comparator
open, zero	open, Vin
$V_0= (2^{N-1}) V_R / 2^N-1$	$V_0= (2^N) V_R / 2^N-1$
direct type	counter type
high cost	a) comparator and ADC are needed
long conversion time	excellent noise rejection
charge balancing ADC	dual slope ADC
direct type	counter type
$V_0= (2^{N-1}) V_R / 2^N-1$	$V_0= (2^N) V_R / 2^N-1$
1 microsec	2 microsec
accuracy	resolution

aperture time	acquisition time
accuracy	resolution
offset error	linearity error
same as	twice
3.75V	4V
DAC	Sample and Hold circuit
4	2
Va = $V_R (N+1)/ 2^n$	Va = $V_R (2^n)/ N$
monotonicity	relative accuracy
monotonicity	relative accuracy
resolution is less	comparator and ADC are needed
successive approximation	parallel comparator
ADC	VCO
counter type ADC	direct type ADC
only i	only ii and iii
n-JFET is ON and n-MOSFET is OFF	n-JFET is OFF and n-MOSFET is ON

only EOC	only SOC
i-B , ii-C, iii-D, iv-A	i-B , ii-A, iii-D, iv-C
time period	frequency
1 bit DAC	2 bit DAC
summing currents	summing voltages

Op3	Op4	Op5
ohmic, closed	ohmic, open	
i,ii only	iii only	
) voltage across the resistor due to bias current will affect the accuracy.	conversion time is less.	
conversion	settling	
dual slope	single slope	
only iii	only i and iii	
only i,ii and iii	only ii and iv	
dual slope	delta sigma	
ohmic, closed	ohmic. Open	
dual slope	parallel	
parallel comparator	flash comparator	
microsecond	second	
8	4	
dual slope	parallel	
LSB = 1 and all other bits to 1	MSB = 1 and all other bits to 0	
rectifiers	clampers	
single slope method	dual slope method	
R-2R ladder method	multiplying type	

less resolutions	wide range of resistor values	
integrating type, comparator type	direct type, integrating type	
only i,ii and iii	only iii	
monotonocity	accuracy	
+/- LSB	+/- MSB	
Voltage increments	percentage of full scale voltage	
only ii and iii	only ii	
4 bit ADC	8 bit ADC	
gain error	accuracy error	
dual slope	charge balancing	
closed, Vin	closed, zero	
$V_0 = (2^{N-1}) V_R / 2^N$	$V_0 = (2^{N-1}) V_R$	
integrating type	tracking type	
b) long conversion time	poor noise rejection	
fastest in operation	slow varying in nature	
parallel comparator ADC	successive approximation ADC	
tracking type	integrating type	
$V_0 = (2^{N-1}) V_R / 2^N$	$V_0 = (2^{N-1}) V_R$	
3 microsec	4 microsec	
linearity	gain	

pull in time	hold time	
linearity	gain	
gain error	accuracy error	
less than	half	
5V	7V	
ADC	Voltage to Time Converter	
16	8	
$Va = V_R (N)/ 2^n$	$Va = V_R (2^n)/ N+1$	
resolution	absolute accuracy	
resolution	absolute accuracy	
long conversion time	poor noise rejection	
dual slope	charge balancing	
V to F converter	V to T converter	
comparator type ADC	integrating type ADC	
i,ii and iii	only i and ii	
n-JFET is ON and n-MOSFET is ON	n-JFET is OFF and n-MOSFET is OFF	

either SOC or EOC	both SOC and EOC	
i-D , ii-A, iii-B, iv-C	i-D , ii-C, iii-B, iv-A	
current	digital	
8 bit DAC	4 bit DAC	
same currents in all ladders	difference currents	

Op6	Answer
	cut-off, open
	i, ii and iii
	current is not constant in all branches
	conversion
	flash
	only i and ii
	only i,ii and iii
	successive approximation
	ohmic, closed
	parallel
	single slope
	nanosecond
	8
	successive approximation
	MSB = 1 and all other bits to 0
	data converters
	weighted resistor method
	R-2R ladder method

	wide range of resistor values
	0
	direct type, integrating type
	only i,ii and iii
	monotonocity
	+/- (1/2) LSB
	percentage of full scale voltage
	only ii and iii
	8 bit ADC
	linearity error
	successive approximation
	closed, Vin
	$V_0 = (2^{N-1}) V_R / 2^N - 1$
	integrating type
	b) long conversion time
	excellent noise rejection
	charge balancing ADC
	integrating type
	$V_0 = (2^N) V_R / 2^N - 1$
	2 microsec
	resolution

	acquisition time
	accuracy
	offset error
	twice
	5V
	Sample and Hold circuit
	8
	Va = V_R (N)/ 2^n
	absolute accuracy
	relative accuracy
	resolution is less
	dual slope
	V to F converter
	integrating type ADC
	i,ii and iii
	n-JFET is ON and n-MOSFET is OFF

	both SOC and EOC
	i-B , ii-C, iii-D, iv-A
	time period
	8 bit DAC
	summing currents