18BECS301 ANALOG ELECTRONIC CIRCUITS

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3	0	4	5

Course Outcome:

At the end of this course, students will demonstrate the ability to

- Understand the characteristics of transistors.
- Design and analyse various rectifier and amplifier circuits.
- Design sinusoidal and non-sinusoidal oscillators.
- Understand the functioning of OP-AMP and design OP-AMP based circuits.

UNIT 1: Diode circuits
(4 Hours)

P-N junction diode, I-V characteristics of a diode; review of half-wave and full-wave rectifiers, Zener diodes, clamping and clipping circuits.

UNIT 2: BJT circuits
(8 Hours)

Structure and I-V characteristics of a BJT; BJT as a switch. BJT as an amplifier: small-signal model, biasing circuits, current mirror; common-emitter, common-base and common- collector amplifiers; Small signal equivalent circuits, high-frequency equivalent circuits

UNIT 3: MOSFET circuits
(8 Hours)

MOSFET structure and I-V characteristics. MOSFET as a switch. MOSFET as an amplifier: small-signal model and biasing circuits, common-source, common-gate and common-drain amplifiers; small signal equivalent circuits - gain, input and output impedances, trans- conductance, high frequency equivalent circuit.

UNIT 4: Differential, multi-stage and operational amplifiers
(8 Hours)

Differential amplifier; power amplifier; direct coupled multi-stage amplifier; internal structure of an operational amplifier, ideal op-amp, non-idealities in an op-amp (Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product)

UNIT 5: Linear and Nonlinear applications of op-amp (14 Hours)

Idealized analysis of op-amp circuits. Inverting and non-inverting amplifier, differential amplifier, instrumentation amplifier, integrator, active filter, P, PI and PID controllers and lead/lag compensator using an op-amp, voltage regulator, oscillators (Wein bridge and phase shift). Analog to Digital Conversion. Hysteretic

Comparator, Zero Crossing Detector, Square-wave and triangular-wave generators. Precision rectifier, peak detector. Monoshot.

TEXT/REFERENCES

1. A. S. Sedra and K. C. Smith, " Microelectronic Circuits" , New York, Oxford University Press, 1998.
2. J. V. Wait, L. P. Huelsman and G. A. Korn, " Introduction to Operational Amplifier theory and applications", McGraw Hill U. S., 1992.
3. J. Millman and A. Grabel, " Microelectronics" , McGraw Hill Education, 1988.
4. P. Horowitz and W. Hill, " The Art of Electronics" , Cambridge University Press, 1989.
5. P. R. Gray, R. G. Meyer and S. Lewis, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, 2001.

STAFF INCHARGE **HOD/ECE**

KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University Established Under Section 3 of UGC Act 1956)

Pollachi Main Road, Eachanari Post,

Coimbatore – 641 021

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE PLAN

NAME OF THE STAFF : Mr.G.ARAVINDH

DESIGNATION : ASSISTANT PROFESSOR

CLASS : B.E-II YEAR CSE

SUBJECT : ANALOG ELECTRONIC CIRCUITS

SUBJECT CODE : 18BECS301

S.No	TOPICS TO BE COVERED	TIME DURATION	SUPPORTING MATERIALS	TEACHING AIDS
UNIT-I DIODE CIRCUITS				
1	Introduction	01	T1 Pg.No :139	BB
2	P-N junction diode, I-V characteristics of a diode	01	T1 Pg.No :140-152	BB
3	Review of half-wave rectifiers	01	T1 Pg.No :172-174	BB
4	Review of full-wave rectifiers	01	T1 Pg.No :174-177	BB
5	Zener diodes	01	T1 Pg.No :167	BB
6	Clamping circuits	01	T1 Pg.No :187	BB
7	Clipping circuits	01	T1 Pg.No :189	BB
Introduction		**01**		
Total Lecture Hours		**06**		
Total Hours		**07**		

UNIT-II BJT CIRCUITS

8	Structure and I-V characteristics of a BJT	01	T1 Pg.No :378-391,392-406	BB
9	BJT as a switch	01	T1 Pg.No :419	BB
10	Small-signal model	01	T1 Pg.No :442-458	BB
11	Biasing circuits, current mirror	01	T1 Pg.No :436-441	BB
12	Common-emitter amplifiers	01	T1 Pg.No :467	BB
13	Common-base amplifiers	01	T1 Pg.No :475	BB
14	Common- collector amplifiers	01	T1 Pg.No :478	BB
15	Small signal equivalent circuits	01	T1 Pg.No :450	BB
16	High-frequency equivalent circuits	01	T1 Pg.No :487	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-III MOSFET CIRCUITS				
17	MOSFET structure and I-V characteristics	01	T1 Pg.No :236-259	BB
18	MOSFET as a switch	01	T1 Pg.No :274	BB
19	MOSFET as an amplifier	01	T1 Pg.No :274-275	BB
20	Small-signal model and biasing circuits	01	T1 Pg.No :280-296	BB
21	Common-source amplifier	01	T1 Pg.No :306	BB
22	Common-gate amplifier	01	T1 Pg.No :311	BB
23	Common-drain amplifier	01	T1 Pg.No :315	BB
24	Small signal equivalent circuits - gain, input and output impedances, trans- conductance	01	T1 Pg.No :290,292	BB
25	High frequency equivalent circuit.	01	T1 Pg.No :320-324	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-IV DIFFERENTIAL, MULTI-STAGE AND OPERATIONAL AMPLIFIERS				
26	Differential amplifier	01	T1 Pg.No :727-738	BB
27	Power amplifier	01	T1 Pg.No :1261-1265	BB
28	Direct coupled multi-stage amplifier	01	T1 Pg.No :1230-1246	BB
29	Internal structure of an operational amplifier	01	T1 Pg.No :893	BB
30	Ideal op-amp	01	T1 Pg.No :64-67	BB
31	Non-idealities in an op-amp (Output offset voltage, input bias current, input offset current, slew rate, gain bandwidth product)	01	T1 Pg.No :94-97	BB
Total Lecture Hours		**06**		
Total Hours		**06**		

UNIT-V LINEAR AND NONLINEAR APPLICATIONS OF OP-AMP				
32	Idealized analysis of op-amp circuits	01	T1 Pg.No :899-902	BB
33	Inverting amplifier and Non-inverting amplifier	01	T1 Pg.No :68-72,77-78	BB
34	Differential amplifier and Instrumentation amplifier	01	T1 Pg.No :81	BB
35	Integrator and Active filter	01	T1 Pg.No :1088-1125	BB
36	P, PI and PID controllers using an op-amp	01	//altairuniversity.com/	BB
37	Lead/lag compensator using an op-amp	01	//altairuniversity.com/	BB
38	Voltage regulator	01	T1 Pg.No :79	BB
39	Oscillators (Wein bridge and phase shift)	01	T1 Pg.No :1171,1174	BB
40	Analog to Digital Conversion	01	T1 Pg.No :925,929	BB
41	Hysteretic Comparator	01	www.electronics-tutorials.com	BB
42	Zero Crossing Detector	01	www.electronics-tutorials.com	BB
43	Square-wave and triangular-wave generators	01	T1 Pg.No :1192-1194	BB
44	Precision rectifier, Peak detector	01	T1 Pg.No :1206-1214	BB

	and Monoshot			
Total Lecture Hours		**13**		
Total Hours		**13**		

Total No of Hours for Introduction: 01 Hrs

Total No of Lecture Hours Planned: 43 Hrs

Total No of Hours Planned : 44 Hours

TEXT BOOKS:

S.NO.	Author(s) Name	Title of the book	Publisher	Year of the publication
1	A.S.Sedra and K.C.Smith	"Microelectronic circuits"	Oxford university press	1998

STAFF IN-CHARGE **HOD/ECE**

3. Diodes and Diode Circuits

3.1 Diode Characteristics

Small-Signal Diodes

Diode: a semiconductor device, which conduct the current in one direction only.

Two terminals: **anode** and **cathode**.

When the positive polarity is at the anode – the diode is **forward biased** and is conducting.

When the positive polarity is at the cathode – the diode is **reversed biased** and is not conducting.

If the reverse-biasing voltage is sufficiently large the diode is in **reverse-breakdown** region and large current flows though it.

Breakdown voltage.

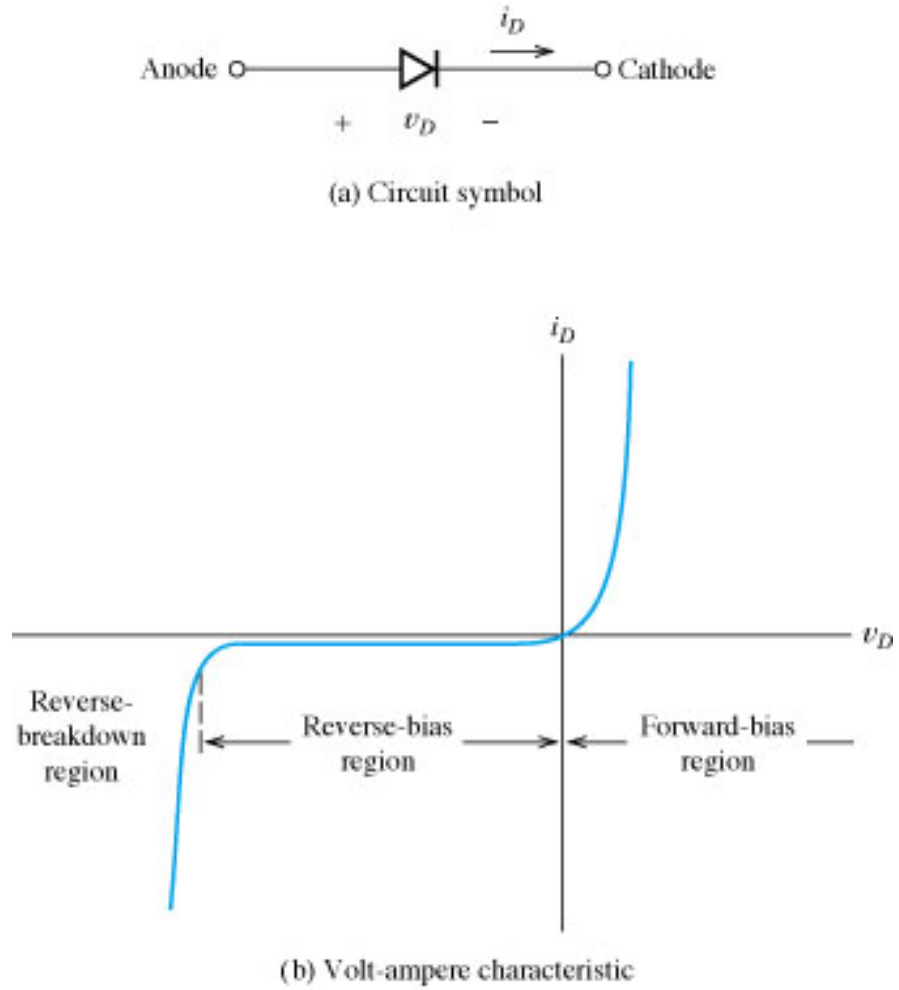


Figure 3.1 Semiconductor diode.

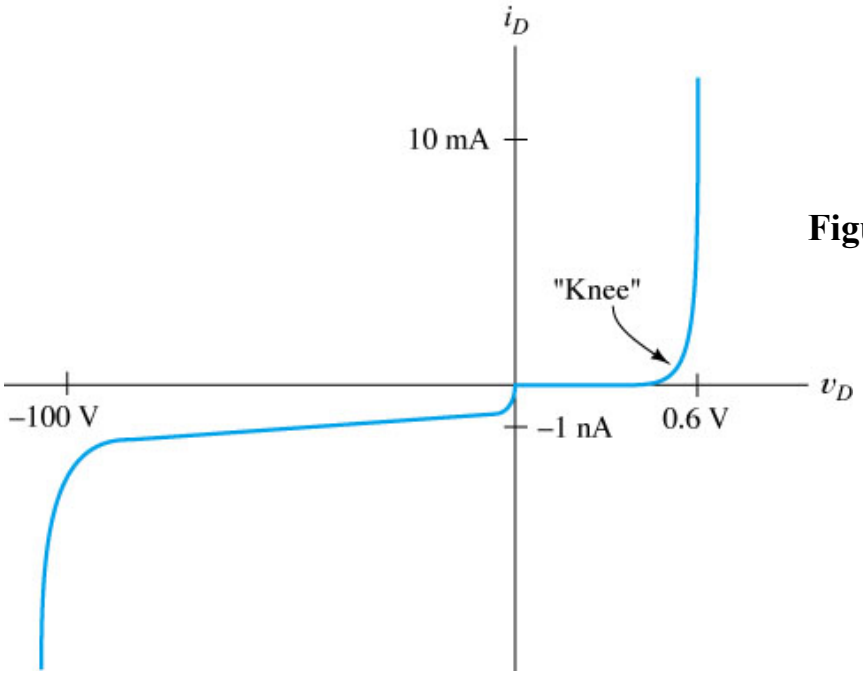


Figure 3.2 Volt-ampere characteristic for a typical small-signal silicon diode at a temperature of 300 K. Notice the changes of scale.

Voltage drop across the diode when forward biased: **0.6-0.7V**.

The current though the diode when reversed biased: ~ **1nA** (10^{-9}A)

Temperature dependence:

- As the temperature increases, the voltage of the knee decreases by 2mV/K.
- The reverse current doubles for each 10K increase in the temperature.

Zener Diodes

Zener diodes: doides intended to operate in breakdown region.

If breakdown voltage > 6V: **avalanche** breakdown.

If breakdown voltage < 6V: **tunneling** mechanism of breakdown.

Figure 3.3 Zener diode symbol.

3.3 The Ideal - Diode Model

Ideal diode:

- perfect conductor with zero voltage drop when the diode is forward biased;
- open circuit, when the diode is reversed biased.

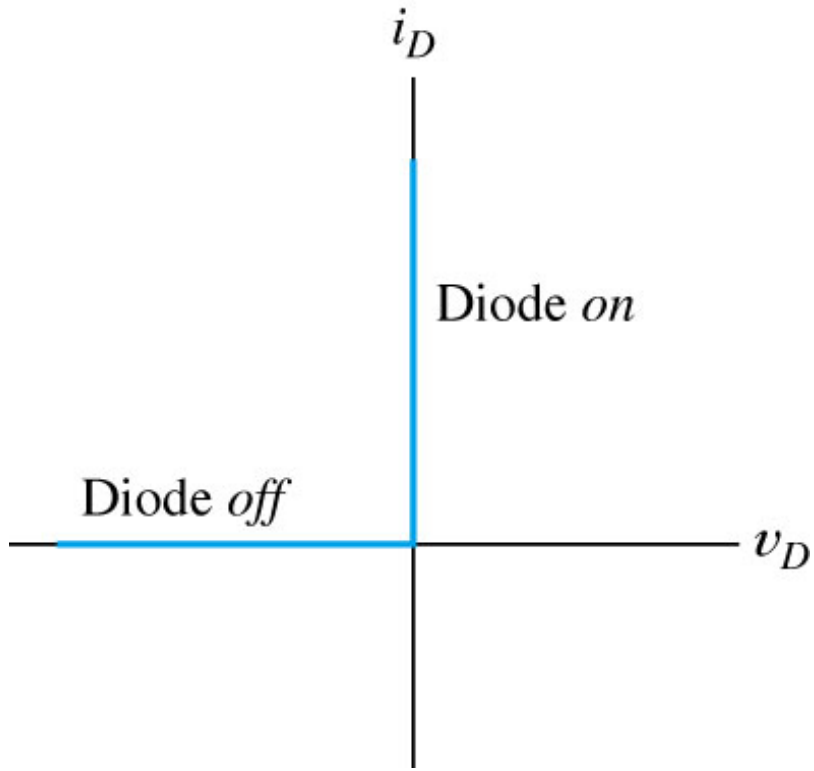
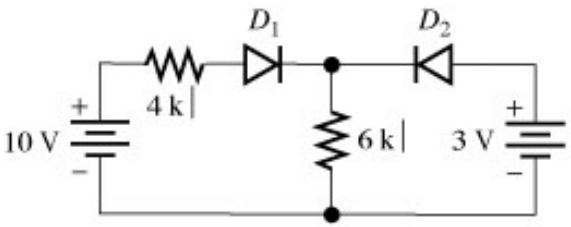


Figure 3.8 Ideal-diode volt-ampere characteristic.

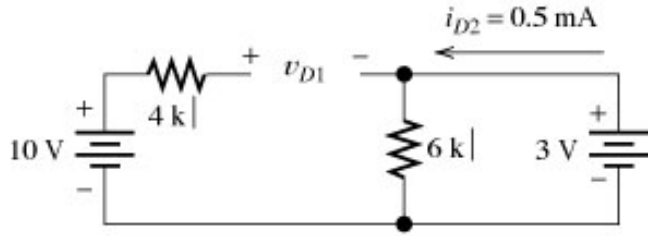
Assumed States for Analysis of Ideal - Diode Circuits

Example 3.3 Circuit Solution By Assumed Diode States

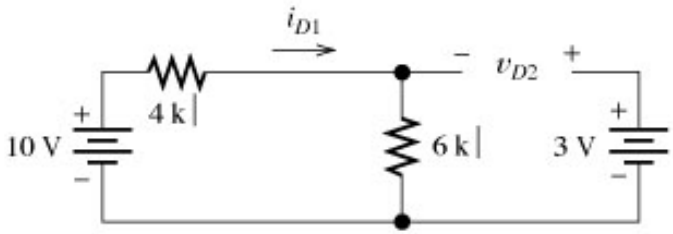
Analyze the circuit illustrated in Figure 3.9a using the ideal - diode model.



(a) Circuit diagram



(b) Equivalent circuit assuming D_1 off and D_2 on (since v_{D1} =+7 V, this assumption is not correct)



(c) Equivalent circuit assuming D_1 on and D_2 off (this is the correct assumption since i_{D1} turns out to be a positive value and v_{D2} turns out to be a negative value)

Figure 3.9 Analysis of a diode circuit using the ideal-diode model.

Solution

Step 1. We start by *assuming that D_1 is off and D_2 is on*.

Step 2. The equivalent circuit is shown in Figure 3.9b. i_{D2}=0.5mA and v_{D1}=7V.

Step 3. We have v_{D1}=+7V, which is not consistent with our assumption.

Another Assumption

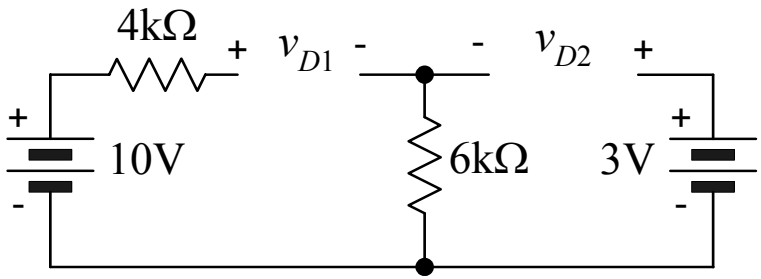
Step 1. We assume that *D_1 is on and D_2 is off.*

Step 2. The equivalent circuit is shown in Figure 3.5c. i_{D1}=1 mA and v_{D2}= -3 V.

Step 3. These conditions are consistent with the assumption.

Exercise 3.2

Show that the condition D_1 off and D_2 off is not valid for the circuit of the Figure 3.9a.



Equivalent circuit to Figure 3.9a when D_1 is off and D_2 is off.

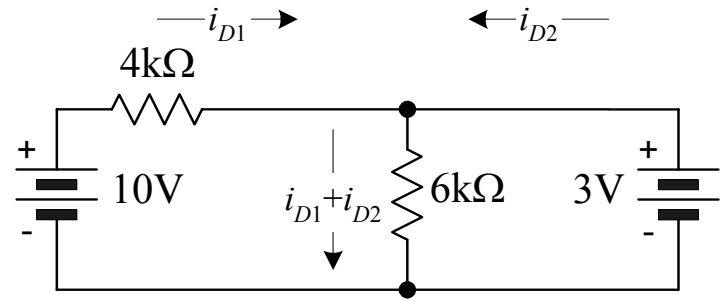
Solution

$v_{D1} = 10\text{V}$; $v_{D2} = 3\text{V}$.

The both diodes must be on since the voltages across them are positive.

Exercise 3.3

Show that the condition D_1 on and D_2 on is not valid for the circuit of the Figure 3.9a.



Equivalent circuit to Figure 3.9a when D_1 is on and D_2 is on.

Solution

$$i_{D1} + i_{D2} = \frac{3\text{V}}{6\text{k}\Omega} = 0.5\text{mA}$$

$$i_{D1} = \frac{10\text{V} - 3\text{V}}{4\text{k}\Omega} = 1.75\text{mA}$$

$$i_{D2} = (i_{D1} + i_{D2}) - i_{D1} = 0.5 - 1.75 = -1.25\text{mA}$$

The negative sign of i_{D2} means that it flows in the opposite direction to the assumed, i.e. from the cathode to the anode of D_2. This is impossible.

3.4 Rectifier Circuits

Rectifiers: circuits, which convert ac power into dc power.

Half - Wave Rectifier Circuits

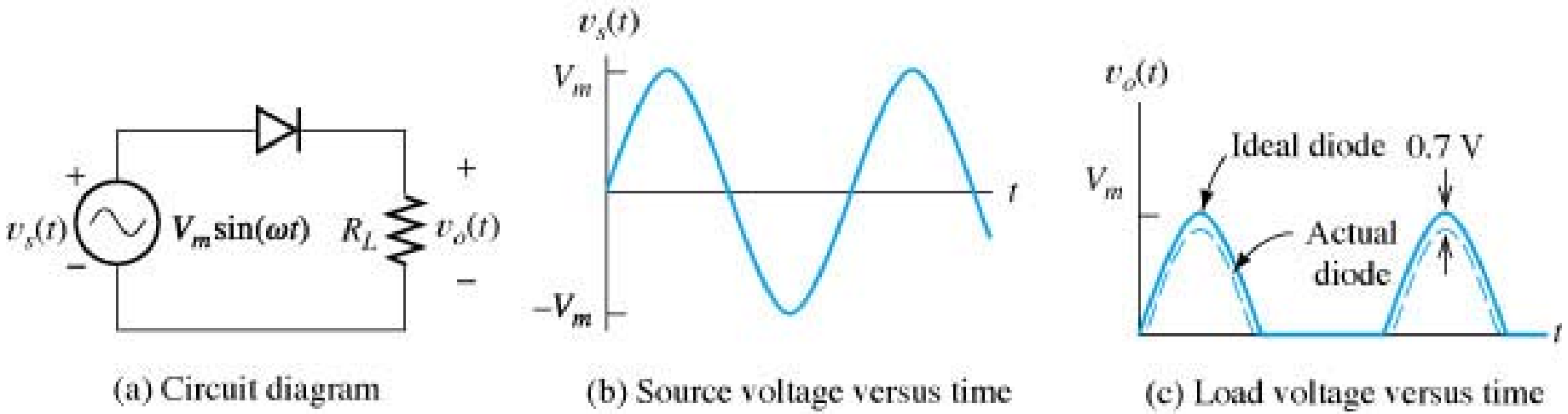
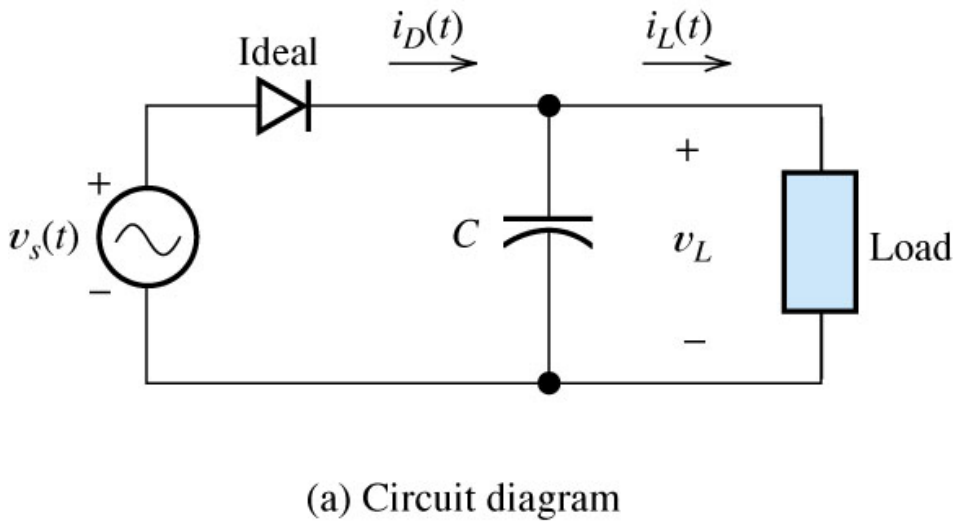


Figure 3.11 Half-wave rectifier with resistive load.

Half - Wave Rectifier with Smoothing Capacitor



(a) Circuit diagram

Figure 3.12a Half-wave rectifier with smoothing capacitor.

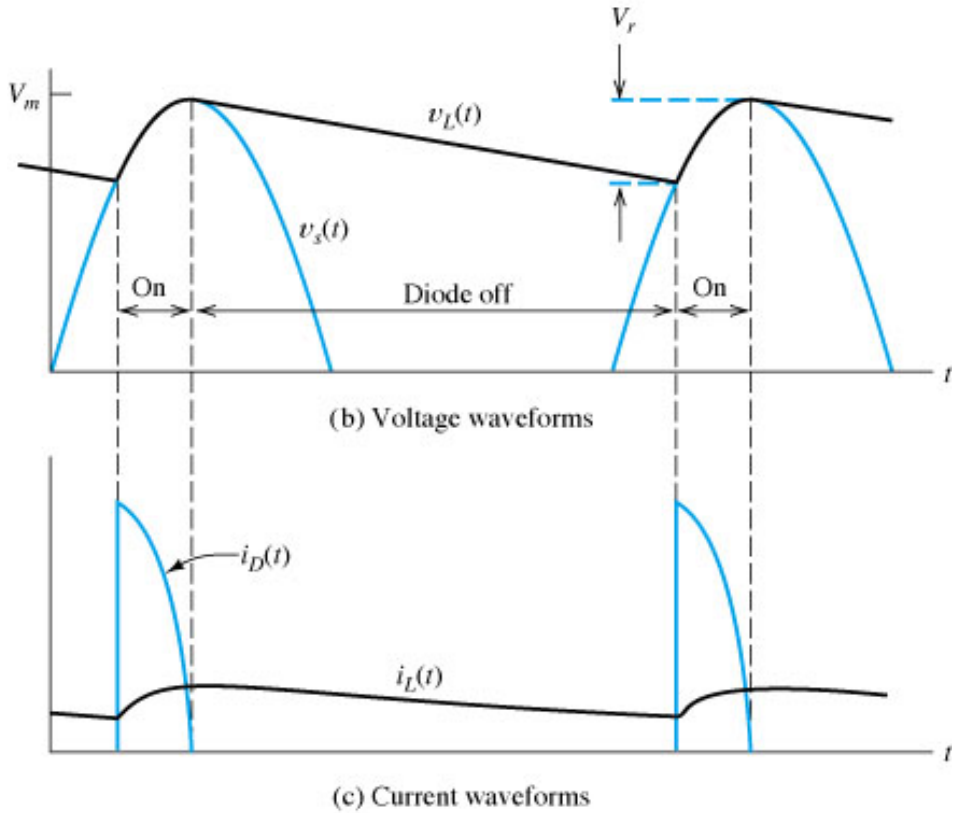


Figure 3.12b & c Half-wave rectifier with smoothing capacitor.

Peak Inverse Voltage

Peak inverse voltage (PIV) across the diode: a parameter, which defines the choice of the diode.
For Figure 3.11 PIV = V_m;
For Figure 3.12 PIV ≈ $2V_m$.

Problem 3.24 Half-wave battery charger.
Consider the battery charging circuit in Figure P3.24 with $V_m = 20\text{V}$, $R = 10\Omega$ and $V_B = 14\text{V}$. Find the peak current assuming an ideal diode. Also, find the percentage of each cycle in which the diode is in on state. Sketch $v_s(t)$ and $i(t)$ to scale against time.

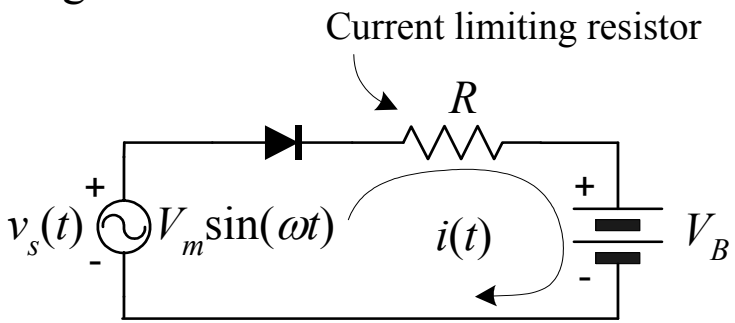


Figure P3.24 Half-wave battery charger.

Solution:

The diode is on when

$$V_m \sin(\omega t) > V_B \quad \text{or} \quad 20\sin(\omega t) > 14$$

The diode goes to on state at

$$20\sin(\omega t) = 14$$

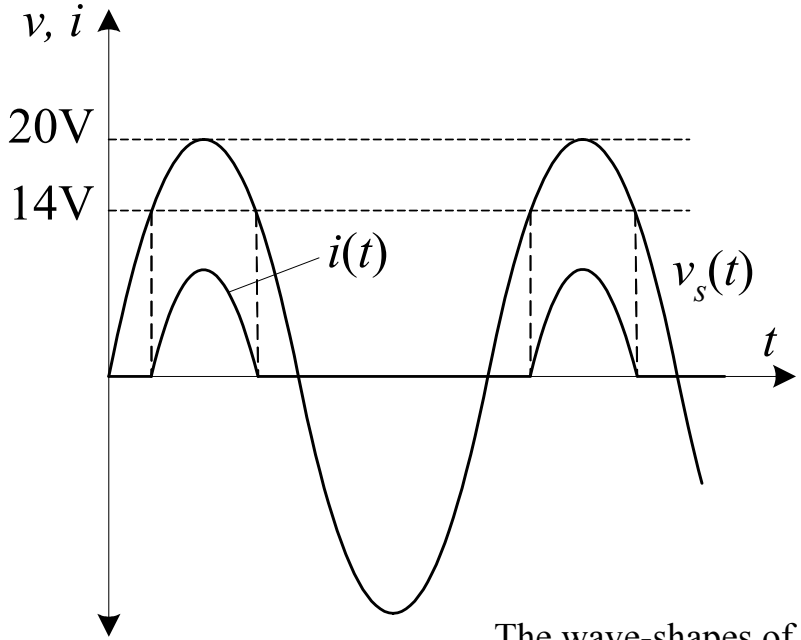
$$\omega t = \arcsin\frac{14}{20} = \arcsin 0.7 \approx 45^0;\ 135^0$$

The diode is on for $45° \le \omega t \le 135°$ or for 90° of the phase angle. The whole period is 360°, so the diode is on for

$$\frac{90^0}{360^0} = 0.25 = 25\% \text{ of the time.}$$

The peak current is when the ac voltage is at the peak and is

$$I_m = \frac{V_m - V_B}{R} = \frac{20-14}{10} = 0.6\text{A}$$



The wave-shapes of $v_s(t)$ and $i(t)$.

Full - Wave Rectifier Circuits

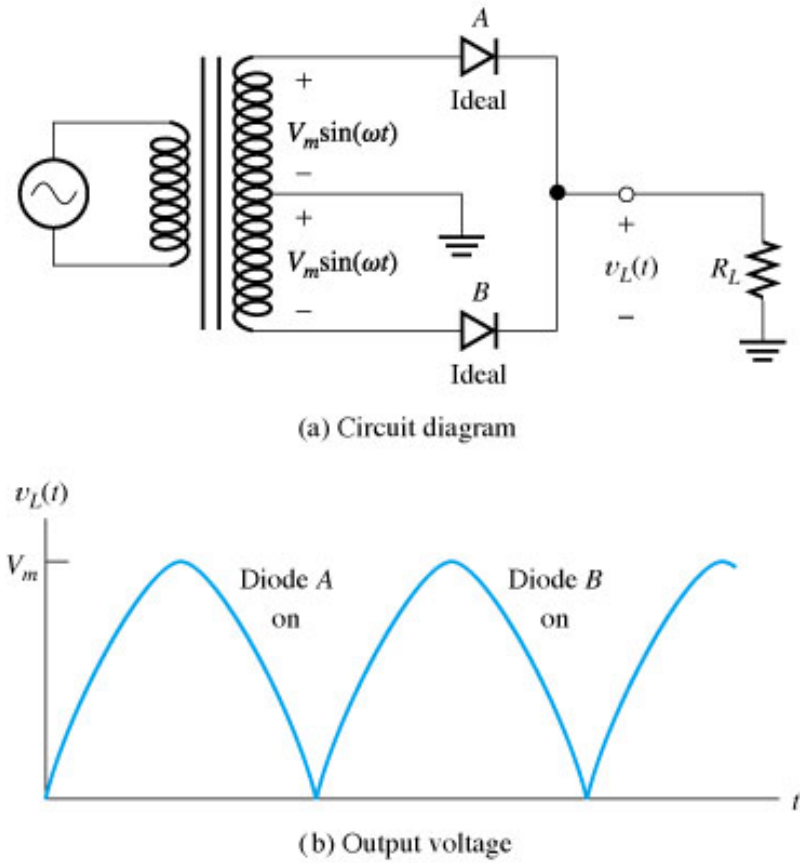


Figure 3.13 Full-wave rectifier.

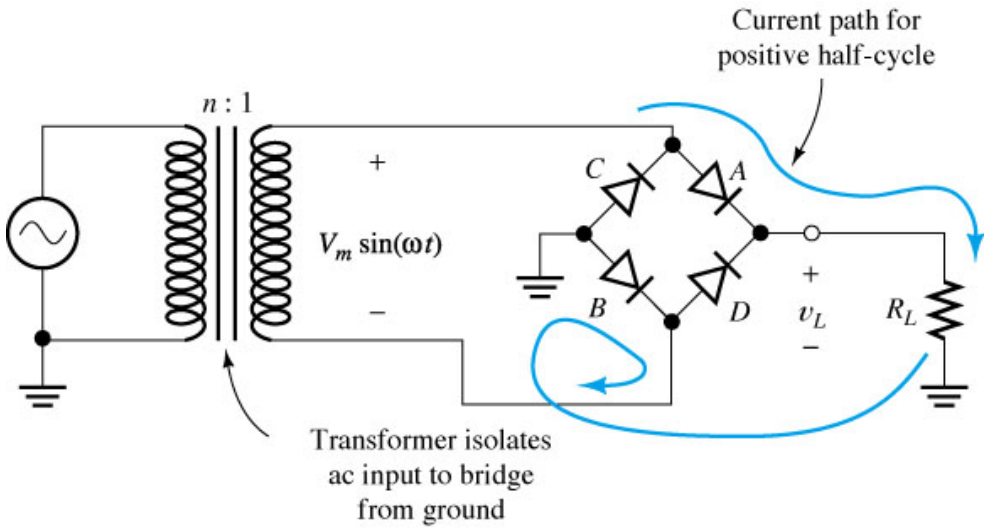


Figure 3.14 Diode-bridge full-wave rectifier.

3.7 Voltage - Regulator Circuits

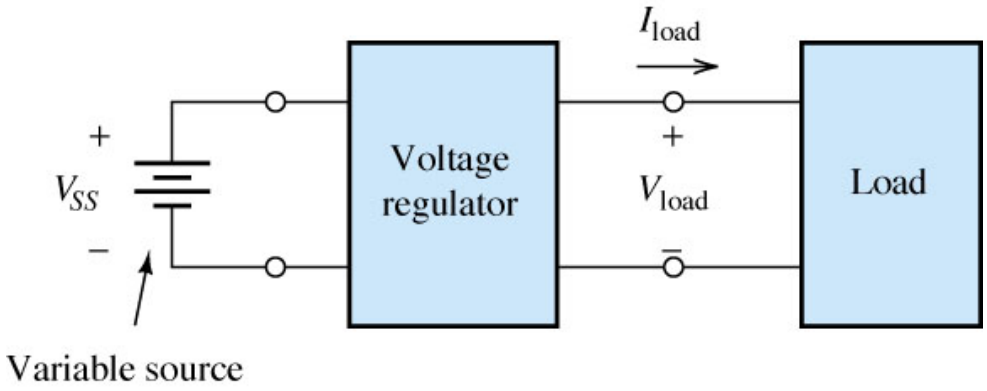


Figure 3.24 A voltage regulator supplies constant voltage to a load.

A Simple Zener-Diode Voltage Regulator

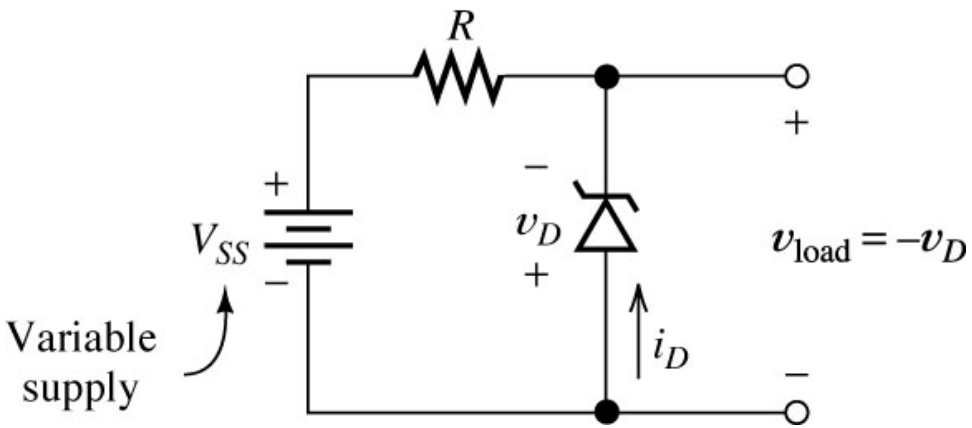
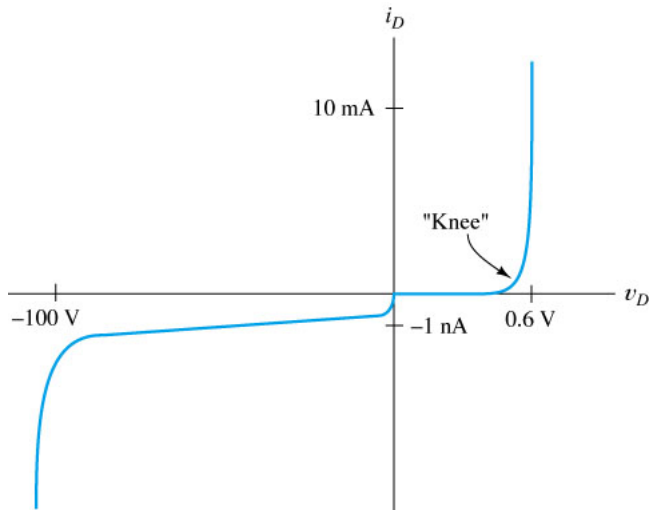


Figure 3.25 A simple regulator circuit that provides a nearly constant output voltage from a variable supply voltage.



In the voltage regulator the zener-diode operates in the breakdown region, which ensures approximately constant voltage across it.

3.6 Linear Small - Signal Equivalent Circuits

Dynamic Resistance

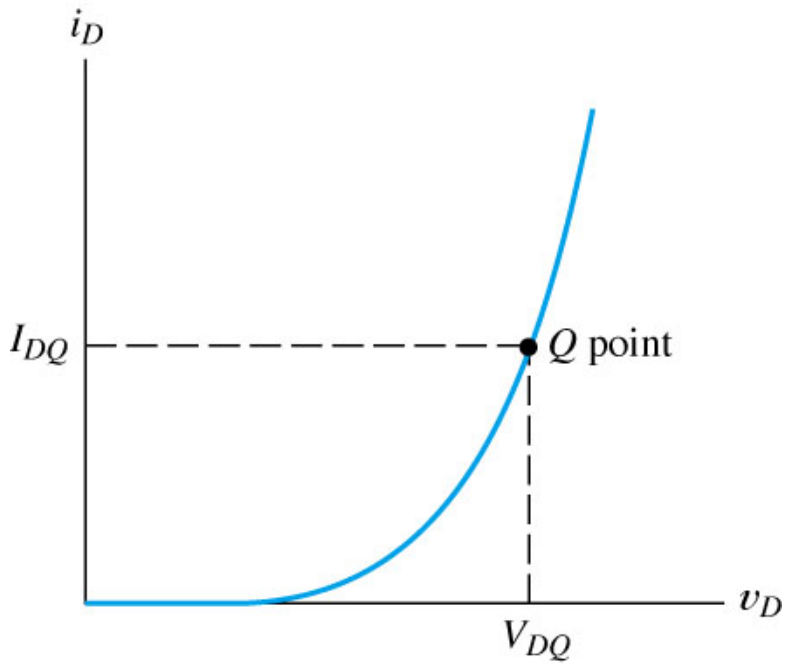


Figure 3.31 Diode characteristic, illustrating the Q-point.

$$\Delta i_D \cong \left(\frac{di_D}{dv_D}\right)_Q \Delta v_D \qquad (3.11)$$

$$r_D \cong \left[\left(\frac{di_D}{dv_D}\right)_Q\right]^{-1} \qquad (3.12)$$

$$\Delta i_D \cong \frac{\Delta v_D}{r_D} \qquad (3.13)$$

$$i_D = \frac{v_D}{r_D} \qquad (3.14)$$

The Shockley Equation

$$i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right)-1\right] \qquad (3.15)$$

I_s – **saturation current**. For small signal diodes at 300K: $I_s \sim 10^{-14}$A.

n – **emission coefficient**; n = 1 .. 2 for small-signal diodes.

V_T – thermal voltage:

$$V_T = \frac{kT}{q} \qquad (3.16)$$

T – absolute temperature in K;

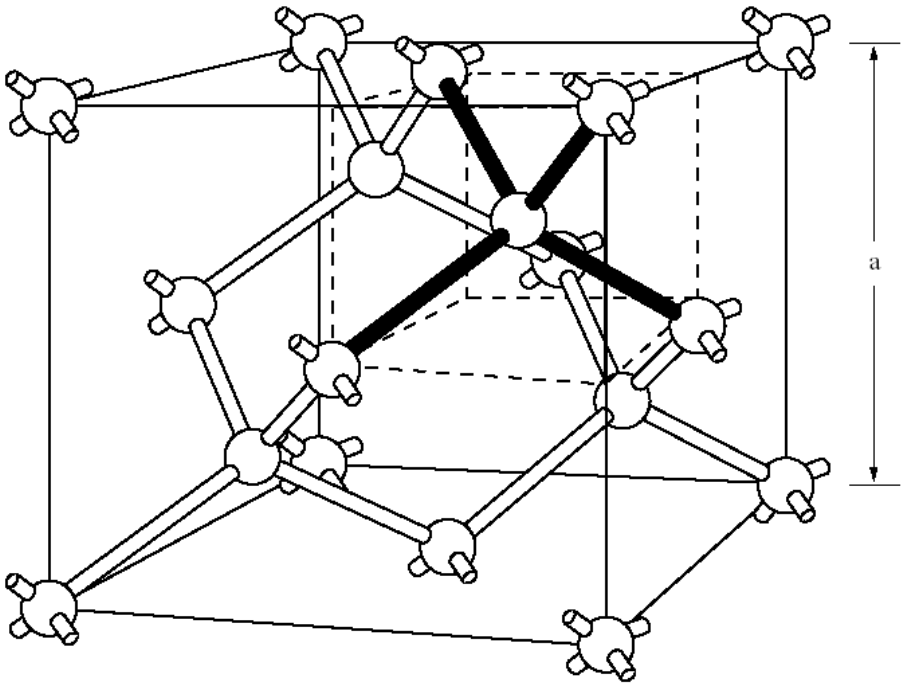
$k = 1.38\times10^{-23}$J/K – the Boltzmann's constant;

$q = 1.60\times10^{-19}$C – the charge of the electron;

At T = 300K $\boldsymbol{V_T \approx 0.026\text{V} = 26\text{mV}}$

3.7 Basic Semiconductor Concepts

Intrinsic Silicon



Crystalline lattice of intrinsic silicon in the space.

Bohr model of the silicon atom:

- 14 electrons surround the nucleus;
- Electron orbits grouped in shells
- Outermost orbit contains 4 electrons – **valence shell**;
- Atoms are arranged in crystalline lattice;
- Each pair of neighbor atoms in the lattice form a **covalent bond**;
- The covalent bond consists from two electrons that orbit around the both atoms. Each atom contributes one electron in the pair.
- At 0K temperature all valence electrons are in bound in the covalence bonds and the conductivity is 0.

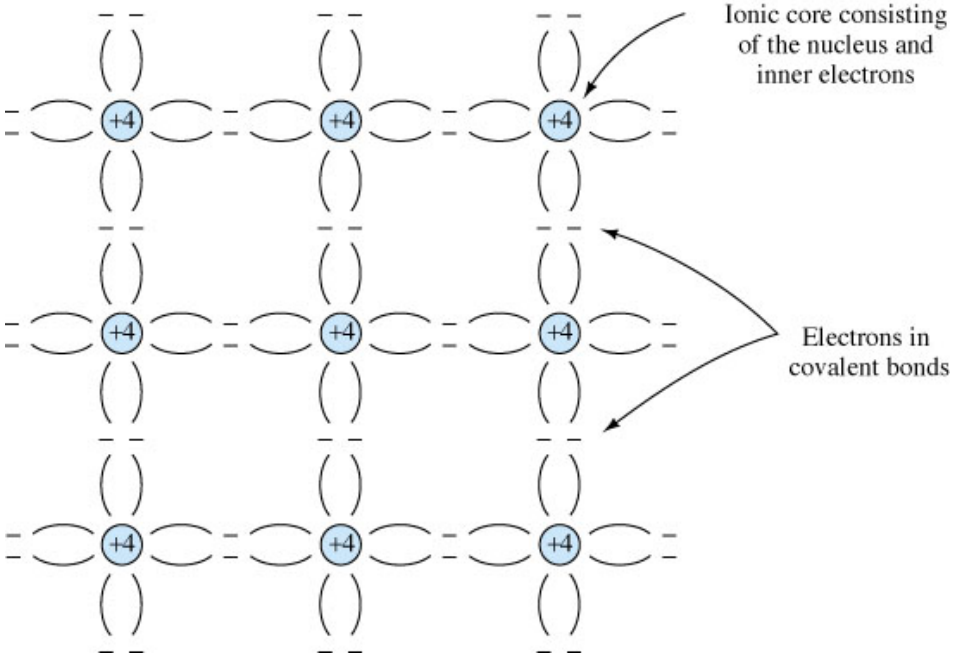


Figure 3.36 Intrinsic silicon crystal (simplified picture in the plane).

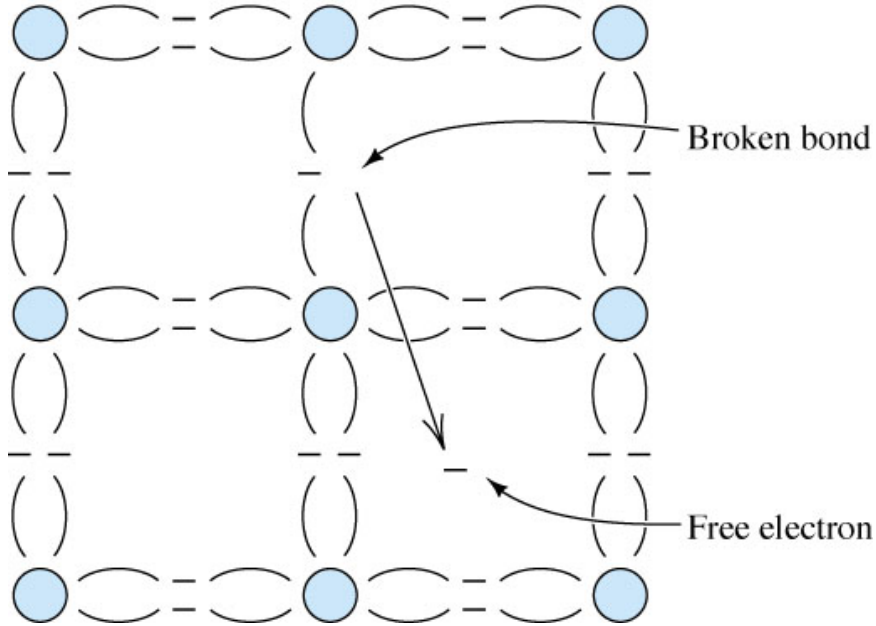


Figure 3.37 Thermal energy can break a bond, creating a vacancy and a free electron, both of which can move freely through the crystal.

Free electrons appear at room temperature due to breaking of the covalent bonds. Only one per 1.4×10^{13} bonds is broken.

The concentration of the free electrons is small, $n_i \approx 10^{14}$ free electrons per cm^3.

The conductivity is small: **semiconductor**.

Conduction by Holes

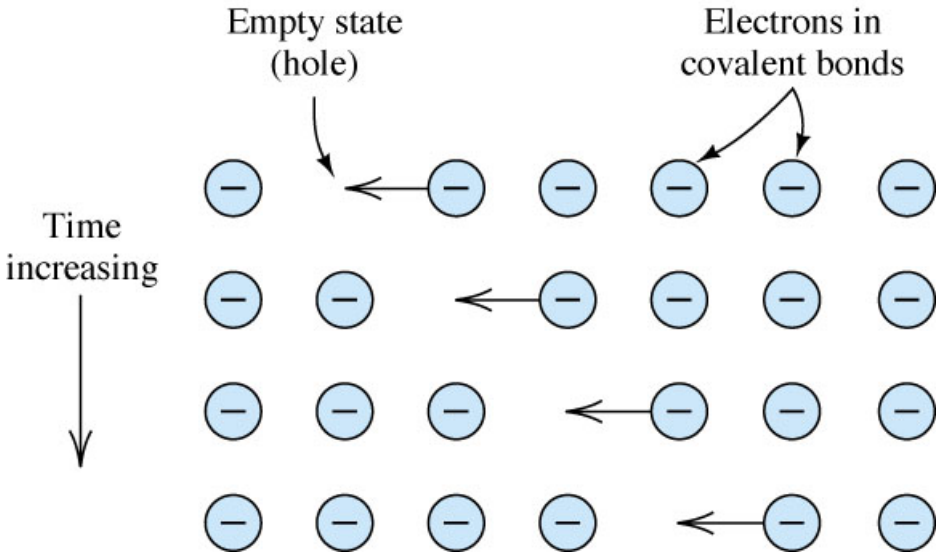


Figure 3.38 As electrons move to the left to fill a hole, the hole moves to the right.

After breaking the bond the atom is positive charged and the vacancy of the electron is called **hole**.

In the intrinsic silicon the concentration of the electrons n_i is equal to the concentration of the holes p_i:

$$n_i = p_i \qquad (3.24)$$

Generation and Recombination

Generation: breaking the covalent bonds and appearing free electrons and holes.

Recombination: free electron encounters a hole.

At higher temperature the rate of the generation is higher.

When the temperature is constant, the generation and recombination are in equilibrium.

n - Type Semiconductor Material

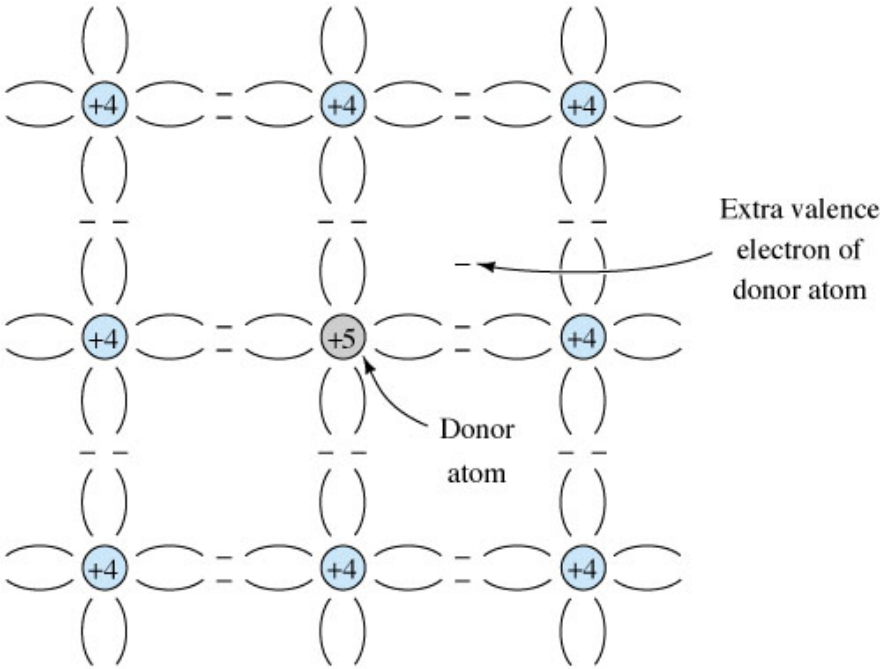


Figure 3.39 *n*-type silicon is created by adding valence five impurity atoms.

Extrinsic semiconductor: silicon with small concentration of impurities, which change its conductivity.

Donor atom: atom of 5th valence. Example: phosphorus.

The extra valence electron of the phosphorus always is free electron.

$$n = p + N_D \qquad (3.25)$$

***n*-type semiconductor:** semiconductor with 5th valence impurities and conductivity, based on the free electrons mostly.

Majority carriers in *n*-type silicon: *electrons*.

Minority carriers in *n*-type silicon: *holes*.

p - Type Semiconductor Material

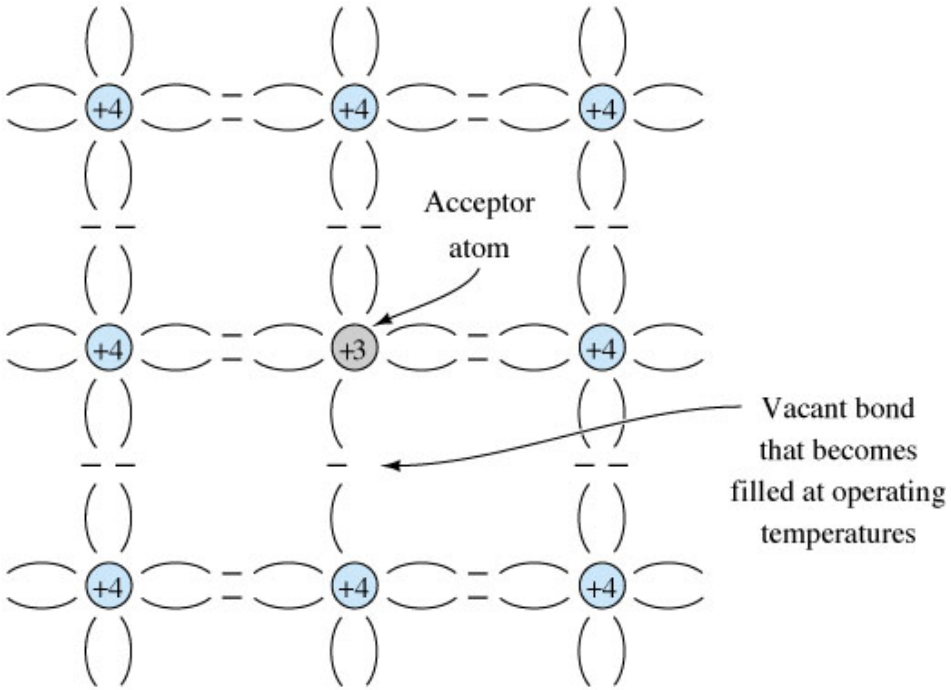


Figure 3.40 *p*-type silicon is created by adding valence three impurity atoms.

Acceptor: atom of 3rd valence. Example: boron.

The acceptor atoms always accept an extra electron, creating negative ionized cores and shortage of free electrons.

$$N_A + n = p \qquad (3.28)$$

***p*-type semiconductor:** semiconductor with 3rd valence impurities and conductivity, based on the holes mostly.

Majority carriers in *p*-type silicon: *holes*.

Minority carriers in *p*-type silicon: *electrons*.

The Mass - Action Law

$$pn = p_i n_i \qquad (3.26)$$

Since $p_i = n_i$

$$pn = n_i^2 \qquad (3.27)$$

Cycling the type of the material

In fabricating the integrated circuits the impurities are added in stages, changing every time the type of the conductivity

$$p + N_D = n + N_A \qquad (3.29)$$

Drift

- The carriers move in random fashion in the crystal due to thermal agitation.
- If electric field is applied to the random motion is added a constant component.
- The averaged motion of the charge carriers due to the electric field: **drift.**
- Drift velocity is proportional to the electric field vector.

$$\mathbf{V}_n = -\mu_n \mathbf{E} \qquad (3.30)$$

$$\mathbf{V}_p = \mu_p \mathbf{E} \qquad (3.31)$$

μ_n is the mobility of the free electrons;
μ_p is the mobility of the holes.

$$\mu_p < \mu_n$$

Diffusion

If there is a difference in the concentration of the charges in the crystal, appears a flow of charges toward the region with small concentration, determining **diffusion current**.

3.8 Physics of the Junction Diode

The Unbiased *pn* Junction

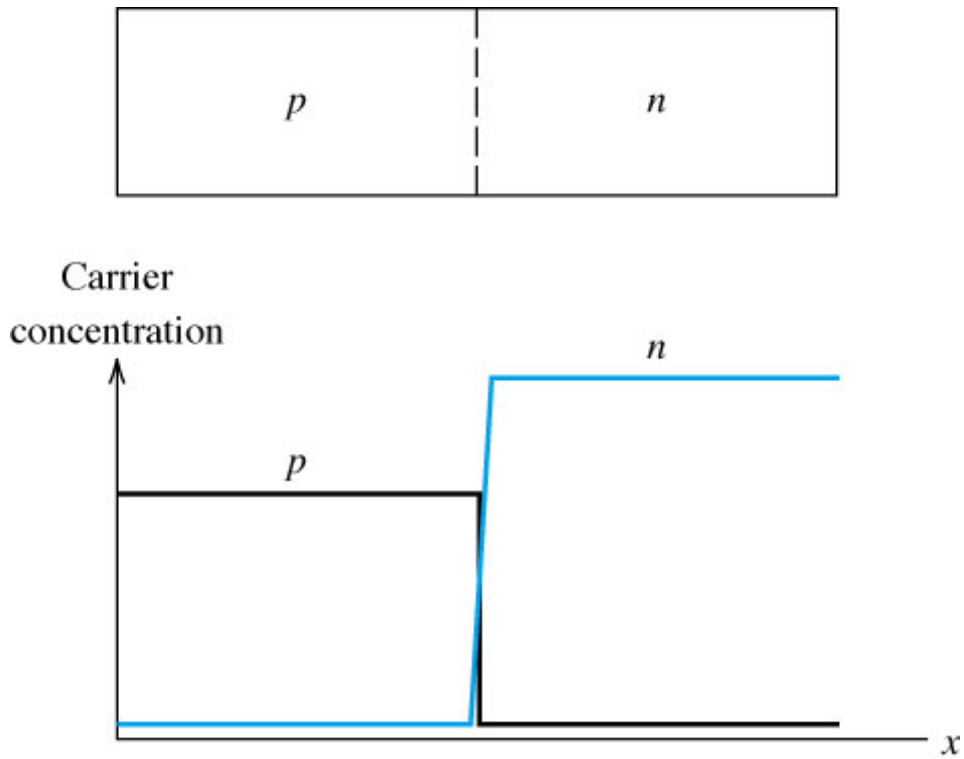


Figure 3.42 If a *pn* junction could be formed by joining a *p*-type crystal to an *n*-type crystal, a sharp gradient of hole concentration and electron concentration would exist at the junction immediately after joining the crystals.

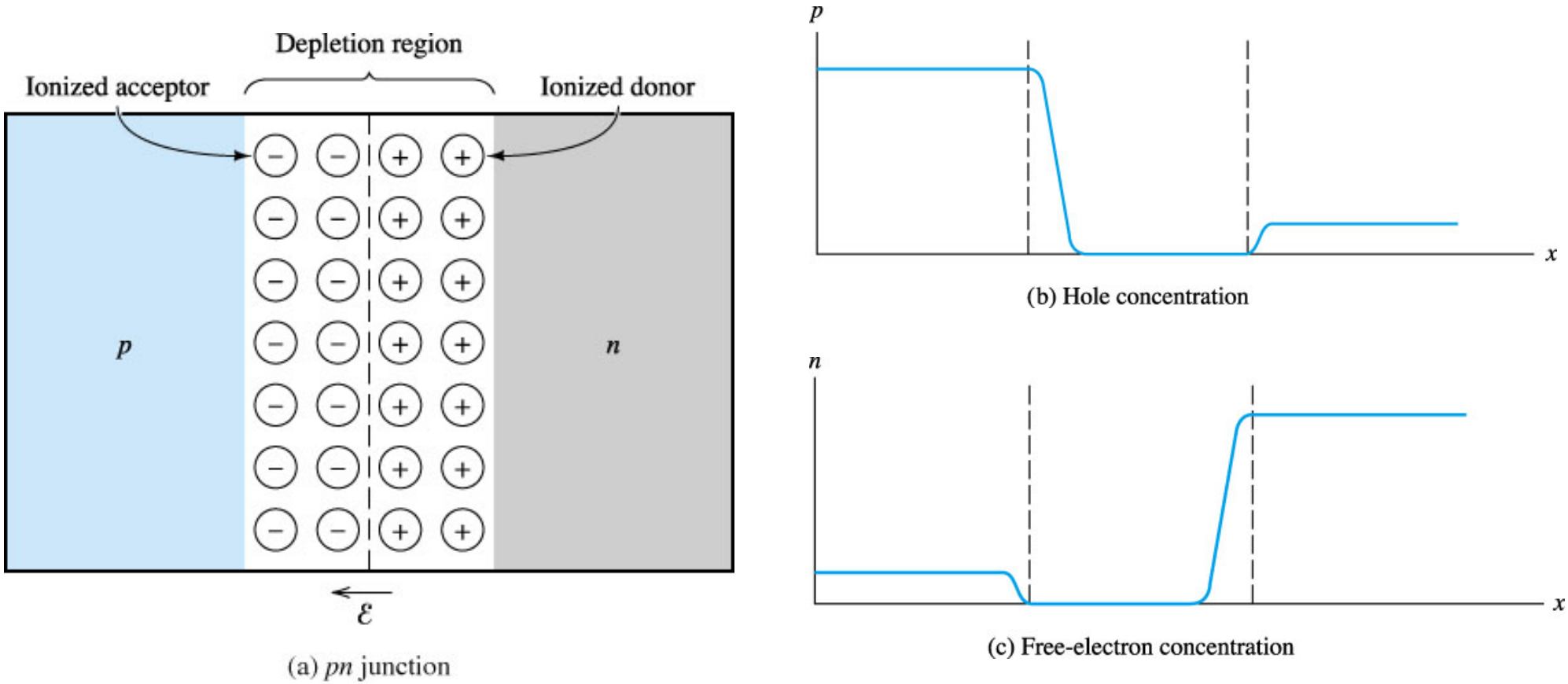


Figure 3.43 Diffusion of majority carriers into the opposite sides causes a **depletion region** to appear at the junction.

The field of depletion region prevents the flow of majority carriers.
A **built-in barrier potential** exists for them due to depletion region.

The *pn* Junction with Reverse Bias

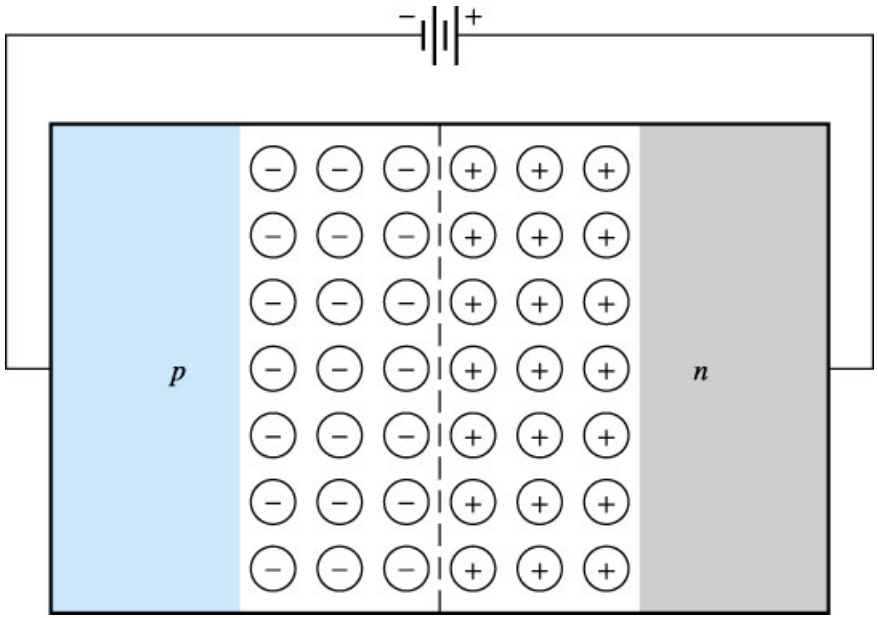


Figure 3.44 Under reverse bias, the depletion region becomes wider.

Reverse bias: when the external voltage has the same polarity as the field of the depletion region.

Reversed biasing extends the depletion region and fully stops the current through the diode.

The *pn* Junction with Forward Bias

Forward bias: when the external voltage has opposite polarity to the field of the depletion region.

Forward biasing narrows the depletion region and reduces the barrier potential. When the barrier potential is reduced to 0, a significant current flows through the diode.

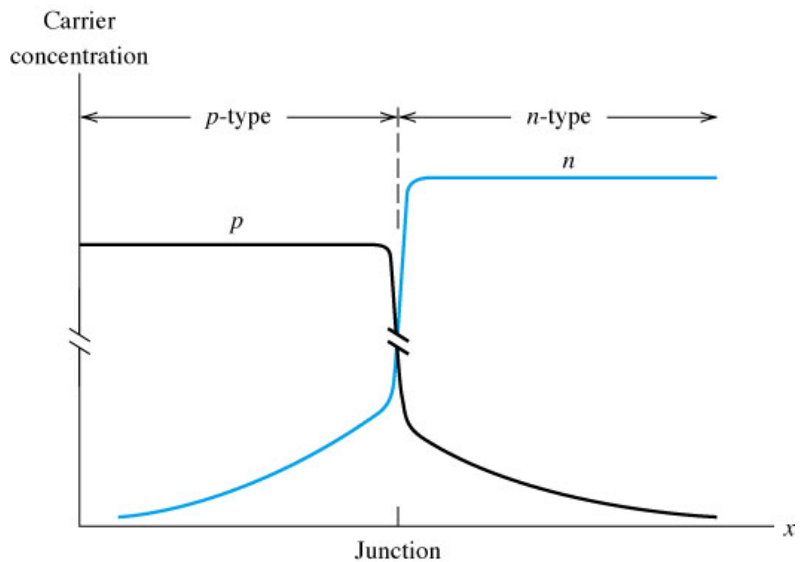


Figure 3.45 Carrier concentration versus distance for a forward biased *pn* junction.

3.9 Switching and High - Frequency Behavior

Review of Capacitance

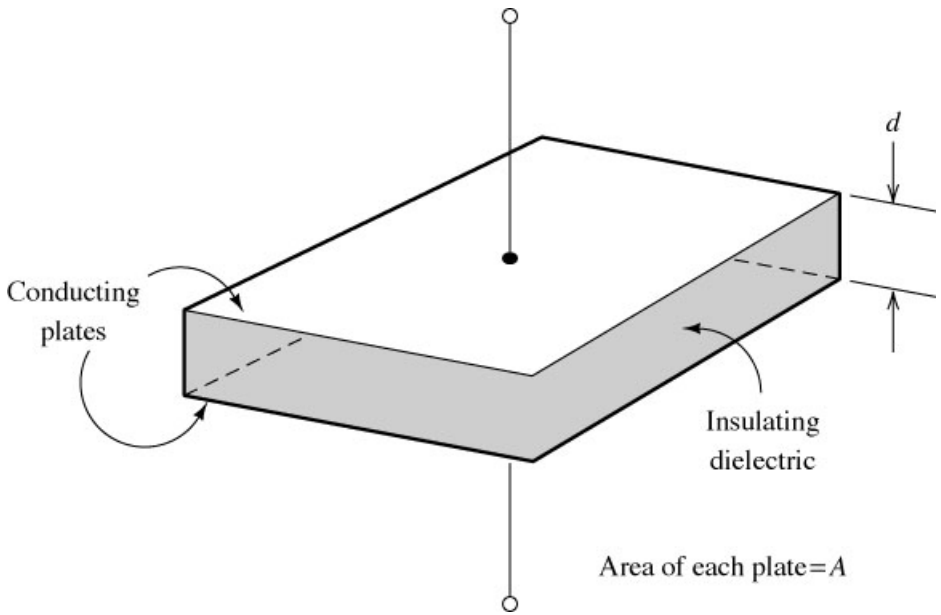


Figure 3.46 Parallel-plate capacitor.

$$Q = CV \qquad (3.33)$$

$$C = \frac{\varepsilon A}{d} \qquad (3.34)$$

Depletion Capacitance

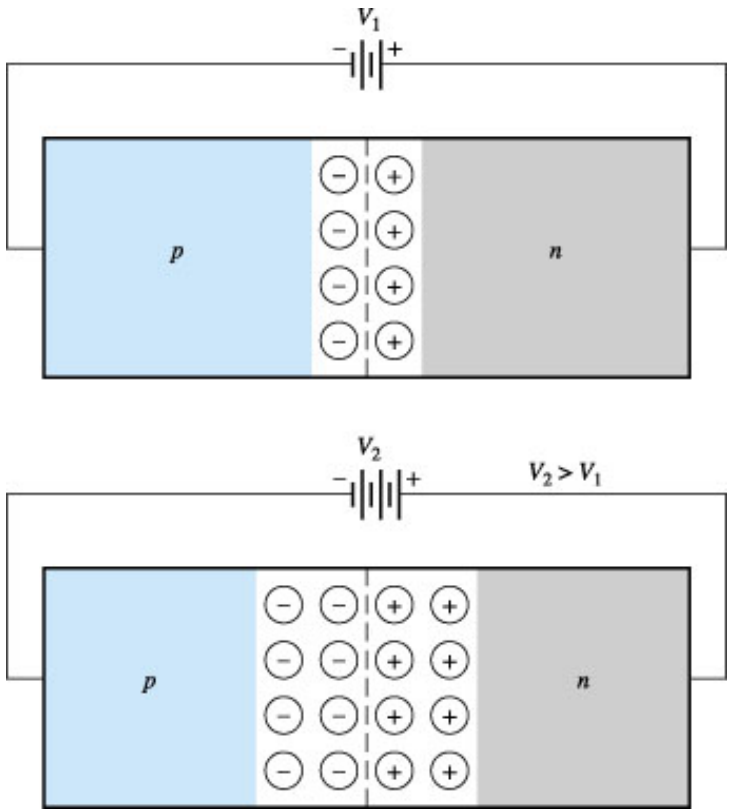


Figure 3.46 As the reverse bias voltage becomes greater, the charge stored in the depletion region increases.

$$C = \left| \frac{dQ}{dv_D} \right| \tag{3.36}$$

$$C = \frac{C_{j0}}{\left[1 - \left(V_{DQ} / \phi_0\right)\right]^m} \tag{3.37}$$

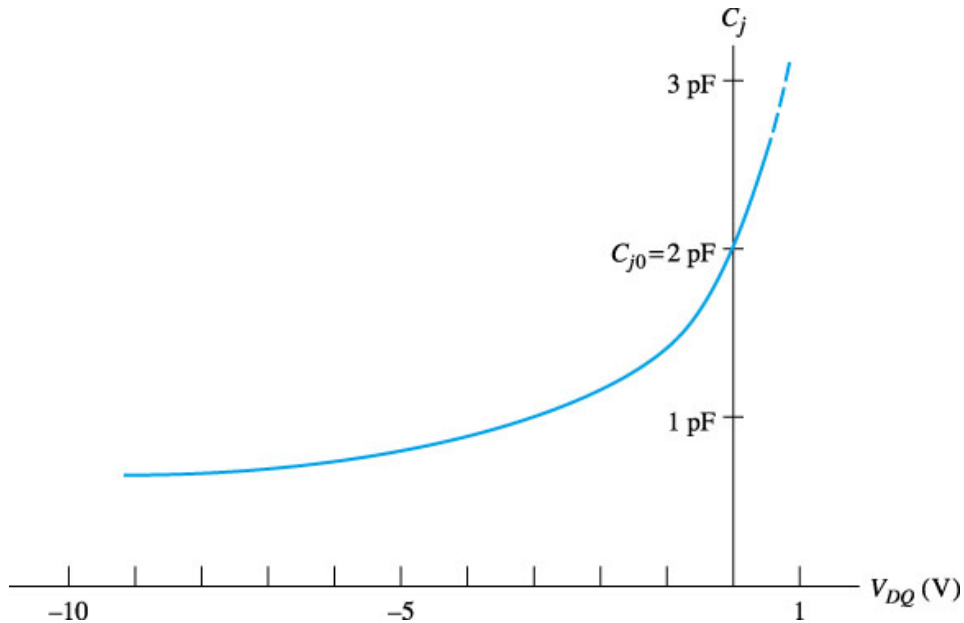


Figure 3.48 Depletion capacitance versus bias voltage for the 1N4148 diode.

Diffusion Capacitance

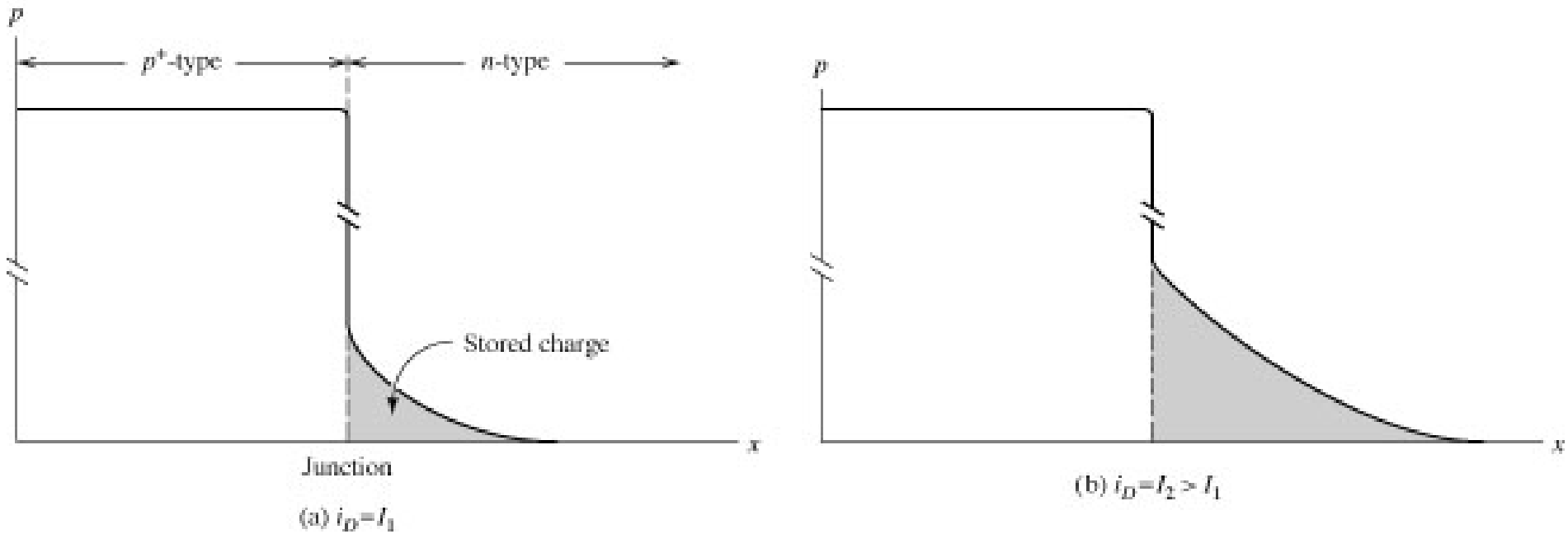


Figure 3.49 Hole concentration versus distance for two values of forward current.

$$C_{dif} = \frac{\tau_T I_{DQ}}{V_T} \qquad (3.38)$$

Complete Small - Signal Diode Model

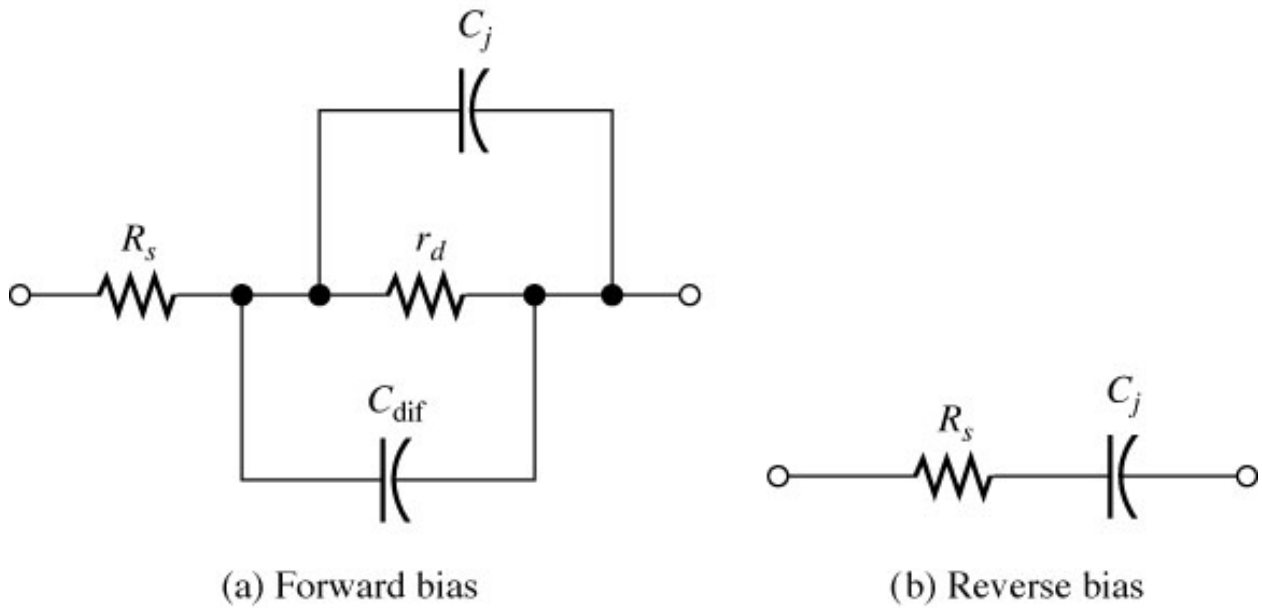


Figure 3.50 Small-signal linear circuits for the *pn*-junction diode.

Large - Signal Switching Behavior

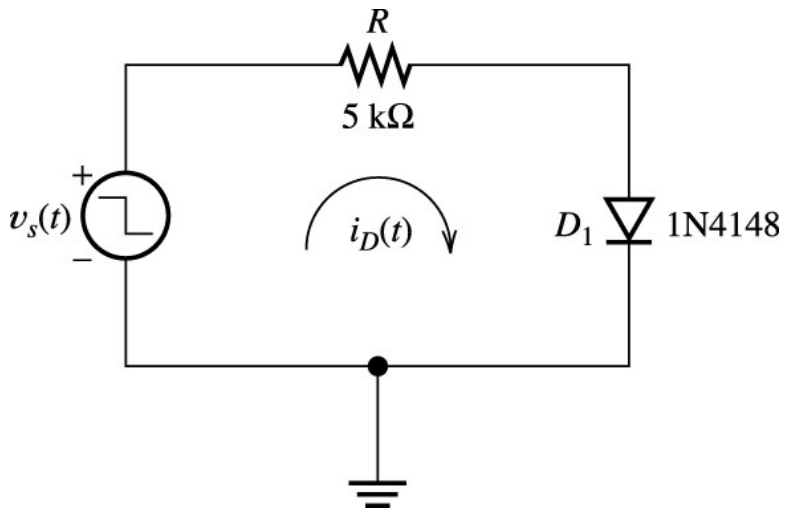


Figure 3.51 Circuit illustrating switching behavior of a *pn*-junction diode.

t_s – **storage interval;**

t_t – **transition time;**

t_{rr} – **reverse recovery time:** total time in which the diode is open after switching

$$t_{rr} = t_s + t_t \qquad (3.40)$$

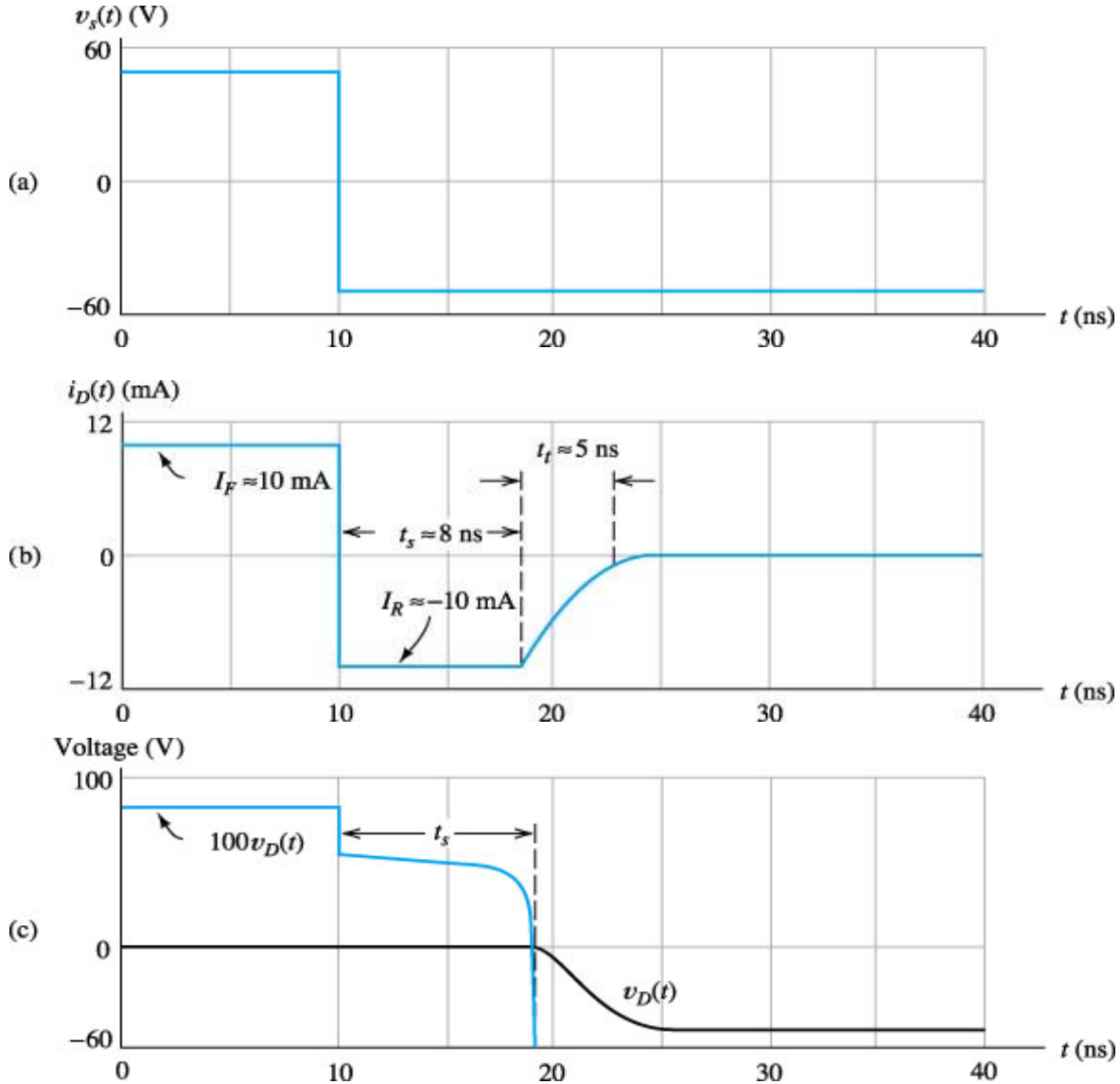


Figure 3.52 Waveforms for the circuit of Figure 3.51.

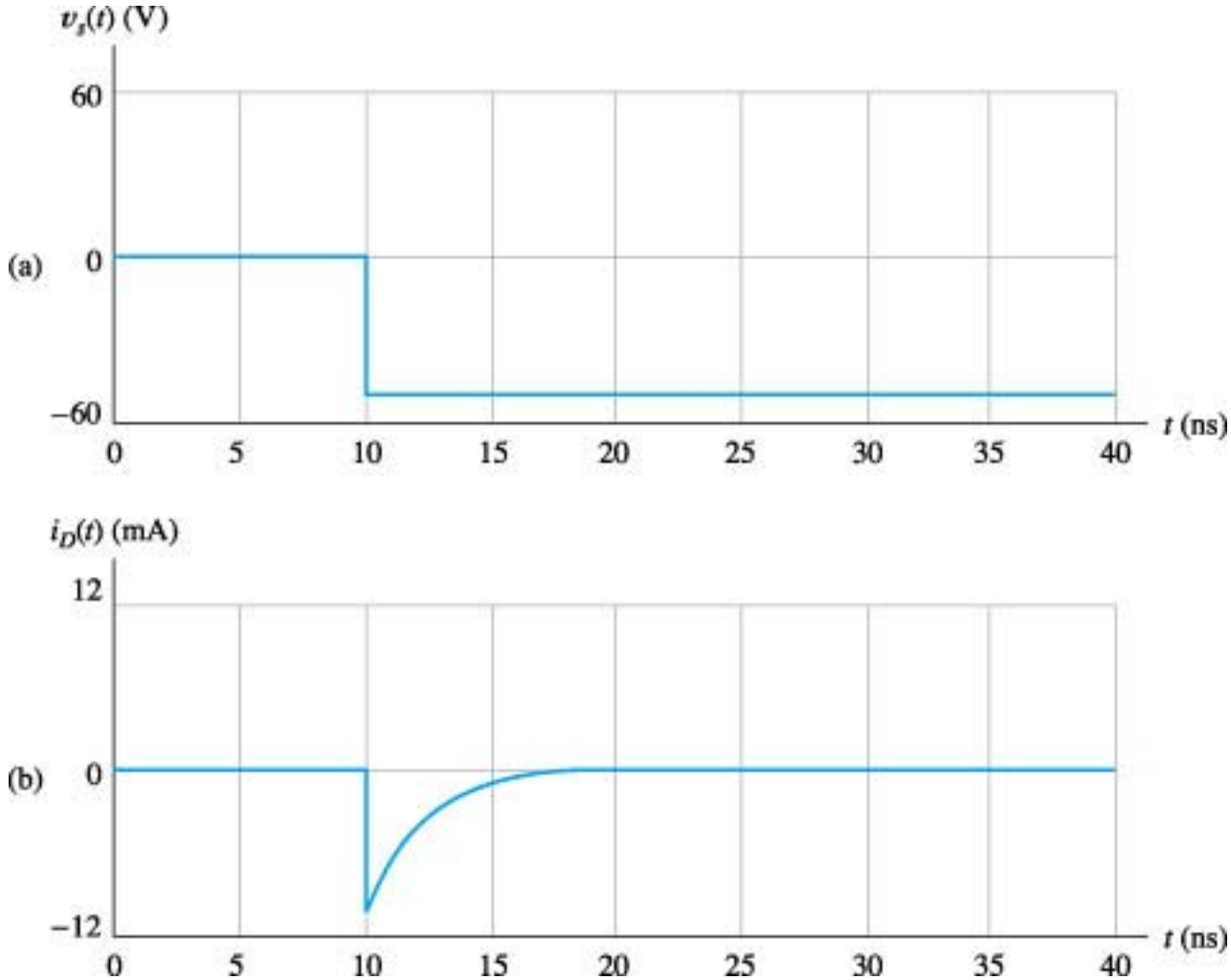


Figure 3.53 Another set of waveforms for the circuit of Figure 3.51. Notice the absence of a storage interval.

BJT Amplifier Circuits

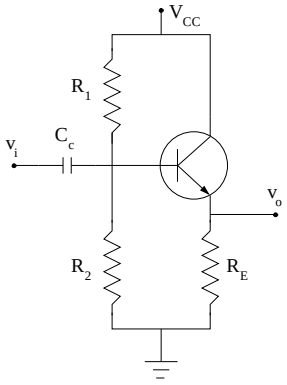
As we have developed different models for DC signals (simple large-signal model) and AC signals (small-signal model), analysis of BJT circuits follows these steps:

DC biasing analysis: Assume all capacitors are open circuit. Analyze the transistor circuit using the simple large signal mode as described in pp 57-58.

AC analysis:
1) Kill all DC sources
2) Assume coupling capacitors are short circuit. The effect of these capacitors is to set a lower cut-off frequency for the circuit. This is analyzed in the last step.
3) Inspect the circuit. If you identify the circuit as a prototype circuit, you can directly use the formulas for that circuit. Otherwise go to step 3. 3) Replace the BJT with its small signal model.
4) Solve for voltage and current transfer functions and input and output impedances (node-voltage method is the best).
5) Compute the cut-off frequency of the amplifier circuit.

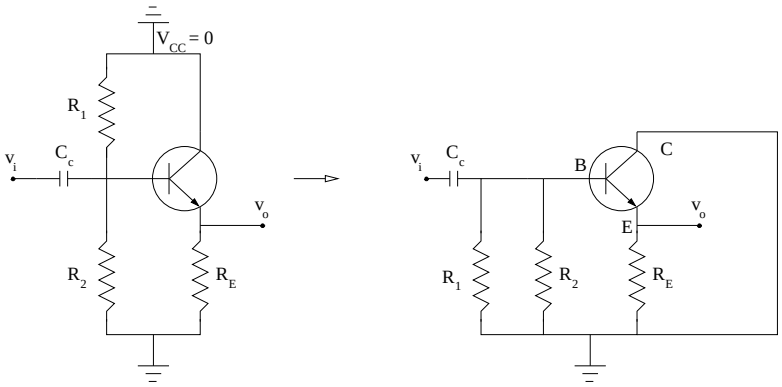
Several standard BJT amplifier configurations are discussed below and are analyzed. Because most manufacturer spec sheets quote BJT "h" parameters, I have used this notation for analysis. Conversion to notation used in most electronic text books (r_π, r_o, and g_m) is straight-forward.

Common Collector Amplifier (Emitter Follower)

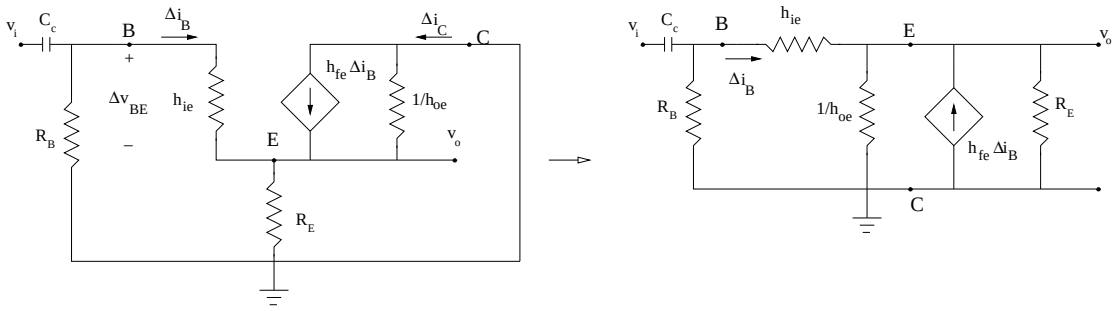


DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 79 with $R_c = 0$. The bias point currents and voltages can be found using procedure of pages 78-81.

AC analysis: To start the analysis, we kill all DC sources:



We can combine R_1 and R_2 into R_B (same resistance that we encountered in the biasing analysis) and replace the BJT with its small signal model:



The figure above shows why this is a common collector configuration: collector is shared between input and output AC signals. We can now proceed with the analysis. Node voltage method is usually the best approach to solve these circuits. For example, the above circuit will have only one node equation for node at point E with a voltage v_o:

$$\frac{v_o - v_i}{r_\pi} + \frac{v_o - 0}{r_o} - \beta \Delta i_B + \frac{v_o - 0}{R_E} = 0$$

Because of the controlled source, we need to write an "auxiliary" equation relating the control current (Δi_B) to node voltages:

$$\Delta i_B = \frac{v_i - v_o}{r_\pi}$$

Substituting the expression for Δi_B in our node equation, multiplying both sides by r_π, and collecting terms, we get:

$$v_i(1+\beta) = v_o \left[1 + \beta + r_\pi \left(\frac{1}{r_o} + \frac{1}{R_E} \right) \right] = v_o \left[1 + \beta + \frac{r_\pi}{r_o \parallel R_E} \right]$$

Amplifier Gain can now be directly calculated:

$$A_v \equiv \frac{v_o}{v_i} = \frac{1}{1 + \dfrac{r_\pi}{(1+\beta)(r_o \parallel R_E)}}$$

Unless R_E is very small (tens of Ω), the fraction in the denominator is quite small compared to 1 and $A_v \approx 1$.

To find the input impedance, we calculate i_i by KCL:

$$i_i = i_1 + \Delta i_B = \frac{v_i}{R_B} + \frac{v_i - v_o}{r_\pi}$$

Since $v_o \approx v_i$, we have $i_i = v_i/R_B$ or

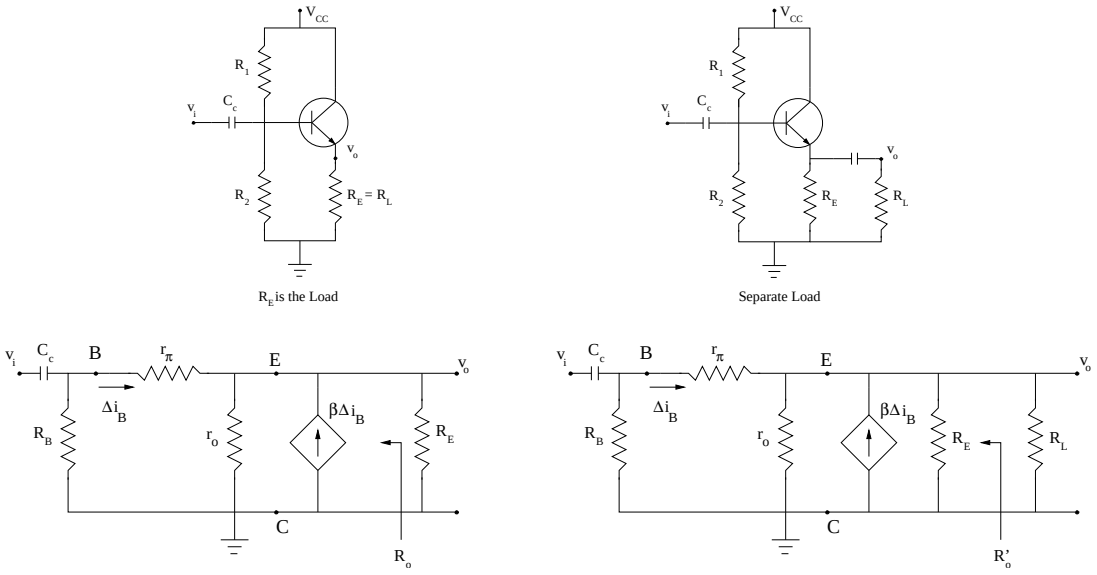
$$R_i \equiv \frac{v_i}{i_i} = R_B$$

Note that R_B is the combination of our biasing resistors R_1 and R_2. With alternative biasing schemes which do not require R_1 and R_2, (and, therefore $R_B \to \infty$), the input resistance of the emitter follower circuit will become large. In this case, we cannot use $v_o \approx v_i$. Using the full expression for v_o from above, the input resistance of the emitter follower circuit becomes:

$$R_i \equiv \frac{v_i}{i_i} = R_B \parallel [r_\pi + (R_E \parallel r_o)(1+\beta)]$$

and it is quite large (hundreds of kΩ to several MΩ) for $R_B \to \infty$. Such a circuit is in fact the first stage of the 741 OpAmp.

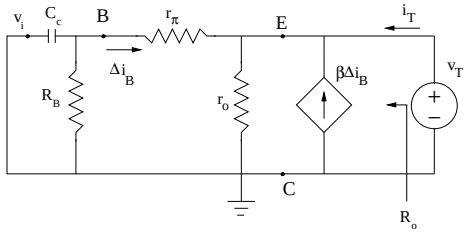
The output resistance of the common collector amplifier (in fact for all transistor amplifiers) is somewhat complicated because the load can be configured in two ways (see figure): First, R_E, itself, is the load. This is the case when the common collector is used as a "current amplifier" to raise the power level and to drive the load. The output resistance of the circuit is R_o as is shown in the circuit model. This is usually the case when values of R_o and A_i (current gain) is quoted in electronic text books.



Alternatively, the load can be placed in parallel to R_E. This is done when the common collector amplifier is used as a buffer ($A_v \approx 1$, R_i large). In this case, the output resistance is denoted by R'_o (see figure). For this circuit, BJT sees a resistance of $R_E \parallel R_L$. Obviously, if we want the load not to affect the emitter follower circuit, we should use R_L to be much

larger than R_E. In this case, little current flows in R_L which is fine because we are using this configuration as a buffer and not to amplify the current and power. As such, value of R_o' or A_i does not have much use.

When R_E is the load, the output resistance can be found by killing the source (short v_i) and finding the Thevenin resistance of the two-terminal network (using a test voltage source).



$$\text{KCL:} \qquad i_T = -\Delta i_B + \frac{v_T}{r_o} - \beta \Delta i_B$$

$$\text{KVL (outside loop):} \qquad -r_\pi \Delta i_B = v_T$$

Substituting for Δi_B from the 2nd equation in the first and rearranging terms we get:

$$R_o \equiv \frac{v_T}{i_T} = \frac{(r_o)\, r_\pi}{(1+\beta)(r_o) + r_\pi} \approx \frac{(r_o)\, r_\pi}{(1+\beta)(r_o)} = \frac{r_\pi}{(1+\beta)} \approx \frac{r_\pi}{\beta} = r_e$$

where we have used the fact that $(1+\beta)(r_o) \gg r_\pi$.

When R_E is the load, the current gain in this amplifier can be calculated by noting $i_o = v_o/R_E$ and $i_i \approx v_i/R_B$ as found above:

$$A_i \equiv \frac{i_o}{i_i} = \frac{R_B}{R_E}$$

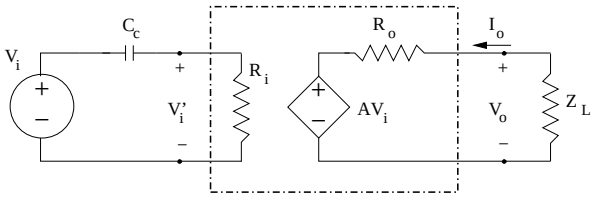
In summary, the general properties of the common collector amplifier (emitter follower) include a voltage gain of unity ($A_v \approx 1$), a very large input resistance $R_i \approx R_B$ (and can be made much larger with alternate biasing schemes). This circuit can be used as buffer for matching impedance, at the first stage of an amplifier to provide very large input resistance (such in 741 OpAmp). As a buffer, we need to ensure that $R_L \gg R_E$. The common collector amplifier can be also used as the last stage of some amplifier system to amplify the current (and thus, power) and drive a load. In this case, R_E is the load, R_o is small: $R_o = r_e$ and current gain can be substantial: $A_i = R_B/R_E$.

Impact of Coupling Capacitor:

Up to now, we have neglected the impact of the coupling capacitor in the circuit (assumed it was a short circuit). This is not a correct assumption at low frequencies. The coupling capacitor results in a lower cut-off frequency for the transistor amplifiers. In order to find the cut-off frequency, we need to repeat the above analysis and include the coupling capacitor

impedance in the calculation. In most cases, however, the impact of the coupling capacitor and the lower cut-off frequency can be deduced be examining the amplifier circuit model.

Consider our general model for any amplifier circuit. If we assume that coupling capacitor is short circuit (similar to our AC analysis of BJT amplifier), $v_i' = v_i$.



Voltage Amplifier Model

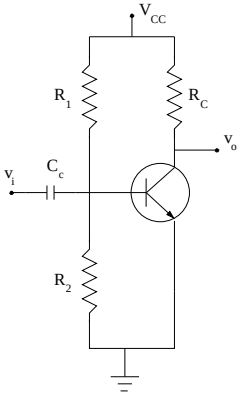
When we account for impedance of the capacitor, we have set up a high pass filter in the input part of the circuit (combination of the coupling capacitor and the input resistance of the amplifier). This combination introduces a lower cut-off frequency for our amplifier which is the same as the cut-off frequency of the high-pass filter:

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c}$$

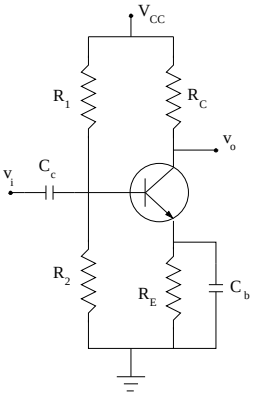
Lastly, our small signal model is a low-frequency model. As such, our analysis indicates that the amplifier has no upper cut-off frequency (which is not true). At high frequencies, the capacitance between BE , BC, CE layers become important and a high-frequency small-signal model for BJT should be used for analysis. You will see these models in upper division courses. Basically, these capacitances results in amplifier gain to drop at high frequencies. PSpice includes a high-frequency model for BJT, so your simulation should show the upper cut-off frequency for BJT amplifiers.

Common Emitter Amplifier

DC analysis: Recall that an emitter resistor is necessary to provide stability of the bias point. As such, the circuit configuration as is shown has as a poor bias. We need to include R_E for good biasing (DC signals) and eliminate it for AC signals. The solution to include an emitter resistance and use a "bypass" capacitor to short it out for AC signals as is shown.



Poor Bias



Good Bias using a by−pass capacitor

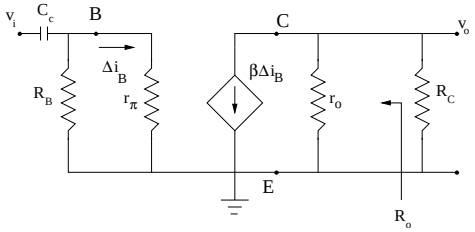
For this new circuit and with the capacitors open circuit, this circuit is the same as our good biasing circuit of page 78. The bias point currents and voltages can be found using procedure of pages 78-81.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. We see that emitter is now common between input and output AC signals (thus, common emitter amplifier. Analysis of this circuit is straightforward. Examination of the circuit shows that:

$$v_i = r_\pi \Delta i_B \qquad v_o = -(R_c \parallel r_o)\,\beta \Delta i_B$$

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\beta}{r_\pi}(R_c \parallel r_o) \approx -\frac{\beta}{r_\pi} R_c = -\frac{R_c}{r_e}$$

$$R_i = R_B \parallel r_\pi \qquad R_o = r_o$$



The negative sign in A_v indicates 180° phase shift between input and output. The circuit has a large voltage gain but has medium value for input resistance.

As with the emitter follower circuit, the load can be configured in two ways: 1) R_c is the load. Then $R_o = r_o$ and the circuit has a reasonable current gain. 2) Load is placed in parallel to R_c. In this case, we need to ensure that $R_L \gg R_c$. Little current will flow in R_L and R_o and A_i values are of not much use.

Lower cut-off frequency: Both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier, both act as a low-pass filter with:

$$\omega_l(coupling) = 2\pi\, f_l = \frac{1}{R_i C_c}$$

$$\omega_l(bypass) = 2\pi\, f_l = \frac{1}{R'_E C_b}$$

$$\text{where} \quad R'_E \equiv R_E \parallel (r_e + \frac{R_B}{\beta})$$

In the case when these two frequencies are far apart, the cut-off frequency of the amplifier is set by the "larger" cut-off frequency. *i.e.,*

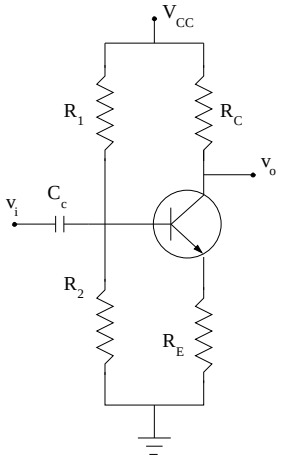
$$\omega_l(bypass) \ll \omega_l(coupling) \quad \rightarrow \quad \omega_l = 2\pi\, f_l = \frac{1}{R_i C_c}$$

$$\omega_l(coupling) \ll \omega_l(bypass) \quad \rightarrow \quad \omega_l = 2\pi\, f_l = \frac{1}{R'_E C_b}$$

When the two frequencies are close to each other, there is no exact analytical formulas, the cut-off frequency should be found from simulations. An approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

Common Emitter Amplifier with Emitter resistance



A problem with the common emitter amplifier is that its gain depend on BJT parameters $A_v \approx (\beta/r_\pi)R_c$. Some form of feedback is necessary to ensure stable gain for this amplifier. One way to achieve this is to add an emitter resistance. Recall impact of negative feedback on OpAmp circuits: we traded gain for stability of the output. Same principles apply here.

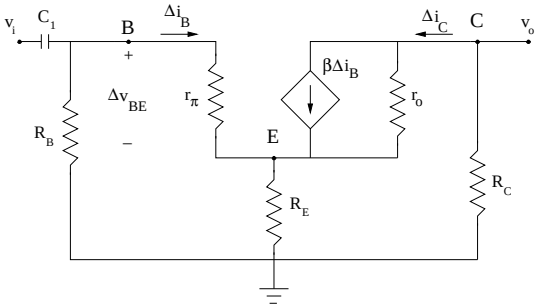
DC analysis: With the capacitors open circuit, this circuit is the same as our good biasing circuit of page 78. The bias point currents and voltages can be found using procedure of pages 78-81.

AC analysis: To start the analysis, we kill all DC sources, combine R_1 and R_2 into R_B and replace the BJT with its small signal model. Analysis is straight forward using node-voltage method.

$$\frac{v_E - v_i}{r_\pi} + \frac{v_E}{R_E} - \beta\Delta i_B + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} + \beta\Delta i_B = 0$$

$$\Delta i_B = \frac{v_i - v_E}{r_\pi} \quad \text{(Controlled source aux. Eq.)}$$



Substituting for Δi_B in the node equations and noting $1 + \beta \approx \beta$, we get:

$$\frac{v_E}{R_E} + \beta\frac{v_E - v_i}{r_\pi} + \frac{v_E - v_o}{r_o} = 0$$

$$\frac{v_o}{R_C} + \frac{v_o - v_E}{r_o} - \beta\frac{v_E - v_i}{r_\pi} = 0$$

Above are two equations in two unknowns (v_E and v_o). Adding the two equation together we get $v_E = -(R_E/R_C)v_o$ and substituting that in either equations we can find v_o.

Alternatively, we can find compact and simple solutions by noting that terms containing r_o in the denominator are usually small as r_o is quite large. In this case, the node equations simplify to (using $r_\pi/\beta = r_e$):

$$v_E\left(\frac{1}{R_E} + \frac{1}{r_e}\right) = \frac{v_i}{r_e} \quad \rightarrow \quad v_E = \frac{R_E}{R_E + r_e}\, v_i$$

$$v_o = \frac{R_C}{r_e}\,(v_E - v_i) = \frac{R_C}{r_e}\,\left(\frac{R_E}{R_E + r_e} - 1\right) v_i = -\frac{R_C}{R_E + r_e}\, v_i$$

Then, the voltage gain and input and output resistance can also be easily calculated:

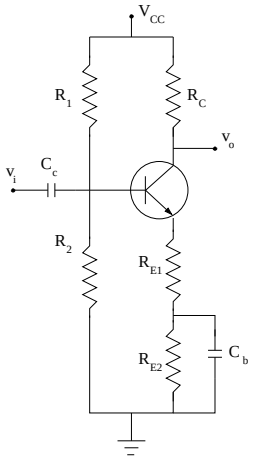
$$A_v = \frac{v_o}{v_i} = -\frac{R_C}{R_E + r_e} \approx -\frac{R_C}{R_E}$$
$$R_i = R_B \parallel [\beta(R_E + r_e)] \qquad R_o = r_e$$

As before the minus sign in A_v indicates a 180° phase shift between input and output signals. Note the impact of negative feedback introduced by the emitter resistance. The voltage gain is independent of BJT parameters and is set by R_C and R_E as $R_E \gg r_e$ (recall OpAmp inverting amplifier!). The input resistance is increased dramatically.

Lower cut-off frequency: The coupling capacitor together with the input resistance of the amplifer lead to a lower cut-off freqnecy for this amplifer (similar to emitter follower). The lower cut-off freqncy is geivn by:

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c}$$

A Possible Biasing Problem: The gain of the common emitter amplifier with the emitter resistance is approximately R_C/R_E. For cases when a high gain (gains larger than 5-10) is needed, R_E may be become so small that the necessary good biasing condition, $V_E = R_E I_E > 1$ V cannot be fulfilled. The solution is to use a by-pass capacitor as is shown. The AC signal sees an emitter resistance of R_{E1} while for DC signal the emitter resistance is the larger value of $R_E = R_{E1} + R_{E2}$. Obviously formulas for common emitter amplifier with emitter resistance can be applied here by replacing R_E with R_{E1} as in deriving the amplifier gain, and input and output impedances, we "short" the bypass capacitor so R_{E2} is effectively removed from the circuit.

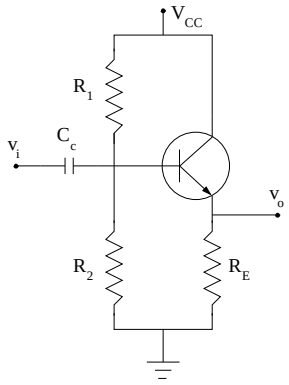


The addition of by-pass capacitor, however, modify the lower cut-off frequency of the circuit. Similar to a regular common emitter amplifier with no emitter resistance, both the coupling and bypass capacitors contribute to setting the lower cut-off frequency for this amplifier. Similarly we find that an approximate formula for the cut-off frequency (accurate within a factor of two and exact at the limits) is:

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$
$$\text{where} \quad R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta})$$

Summary of BJT Amplifiers

Common Collector (Emitter Follower):



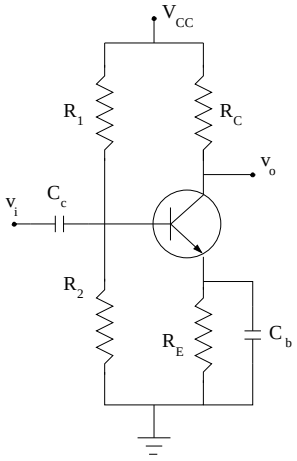
$$A_v = \frac{(R_E \parallel r_o)(1+\beta)}{r_\pi + (R_E \parallel r_o)(1+\beta)} \approx 1$$

$$R_i = R_B \parallel [r_\pi + (R_E \parallel r_o)(1+\beta)] \approx R_B$$

$$R_o = \frac{(r_o)\, r_\pi}{(1+\beta)(r_o) + r_\pi} \approx \frac{r_\pi}{\beta} = r_e$$

$$2\pi\, f_l = \frac{1}{R_i C_c}$$

Common Emitter:



$$A_v = -\frac{\beta}{r_\pi}(R_c \parallel r_o) \approx -\frac{\beta}{r_\pi} R_c = -\frac{R_c}{r_e}$$

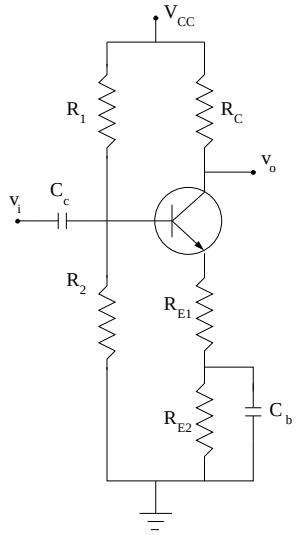
$$R_i = R_B \parallel r_\pi$$

$$R_o = r_o$$

$$2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

$$\text{where} \quad R'_E \equiv R_E \parallel (r_e + \frac{R_B}{\beta})$$

Common Emitter with Emitter Resistance:



$$A_v = -\frac{R_C}{R_{E1} + r_e} \approx -\frac{R_C}{R_{E1}}$$

$$R_i = R_B \parallel [\beta(R_{E1} + r_e)]$$

$$R_o = r_e$$

If R_{E2} and bypass capacitors are <u>not</u> present, replace R_{E1} with R_E in above formula and

$$2\pi\, f_l = \frac{1}{R_i C_c}$$

If R_{E2} and bypass capacitor are present,

$$\omega_l = 2\pi\, f_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b}$$

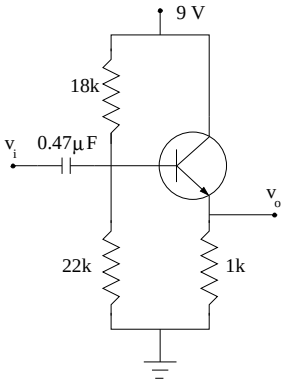
$$\text{where} \quad R'_E \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta})$$

Examples of Analysis and Design of BJT Amplifiers

Example 1: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad \beta = h_{fe} = 200 \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$

DC analysis:



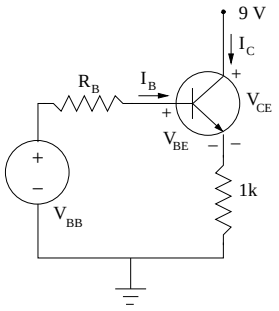
Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters):

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}\Omega$$

$$V_{BB} = \frac{22}{18+22} 9 = 4.95 \text{ V}$$

KVL: $V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{2.1} + 10^3 \right)$$



$$I_E = 4 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 20 \ \mu\text{A}$$

KVL: $V_{CC} = V_{CE} + 10^3 I_E$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$

DC Bias summary: $I_E \approx I_C = 4$ mA, $\quad I_B = 20$ μA, $\quad V_{CE} = 5$ V

AC analysis: The circuit is a common collector amplifier. Using the formulas in page 98,

$$A_v \approx 1$$

$$R_i \approx R_B = 9.9 \ k\Omega$$

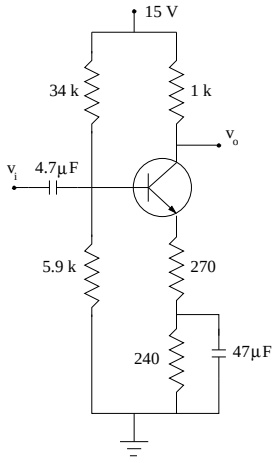
$$R_o \approx r_e = 25 \ \Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_B C_c} = \frac{1}{2\pi \times 9.9 \times 10^3 \times 0.47 \times 10^{-6}} = 36 \text{ Hz}$$

Example 2: Find the bias point and AC amplifier parameters of this circuit (Manufacturers' spec sheets give: $h_{fe} = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad \beta = h_{fe} = 200 \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$

DC analysis:



Replace R_1 and R_2 with their Thevenin equivalent and proceed with DC analysis (all DC current and voltages are denoted by capital letters). Since all capacitors are replaced with open circuit, the emitter resistance for DC analysis is $270+240 = 510$ Ω.

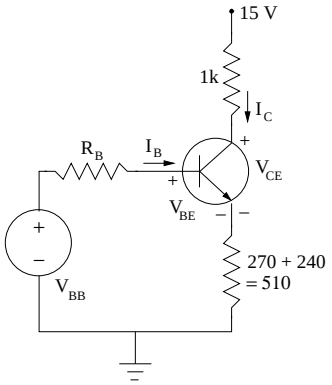
$$R_B = 5.9 \text{ k} \parallel 34 \text{ k} = 5.0 \text{ k}\Omega$$

$$V_{BB} = \frac{5.9}{5.9 + 34} 15 = 2.22 \text{ V}$$

KVL: $V_{BB} = R_B I_B + V_{BE} + 510 I_E \qquad I_B = \dfrac{I_E}{1+\beta} = \dfrac{I_E}{201}$

$$2.22 - 0.7 = I_E \left(\frac{5.0 \times 10^3}{2.1} + 510 \right)$$

$$I_E = 3 \text{ mA} \approx I_C, \qquad I_B = \frac{I_C}{\beta} = 15 \ \mu\text{A}$$



KVL: $V_{CC} = 1000 I_C + V_{CE} + 510 I_E$

$$V_{CE} = 15 - 1,510 \times 3 \times 10^{-3} = 10.5 \text{ V}$$

DC Bias: $I_E \approx I_C = 3$ mA, $\quad I_B = 15$ μA, $\quad V_{CE} = 10.5$ V

AC analysis: The circuit is a common collector amplifier with an emitter resistance. Note that the 240 Ω resistor is shorted out with the by-pass capacitor. It only enters the formula for the lower cut-off frequency. Using the formulas in page 98:

$$A_v = \frac{R_C}{R_{E1} + r_e} = \frac{1,000}{270 + 25} = 3.39$$

$$R_i \approx R_B = 5.0 \text{ k}\Omega \qquad\qquad R_o \approx r_e = 25 \ \Omega$$

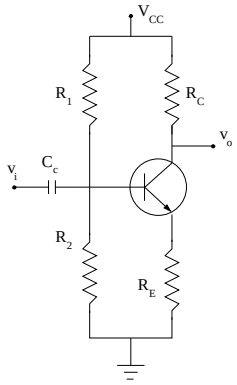
$$R'_E = \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta}) = 240 \parallel (270 + 25 + \frac{5,000}{200}) = 137 \ \Omega$$

$$f_l = \frac{\omega_l}{2\pi} = \frac{1}{2\pi R_i C_c} + \frac{1}{2\pi R'_E C_b} =$$

$$\frac{1}{2\pi \times 5,000 \times 4.7 \times 10^{-6}} + \frac{1}{2\pi \times 137 \times 47 \times 10^{-6}} = 31.5 \text{ Hz}$$

Example 3: Design a BJT amplifier with a gain of 4 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3$ mA and $V_{CE} = 7.5$ V. (Manufacturers' spec sheets give: $\beta_{min} = 100$, $\beta = 200$, $h_{ie} = 5$ kΩ, $h_{oe} = 10$ μS).

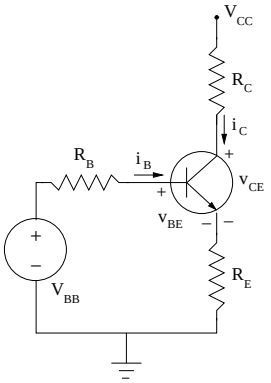
$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$



The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 98 ($r_e = r_\pi / h_{fe} = 25\ \Omega$),

$$|A_v| = \frac{R_C}{R_E + r_e} \approx \frac{R_C}{R_E} = 4$$

The lower cut-off frequency will set the value of C_c.



We start with the DC bias: As V_{CC} is not given, we need to choose it. To set the Q-point in the middle of load line, set $V_{CC} = 2V_{CE} = 15$ V. Then, noting $I_C \approx I_E$,:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$
$$15 - 7.5 = 3 \times 10^{-3}(R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$

Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier, $A_V = 4$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 4 \quad \rightarrow \quad 4R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 500 \ \Omega, R_C = 2. \text{ k}\Omega$$

Commercial values are $R_E = 510\ \Omega$ and $R_C = 2$ kΩ. Use these commercial values for the rest of analysis.

We need to check if $V_E > 1$ V, the condition for good biasing. $V_E = R_E I_E = 510 \times 3 \times 10^{-3} = 1.5 > 1$, it is OK (See next example for the case when V_E is smaller than 1 V).

We now proceed to find R_B and V_{BB}. R_B is found from good bias condition and V_{BB} from a KVL in BE loop:

$$R_B \ll (\beta + 1)R_E \quad \rightarrow \quad R_B = 0.1(\beta_{min} + 1)R_E = 0.1 \times 101 \times 510 = 5.1 \text{ k}\Omega$$
$$\text{KVL:} \quad V_{BB} = R_B I_B + V_{BE} + R_E I_E$$
$$V_{BB} = 5.1 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 510 \times 3 \times 10^{-3} = 2.28 \text{ V}$$

Bias resistors R_1 and R_2 are now found from R_B and V_{BB}:

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 5 \text{ k}\Omega$$
$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{2.28}{15} = 0.152$$

R_1 can be found by dividing the two equations: $R_1 = 33$ kΩ. R_2 is found from the equation for V_{BB} to be $R_2 = 5.9$ kΩ. Commercial values are $R_1 = 33$ kΩ and $R_2 = 6.2$ kΩ.

Lastly, we have to find the value of the coupling capacitor:

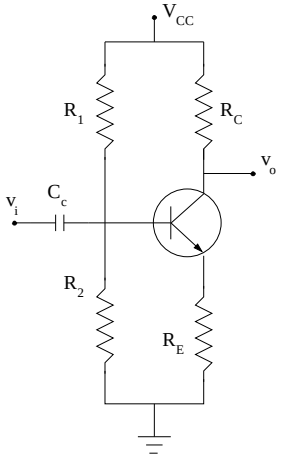
$$\omega_l = \frac{1}{R_i C_c} = 2\pi \times 100$$

Using $R_i \approx R_B = 5.1$ kΩ, we find $C_c = 3 \times 10^{-7}$ F or a commercial values of $C_c = 300$ nF.

So, are design values are: $R_1 = 33$ kΩ, $R_2 = 6.2$ kΩ, $R_E = 510$ Ω, $R_C = 2$ kΩ. and $C_c = 300$ nF.

Example 4: Design a BJT amplifier with a gain of 10 and a lower cut-off frequency of 100 Hz. The Q point parameters should be $I_C = 3$ mA and $V_{CE} = 7.5$ V. A power supply of 15 V is available. Manufacturers' spec sheets give: $\beta_{min} = 100$, $h_{fe} = 200$, $r_\pi = 5$ kΩ, $h_{oe} = 10$ μS.

$$r_\pi = h_{ie} = 5 \text{ k}\Omega \qquad r_o = \frac{1}{h_{oe}} = 100 \text{ k}\Omega \qquad r_e = \frac{r_\pi}{\beta} = 25 \ \Omega$$



The prototype of this circuit is a common emitter amplifier with an emitter resistance. Using formulas of page 98:

$$|A_v| = \frac{R_C}{R_E + r_e} \approx \frac{R_C}{R_E} = 10$$

The lower cut-off frequency will set the value of C_c.

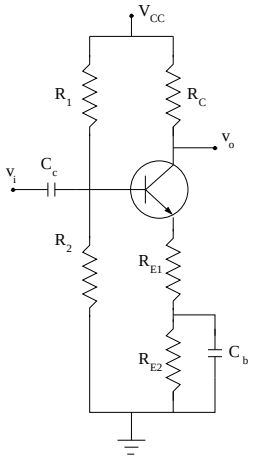
We start with the DC bias: As the power supply voltage is given, we set $V_{CC} = 15$ V. Then, noting $I_C \approx I_E$,:

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$
$$15 - 7.5 = 3 \times 10^{-3}(R_C + R_E) \quad \rightarrow \quad R_C + R_E = 2.5 \text{ k}\Omega$$

Values of R_C and R_E can be found from the above equation together with the AC gain of the amplifier $A_V = 10$. Ignoring r_e compared to R_E (usually a good approximation), we get:

$$\frac{R_C}{R_E} = 10 \quad \rightarrow \quad 10R_E + R_E = 2.5 \text{ k}\Omega \quad \rightarrow \quad R_E = 227\ \Omega, R_C = 2.27 \text{ k}\Omega$$

We need to check if $V_E > 1$ V which is the condition for good biasing: $V_E = R_E I_E = 227 \times 3 \times 10^{-3} = 0.69 < 1$. Therefore, we need to use a bypass capacitor and modify our circuits as is shown.



For DC analysis, the emitter resistance is $R_{E1} + R_{E2}$ while for AC analysis, the emitter resistance will be R_{E1}. Therefore:

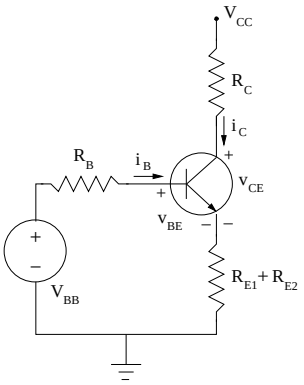
$$\text{DC Bias:} \quad R_C + R_{E1} + R_{E2} = 2.5 \text{ k}\Omega$$

$$\text{AC gain:} \quad A_v = \frac{R_C}{R_{E1}} = 10$$

Above are two equations in three unknowns. A third equation is derived by setting $V_E = 1$ V to minimize the value of $R_{E1} + R_{E2}$.

$$V_E = (R_{E1} + R_{E2}) I_E$$

$$R_{E1} + R_{E2} = \frac{1}{3 \times 10^{-3}} = 333$$



Now, solving for R_C, R_{E1}, and R_{E2}, we find $R_C = 2.2$ kΩ, $R_{E1} = 220\ \Omega$, and $R_{E2} = 110\ \Omega$ (All commercial values).

We can now proceed to find R_B and V_{BB}:

$$R_B \ll (\beta + 1)(R_{E1} + R_{E2})$$

$$R_B = 0.1(\beta_{min} + 1)(R_{E1} + R_{E2}) = 0.1 \times 101 \times 330 = 3.3 \text{ k}\Omega$$

$$\text{KVL:} \quad V_{BB} = R_B I_B + V_{BE} + R_E I_E$$

$$V_{BB} = 3.3 \times 10^3 \frac{3 \times 10^{-3}}{201} + 0.7 + 330 \times 3 \times 10^{-3} = 1.7 \text{ V}$$

Bias resistors R_1 and R_2 are now found from R_B and $V_B B$:

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} = 3.3 \text{ k}\Omega$$

$$\frac{V_{BB}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{1}{15} = 0.066$$

R_1 can be found by dividing the two equations: $R_1 = 50$ kΩ and R_2 is found from the equation for V_{BB} to be $R_2 = 3.6$k Ω. Commercial values are $R_1 = 51$ kΩ and $R_2 = 3.6$k Ω

Lastly, we have to find the value of the coupling and bypass capacitors:

$$R'_E = \equiv R_{E2} \parallel (R_{E1} + r_e + \frac{R_B}{\beta}) = 110 \parallel (220 + 25 + \frac{3,300}{200}) = 77.5\ \Omega$$
$$R_i \approx R_B = 3.3\ \text{k}\Omega$$
$$\omega_l = \frac{1}{R_i C_c} + \frac{1}{R'_E C_b} = 2\pi \times 100$$

This is one equation in two unknown (C_c and C_B) so one can be chosen freely. Typically $C_b \gg C_c$ as $R_i \approx R_B \gg R_E \gg R'_E$. This means that unless we choose C_c to be very small, the cut-off frequency is set by the bypass capacitor. The usual approach is the choose C_b based on the cut-off frequency of the amplifier and choose C_c such that cut-off frequency of the $R_i C_c$ filter is at least a factor of ten lower than that of the bypass capacitor. Note that in this case, our formula for the cut-off frequency is quite accurate (see discussion in page 95) and is

$$\omega_l \approx \frac{1}{R'_E C_b} = 2\pi \times 100$$

This gives $C_b = 20\ \mu$F. Then, setting

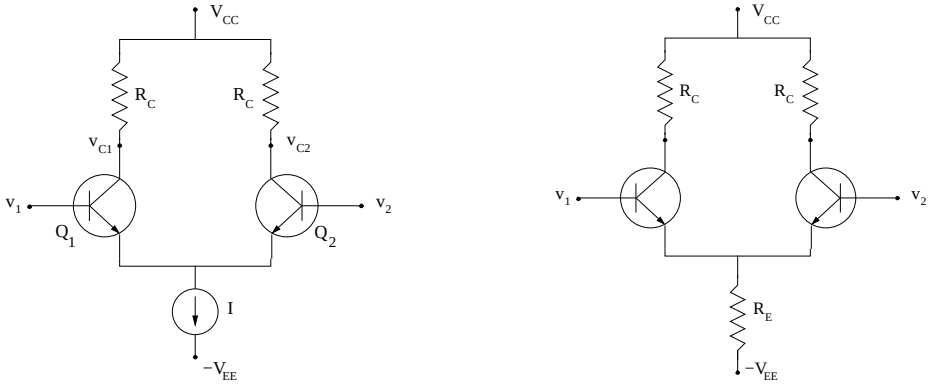
$$\frac{1}{R_i C_c} \ll \frac{1}{R'_E C_b}$$
$$\frac{1}{R_i C_c} = 0.1 \frac{1}{R'_E C_b}$$
$$R_i C_c = 10 R'_E C_b \quad \rightarrow \quad C_c = 4.7^{-6} = 4.7\ \mu\text{F}$$

So, are design values are: $R_1 = 50$ kΩ, $R_2 = 3.6$ kΩ, $R_{E1} = 220\ \Omega$, $R_{E2} = 110\ \Omega$, $R_C = 2.2$ kΩ, $C_b = 20\ \mu$F, and $C_c = 4.7\ \mu$F.

An alternative approach is to choose C_b (or C_c) and compute the value of the other from the formula for the cut-off frequency. For example, if we choose $C_b = 47\ \mu$F, we find $C_c = 0.86\ \mu$F.

BJT Differential Pairs: Emitter-Coupled Logic and Difference Amplifiers

The differential pairs are the most widely used circuit building block in analog ICs. They are made from both BJT and variant of Field-effect transistors (FET). In addition, BJT differential pairs are the basis for the very-high-speed logic circuit family called Emitter-Coupled Logic (ECL).



The circuit above (on the left) shows the basic BJT differential-pair configuration. It consists of two matched BJTs with emitters coupled together. On ICs, the differential pairs are typically biased by a current source as is shown (using a variant of current mirror circuit). The differential pair can be also biased by using an emitter resistor as is shown on the circuit above right. This variant is typically used when simple circuits are built from individual components (it is not very often utilized in modern circuits). Here we focus on the differential pairs that are biased with a current source.

The circuit has two inputs, v_1 and v_2 and the output signals can be extracted from the collector of both BJTs (v_{C1} and v_{C2}). Inspection of the circuit reveal certain properties. By KCL we find that $i_{C1} + i_{C2} \approx i_{E1} + i_{E2} = I$. That is the two BJTs share the current I between them. So, in general, $i_{C1} \approx i_{E1} \leq I$ and $i_{C2} \approx i_{E2} \leq I$. It is clear that at least one of the BJT pair should be ON (*i.e.,* not in cut-off) in order to satisfy the above equation (both i_{E1} and i_{E2} cannot be zero). Value of R_C is chosen such that either BJT will be in active-linear if its collector current reaches its maximum value of I.

$$V_{CC} = R_C i_{C1} + v_{CE1} + V_{ICS} - V_{EE}$$

$$v_{CE1} = V_{CC} + V_{EE} + V_{ICS} - R_C i_{C1} > v_\gamma$$

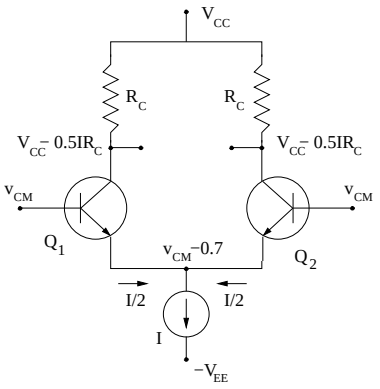
$$R_C < \frac{V_{CC} + V_{EE} + V_{ICS} - V_\gamma}{I} < \frac{V_{CC} + V_{EE} - V_\gamma}{I}$$

With this choice for R_C, both BJTs will either be in cut-off or active-linear (and never in saturation).

Lastly, if we write a KVL through a loop that contains the input voltage sources and both base-emitter junctions, we will have:

KVL: $\quad -v_1 + v_{BE1} - v_{BE2} + v_2 = 0 \quad \rightarrow \quad v_{BE1} - v_{BE2} = v_1 - v_2$

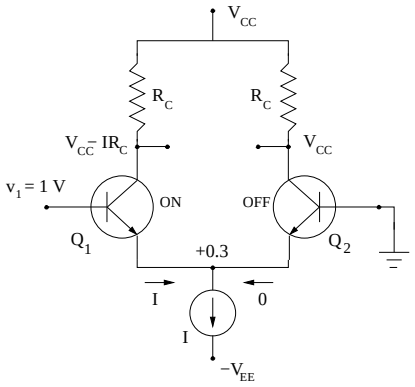
To understand the behavior of the circuit, let's assume that a common voltage of v_{CM} is applied to both inputs: $v_1 = v_2 = v_{CM}$ (CM stands for Common Mode). Then, $v_{BE1} - v_{BE2} = v_1 - v_2 = 0$ or $v_{BE1} = v_{BE2}$. Because identical BJTs are biased with same v_{BE}, we should have $i_{E1} = i_{E2}$ and current I is divided equally between the pair:



KCL: $\quad i_{C1} \approx i_{E1} = 0.5I \quad$ and $\quad i_{C2} \approx i_{E2} = 0.5I.$

As such, both BJTs will be in active linear, $v_{BE1} = v_{BE2} = 0.7$ V and the output voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$ will appear at both collectors.

Now, let's assume $v_1 = 1$ V and $v_2 = 0$. Writing KVL on a loop that contains both input voltage sources, we get:



KVL: $\quad v_{BE1} - v_{BE2} = v_1 - v_2 = 1$ V

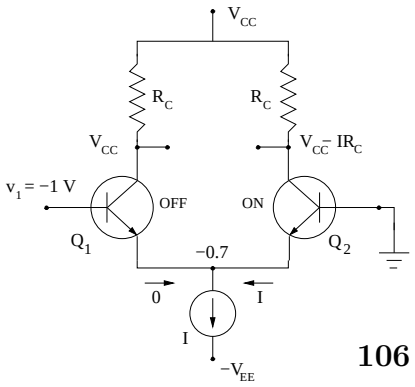
Because $v_{BE} \leq v_\gamma = 0.7$ V, the only way that the above equation can be satisfied is for v_{BE2} to be negative: Q_2 is in cut-off and $i_{E2} = 0$. Because of the current sharing properties, Q_1 should be on and carry current I. Thus:

$$v_{BE1} = 0.7 \text{ V}, \quad v_{BE2} = v_{BE1} - 1 = -0.3 \text{ V}$$

$$i_{C1} = i_{E1} = I, \quad i_{C2} = i_{E2} = 0$$

And voltages of $v_{C1} = V_{CC} - IR_C$ and $v_{C2} = V_{CC}$ will develop at the collectors of the BJT pair. One can easily show that for any $v_1 - v_2 > v_\gamma = 0.7$ V, Q_1 will be ON with $i_{C1} = i_{E1} = I$ and $v_{C1} = V_{CC} - IR_C$; and Q_2 will be OFF with $i_{C2} = i_{E2} = 0$ and $v_{C2} = V_{CC}$.

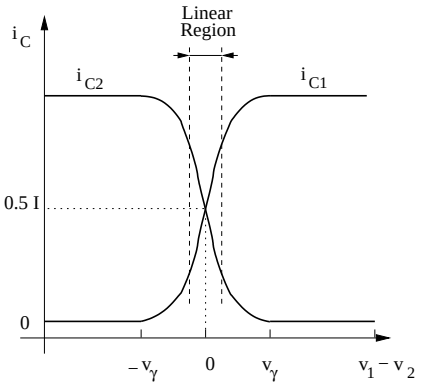
If we now apply $v_1 = -1$ V and $v_2 = 0$, the reverse of the above occurs:



KVL: $\quad v_{BE1} - v_{BE2} = v_1 - v_2 = -1$ V

In this case, Q_2 will be ON and carry current I and Q_1 will be OFF. Again, it is easy to show that this is true for any $v_1 - v_2 < -v_\gamma = -0.7$ V.

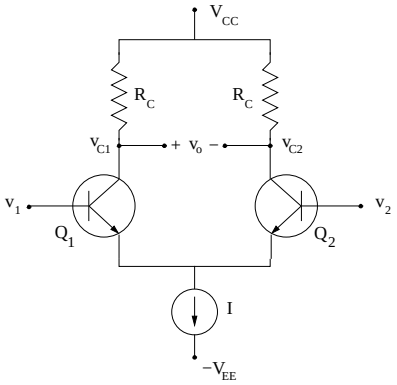
The response of the BJT differential pair to a pair of input signals with $v_d = v_1 - v_2$ is summarized in this graph. When v_d is large, the collector voltages switch from one state v_{CC} to another state $v_{CC} - IR_C$ depending on the sign v_d. As such, the differential pair can be used as a logic gate and a family of logic circuits, emitter-coupled logic, is based on differential pairs. In fact, because a BJT can switch very rapidly between cut-off and active-linear regimes, ECL circuits are the basis for very fast logic circuits today.



For small v_d (typically ≤ 0.2 V), the circuit behaves as a linear amplifier. In this case, the circuit is called a differential amplifier and is the most popular building block of analog ICs.

Differential Amplifiers

The properties of the differential amplifier above (case of v_d small) can be found in a straight-forward manner. The input signals v_1 and v_2 can be written in terms of their difference $v_d = v_1 - v_2$ and their average (common-mode voltage v_{CM}) as:



$$v_{CM} = \frac{v_1 + v_2}{2} \quad \text{and} \quad v_d = v_1 - v_2$$

$$v_1 = v_{CM} + 0.5v_d$$

$$v_2 = v_{CM} - 0.5v_d$$

The response of the circuit can now be found using superposition principle by considering the response to: case 1) $v_1 = v_{CM}$ and $v_2 = v_{CM}$ and case 2) $v_1 = 0.5v_d$ and $v_2 = -0.5v_d$. The response of the circuit to case 1, $v_1 = v_2 = v_{CM}$, was found in page 108. Effectively, v_{CM} sets the bias point for both BJTs with $i_{C1} = i_{E1} = i_{C2} = i_{E2} = 0.5I$, collector voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$, and a difference of zero between to collector voltages, $v_o = v_{C1} - v_{C2} = 0$.

To find the response of the circuit to case 2, $v_1 = 0.5v_d$ and $v_2 = -0.5v_d$, we can use our small signal model (since v_d is small). Examination of the circuit reveals that each of the BJTs form a common emitter amplifier configuration (with no emitter resistor). Using our analysis of common emitter amplifiers ($A_v = R_C/r_e$), we have:

$$v_{c1} = A_v v_i = \frac{R_C}{r_e}(0.5v_d) \quad \text{and} \quad v_{c2} = A_v v_i = \frac{R_C}{r_e}(-0.5v_d)$$

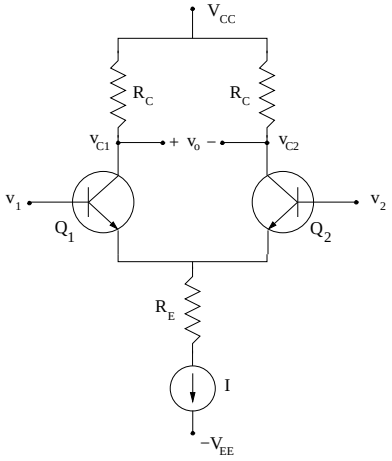
$$v_o = v_{c1} - v_{c2} = \frac{R_C}{r_e} v_d$$

Summing the responses for case 1 and 2, we find that the output voltage of this amplifier is

$$v_o = 0 + \frac{R_C}{r_e}\, v_d = \frac{R_C}{r_e}\, v_d \quad \rightarrow \quad A_v = \frac{R_C}{r_e}$$

similar to a common emitter amplifier. The additional complexity of this circuit compared to our standard common emitter amplifier results in three distinct improvements:
1) This is a "DC" amplifier and does not require a coupling capacitor.
2) Absence of biasing resistors ($R_b \rightarrow \infty$) leads to a higher input resistance, $R_i = r_\pi \parallel R_B = r_\pi$.
3) Elimination of biasing resistors makes it more suitable for IC implementation.

It should be obvious that a differential amplifier configuration can be developed which is similar to a common emitter amplifier with a emitter resistor (to stabilize the gain and increase the input resistance dramatically). Such a circuit is shown. Note that R_E in this circuit is not used to provide stable DC biasing (current source does that). Its function is to provide negative feedback for amplification of small signal, v_d. Following the above procedure, one can show that the gain of this amplifier configuration is:



$$v_o = \frac{R_C}{R_E + r_e}\, v_d \quad \rightarrow \quad A_v = \frac{R_C}{R_E + r_e}$$

As with standard CE amplifer with emitter resistance, the input impdenace is also increased dramatically by negative feedback of R_E (and absence of biasing resistors, $R_b \rightarrow \infty$):

$$R_i = R_B \parallel [\beta(R_{E1} + r_e)] = \beta(R_{E1} + r_e)$$

Module 1

Power Semiconductor Devices

Lesson 6

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Constructional Features, operating principle and characteristics of Power Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

Instructional Objectives

On completion the student will be able to

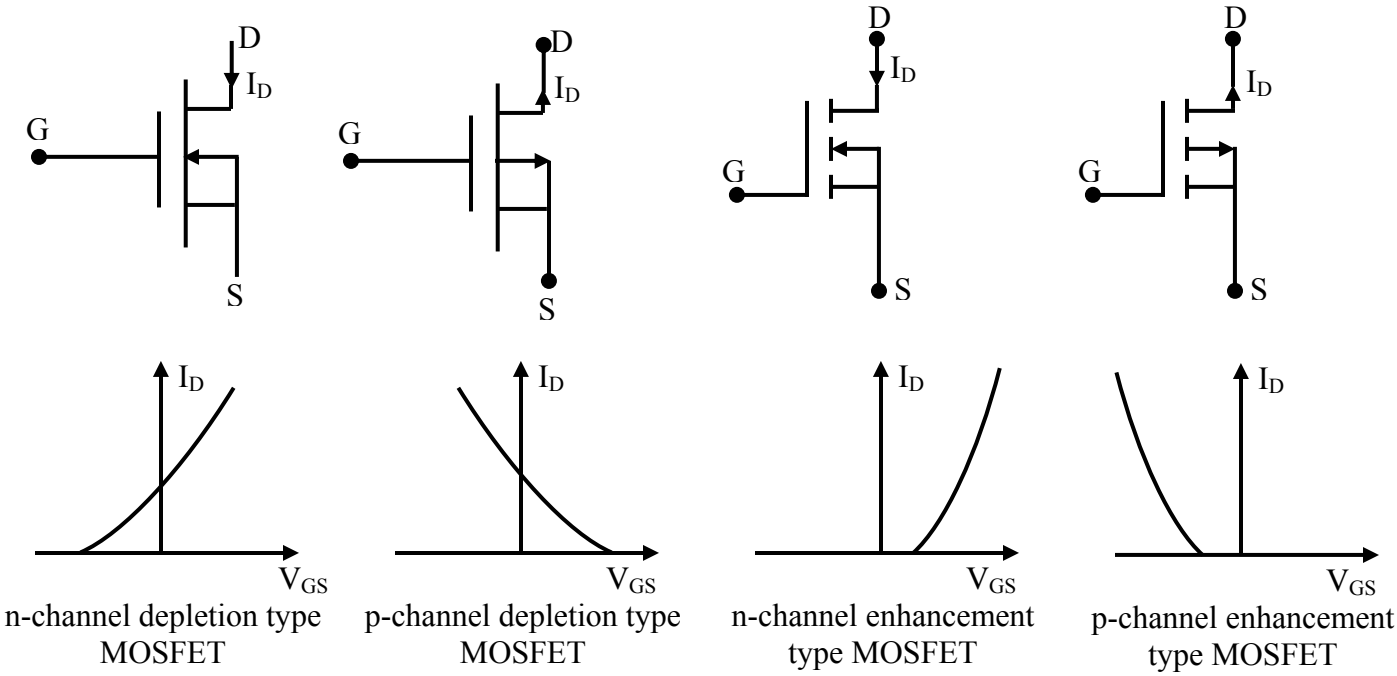
- Differentiate between the conduction mechanism of a MOSFET and a BJT.
- Explain the salient constructional features of a MOSFET.
- Draw the output i-v characteristics of a MOSFET and explain it in terms of the operating principle of the device.
- Explain the difference between the safe operating area of a MOSFET and a BJT.
- Draw the switching characteristics of a MOSFET and explain it.
- Design the gate drive circuit of a MOSFET.
- Interpret the manufacturer's data sheet rating of a MOSFET.

6.1 Introduction

Historically, bipolar semiconductor devices (i.e, diode, transistor, thyristor, thyristor, GTO etc) have been the front runners in the quest for an ideal power electronic switch. Ever since the invention of the transistor, the development of solid-state switches with increased power handling capability has been of interest for expending the application of these devices. The BJT and the GTO thyristor have been developed over the past 30 years to serve the need of the power electronic industry. Their primary advantage over the thyristors have been the superior switching speed and the ability to interrupt the current without reversal of the device voltage. All bipolar devices, however, suffer from a common set of disadvantages, namely, (i) limited switching speed due to considerable redistribution of minority charge carriers associated with every switching operation; (ii) relatively large control power requirement which complicates the control circuit design. Besides, bipolar devices can not be paralleled easily.

The reliance of the power electronics industry upon bipolar devices was challenged by the introduction of a new MOS gate controlled power device technology in the 1980s. The power MOS field effect transistor (MOSFET) evolved from the MOS integrated circuit technology. The new device promised extremely low input power levels and no inherent limitation to the switching speed. Thus, it opened up the possibility of increasing the operating frequency in power electronic systems resulting in reduction in size and weight. The initial claims of infinite current gain for the power MOSFET were, however, diluted by the need to design the gate drive circuit to account for the pulse currents required to charge and discharge the high input capacitance of these devices. At high frequency of operation the required gate drive power becomes substantial. MOSFETs also have comparatively higher on state resistance per unit area of the device cross section which increases with the blocking voltage rating of the device. Consequently, the use of MOSFET has been restricted to low voltage (less than about 500 volts) applications where the ON state resistance reaches acceptable values. Inherently fast switching speed of these devices can be effectively utilized to increase the switching frequency beyond several hundred kHz.

From the point of view of the operating principle a MOSFET is a voltage controlled majority carrier device. As the name suggests, movement of majority carriers in a MOSFET is controlled by the voltage applied on the control electrode (called gate) which is insulated by a thin metal oxide layer from the bulk semiconductor body. The electric field produced by the gate voltage modulate the conductivity of the semiconductor material in the region between the main current carrying terminals called the Drain (D) and the Source (S). Power MOSFETs, just like their integrated circuit counterpart, can be of two types (i) depletion type and (ii) enhancement type. Both of these can be either **n**- channel type or **p**-channel type depending on the nature of the bulk semiconductor. Fig 6.1 (a) shows the circuit symbol of these four types of MOSFETs along with their drain current vs gate-source voltage characteristics (transfer characteristics).



(a)

(b)

Fig 6.1: Different types of power MOSFET.
(a) Circuit symbols and transfer characteristics
(b) Photograph of n-channel enhancement type MOSFET.

From Fig 6.1 (a) it can be concluded that depletion type MOSFETs are normally ON type switches i.e, with the gate terminal open a nonzero drain current can flow in these devices. This is not convenient in many power electronic applications. Therefore, the enhancement type MOSFETs (particularly of the n-channel variety) is more popular for power electronics applications. This is the type of MOSFET which will be discussed in this lesson. Fig 6.1 (b) shows the photograph of some commercially available n-channel enhancement type Power MOSFETs.

6.2 Constructional Features of a Power MOSFET

As mentioned in the introduction section, Power MOSFET is a device that evolved from MOS integrated circuit technology. The first attempts to develop high voltage MOSFETs were by redesigning lateral MOSFET to increase their voltage blocking capacity. The resulting technology was called lateral double deffused MOS (DMOS). However it was soon realized that

much larger breakdown voltage and current ratings could be achieved by resorting to a vertically oriented structure. Since then, vertical DMOS (VDMOS) structure has been adapted by virtually all manufacturers of Power MOSFET. A power MOSFET using VDMOS technology has vertically oriented three layer structure of alternating **p** type and **n** type semiconductors as shown in Fig 6.2 (a) which is the schematic representation of a single MOSFET cell structure. A large number of such cells are connected in parallel (as shown in Fig 6.2 (b)) to form a complete device.

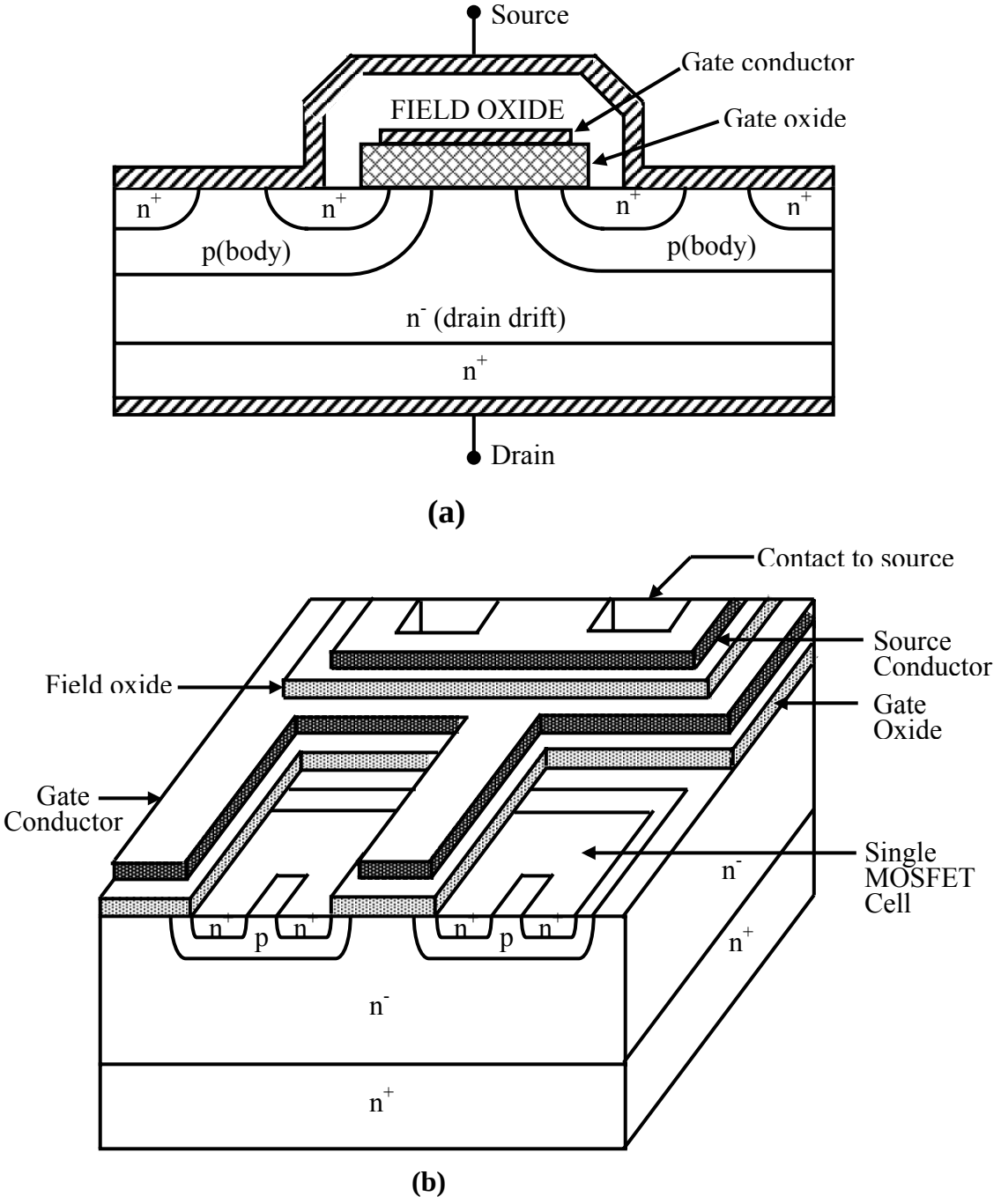


Fig. 6.2: Schematic construction of a power MOSFET
(a) Construction of a single cell.
(b) Arrangement of cells in a device.

The two $\mathbf{n^+}$ end layers labeled "Source" and "Drain" are heavily doped to approximately the same level. The **p** type middle layer is termed the body (or substrate) and has moderate doping level (2 to 3 orders of magnitude lower than $\mathbf{n^+}$ regions on both sides). The $\mathbf{n^-}$ drain drift region has the lowest doping density. Thickness of this region determines the breakdown voltage of the device. The gate terminal is placed over the $\mathbf{n^-}$ and **p** type regions of the cell structure and is insulated from the semiconductor body be a thin layer of silicon dioxide (also called the gate oxide). The source and the drain region of all cells on a wafer are connected to the same metallic contacts to form the Source and the Drain terminals of the complete device. Similarly all gate terminals are also connected together. The source is constructed of many (thousands) small polygon shaped areas that are surrounded by the gate regions. The geometric shape of the source regions, to same extent, influences the ON state resistance of the MOSFET.

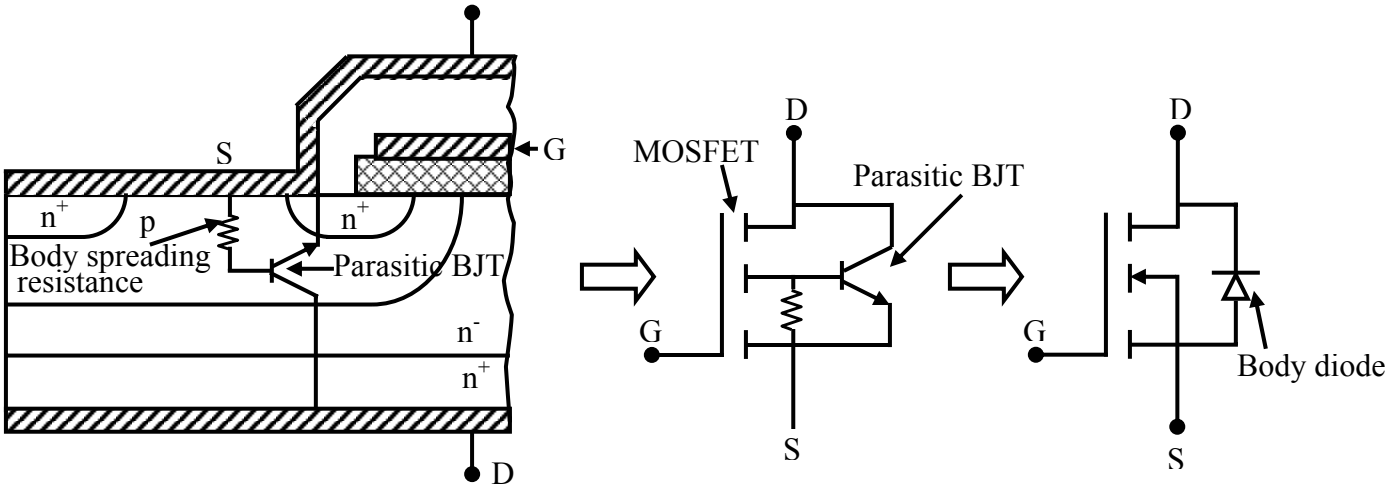


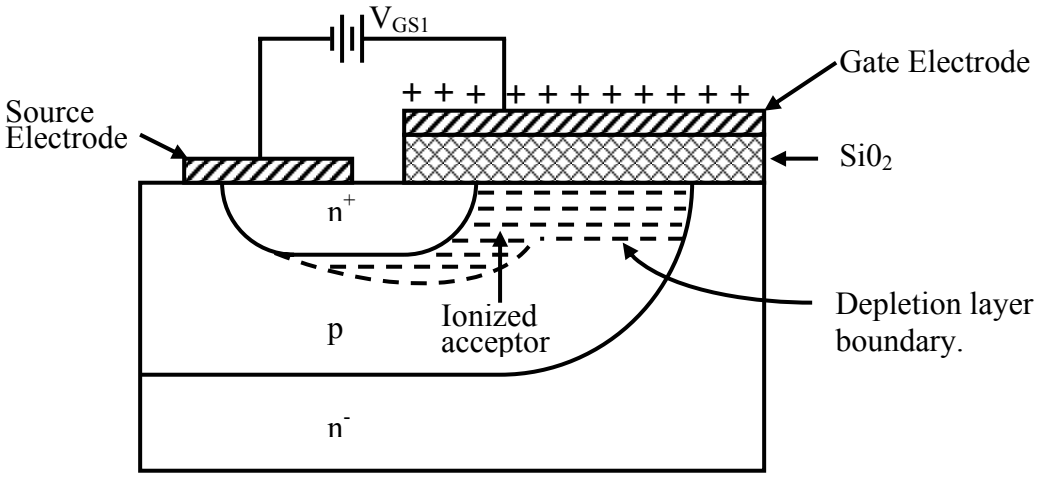
Fig. 6.3: Parasitic BJT in a MOSFET cell.

One interesting feature of the MOSFET cell is that the alternating $\mathbf{n^+}$ $\mathbf{n^-}$ **p** $\mathbf{n^+}$ structure embeds a parasitic BJT (with its base and emitter shorted by the source metallization) into each MOSFET cell as shown in Fig 6.3. The nonzero resistance between the base and the emitter of the parasitic **npn** BJT arises due to the body spreading resistance of the **p** type substrate. In the design of the MOSFET cells special care is taken so that this resistance is minimized and switching operation of the parasitic BJT is suppressed. With an effective short circuit between the body and the source the BJT always remain in cut off and its collector-base junction is represented as an anti parallel diode (called the body diode) in the circuit symbol of a Power MOSFET.

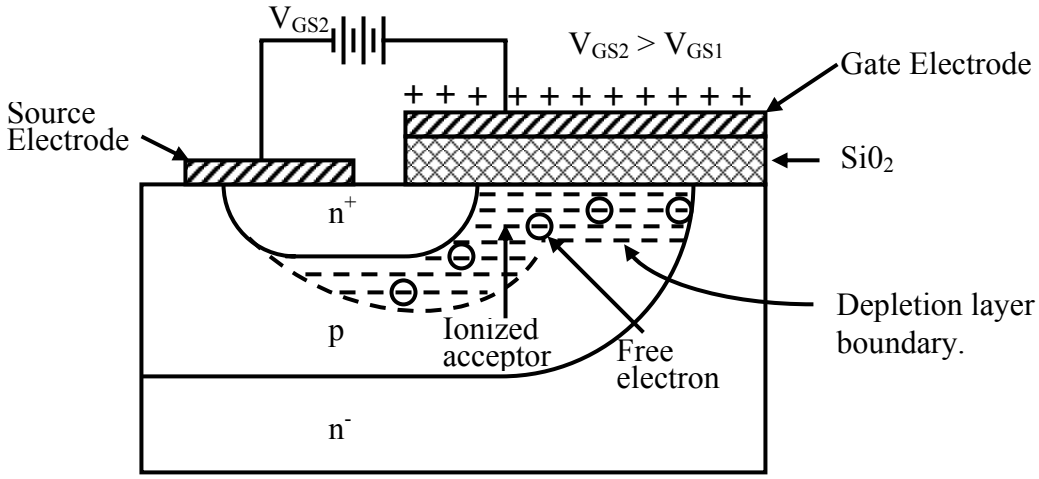
6.3 Operating principle of a MOSFET

At first glance it would appear that there is no path for any current to flow between the source and the drain terminals since at least one of the **p** **n** junctions (source – body and body-Drain) will be reverse biased for either polarity of the applied voltage between the source and the drain. There is no possibility of current injection from the gate terminal either since the gate oxide is a very good insulator. However, application of a positive voltage at the gate terminal with respect to the source will covert the silicon surface beneath the gate oxide into an **n** type layer or "channel", thus connecting the Source to the Drain as explained next.

The gate region of a MOSFET which is composed of the gate metallization, the gate (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in Fig 6.4 (a).



(a)



(b)

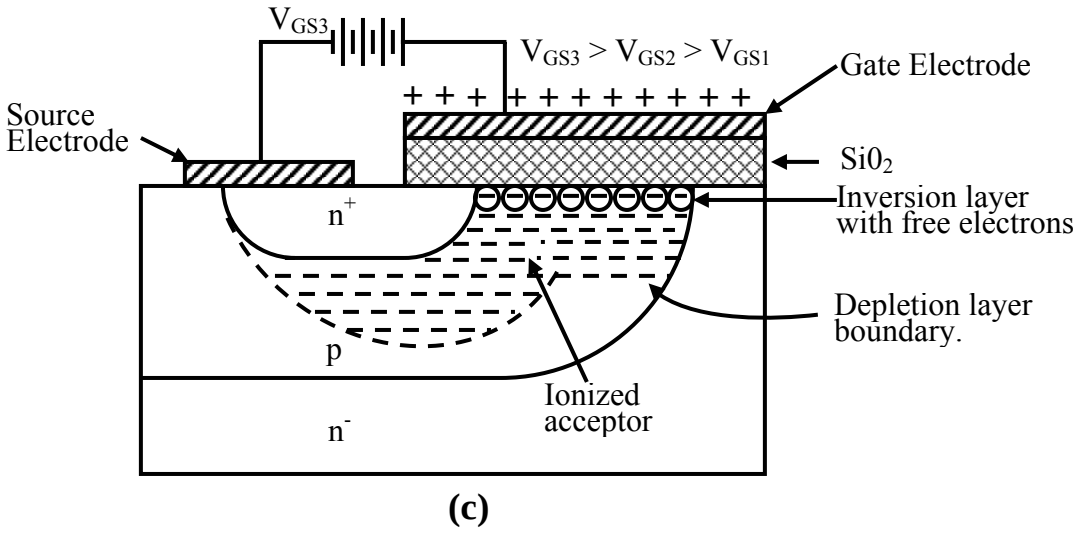


Fig. 6.4: Gate control of MOSFET conduction.
(a) Depletion layer formation;
(b) Free electron accumulation;
(c) Formation of inversion layer.

The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the **p** type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as shown in Fig 6.4 (b). The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig 6.4 (c). The inversion layer has all the properties of an **n** type semiconductor and is a conductive path or "channel" between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an **n-** type "channel" created by the electric field due to gate source voltage it is called "Enhancement type n-channel MOSFET".

The value of V_{GS} at which the inversion layer is considered to have formed is called the "Gate – Source threshold voltage V_{GS} (th)". As V_{GS} is increased beyond V_{GS}(th) the inversion layer gets some what thicker and more conductive, since the density of free electrons increases further with increase in V_{GS}. The inversion layer screens the depletion layer adjacent to it from increasing V_{GS}. The depletion layer thickness now remains constant.

Exercise 6.1 (after section 6.3)

1. Fill in the blank(s) with the appropriate word(s)

   i. A MOSFET is a _____ controlled _____ carrier device.

   ii. Enhancement type MOSFETs are normally _____devices while depletion type MOSFETs are normally _____ devices.

   iii. The Gate terminal of a MOSFET is isolated from the semiconductor by a thin layer of _____.

   iv. The MOSFET cell embeds a parasitic _____ in its structure.

   v. The gate-source voltage at which the _____ layer in a MOSFET is formed is called the _____ voltage.

   vi. The thickness of the _____ layer remains constant as gate source voltage is increased beyond the _____ voltage.

Answer: (i) voltage, majority; (ii) off, on; (iii) SiO_2, (iv) BJT, (v) inversion, threshold; (vi) depletion, threshold.

2. What are the main constructional differences between a MOSFET and a BJT? What effect do they have on the current conduction mechanism of a MOSFET?

   Answer: A MOSFET like a BJT has alternating layers of **p** and **n** type semiconductors. However, unlike BJT the **p** type body region of a MOSFET does not have an external electrical connection. The gate terminal is insulated for the semiconductor by a thin layer of SiO_2. The body itself is shorted with $\mathbf{n}^+$ type source by the source metallization. Thus minority carrier injection across the source-body interface is prevented. Conduction in a MOSFET occurs due to formation of a high density **n** type channel in the **p** type body region due to the electric field produced by the gate-source voltage. This **n** type channel connects $\mathbf{n}^+$ type source and drain regions. Current conduction takes place between the drain and the source through this channel due to flow of electrons only (majority carriers). Where as in a BJT, current conduction occurs due to minority carrier injection across the Base-Emitter junction. Thus a MOSFET is a voltage controlled majority carrier device while a BJT is a minority carrier bipolar device.

6.4 Steady state output i-v characteristics of a MOSFET

The MOSFET, like the BJT is a three terminal device where the voltage on the gate terminal controls the flow of current between the output terminals, Source and Drain. The source terminal is common between the input and the output of a MOSFET. The output characteristics of a MOSFET is then a plot of drain current (i_D) as a function of the Drain – Source voltage (v_{DS}) with gate source voltage (v_{GS}) as a parameter. Fig 6.5 (a) shows such a characteristics.

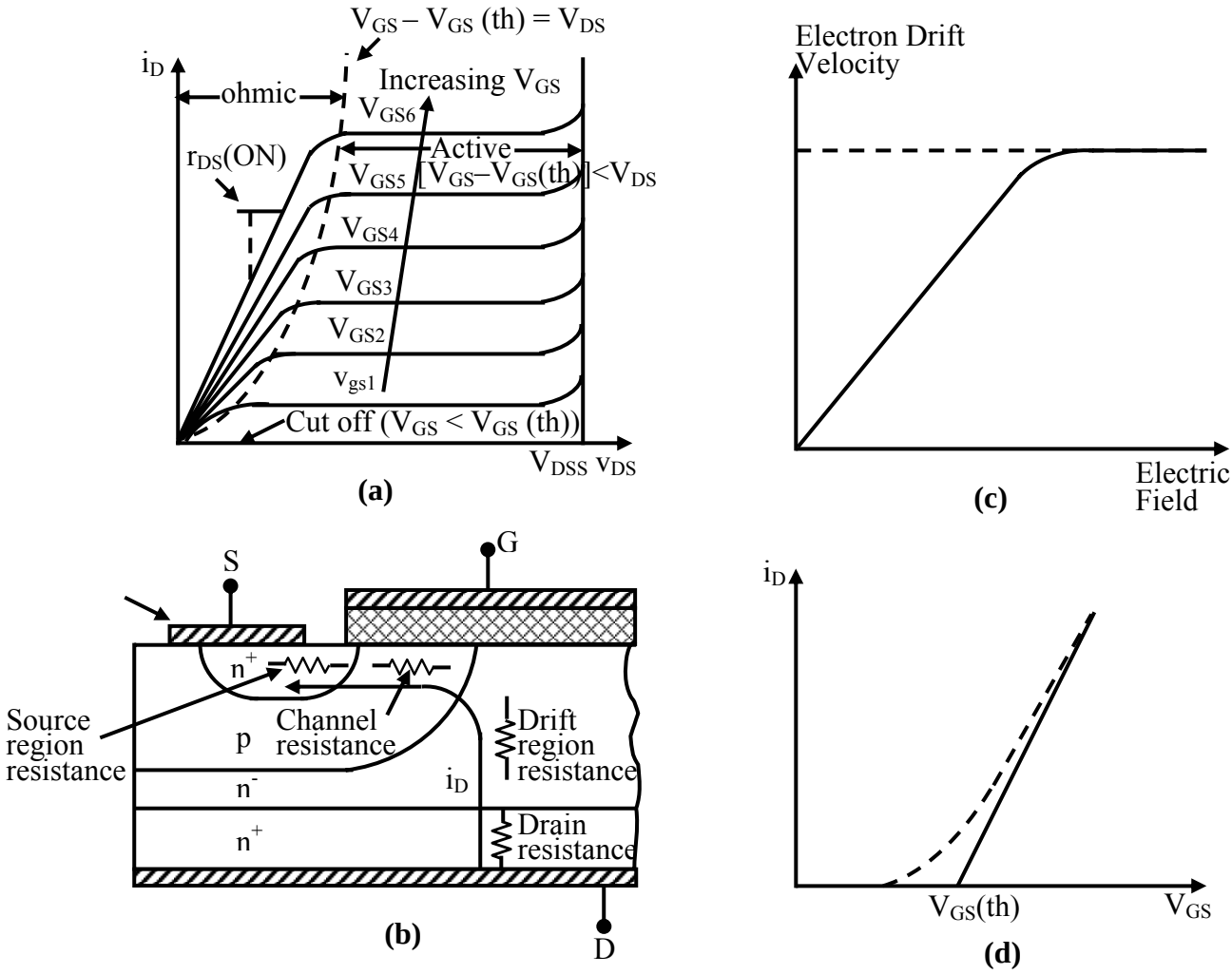


Fig. 6.5: Output i-v characteristics of a Power MOSFET
(a) i-v characteristics;
(b) Components of ON-state resistance;
(c) Electron drift velocity vs Electric field;
(d) Transfer

With gate-source voltage (V_{GS}) below the threshold voltage (v_{GS} (th)) the MOSFET operates in the cut-off mode. No drain current flows in this mode and the applied drain–source voltage (v_{DS}) is supported by the body-collector **p-n** junction. Therefore, the maximum applied voltage should be below the avalanche break down voltage of this junction (V_{DSS}) to avoid destruction of the device.

When V_{GS} is increased beyond $v_{GS}(th)$ drain current starts flowing. For small values of v_{DS} ($v_{DS} < (v_{GS} - v_{GS}(th))$ i_D is almost proportional to v_{DS}. Consequently this mode of operation is called "ohmic mode" of operation. In power electronic applications a MOSFET is operated either in the cut off or in the ohmic mode. The slope of the $v_{DS} - i_D$ characteristics in this mode is called the ON state resistance of the MOSFET (r_{DS} (ON)). Several physical resistances as shown in Fig 6.5 (b) contribute to r_{DS} (ON). Note that r_{DS} (ON) reduces with increase in v_{GS}. This is mainly due to reduction of the channel resistance at higher value of

v_{GS}. Hence, it is desirable in power electronic applications, to use as large a gate-source voltage as possible subject to the dielectric break down limit of the gate-oxide layer.

At still higher value of v_{DS} ($v_{DS} > (v_{GS} - v_{GS}(th))$ the $i_D - v_{DS}$ characteristics deviates from the linear relationship of the ohmic region and for a given v_{GS}, i_D tends to saturate with increase in v_{DS}. The exact mechanism behind this is rather complex. It will suffice to state that, at higher drain current the voltage drop across the channel resistance tends to decrease the channel width at the drain drift layer end. In addition, at large value of the electric field, produced by the large Drain – Source voltage, the drift velocity of free electrons in the channel tends to saturate as shown in Fig 6.5 (c). As a result the drain current becomes independent of V_{DS} and determined solely by the gate – source voltage v_{GS}. This is the active mode of operation of a MOSFET. Simple, first order theory predicts that in the active region the drain current is given approximately by

$$i_D = K(v_{GS} - v_{GS}(th))^2 \qquad (6.1)$$

Where K is a constant determined by the device geometry.

At the boundary between the ohmic and the active region

$$v_{DS} = v_{GS} - v_{GS}(th) \qquad (6.2)$$

$$\text{Therefore, } i_D = Kv_{DS}^2 \qquad (6.3)$$

Equation (6.3) is shown by a dotted line in Fig 6.5 (a). The relationship of Equation (6.1) applies reasonably well to logic level MOSFETs. However, for power MOSFETs the transfer characteristics (i_D vs v_{GS}) is more linear as shown in Fig 6.5 (d).

At this point the similarity of the output characteristics of a MOSFET with that of a BJT should be apparent. Both of them have three distinct modes of operation, namely, (i)cut off, (ii) active and (iii) ohmic (saturation for BJT) modes. However, there are some important differences as well.

- Unlike BJT a power MOSFET does not undergo second break down.
- The primary break down voltage of a MOSFET remains same in the cut off and in the active modes. This should be contrasted with three different break down voltages (V_{SUS}, V_{CEO} & V_{CBO}) of a BJT.
- The ON state resistance of a MOSFET in the ohmic region has positive temperature coefficient which allows paralleling of MOSFET without any special arrangement for current sharing. On the other hand, v_{CE} (sat) of a BJT has negative temperature coefficient making parallel connection of BJTs more complicated.

As in the case of a BJT the operating limits of a MOSFET are compactly represented in a Safe Operating Area (SOA) diagram as shown in Fig 6.6. As in the case of the FBSOA of a

BJT the SOA of a MOSFET is plotted on a log-log graph. On the top, the SOA is restricted by the absolute maximum permissible value of the drain current (I_{DM}) which should not be exceeded even under pulsed operating condition. To the left, operating restriction arise due to the non zero value of $r_{DS}(ON)$ corresponding to $v_{GS} = v_{GS}(Max)$. To the right, the first operating restriction is due to the limit on the maximum permissible junction temperature rise which depends on the power dissipation inside the MOSFET. This limit is different for DC (continuous) and pulsed operation of different pulse widths. As in the case of a BJT the pulsed safe operating areas are useful for shaping the switching trajectory of a MOSFET. A MOSFET does not undergo "second break down" and no corresponding operating limit appears on the SOA. The final operation limit to the extreme right of the SOA arises due to the maximum permissible drain source voltage (V_{DSS}) which is decided by the avalanche break down voltage of the drain -body **p-n** junction. This is an instantaneous limit. There is no distinction between the forward biased and the reverse biased SOAs for the MOSFET. They are identical.

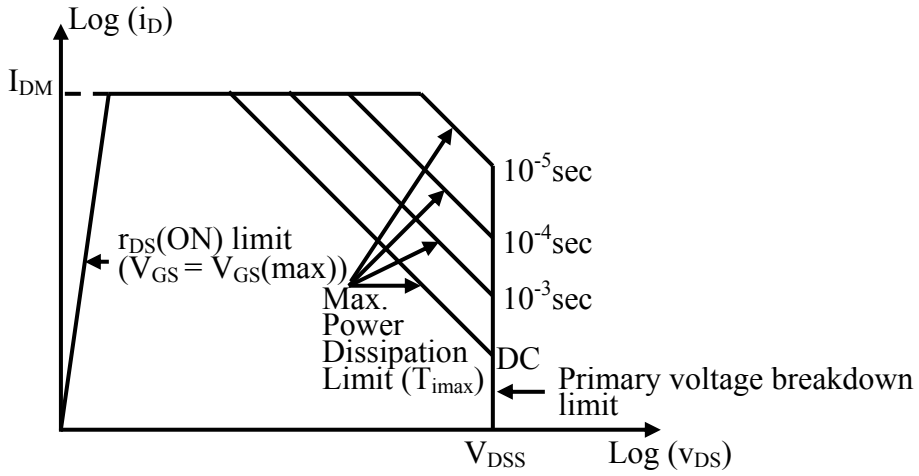


Fig. 6.6: Safe operating area of a MOSFET.

Due to the presence of the anti parallel "body diode", a MOSFET can not block any reverse voltage. The body diode, however, can carry an RMS current equal to I_{DM}. It also has a substantial surge current carrying capacity. When reverse biased it can block a voltage equal to V_{DSS}.

For safe operation of a MOSFET, the maximum limit on the gate source voltage (V_{GS} (Max)) must be observed. Exceeding this voltage limit will cause dielectric break down of the thin gate oxide layer and permanent failure of the device. It should be noted that even static charge inadvertently put on the gate oxide by careless handling may destroy it. The device user should ground himself before handling any MOSFET to avoid any static charge related problem.

Exercise 6.2

Fill in the blank(s) with the appropriate word(s)

i. A MOSFET operates in the _____ mode when $v_{GS} < v_{GS}(th)$

ii. In the ohmic region of operation of a MOSFET $v_{GS} - v_{GS}$ (th) is greater than _____.

iii. r_{DS} (ON) of a MOSFET _____ with increasing v_{GS}.

iv. In the active region of operation the drain current i_D is a function of _____ alone and is independent of _____.

v. The primary break down voltage of MOSFET is _____ of the drain current.

vi. Unlike BJT a MOSFET does not undergo _____.

vii. _____ temperature coefficient of r_{DS}(ON) of MOSFETs facilitates easy _____ of the devices.

viii. In a Power MOSFET the relation ship between i_D and $v_{GS} - v_{GS}$(th) is almost _____ in the active mode of operation.

ix. The safe operating area of a MOSFET is restricted on the left hand side by the _____ limit.

Answer: (i) Cut off; (ii) v_{DS}; (iii) decreases; (iv) v_{GS}, v_{DS}; (v) independent; (vi) second break down; (vii) Positive, paralleling; (viii) linear; (ix) r_{DS} (ON);

6.5 Switching characteristics of a MOSFET

6.5.1 Circuit models of a MOSFET cell

Like any other power semiconductor device a MOSFET is used as a switch in all power electronic converters. As a switch a MOSFET operates either in the cut off mode (switch off) or in the ohmic mode (switch on). While making transition between these two states it traverses through the active region. Being a majority carrier device the switching process in a MOSFET does not involve any inherent delay due to redistribution of minority charge carriers. However, formation of the conducting channel in a MOSFET and its disappearance require charging and discharging of the gate-source capacitance which contributes to the switching times. There are several other capacitors in a MOSFET structure which are also involved in the switching process. Unlike bipolar devices, however, these switching times can be controlled completely by the gate drive circuit design.

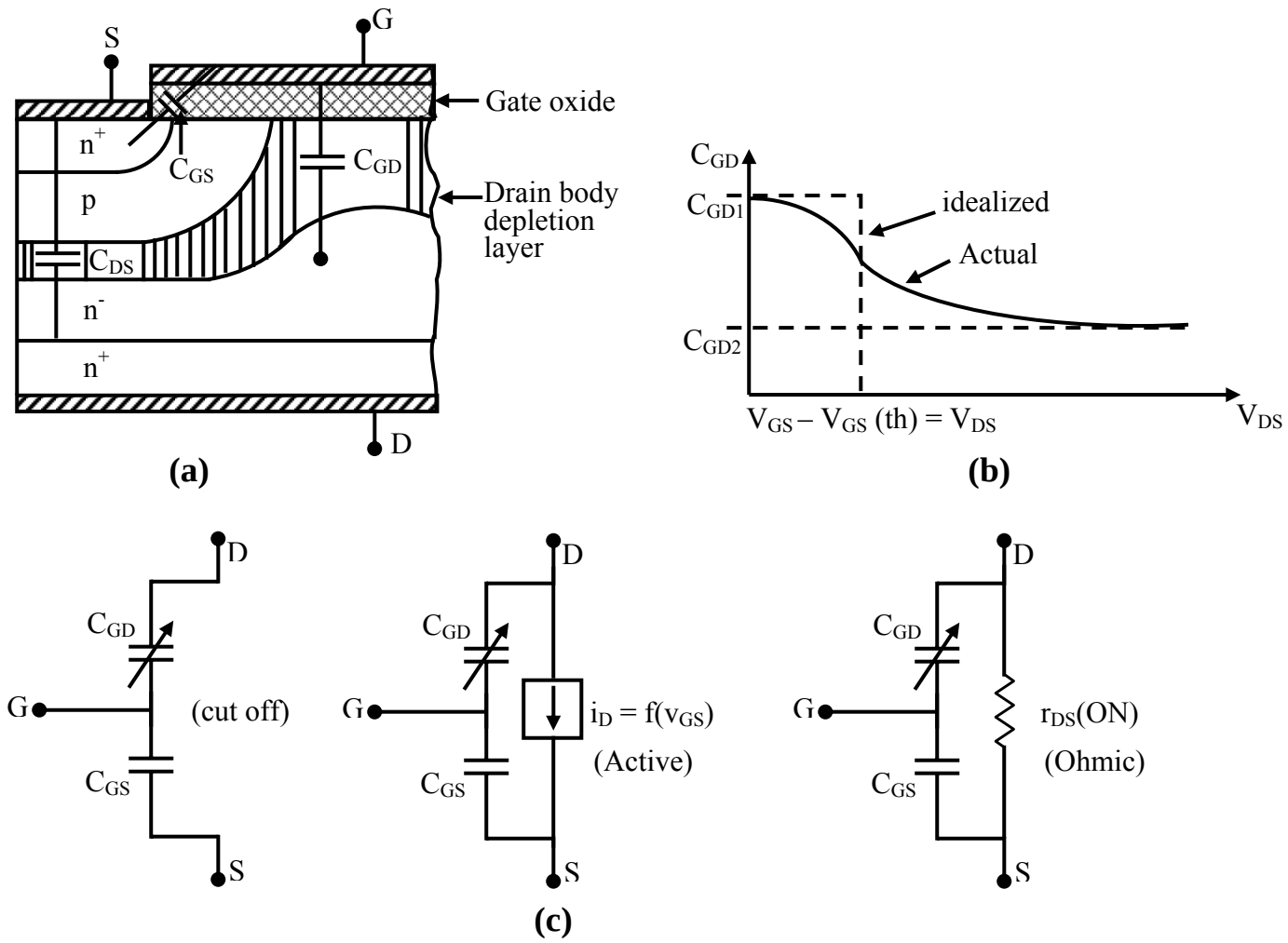


Fig. 6.7: Circuit model of a MOSFET
(a) MOSFET capacitances
(b) Variation of C_{GD} with V_{DS}
(c) Circuit models.

Fig 6.7 (a) shows three important capacitances inherent in a MOSFET structure. The most prominent capacitor in a MOSFET structure is formed by the gate oxide layer between the gate metallization and the $\mathbf{n}^+$ type source region. It has the largest value (a few nano farads) and remains more or less constant for all values of v_{GS} and v_{DS}. The next largest capacitor (a few hundred pico forwards) is formed by the drain – body depletion region directly below the gate metallization in the $\mathbf{n}^-$ drain drift region. Being a depletion layer capacitance its value is a strong function of the drain source voltage v_{DS}. For low values of v_{DS} ($v_{DS} < (v_{GS} - v_{GS}(th))$) the value of C_{GD} (C_{GD2}) is considerably higher than its value for large v_{DS} as shown in Fig 6.7 (b). Although variation of C_{GD} between C_{GD1} and C_{GD2} is continuous a step change in the value of C_{GD} at $v_{DS} = v_{GS} - v_{GS}(th)$ is assumed for simplicity. The lowest value capacitance is formed between the drain and the source terminals due to the drain – body depletion layer away form the gate metallization and below the source metallization. Although this capacitance is important for some design considerations (such as snubber design, zero voltage switching etc) it does not appreciably affect the "hard switching" performance of a MOSFET. Consequently, it will be neglected in our discussion. From the

above discussion and the steady state characteristics of a MOSFET the circuit models of a MOSFET in three modes of operation can be drawn as shown in Fig 6.7 (c).

6.5.2 Switching waveforms

The switching behavior of a MOSFET will be described in relation to the clamped inductive circuit shown in Fig 6.8. For simplicity the load current is assumed to remain constant over the small switching interval. Also the diode D_F is assumed to be ideal with no reverse recovery current. The gate is assumed to be driven by an ideal voltage source giving a step voltage between zero and V_{gg} in series with an external gate resistance R_g.

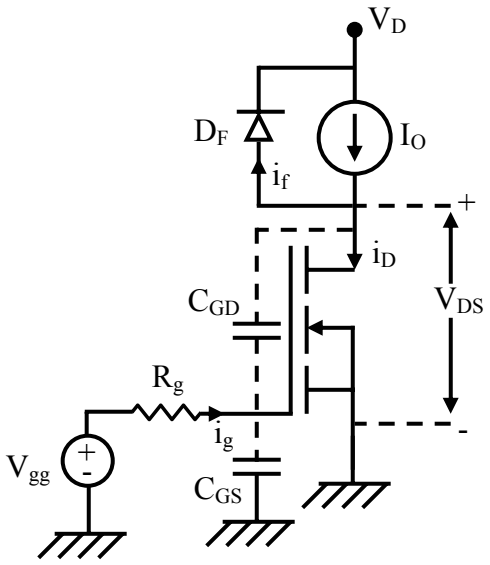


Fig. 6.8: Clamped inductive switching circuit using a MOSFET.

To turn the MOSFET on, the gate drive voltage changes from zero to V_{gg}. The gate source voltage which was initially zero starts rising towards V_{gg} with a time constant $\tau_1 = R_g (C_{GS} + C_{GD1})$ as shown in Fig 6.9.

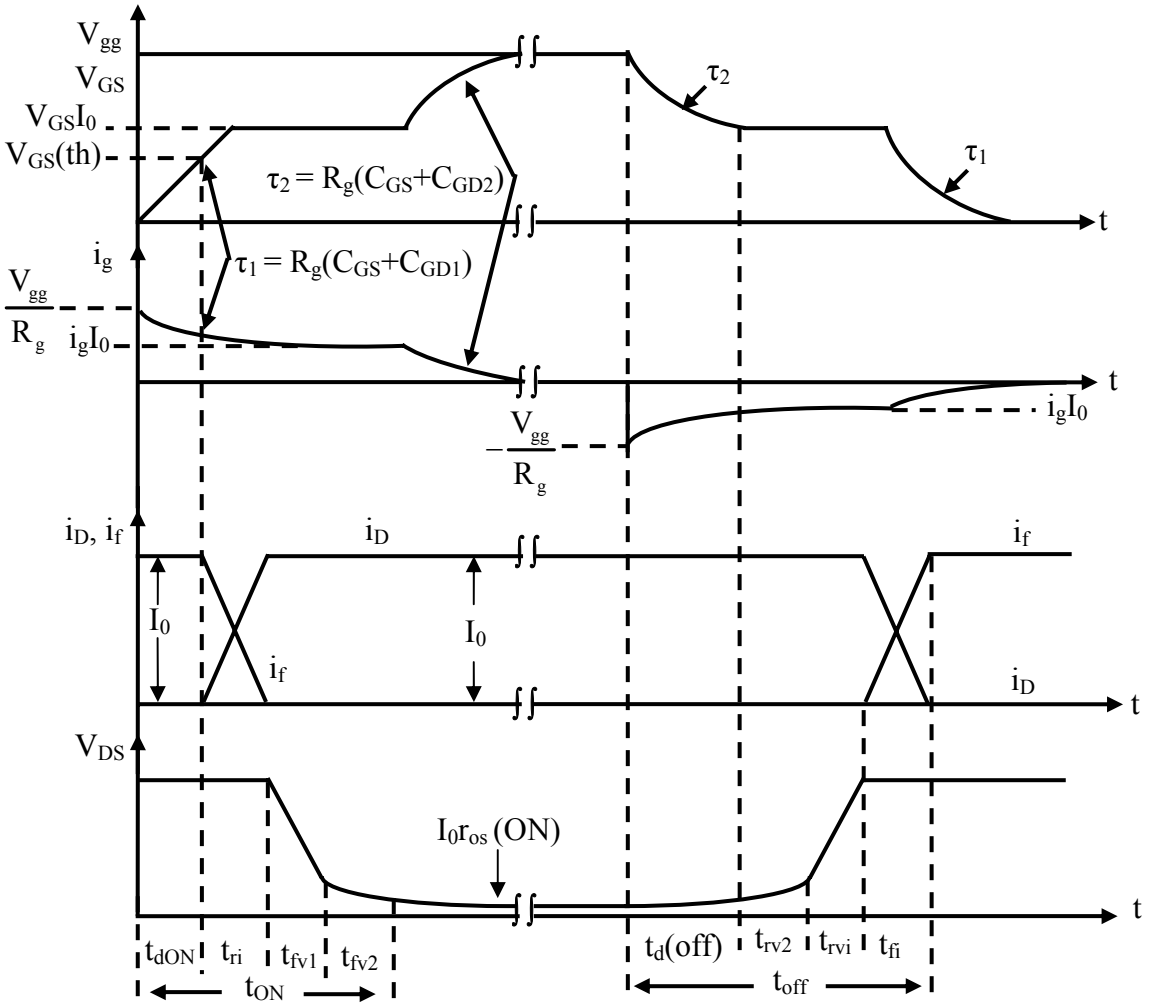


Fig. 6.9: Switching waveforms of a clamped inductive switching circuit using MOSFET

Note that during this period the drain voltage v_{DS} is clamped to the supply voltage V_D through the free wheeling diode D_F. Therefore, C_{GS} and C_{GD} can be assumed to be connected in parallel effectively. A part of the total gate current ig charges C_{GS} while the other part discharges C_{GD}.

Till v_{GS} reaches v_{GS} (th) no drain current flows. This time period is called turn on delay time (t_d(ON)). Note that t_d(ON) can be controlled by controlling R_g. Byond t_d(ON) i_D increases linearly with v_{GS} and in a further time t_{ri} (current rise time) reaches I_o. The corresponding value of v_{GS} and i_g are marked as V_{GS} I_o and i_g I_o respectively in Fig 6.9.

At this point the complete load current has been transferred to the MOSFET from the free wheeling diode D_F. i_D does not increase byond this point. Since in the active region i_D and v_{GS} are linearly related, v_{GS} also becomes clamped at the value $v_{GS}I_o$. The gate current i_g now discharges C_{GD} and the drain voltage starts falling.

$$\frac{d}{dt}v_{DS} = \frac{d}{dt}\left(v_{GS} + v_{GD}\right) = \frac{d}{dt}v_{GD} = \frac{i_g}{C_{GD}} = \frac{V_{GG} - V_{GS}I_o}{C_{GD}R_g} \qquad (6.4)$$

The fall of v_{DS} occurs in two distinct intervals. When the MOSFET is in the active region ($v_{DS} > (v_{GS} - v_{GS}(th))$ $C_{GD} = C_{GD1}$.Since $C_{GD1} << C_{GD2}$, v_{DS} falls rapidly. This fast fall time of v_{DS} is marked t_{fv1} in Fig 6.9. However, once in the ohmic region, $C_{GD} = C_{GD2} >> C_{GD1}$. Therefore, rate of fall of v_{DS} slows down considerably (t_{fv2}). Once v_{DS} reaches its on state value ($r_{DS}(ON)$ I_o) v_{GS} becomes unclamped and increases towards V_{gg} with a time constant $\tau_2 = R_g (C_{GS} + C_{GD2})$. Note that all switching periods can be reduced by increasing Vgg or / and decreasing Rg. The total turn on time is $t_{ON} = t_d(ON) + t_{ri} + t_{fv1} + t_{fv2}$.

To turn the MOSFET OFF, V_{gg} is reduced to zero triggering the exact reverse process of turn on to take place. The corresponding waveforms and switching intervals are show in Fig 6.9. The total turn off time $t_{off} = t_d(off) + t_{rv1} + t_{rv2} + t_{fi}$.

6.5.3 MOSFET Gate Drive

MOSFET, being a voltage controlled device, does not require a continuous gate current to keep it in the ON state. However, it is required to charge and discharge the gate-source and the gate-drain capacitors in each switching operation. The switching times of a MOSFET essentially depends on the charging and discharging rate of these capacitors. Therefore, if fast charging and discharging of a MOSFET is desired at fast switching frequency the gate drive power requirement may become significant. Fig 6.10 (a) shows a typical gate drive circuit of a MOSFET.

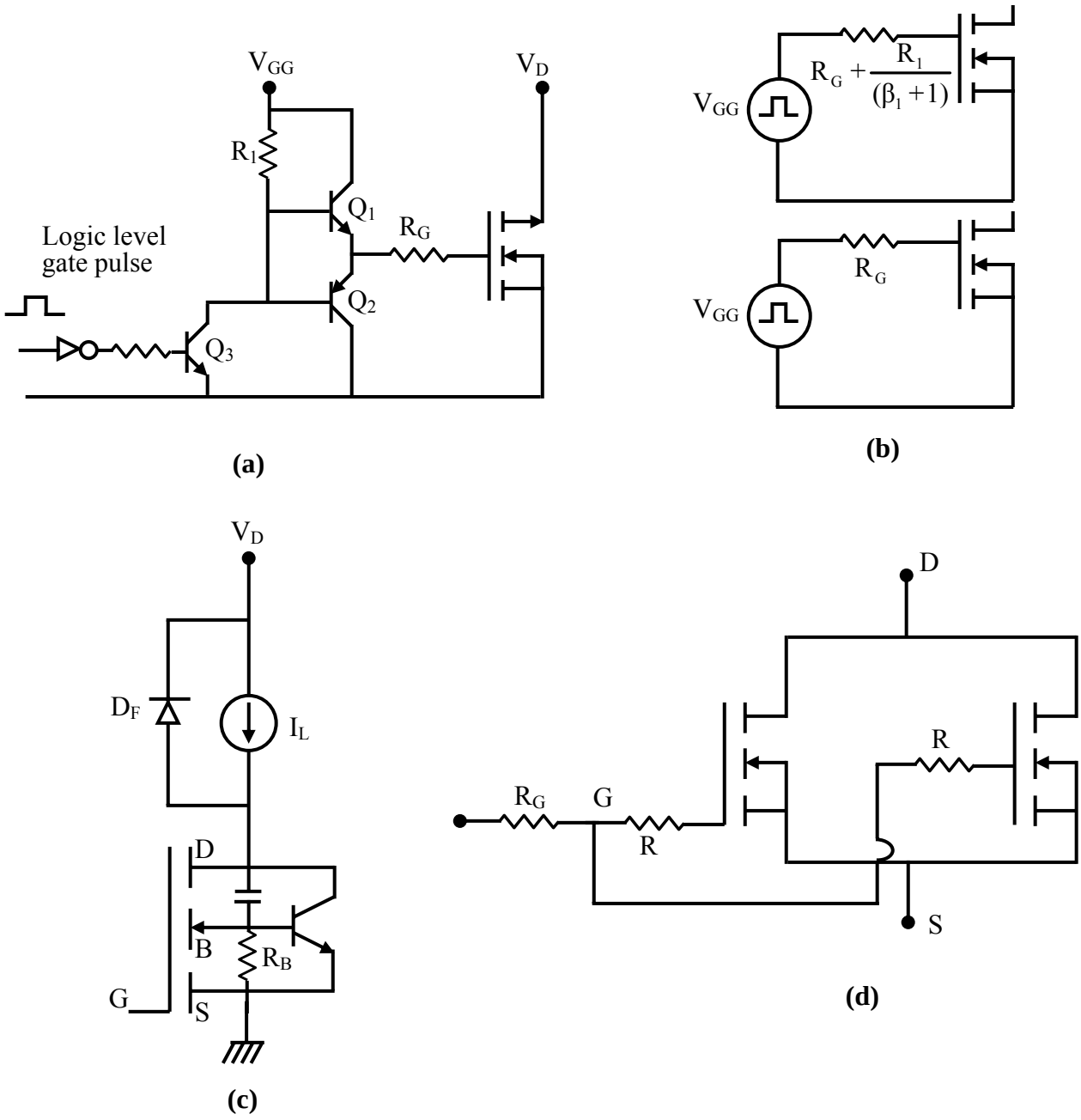


Fig. 6.10: MOSFET gate drive circuit.
(a) Gate drive circuit; (b) Equivalent circuit during turn on and off;
(b) Effect of parasitic BJT; (d) Parallel connection of MOSFET's.

To turn the MOSFET on the logic level input to the inverting buffer is set to high state so that transistor Q_3 turns off and Q_1 turns on. The top circuit of Fig 6.10 (b) shows the equivalent circuit during turn on. Note that, during turn on Q_1 remains in the active region. The effective gate resistance is $R_G + R_1 / (\beta_1 + 1)$. Where, β_1 is the dc current gain of Q_1.

To turn off the MOSFET the logic level input is set to low state. Q_3 and Q_2 turns on whole Q_1 turns off. The corresponding equivalent circuit is given by the bottom circuit of Fig 6.10 (b)

The switching time of the MOSFET can be adjusted by choosing a proper value of R_G. Reducing R_G will incase the switching speed of the MOSFET. However, caution should be exercised while increasing the switching speed of the MOSFET in order not to turn on the parasitic BJT in the MOSFET structure inadvertently. The drain-source capacitance (C_{DS}) is actually connected to the base of the parasitic BJT at the **p** type body region. The body source short has some nonzero resistance. A very fast rising drain-source voltage will send sufficient displacement current through C_{DS} and R_B as shown in Fig 6.10 (c). The voltage drop across R_B may become sufficient to turn on the parasitic BJT. This problem is largely avoided in a modern MOSFET design by increasing the effectiveness of the body-source short. The devices are now capable of dv_{DS}/dt in excess to 10,000 V/μs. Of course, this problem can also be avoided by slowing down the MOSFET switching speed.

Since MOSFET on state resistance has positive temperature coefficient they can be paralleled without taking any special precaution for equal current sharing. To parallel two MOSFETs the drain and source terminals are connected together as shown in Fig 6.10 (d). However, small resistances (R) are connected to individual gates before joining them together. This is because the gate inputs are highly capacitive with almost no losses. Some stray inductance of wiring may however be present. This stray inductance and the MOSFET capacitance can give rise to unwanted high frequency oscillation of the gate voltage that can result in puncture of the gate qxide layer due to voltage increase during oscillations. This is avoided by the damping resistance R.

Exercise 6.3

1. Fill in the blank(s) with the appropriate word(s)

   i. The Gate-Source capacitance of a MOSFET is the _____ among all three capacitances.

   ii. The Gate-Drain transfer capacitance of a MOSFET has large value in the _____ region and small value in the _____ region.

   iii. During the turn on delay time the MOSFET gate source voltage rises from zero to the _____ voltage.

   iv. The voltage fall time of a MOSFET is _____ proportional to the gate charging resistance.

   v. Unlike BJT the switching delay times in a MOSFET can be controlled by proper design of the _____ circuit.

Answer: (i) largest; (ii) ohmic, active; (iii) threshold; (iv) inversely; (v) gate drive.

2. A Power MOSFET has the following data
C_{GS} = 800 pF ; C_{GD} = 150 pF; g_f= 4; $v_{GS}(th)$ = 3V;
It is used to switch a clamped inductive load (Fig 6.8) of 20 Amps with a supply voltage V_D= 200V. The gate drive voltage is v_{gg} = 15V, and gate resistance R_g = 50Ω. Find out maximum value of $\left|\frac{di_d}{dt}\right|$ and $\left|\frac{dv_{DS}}{dt}\right|$ during turn ON.

Answer: During turn on

$$i_D \approx g_f\left(v_{gs} - v_{gs}(th)\right)$$

$$\therefore \frac{di_D}{dt} = g_f \frac{dv_{gs}}{dt}$$

But $\left(C_{GS} + C_{GD}\right)\frac{dv_{gs}}{dt} = \frac{V_{gg} - v_{gs}}{R_g}$

$$\therefore \frac{di_D}{dt} = g_f \frac{dv_{gs}}{dt} = \frac{g_f}{R_g\left(C_{GS} + C_{GD}\right)}\left(V_{gg} - v_{gs}\right)$$

$$\therefore \left|\frac{di_D}{dt}\right|_{Max} = \frac{g_f}{R_g\left(C_{GS} + C_{GD}\right)}\left(V_{gg} - v_{gs}\Big|_{Min}\right) = \frac{g_f\left(V_{gg} - v_{gs}(th)\right)}{R_g\left(C_{GS} + C_{GD}\right)}$$

since for $v_{gs} < v_{gs}(th)$ $\quad i_D = \frac{di_D}{dt} = 0$

$$\therefore \left|\frac{di_D}{dt}\right|_{Max} = \frac{4}{50 \times 950 \times 10^{-12}}(15 - 3) = 1.01 \times 10^9 \text{ A/sec}$$

From equation (6.4)

$$\left|\frac{dv_{DS}}{dt}\right| = \frac{V_{gg} - V_{GS,I_o}}{C_{GD}\ R_g}$$

For I_o = 20 A, $v_{gs}(th)$ = 3V, and g_f= 4

$$V_{GS,I_o} = \frac{I_o}{g_f} + v_{gs}(th) = \frac{20}{4} + 3 = 8 \text{ volts}$$

$$\therefore \left|\frac{dv_{DS}}{dt}\right| = \frac{15 - 8}{150 \times 10^{-12} \times 50} = 933 \times 10^6 \text{ V/sec}.$$

6.6 MOSFET Ratings

Steady state operating limits of a MOSFET are usually specified compactly as a safe operating area (SOA) diagram. The following limits are specified.

V_{DSS}: This is the drain-source break down voltage. Exceeding this limit will destroy the device due to avalanche break down of the body-drain **p-n** junction.

I_{DM}: This is the maximum current that should not be exceeded even under pulsed current operating condition in order to avoid permanent damage to the bonding wires.

Continuous and Pulsed power dissipation limits: They indicate the maximum allowable value of the V_{DS}, i_D product for the pulse durations shown against each limit. Exceeding these limits will cause the junction temperature to rise beyond the acceptable limit.

All safe operating area limits are specified at a given case temperature.

In addition, several important parameters regarding the dynamic performance of the device are also specified. These are

Gate threshold voltage (V_{GS} (th)): The MOSFET remains in the cut off region when v_{GS} in below this voltage. V_{GS} (th) decreases with junction temperature.

Drain Source on state resistance (r_{DS} (ON)): This is the slope of the $i_D - v_{DS}$ characteristics in the ohmic region. Its value decreases with increasing v_{GS} and increases with junction temperature. r_{DS} (ON) determines the ON state power loss in the device.

Forward Transconductance (g_{fs}): It is the ratio of i_D and ($v_{GS} - v_{GS}$(th)). In a MOSFET switching circuit it determines the clamping voltage level of the gate – source voltage and thus influences dv_{DS}/dt during turn on and turn off.

Gate-Source breakdown voltage: Exceeding this limit will destroy the gate structure of the MOSFET due to dielectric break down of the gate oxide layer. It should be noted that this limit may by exceeded even by static charge deposition. Therefore, special precaution should be taken while handing MOSFETs.

Input, output and reverse transfer capacitances (C_{GS}, C_{DS} & C_{GD}): Value of these capacitances are specified at a given drain-source and gate-source voltage. They are useful for designing the gate drive circuit of a MOSFET.

In addition to the main MOSFET, specifications pertaining to the "body diode" are also provided. Specifications given are

Reverse break down voltage: This is same as V_{DSS}

Continuous ON state current (I_S): This is the RMS value of the continuous current that can flow through the diode.

Pulsed ON state current (I_{SM}): This is the maximum allowable RMS value of the ON state current through the diode given as a function of the pulse duration.

Forward voltage drop (v_F): Given as an instantaneous function of the diode forward current.

Reverse recovery time (t_{rr}) and Reverse recovery current (I_{rr}): These are specified as functions of the diode forward current just before reverse recovery and its decreasing slope (di_F/dt).

Exercise 6.4

Fill in the blank(s) with the appropriate word(s)

i. The maximum voltage a MOSFET can with stand is _____ of drain current.

ii. The FBSOA and RBSOA of a MOSFET are _____.

iii. The gate source threshold voltage of a MOSFET _____ with junction temperature while the on state resistance _____ with junction temperature.

iv. The gate oxide of a MOSFET can be damaged by _____ electricity.

v. The reverse break down voltage of the body diode of a MOSFET is equal to _____ while its RMS forward current rating is equal to _____.

Answer: (i) independent; (ii) identical; (iii) decreases, increases; (iv) static; (v) V_{DSS}; I_{DM}.

Reference

[1] "Evolution of MOS-Bipolar power semiconductor Technology", B. Jayant Baliga, Proceedings of the IEEE, VOL.76, No-4, April 1988.

[2] "Power Electronics ,Converters Application and Design" Third Edition, Mohan, Undeland, Robbins. John Wiley & Sons Publishers 2003.

[3] GE – Power MOSFET data sheet.

Lesson Summary

- MOSFET is a voltage controlled majority carrier device.
- A Power MOSFET has a vertical structure of alternating **p** and **n** layers.
- The main current carrying terminals of an **n** channel enhancement mode MOSFET are called the Drain and the Source and are made up of $\mathbf{n}^+$ type semiconductor.
- The control terminal is called the Gate and is isolated form the bulk semiconductor by a thin layer of SiO_2.
- **p** type semiconductor body separates $\mathbf{n}^+$ type source and drain regions.
- A conducting **n** type channel is produced in the **p** type body region when a positive voltage greater than a threshold voltage is applied at the gate.
- Current conduction in a MOSFET occurs by flow of electron from the source to the drain through this channel.
- When the gate source voltage is below threshold level a MOSFET remains in the "Cut Off" region and does not conduct any current.
- With $v_{GS} > v_{GS}$ (th) and $v_{DS} < (v_{GS} - v_{GS}$ (th)) the drain current in a MOSFET is proportional to v_{DS}. This is the "Ohmic region" of the MOSFET output characteristics.
- For larger values of v_{DS} the drain current is a function of v_{GS} alone and does not depend on v_{Ds}. This is called the "active region" of the MOSFET.
- In power electronic applications a MOSFET is operated in the "Cut Off" and Ohmic regions only.
- The on state resistance of a MOSFET (V_{DS} (ON)) has a positive temperature coefficient. Therefore, MOSFETs can be easily paralleled.
- A MOSFET does not undergo second break down.
- The safe operating area (SOA) of a MOSFET is similar to that of a BJT except that it does not have a second break down limit.
- Unlike BJT the maximum forward voltage withstanding capability of a MOSFET does not depend on the drain current.
- The safe operating area of a MOSFET does not change under Forward and Reverse bias conditions.
- The drain – body junction in a MOSFET structure constitute an anti parallel diode connected between the source and the drain. This is called the MOSFET "body – diode."
- The body diode of a MOSFET has the same break down voltage and forward current rating as the main MOSFET.
- The switching delays in a MOSFET are due to finite charging and discharging time of the input and output capacitors.
- Switching times of a MOSFET can be controlled completely by external gate drive design.

- The input capacitor along with the gate drive resistance determine the current rise and fall time of a MOSFET during switching.
- The transfer capacitor (C_{gd}) determines the drain voltage rise and fall times.
- r_{DS} (ON) of a MOSFET determines the conduction loss during ON period.
- r_{DS} (ON) reduces with higher v_{gs}. Therefore, to minimize conduction power loss maximum permissible v_{gs} should be used subject to dielectric break down of the gate oxide layer.
- The gate oxide layer can be damaged by static charge. Therefore MOSFETs should be handled only after discharging one self through proper grounding.
- For similar voltage rating, a MOSFET has a relatively higher conduction loss and lower switching loss compared to a BJT. Therefore, MOSFETs are more popular for high frequency (>50 kHz) low voltage (<100 V) circuits.

Practice Problems and Answers

Practice Problems

1. How do you expect the gate source capacitance of a MOSFET to varry with gate source voltage. Explain your answer.

2. The gate oxide layer of a MOSFET is 1000 Angstrom thick Assuming a break down field strength of 5×10^6 V/cm and a safely factor of 50%, find out the maximum allowable gate source voltage.

3. Explain why in a high voltage MOSFET switching circuit the voltage rise and fall time is always greater than current fall and rise times.

4. A MOSFET has the following parameters

   $V_{GS}(th) = 3V$, $g_{fs} = 3$, $C_{GS} = 800$ PF, $C_{GD} = 250$ PF. The MOSFET is used to switch an inductive load of 15 Amps from 150V supply. The switching frequency is 50 kHz. The gate drive circuit has a driving voltage of 15V and output resistance of 50Ω. Find out the switching loss in the MOSFET.

Answer to practice problems

1. When the gate voltage is zero the thickness of the gate-source capacitance is approximately equal to the thickness of the gate oxide layer. As the gate source voltage increases the width of the depletion layer in the **p** body region also increases. Since the depletion layer is a region of immobile charges it in effect increases the thickness of the gate-source capacitance and hence the value of this capacitances decreases with increasing v_{GS}. However, as v_{GS} is increased further free electrons generated by thermal ionization get attracted towards the gate oxide-semiconductor interface. These free electrons screen the depletion layer partially and the gate-source capacitance starts increasing again. When v_{GS} is above v_{gs} (th) the inversion layer completely screens the depletion layer and the effective thickness of the gate-source capacitance becomes once again equal to the thickness of the oxide layer. There after the value of C_{GS} remains more or less constant.

2. From the given data the break down gate source voltage

$$v_{GS}\Big|_{BD} = E_{BD} \times t_{gs}$$

where E_{BD} = Break down field strength

t_{gs} = thickness of the oxide layer.

So $v_{GS}\Big|_{BD} = 5\times10^{6}\times1000\times10^{-8} = 50\text{V}$

Let $v_{gs}\Big|_{Max}$ be the maximum allowable gate source voltage assuming 50% factor of safety.

$$\therefore \quad 1.5 \;\; v_{gs}\Big|_{Max} = v_{GS}\Big|_{BD} = 50\text{ V}$$

$$\therefore v_{gs}\Big|_{Max} = \frac{50}{1.5}\text{V} \approx 33\text{ Volts.}$$

3. We Know that for MOSFET

$$i_D = g_{fs}\left(V_{GS} - V_{GS}(th)\right)$$

$$\therefore \quad \frac{di_D}{dt} = g_{fs}\frac{d}{dt}v_{GS} = g_{fs}\frac{\left(V_{gg} - v_{GS}\right)}{R_g\ C_{GS}}$$

During current rise $V_{gg} >> v_{GS}$

$$\therefore \frac{di_D}{dt} \approx \frac{g_{fs}}{R_g C_{GS}}V_{gg}$$

$$\therefore t_{ri} = t_{fi} \approx \frac{I_o}{g_{fs}V_{gg}}\ R_g C_{GS} \quad \text{where } I_o = \text{load current.}$$

Now From equation (6.4)

$$\frac{d}{dt}v_{DS} = \frac{V_{gg} - V_{gs}, I_o}{R_g\ C_{GD}} \approx \frac{V_{gg}}{R_g\ C_{GD}}$$

Since $V_{gg} >> V_{gs}$, I_o

$$\therefore t_{rr} = t_{fv} \approx \frac{V_D}{V_{gg}} R_g C_{GD} \quad \text{where } V_D = \text{Load voltage.}$$

$$\therefore \quad \frac{t_{ri}}{t_{rr}} = \frac{t_{fi}}{t_{fr}} = \frac{I_o}{V_D} \quad \frac{C_{GS}}{g_{fs} C_{GD}}$$

That is current rise and fall times are much shorter than voltage rise and fall times.

4. Referring to Fig 6.9 energy loss during switching occurs during intervals t_{ri} , t_{fv1}, t_{fv2}, t_{rv2},t_{rv1}, and t_{fi}. For simplicity it will be assumed that $t_{fv2} = t_{rv2} = 0$. Also the rise and fall of i_D and v_{DS} will be assumed to be linear.

During t_{ri}

$$i_D = g_{fs}(v_{gs} - v_{gs}(th))$$

$$\therefore \frac{di_D}{dt} = g_{fs} \frac{d}{dt} v_{gs} = g_{fs} \frac{V_{gg} - v_{gs}}{(C_{GS} + C_{GD})R_g}$$

$$\therefore \frac{di_D}{dt} \approx \frac{g_{fs} V_{gg}}{(C_{GS} + C_{GD})R_g} \text{since} V_{gg} >> v_{gs} \text{ during current rise}$$

$$\therefore t_{ri} = \frac{I_o}{g_{fs} V_{gg}} (C_{GS} + C_{GD}) R_g$$

Energy loss during t_{ri} is

$$E_{ON1} = \frac{1}{2} t_{ri} V_D Io = \frac{V_D I_o^2}{2 g_{fs} V_{gg}} (C_{GS} + C_{GD}) R_g$$

During t_{fv}

$$\frac{dV_{DS}}{dt} = \frac{V_{gg} - V_{gs,} I_o}{C_{GD} R_g}$$

$$\text{But } V_{gs}, I_o = \frac{I_o}{g_{fs}} + v_{gs}(th)$$

$$\therefore \frac{dV_{DS}}{dt} = \frac{V_{gg} - v_{gs}(th) - I_o / g_{fs}}{R_g C_{GD}}$$

$$\therefore t_{fv} = \frac{V_D}{V_{gg} - V_{gs}(th) - I_o / g_{fs}} R_g C_{GD}$$

Energy loss during t_{fv} is

$$E_{ON2} = 1/2 \, t_{fv} I_o V_D$$

$$= \frac{V_D{}^2 I_o}{2\left(V_{gg} - v_{gs}(th) - I_o / g_{fs} \right)} R_g C_{GD}$$

$\therefore$ Energy loss during Turn on is

$$E_{ON} = E_{ON1} + E_{ON2} = \frac{V_D I_o R_g}{2}\left[\frac{I_o\left(C_{GS}+C_{GD}\right)}{g_{fs}V_{gg}} + \frac{V_D C_{GD}}{\left(V_{gg} - V_{gs}(th)\right)}\right]$$

From the symmetry of the Turn ON and the Turn OFF operation of MOSFET (i.e. $t_{ri} = t_{fi}$, $t_{fv} = t_{rv}$)

$$E_{ON} = E_{OFF}$$

$\therefore$ Total switching energy lass is $E_{sw} = E_{ON} + E_{OFF} = 2\,E_{ON}$

$$\therefore\ E_{sw} = V_D I_o R_g C_{GD}\left[\frac{I_o/g_{fs}}{V_{gg}}\left(1+\frac{C_{GS}}{C_{GD}}\right) + \frac{VD/V_{gg}}{\frac{V_{gs}(th)}{V_{gg}} - \frac{I_o/g_{fs}}{V_{gg}}}\right]$$

$$\therefore\ P_{sw}E_{sw} = V_D I_o R_g C_{GD} f_{sw}\left[\left(1+\frac{C_{GS}}{C_{GD}}\right)\frac{I_o/g_{fs}}{V_{gg}} + \frac{VD/V_{gg}}{1 - \frac{v_{gs}(th)}{V_{gg}} - \frac{I_o/g_{fs}}{v_{gg}}}\right]$$

Substituting the values given

$P_{sw} = 32$ mw,

Linear Amplifiers and OpAmps

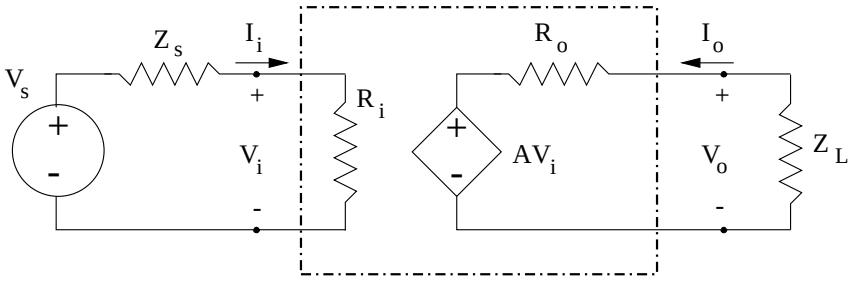
References: Hayes & Horowitz (pp 163-240), Rizzoni (Chapter ?)

Amplifiers are two-port networks in which the output voltage or current is directly proportional to either input voltage or current. Four different kind of amplifiers exits:

Voltage amplifier:	$A_v = V_o/V_i = constant$
Current amplifier:	$A_i = I_o/I_i = consantt$
Transconductance amplifier:	$G_m = I_o/V_i = constant$
Transresistance amplifier:	$R_m = V_o/I_i = constant$

Our focus in this course is on voltage amplifiers (we will see a transconductance amplifier).

Voltage amplifiers can be accurately modeled with three circuit elements as shown below. A good voltage amplifier has a large input resistance, R_i, and a small output resistance, R_o. An ideal voltage amplifier has, $R_i \to \infty$ and $R_o \to 0$.



Voltage Amplifier Model

Practical Amplifiers

Real voltage amplifiers differ from the ideal amplifiers. Not only, the input resistance is not infinite and the output resistance is not zero, but the amplifier works properly only in certain conditions. One should always be aware of the range where the circuit acts as a linear (ideal) amplifier, *i.e.,* the output is proportional to the input with the ratio of $A_v = V_o/V_i = constant$ (exactly the same waveform) .

Amplifier Saturation: Amplifiers do not create power. Rather, they act as a "valve" adjusting the power flow from the power supply into the load according to the input signal. As such, the output voltage amplifier cannot exceed the power supply voltage (it is usually lower because of voltage drop across some active elements). The fact that the output voltage of a practical amplifier cannot exceed certain threshold value is called saturation. A voltage amplifier behaves linearly, *i.e.,* $V_o/V_i = A_v = constant$ as long as the output voltage remains below the "saturation" voltage,

$$-V_{sat} < V_o < V_{sat}$$

Note that the saturation voltage, in general, is not symmetric, *i.e.,* $-V_{sat,1} < V_o < V_{sat,2}$.

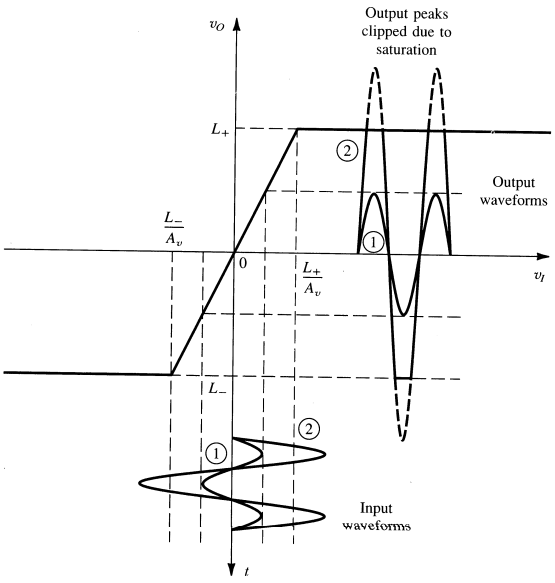
For an amplifier with a given gain, A_v, the above range of V_o translate into a certain range for V_i

$$-V_{sat} < V_o < V_{sat}$$

$$-V_{sat} < A_v V_i < V_{sat}$$

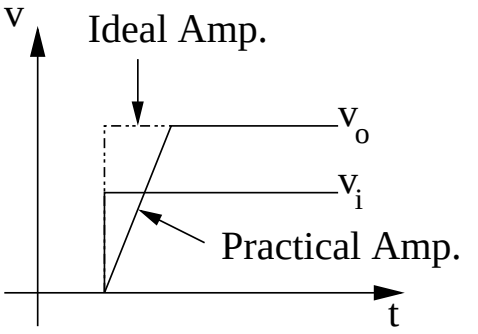
$$-\frac{V_{sat}}{A_v} < V_i < \frac{-V_{sat}}{A_v}$$

i.e., any amplifier will enter its saturation region if V_i is raised above certain limit. The figure shows how the amplifier output clips when amplifier is not in the linear region.



Amplifier Bandwidth: Typically, amplifiers work in a certain range of frequencies. Their gain, $A_v = V_o/V_i$ drops outside this range. The voltage transfer function (gain) of an amplifier is plotted similar to that of filters (Bode plots). It looks similar to those of a band-pass filter or a low-pass filter. Cut-off frequencies and bandwidth of the amplifier is defined similar to those of filters (3 dB drop from the maximum value). In terms of frequency response, voltage amplifiers are divided into two categories. (1) AC amplifiers which only amplify AC signals. Their Bode plots look like a band-pass filter. (2) DC amplifiers which amplify both DC signals and AC signals up to a certain frequency. Their Bode plots look like a low-pass filter. For this class amplifiers, the bandwidth is equal to the cut-off frequency (lower cut-off frequency is set to zero!).

Rise Time: In an ideal amplifier, if the input voltage is a unit step function, the output voltage will also be a unit step function as shown. A practical amplifier cannot change its output instantaneously if the input changes suddenly. It takes some time (a short but finite time) for the amplifier output voltage to reach its nominal level. The maximum rate of change in the output voltage is called the rise time.



Maximum Output Current: Voltage amplifiers are designed to amplify the voltage and not the current. However, nothing prevents a user to attach a small load to the output, drawing a large current. As the load resistance is decreased, the output current of amplifier

is increased. At the certain output current, the output signal of the amplifier does not resemble the input signal. This is due to "maximum output current limitation."

There are other limitations of a practical amplifier such as signal-to-noise ratio, nonlinear distortion, etc. which are out of the scope of this course.

How to measure A_v, R_i, R_o

Measuring A_v is straight forward. Apply a sinusoidal input signal with amplitude V_i to the input, measure the amplitude of the input and output signals (make sure that the amplifier is not in saturation and signal is not clipped), and compute $A_v = V_o/V_i$. Note that A_v is in general depends on frequency. There may also been some phase difference between V_i and V_o similar to filters.

Measuring input and output resistances (or impedances) is not trivial as for a good amplifier R_o is small and R_i is large. Large value of R_i means that the input current I_i is small and is difficult to measure. In this case, the solution is to add a resistance R_1 (measured accurately) in series with the input, measure the voltage across this resistor, V_1, and find the current, $I_i = V_1/R_1$. Obviously R_1 should be large enough such that V_1 can be measured accurately. Typically we have to use $R_1 \sim R_i$.

To measure R_o, we can use the same technique described in page 6 to find the equivalent Thevenin resistance of a circuit. This is the best method as the best fit approximation to several data points, minimizes the measurement error. One can find the output resistance less accurately by doing only two measurements. For a given V_i, (1) Measure V_o in the presence of a very large resistance (*e.g.,* internal resistance of scope). Call this V_{oc}. From the amplifier model of previous page,

$$V_o = AV_i = V_{oc}$$

Next, measure V_o with an accurately measured R_L. Using the amplifier model of page 28, we have

$$\frac{V_o}{AV_i} = \frac{R_L}{R_L + R_o} \qquad \rightarrow \qquad \frac{V_o}{V_{oc}} = \frac{R_L}{R_L + R_o}$$

$$\frac{R_o}{R_L} = \frac{V_{oc}}{V_o} - 1$$

Obviously, we have to choose R_L such that V_o/V_{oc} is sufficiently different from 1 (at least by 10 times of the measurement accuracy).

In some cases, we cannot reduce R_L to a low enough level such that V_{oc}/V_o is sufficiently different from 1. This is due to the maximum output current limitation (we will revisit this for OpAmps). In such cases, we can still find a "bound" for R_o. Suppose R_L is the smallest resistance that we can use and get the desired output and at this value of R_L, $V_{oc} \approx V_o$. If the relative measurement error is ϵ, then:

$$V_o|_{real} \leq V_o|_{measured}\,(1 \pm \epsilon) \qquad V_{oc}|_{real} \leq V_{oc}|_{measured}\,(1 \pm \epsilon)$$

$$\frac{V_o}{V_{oc}}\Big|_{real} \leq 1 \pm 2\epsilon$$

$$\frac{R_o}{R_L} \leq 2\epsilon \qquad \rightarrow \qquad R_o \leq 2\epsilon R_L$$

So, for example, if the accuracy of the scope is 3% and the minimum R_L we could use was 1 kΩ, the bound for $R_o \leq 2 \times 0.03 \times 1000 = 60\ \Omega$.

Feedback

Not only a good amplifier should have sufficient gain, its performance should be insensitive to environmental and manufacturing conditions, should have a large R_i, a small R_o, a sufficiently large bandwidth, *etc.* It is easy to make an amplifier with a very large gain. A typical transistor circuit can easily have a gain of 100 or more. A three-stage transistor amplifier can easily get gains of 10^6. Other characteristics of a good amplifier is hard to achieve. For example, the β of a BJT changes with operating temperature making the gain of the three-stage amplifier vary widely. The system can be made to be insensitive to environmental and manufacturing conditions by the use of feedback. Feedback also helps in other regards.

Principle of feedback: The input to the circuit is modified by "feeding" a signal proportional to the output value "back" to the input. There are two types of feedback (remember the example of a car in the freeway discussed in the class):

1. Negative feedback: As the output is increased, the input signal is decreased and *vice versa.* Negative feedback stabilizes the output to the desired level. Linear system employs negative feedback.

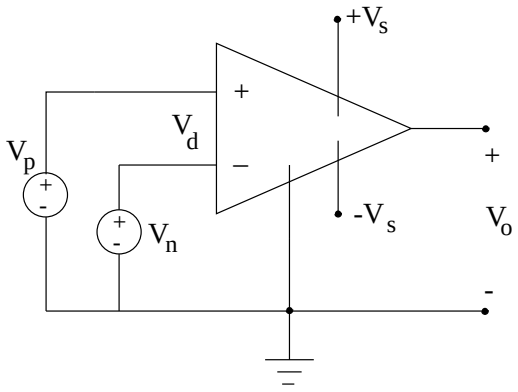
2. Positive feedback: As the output is increased, the input signal is increased and *vice versa.* Positive feedback leads to instability. (But, it has its uses!)

We will explore the concept of feedback in the context of operational amplifiers.

OpAmps as linear amplifiers

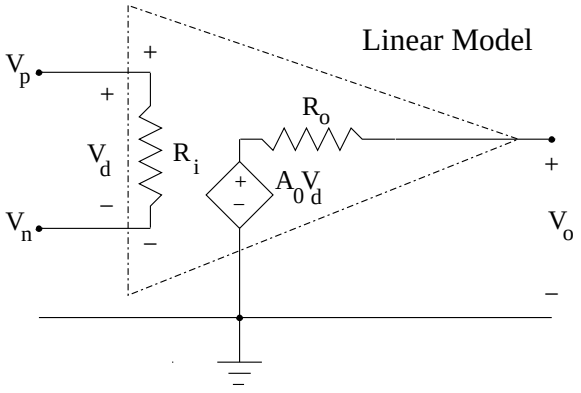
Operational amplifiers (OpAmps) are general purpose voltage amplifiers employed in a variety of circuits. OpAmps are "DC" amplifiers with a very large gain, A_0 (10^5 to 10^6), high input impedance ($> 1-10$ MΩ), and low output resistance ($< 100\ \Omega$). They are constructed as a "difference" amplifier, *i.e.,* the output signal is proportional to the difference between the two input signals.

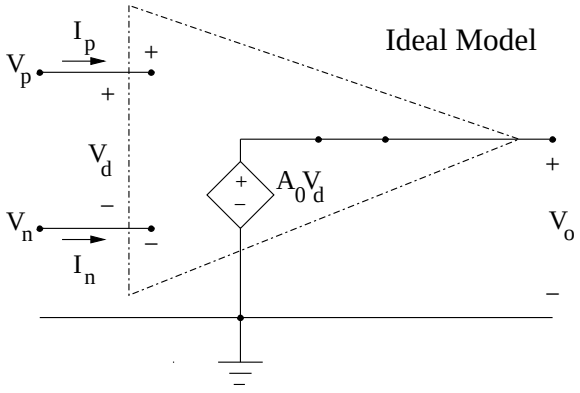
$$V_o = A_0 V_d = A_0(V_p - V_n)$$



V_s and $-V_s$ are power supply attachments. They set the saturation voltages for the OpAmp circuit (within 0.2 V). Power supply ground should also be connected to the OpAmp ground. + and − terminals of the OpAmp are called, respectively, non-inverting and inverting terminals.

OpAmp Models



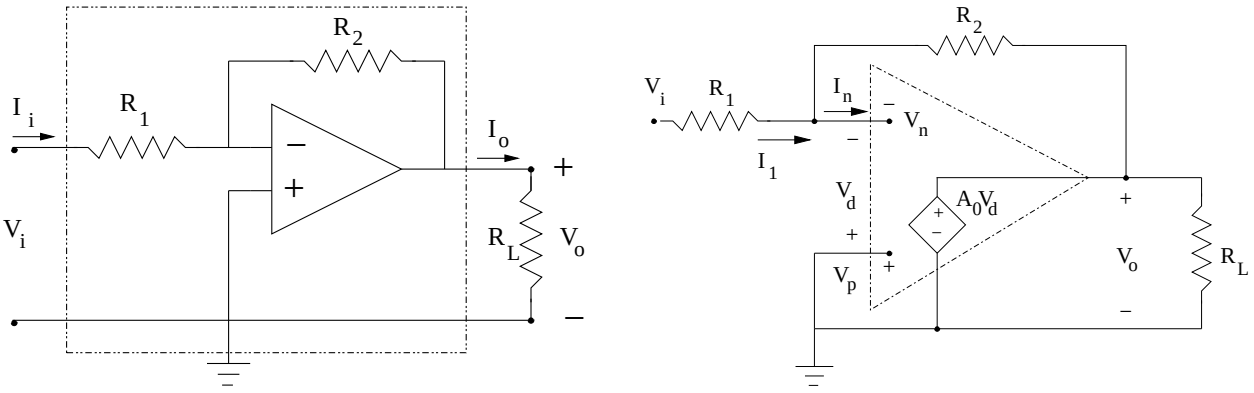


Because R_i is very large and R_o is very small, ideal model of the OpAmp assumes $R_i \to \infty$ and $R_o \to 0$. Ideal model is usually a very good model for OpAmp circuits. Very large input resistance also means that the input current into an OpAmp is very small:

First Golden Rule of OpAmps: $I_p \approx I_n \approx 0$ (Also called "Virtual Open Principle")

An important feature of OpAmp is that because the gain is very high, the OpAmp will be in the saturation region without negative feedback. For example, take an OpAmp with a gain of 10^5 and $V_{sat} = 15$ V. Then, for OpAmp to be in linear region, $V_i \leq 15 \times 10^{-5} = 150\ \mu$V (a very small value). OpAmps are never used by themselves. They are always part of a circuit which employ either negative feedback (*e.g.,* linear amplifiers, active filters) or positive feedback (*e.g.,* comparators). Examples below shows several OpAmp circuits with negative feedback.

Inverting Amplifier



The first step in solving OpAmp circuits is to replace the OpAmp with its circuit model (ideal model is usually very good).

$$V_p = 0, \qquad V_o = A_0 V_d = A_0(V_p - V_n) = -A_0 V_n$$

Using node-voltage method and noting $I_n \approx 0$:

$$\frac{V_n - V_i}{R_1} + \frac{V_n - V_o}{R_2} = 0$$

Substituting for $V_n = -V_o/A_0$ and multiplying the equation by R_2, we have:

$$-\frac{R_2}{A_0 R_1} V_o - \frac{R_2}{R_1} V_i - \frac{V_o}{A_0} - V_o = 0 \qquad \rightarrow \qquad V_o \left[1 + \frac{1}{A_0} + \frac{R_2}{A_0 R_1}\right] = -\frac{R_2}{R_1} V_i$$

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \frac{1}{1 + \dfrac{1}{A_0} + \dfrac{R_2}{A_0 R_1}}$$

Since OpAmp gain is very large, $1/A_0 \ll 1$. Also if R_2 and R_1 are chosen such that their ratio is not very large, $R_2/R_1 \ll A_0$ or $R_2/(A_0 R_1) \ll 1$, then the voltage transfer function of the OpAmp is

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

The circuit is called an inverting amplifier because the voltage transfer function is "negative." (A "negative" sinusoidal function looks inverted.) The negative sign means that there is 180° phase shift between input and output signals.

Note that the voltage transfer function is "independent" of the OpAmp gain, A_0, and is only set by the values of the resistors R_1 and R_2. While A_0 is quite sensitive to environmental and manufacturing conditions (can very by a factor of 10 to 100), the resistor values are quite insensitive and, thus, the gain of the system is quite stable. This stability is achieved by negative feedback, the output of the OpAmp is connected via R_2 to the inverting terminal of OpAmp. If V_o increases, this resistor forces V_n to increase, reducing $V_d = V_p - V_n$ and $V_o = A_0 V_d$, and stabilizes the OpAmp output.

An important feature of OpAmp circuits with negative feedback is that because the OpAmp is NOT saturated, $V_d = V_o/A_0$ is very small (because A_0 is very large). As a result,

$$\text{Negative Feedback} \quad \rightarrow \quad V_d \approx 0 \quad \rightarrow \quad V_n \approx V_p$$

Second Golden Rule of OpAmps: For OpAmps circuits with negative feedback, the OpAmp adjusts its output voltage such that $V_d \approx 0$ or $V_n \approx V_p$ (also called "Virtual Short Principle"). This rule is derived by assuming $A \rightarrow \infty$. Thus, V_o cannot be found from $V_o = A_0 v_d = \infty \times 0 =$ indefinite value. The virtual short principle replace $V_o = A_0 v_d$ expression with $V_d \approx 0$.

The above rule simplifies solution to OpAmp circuits dramatically. For example, for the inverting amplifier circuit above, we will have:

$$\text{Negative Feedback} \quad \rightarrow \quad V_n \approx V_p \approx 0$$

$$\frac{V_n - V_i}{R_1} + \frac{V_n - V_o}{R_2} = 0 \quad \rightarrow \quad \frac{V_i}{R_1} + \frac{V_o}{R_2} = 0 \quad \rightarrow \quad \frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

Input and Output resistances of inverting amplifier configuration: From the circuit,

$$I_i = \frac{V_i - 0}{R_1} \quad \rightarrow \quad R_i = \frac{V_i}{I_i} = R_1$$

The input impedance of the inverting amplifier circuit is R_1 (although input impedance of OpAmp is infinite).

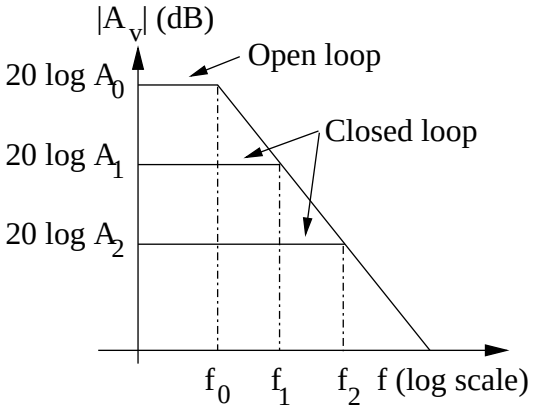
The output impedance of the circuit is "zero" because V_o is independent of R_L (V_o does not change when R_L is changed).

Amplifier Bandwidth:

The voltage gain for the inverting amplifier is $-R_2/R_1$ and is independent of frequency–same gain for a DC signal ($\omega \rightarrow 0$) as for high frequencies. However, this voltage gain has been found using an ideal OpAmp model (ideal OpAmp parameters are independent of frequency).

A major concern for any amplifier circuit is its stability (which you will study in depth in junior and senior courses). Basically, any amplifier circuit produce a phase-shift in the output voltage. Once the phase shift becomes smaller than -180° (more negative), negative feedback becomes positive feedback. The amplifier gain should be less than 1 at these frequencies for stable operation. In a practical OpAmp, the open loop gain, A_0, is usually very large, ranging 10^5 to 10^6. To reduce the gain at high frequencies and avoid instability, the voltage gain (or voltage transfer function) of a practical OpAmp looks like a low-pass filter as shown (marked by open loop meaning no feedback). This is achieved by an adding of a relatively large capacitor in the OpAmp circuit chip (internally compensated OpAmps) or by providing for connection of such a capacitor outside the chip (uncompensated OpAmp). In order for the OpAmp gain to become smaller than 1 at high frequencies, the open-loop bandwidth, f_0 (which is the same as cut-off frequency) is usually small (10 to 100 Hz, typically).

Recall the inverting amplifier circuit discussed above. In that circuit, the voltage transfer function was independent of A_0 as long as $R_2/R_1 \ll A_0$. But R_2/R_1 is the iverting amplifier circuit gain (call it $A_1 = |V_o/V_i| = R_2/R_1$). Thus, the negative feedback worked as long as $A_1 \ll A_0$. Since A_0 decreases at higher frequencies, one will encountered a frequency, above which $A_1 = R_2/R1 \ll A_0$ is violated (See figure for closed-loop). Below this frequency, the amplifier gain is independent of frequency while above that frequency, we revert back to the open-loop gain curve. One can show that:



$$A_0 f_0 = A_1 f_1 = f_u = constant$$

Therefore, the product of the gain and bandwidth (which the same as the cut-off frequency) of the "amplifier circuit" is a constant and is equal to the product of open-loop gain and open-loop bandwidth. This product is given in manufacturer spec sheet for each OpAmp and sometimes is denoted as "unity gain bandwidth," f_u. Note that gain in the expression above is NOT in dB, rather it is the value of $|V_o/V_i|$.

How to solve OpAmp circuits:

1) Replace the OpAmp with its circuit model.
2) Check for negative feedback, if so, write down $V_p \approx V_n$.
3) Solve. Best method is usually node-voltage method. You can solve simple circuits with KVL and KCLs. Do not use mesh-current method.

Physical Limitations of OpAmps

OpAmps, like other voltage amplifiers, behave linearly only under certain conditions (see page 28-29). Several limitations of OpAmp circuits are discussed before.

1. Voltage-supply limit or Saturation: $v_s^- < v_o < v_s^+$ which limits the maximum output voltage (or a for a given gain, limits the maximum input voltage). If an amplifier is saturated, one can recover the linear regime by reducing the input amplitude.

2. Frequency Response limit: A practical amplifier has a finite bandwidth. For OpAmps circuits with negative feedback, one can trade gain with bandwidth:

$$A_0\omega_0 = A\omega \quad \text{or} \quad A_0 f_0 = Af = f_u$$

Note that gain in the expression above is NOT in dB, rather it is the value of $|V_o/V_i|$.

3. Maximum output current limit: A voltage amplifier model (OpAmp also) includes a controlled voltage source in its output circuit. This means that for a given input signal, this controlled source will have a fixed voltage independent of the current drawn from it. If we attach a load to the circuit and start reducing the load resistance, the output voltage remains a constant and load current will increase. Following this model, one could reduce the load resistance to a very small value and draw a very large current from the amplifier.

In reality, this does not happen. Each voltage amplifier has a limited capability in providing output current. This maximum output current limit is also called the "Short-Circuit Output Current," I_{SC}. If one tries to exceed this current limit, the voltage amplifier will not behave linearly; the output current will not increase, rather the current stays constant and the output voltage and the gain will decrease.

If the a fixed load resistance, R_L, is connected to the amplifier, the maximum output current means that the output voltage cannot exceed the $R_L I_{SC}$:

$$-R_L I_{SC} \leq v_o \leq R_L I_{SC}$$

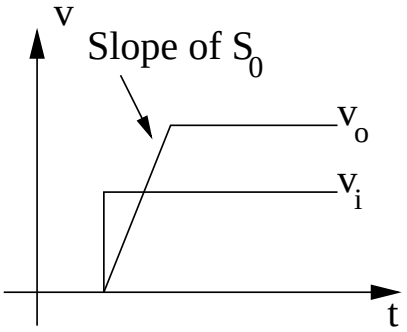
In this case, the maximum output current limit manifests itself in a form similar to amplifier saturation. The output voltage waveform will be clipped at value of $R_L I_{SC}$. Two options are available to avoid the maximum current limit: (1) Increasing R_L as is seen from the above equation, (2) decreasing v_o by decreasing the input amplitude.

Note: The maximum output current of the OpAmp amplifier configuration is NOT the same as the maximum output current of the OpAmp itself. For example in the inverting amplifier configuration, the maximum output current of the amplifier is smaller than I_{SC} of OpAmp because OpAmp has to supply current to both the load (maximum output current of amplifier configuration itself) and the feedback resistor R_2.

4. Slew rate (Rise Time):

If input changes suddenly, the OpAmp cannot change its output instantaneously. The maximum rate of change of the output of an OpAmp is called the "slew rate" (given usually in the units of V/μs):

$$S_0 \equiv \left.\frac{dv_o}{dt}\right|_{Max}$$



Slew rate affects all signals (not limited to square waves). For example, at high enough frequency and/or at high enough amplitude, a sinusoidal input turns into a triangular output signal. As an example, consider an inverting amplifier with a gain of $A = 10$, build with an OpAmp with a slew rate of $S_0 = 1$ V/μS. The input is a sinusoidal wave with an amplitude of $V_i = 1$ V and frequency of ω.

$$v_i = V_i \cos(\omega t) \quad \rightarrow \quad v_o = -AV_i \cos(\omega t)$$

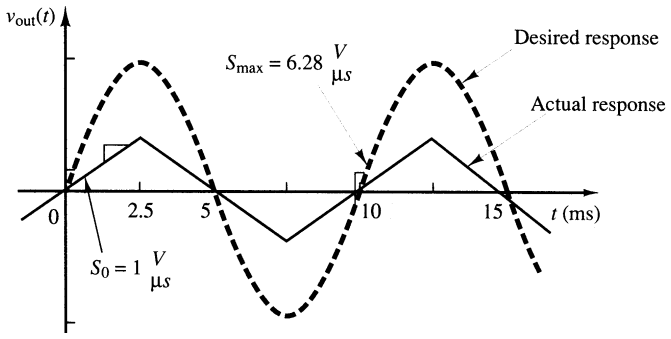
$$\frac{dv_o}{dt} = +AV_i\omega \sin(\omega t) \quad \rightarrow \quad \left.\frac{dv_o}{dt}\right|_{Max} = AV_i\omega$$

The slew rate limit means that

$$\left.\frac{dv_o}{dt}\right|_{Max} = AV_i\omega \leq S_0$$

For the example above, $V_i = 1$ V, $A = 10$, and $S_0 = 1$ V/μS, we have

$$\left.\frac{dv_o}{dt}\right|_{Max} = 10\omega \leq 10^6 \quad \rightarrow \quad \omega \leq 10^5$$



Which means that at frequencies above 10^5 rad/s, the output will depart from a sinusoidal signal due to the slew rate limit. Because for the sinusoidal wave, the slew rate limit is in the form $AV_i\omega \leq S_0$, one can avoid this nonlinear behavior by either decreasing the frequency, or by lowering the amplifier gain, or reducing the input signal amplitude.

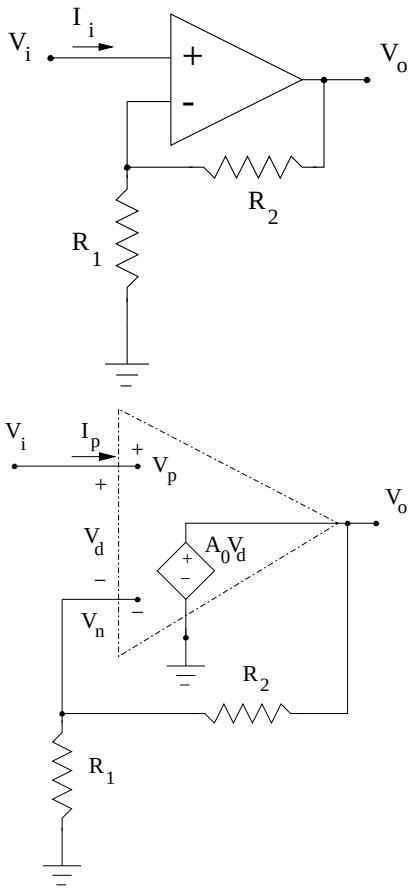
5. Other limits: OpAmps have other physical limitations such as Input offset voltage, Input bias current, and Common-mode reject ratio (CMMR). Consult Rizzoni for a description of these limitations.

Non-inverting Amplifier

$$V_p = V_i$$

$$\text{Negative Feedback} \quad \rightarrow \quad V_n \approx V_p = V_i$$

$$\frac{V_n - 0}{R_1} + \frac{V_n - V_o}{R_2} = 0$$



Note that you should not write a node equation at OpAmp output as its a node attached to a voltage source. The value of V_o is AV_d and is indefinite. Instead of using this equation, we use $V_d \approx 0$ as was discussed in page 34.

Substituting for $V_n = V_i$, we get

$$\frac{R_2}{R_1} V_i + V_i - V_o = 0$$

$$\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

Input Resistance:
$I_i = I_p = 0$. Therefore, $R_i \rightarrow \infty$.

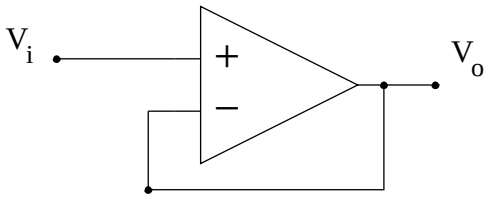
Output Resistance:
V_o is independent of R_L, so $R_o = 0$.

Note that $R_i \rightarrow \infty$ and $R_o = 0$ should be taken in the context that we are using an "ideal" OpAmp model. In reality, the above circuit will have input and output resistances equal to that of the OpAmp itself.

Voltage Follower

In some cases, we have two-terminal networks which do not match well, *i.e,* the input impedance of the later stage is not very large, or the output impedance of preceding stage is not low enough. A "buffer" circuit is usually used in between these two circuits to solve the matching problem. These "buffer" circuit typically have a gain of 1 but have a very large input impedance and a very small output impedance. Because their gains are 1, they are also called "voltage followers."

The non-inverting amplifier above has $R_i \rightarrow \infty$ and $R_o = 0$ and, therefore, can be turned into a voltage follower (buffer) by adjusting R_1 and R_2 such that the gain is 1.



$$\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1} = 1 \quad \rightarrow \quad R_2 = 0$$

So by setting $R_2 = 0$, we have $V_o = V_i$ or a gain of unity. We note that this expression is valid for any value of R_1. As we want to minimize the number of components in a circuit as a rule (cheaper circuits!) we set $R_1 = \infty$ (open circuit) and remove R_1 from the circuit.

Inverting Summer

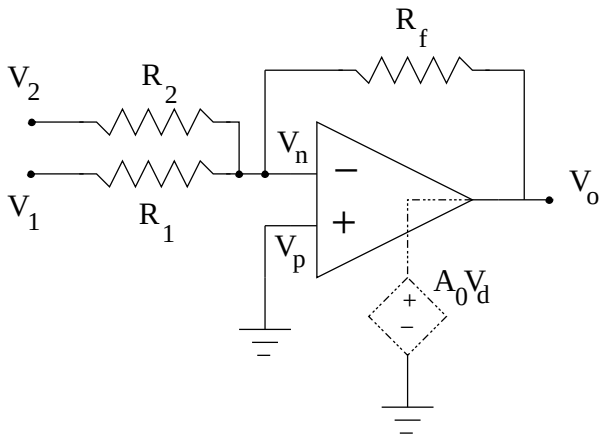
$V_p = 0$

Negative Feedback: $V_n \approx V_p = 0$

$$\frac{V_n - V_1}{R_1} + \frac{V_n - V_2}{R_2} + \frac{V_n - V_o}{R_f} = 0$$

$$V_o = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2$$

So, this circuit adds (sums) two signals. An example of the use of this circuit is to add a DC offset to a sinusoidal signal.



Non-Inverting Summer

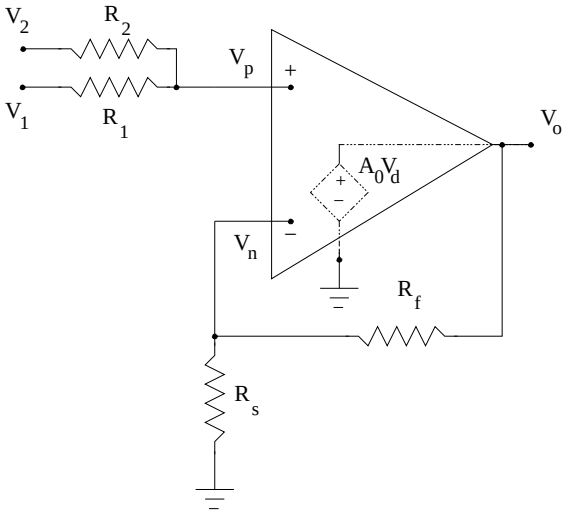
Negative Feedback: $V_n \approx V_p$

$$\frac{V_p - V_1}{R_1} + \frac{V_p - V_2}{R_2} = 0 \quad \longrightarrow$$

$$V_p\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{V_1}{R_1} + \frac{V_2}{R_2}$$

$$\frac{V_n - 0}{R_s} + \frac{V_n - V_o}{R_f} = 0 \longrightarrow$$

$$V_o = \left(1 + \frac{R_f}{R_s}\right)V_n$$

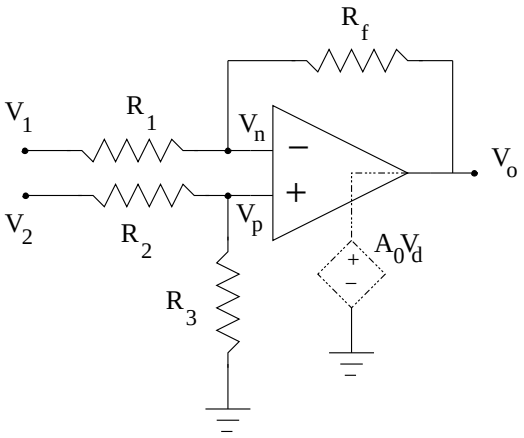


Substituting for V_n in the second equation from the first (noting $V_p = V_n$):

$$V_o = \frac{1 + R_f/R_s}{1/R_1 + 1/R_2}\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

So, this circuit also signal adds (sums) two signals. It does not, however, inverts the signals.

Difference Amplifier



Negative Feedback: $V_n \approx V_p$

$$\frac{V_p - V_2}{R_2} + \frac{V_p - 0}{R_3} = 0 \quad \longrightarrow$$

$$V_n \approx V_p = \frac{R_3}{R_2 + R_3} V_2$$

$$\frac{V_n - V_1}{R_1} + \frac{V_n - V_o}{R_f} = 0$$

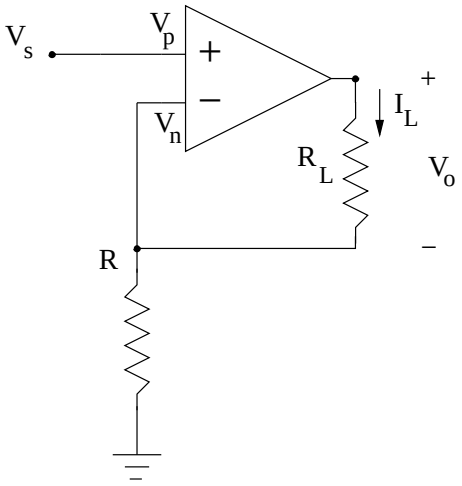
Substituting for V_n in the 2nd equation, one can get:

$$V_o = -\frac{R_f}{R_1} V_1 + \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}\right) V_2$$

If one choose the resistors such that $\frac{R_3}{R_2} = \frac{R_f}{R_1}$, then

$$V_o = \frac{R_f}{R_1}(V_2 - V_1)$$

Current Source



Negative Feedback: $V_n \approx V_p = V_s$

$$i_L = \frac{V_n}{R} = \frac{V_s}{R} = constant$$

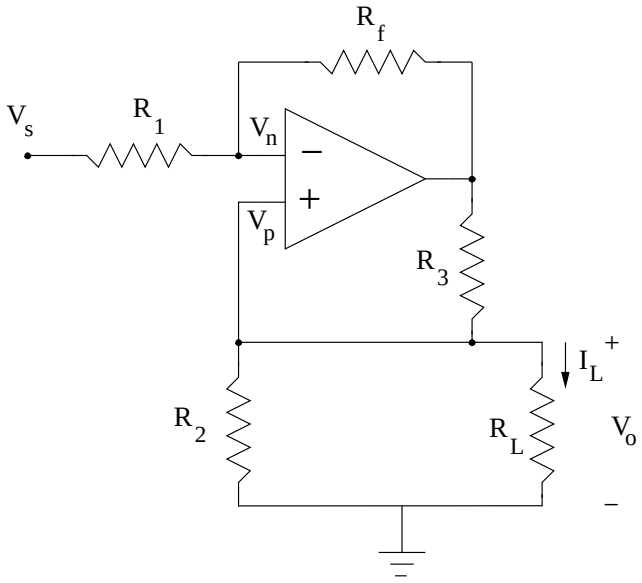
For a fixed value of V_s, the current I_L is independent of value of R_L and output voltage V_o. As such, this circuit is an independent current source.

The value of the current can be adjusted by changing V_s (for a fixed R_L. Therefore, this circuit is also a "voltage to current" converter or a "transconductance" amplifier.

Grounded Current Source

The problem with the above current source is that the load is not grounded. This may not be desirable in some cases. This circuit here is also a current source with a grounded load.

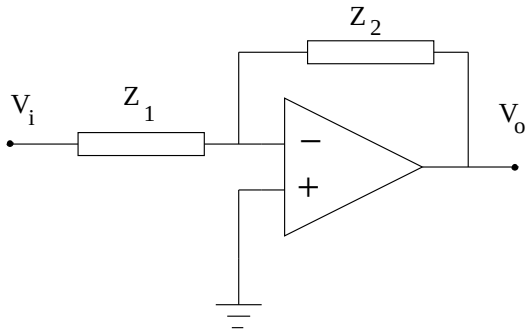
Question: Compute I_L and show that it is independent of R_L.



Active Filters, Integrators & Differentiators

Consider the circuit shown. This is an inverting amplifier with impedances instead of resistors. Following the inverting amplifier solution, we find:

$$H(j\omega) = \frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$



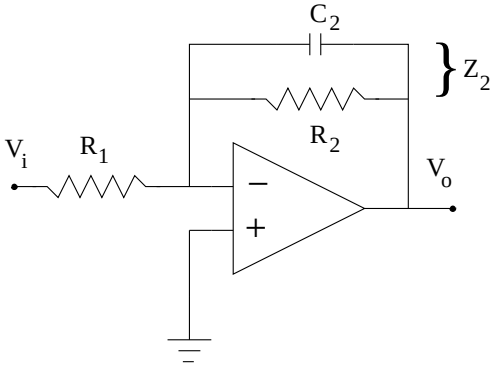
Various filter circuits can be made with different choices for Z_1 and Z_2:

1st Order Low-Pass Filter:

$$Z_1 = R_1$$

$$Z_2 = R_2 \parallel C_2 = \frac{R_2}{1 + j\omega C_2 R_2}$$

$$H(j\omega) = -\frac{Z_2}{Z_1} = -\frac{R_2/R_1}{1 + j\omega C_2 R_2}$$



Compare the above voltage transfer function with the general expression for a 1st order low-pass filter:

$$H(j\omega) = \frac{K}{1 + j\omega/\omega_c}$$

We find that the above circuit is a low pass filter with

$$K = -\frac{R_2}{R_1} \qquad \text{and} \qquad \omega_c = \frac{1}{R_2 C_2}$$

The minus sign in front of K indicates an additional $-180°$ phase shift. A low-pass RC or RL filter has a phase shift of $0°$ at low frequencies and $-90°$ at high frequencies. The above amplifier has a phase shift of $-180°$ at low frequencies and $-270°$ at high frequencies (or alternatively $+180°$ at low frequencies and $+90°$ at high frequencies as we can add $360°$ to the phase angle). Another difference with passive RC or RL filters is that the gain, $K = R_2/R_1$ can be set to be larger than one (*i.e.,* amplify the signals in the pass band). As such this kind of filters are called "active filters."

Input Resistance: $R_i = R_1$.

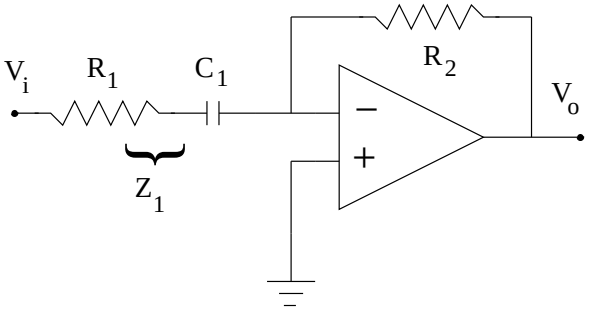
Output Resistance: $R_o = 0$ (OpAmp output resistance).

1st Order High-Pass Filter:

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = R_1\left(1 - j\frac{1}{\omega C_1 R_1}\right)$$

$$Z_2 = R_2$$

$$H(j\omega) = -\frac{Z_2}{Z_1} = -\frac{R_2/R_1}{1 - j\dfrac{1}{\omega C_1 R_1}}$$



Comparing the above voltage transfer function with the general expression for a 1st order high-pass filter,

$$H(j\omega) = \frac{K}{1 - j\omega_c/\omega}$$

We find that the above circuit is a high-pass filter with

$$K = -\frac{R_2}{R_1} \qquad \text{and} \qquad \omega_c = \frac{1}{R_1 C_1}$$

Again, the minus sign in K indicates an additional $-180°$ phase shift. A high-pass RC or RL filter has a $90°$ at low frequencies and $0°$ at high frequencies. The above amplifier has a phase shift of $-90°$ at low frequencies and $-180°$ at high frequencies.

Input Resistance: $R_i = Z_1$ and $R_i|_{min} = R_1$.

Output Resistance: $R_o = 0$ (OpAmp output resistance).

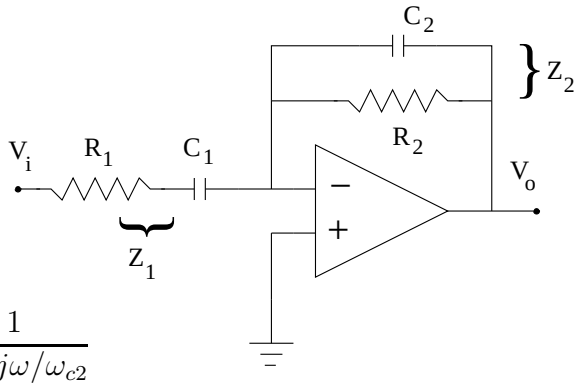
2nd Order Band-Pass Filter:

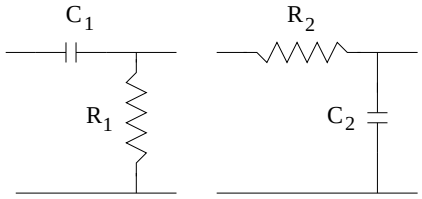
$$Z_1 = R_1 + \frac{1}{j\omega C_1} = R_1\left(1 - j\frac{1}{\omega C_1 R_1}\right)$$

$$Z_2 = R_2 \parallel C_2 = \frac{R_2}{1 + j\omega C_2 R_2}$$

Defining $\omega_{c1} = \dfrac{1}{R_1 C_1}, \quad \omega_{c2} = \dfrac{1}{R_2 C_2}$

$$H(j\omega) = -\frac{Z_2}{Z_1} = -\frac{R_2}{R_1} \times \frac{1}{1 - j\omega_{c1}/\omega} \times \frac{1}{1 + j\omega/\omega_{c2}}$$





As can be seen, the voltage transfer function looks like a high-pass and a low-pass filter put together (a wide-band, band-pass filter).

To find the cut-off frequencies, bandwidth, etc. of this filter, it is simplest to write $H(j\omega)$ in the form similar to the general form for 2nd order band-pass filters:

$$H(j\omega) = \frac{K}{1 + jQ\left(\dfrac{\omega}{\omega_0} - \dfrac{\omega_0}{\omega}\right)}$$

To do so, we rearrange the terms in the expression for $H(j\omega)$ of the above filter to get: (Trick is to make the denominator of $H(j\omega)$ to look like $1 + j...$)

$$H(jw) = -\frac{R_2}{R_1} \times \frac{1}{1 + \dfrac{\omega_{c1}}{\omega_{c2}} + j\left(\dfrac{\omega}{\omega_{c2}} - \dfrac{\omega_{c1}}{\omega}\right)} = \frac{-\dfrac{R_2/R_1}{1 + \omega_{c1}/\omega_{c2}}}{1 + j\left(1 + \dfrac{\omega_{c1}}{\omega_{c2}}\right)^{-1}\left(\dfrac{\omega}{\omega_{c2}} - \dfrac{\omega_{c1}}{\omega}\right)}$$

We compare the above expression with the general form for 2nd order band-pass filters. The two equations should be identical for all value of ω. Thus:

$$K = -\frac{R_2/R_1}{1 + \omega_{c1}/\omega_{c2}}$$

$$\frac{Q}{\omega_0} = \left(1 + \frac{\omega_{c1}}{\omega_{c2}}\right)^{-1} \times \frac{1}{\omega_{c2}} \qquad \text{and} \qquad Q\omega_0 = \left(1 + \frac{\omega_{c1}}{\omega_{c2}}\right)^{-1} \times \omega_{c1}$$

The last two equations should be solved to find Q and ω_0:

$$\omega_0 = \sqrt{\omega_{c1}\omega_{c2}} \qquad \text{and} \qquad Q = \frac{\omega_0}{\omega_{c2} - \omega_{c1}}$$

Values of band-width, B, and upper and lower cut-off frequencies can then be calculated from ω_0 and Q values above (see pages 20 and 21).

For a **wide-band** band-pass filter, expressions for K, Q, and ω_0 simplify considerably:

$$\frac{\omega_{c1}}{\omega_{c2}} \ll 1 \quad \rightarrow \quad K \approx -\frac{R_2}{R_1}, \quad Q \approx \sqrt{\frac{\omega_{c1}}{\omega_{c2}}}, \quad \omega_u \approx \omega_{c2} = \frac{1}{R_2 C_2}, \quad \omega_l \approx \omega_{c1} = \frac{1}{R_1 C_1}$$

Note that $-$ sign in K signifies an additional -180° phase shift.

Question: Computer R_i and R_o of the above filter.

The above procedure can be used for any order filter. For 2nd order, band-pass filters, an alternative method exists that sometimes leads to less algebra. Consider the general form of 2nd-order band-pass filters:

$$H(j\omega) = \frac{K}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}$$

The following observation can made: 1) $H(j\omega = \omega_0)$ is purely real (the imaginary part in the denominator is exactly zero). This can be used to find ω_0, 2) $H(j\omega = \omega_0) = K$. This can be used to find K. 3) At very low frequencies, $H(j\omega \rightarrow 0) \approx -jK\omega/(Q\omega_0)$. This can be used to find Q. The first two steps are shown below.

Using the expression for $H(j\omega)$ of our 2nd-order active bandpass-filter from previous page, we note that $H(j\omega)$ is purely real when

$$\frac{\omega}{\omega_{c2}} - \frac{\omega_{c1}}{\omega} = 0 \qquad \rightarrow \qquad \omega = \omega_0 = \sqrt{\omega_{c1}\omega_{c2}}$$

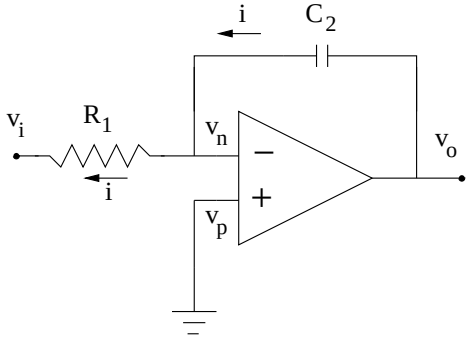
Next, calculating $H(j\omega = \omega_0)$, we get:

$$H(j\omega = \omega_0) = K = -\frac{R_2/R_1}{1 + \omega_{c1}/\omega_{c2}}$$

Important Note: In the analysis of active filters using OpAmps, we have assumed an ideal OpAmp with an infinite bandwidth. In principle, one should include the fact that OpAmp gain will drop at high frequencies. Alternatively, one can assume an ideal OpAmp in the analysis if the bandwidth of the OpAmp is at least ten times larger than the highest frequency of interest. The bandwidth of the OpAmp should be calculated based on the gain of the circuit, K.

Integrator

In the integrator and differentiator circuits below, the input is assumed to be an arbitrary function of time (it does not have to be a sinusoidal function). Voltages and currents are written in lower case to remind you of this fact.



Negative feedback $\rightarrow$ $v_p = v_n = 0$

$$i = C_2 \frac{dv_c}{dt} = C_2 \frac{d(v_o - v_n)}{dt} = C_2 \frac{dv_o}{dt}$$

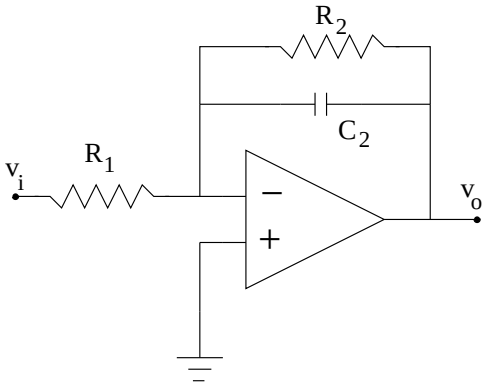
Also, $$i = \frac{v_n - v_i}{R_1} = -\frac{v_i}{R_1}$$

Thus: $$-\frac{v_i}{R_1} = C_2 \frac{dv_o}{dt} \quad \rightarrow \quad \frac{dv_o}{dt} = -\frac{1}{R_1 C_2} v_i$$

$$v_o(t) - v_o(0) = -\frac{1}{R_1 C_2} \int_0^t v_i(t')dt'$$

So the output of this circuit is proportional to the integral of the input.

Examples of use of such circuit include making a triangular wave from a square wave (as is done in the function generator), charge amplifiers, and analog computers (see Rizzoni for these circuits).



The problem with this circuit is that it is too good! It integrates everything including noise. Low frequency noise is a considerable problem because even small DC inputs are integrated rapidly, increasing v_o, and saturating the OpAmp. Solution is to add a resistor R_2 parallel to C_2 that discharges the capacitor in long times, getting rid of integrated DC noise. The value of the resistor is chosen such that the time constant of this RC circuit $\tau = R_2 C_2$ is about 100 times the period of the lowest frequency signal of interest. Addition of R_2 makes the circuit look like a low-pass filter.

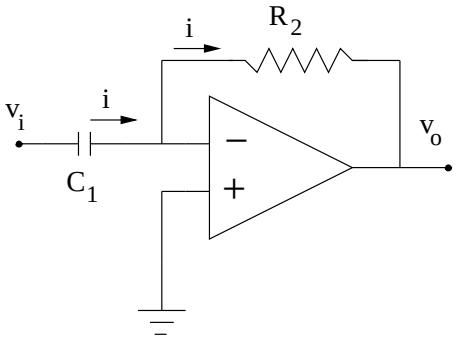
Differentiator

Negative feedback $\rightarrow$ $v_p = v_n = 0$

$$i = C_1 \frac{dv_c}{dt} = C_1 \frac{d(v_i - v_n)}{dt} = C_1 \frac{dv_i}{dt}$$

Also, $$i = \frac{v_n - v_o}{R_2} = -\frac{v_o}{R_2}$$

Thus: $$v_o(t) = -R_2 C_1 \frac{dv_i}{dt}$$

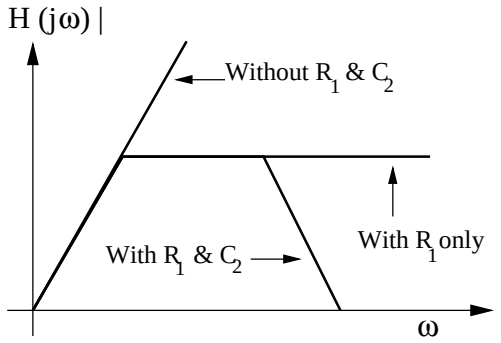


So the output of this circuit is proportional to the derivative of the input.

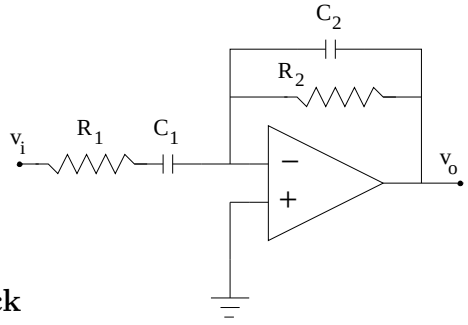
In practice, this circuit does not work as advertised. The problem can be seen by assuming that the input is a sinusoidal wave and finding the transfer function for the circuit:

$$H(j\omega) = \frac{V_o}{V_i} = -\frac{R_2}{1/(j\omega C_1)} = -j\omega R_2 C_1$$

As can be seen when ω becomes large, V_o becomes large (because of derivative of $\cos \omega t = -\omega \sin(\omega t)$). So, practically, this circuit is not a differentiator, rather it is a "high-frequency-noise amplifier." Bode plots of $H(j\omega)$ shows that the transfer function is a line with a slope of +6 dB/octave.



The solution is to attenuate the amplitude of high-frequency signals by adding a resistance R_1 in series with C_1. At low frequencies, C_1 dominate and the circuit is a differentiator. At high frequencies, R_1 dominates and the circuit becomes a simple amplifier.



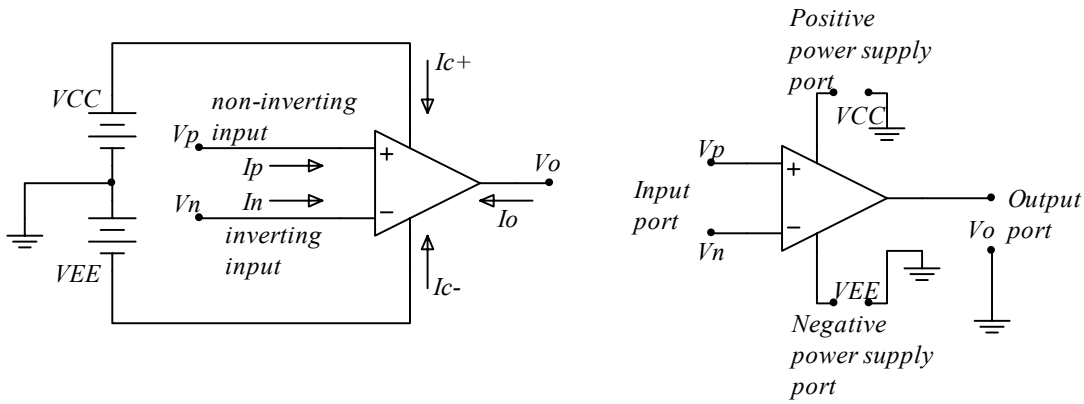
Stability of OpAmp circuits with negative feedback

As noted before, the OpAmp gain has a negative phase shift at high frequencies. If the closed-loop gain is greater than 1 when OpAmp phase shift becomes smaller than $-180°$ (becomes more negative), negative feedback becomes positive feedback and the circuit becomes unstable. Stability of feedback amplifiers will be discussed next year in the breadth courses (such as ECE102). Both active high-pass filter and differentiator circuits above are specially susceptible to this problem because of the raise in the gain at low frequencies. If a circuit encounters this problem (specially for uncompensated OpAmps), the solution is to add a capacitor C_2 to the circuit as shown to make the circuit look like a band-pass filter attenuating the high-frequency signals. For the differentiator circuit above, value of C_2 is chosen such that the circuit gain is less than 1 when phase shift is 180°.

Operational Amplifiers

Introduction

The operational amplifier (op-amp) is a voltage controlled voltage source with very high gain. It is a five terminal four port active element. The symbol of the op-amp with the associated terminals and ports is shown on Figure 1(a) and (b).



(a) (b)

Figure 1. Symbol and associated notation of op-amp

The power supply voltages *VCC* and *VEE* power the operational amplifier and in general define the output voltage range of the amplifier. The terminals labeled with the "+" and the "-" signs are called non-inverting and inverting respectively. The input voltage *Vp* and *Vn* and the output voltage *Vo* are referenced to ground.

The five terminals of the op-amp form one (complicated) node and if the currents are defined as shown on Figure 1(a) the KCL requires that

$$In + Ip + Ic_{+} + Ic_{-} + Io = 0 \tag{1.1}$$

Therefore for current balance we must include all currents. This is what defines an active element. If we just consider the signal terminals then there is no relationship between their currents. In particular,

$$In + Ip + Io \neq 0 \tag{1.2}$$

The equivalent circuit model of an op-amp is shown on Figure 2. The voltage *Vi* is the differential input voltage $Vi = Vp - Vn$. *Ri* is the input resistance of the device and *Ro* is the output resistance. The gain parameter A is called the open loop gain. The open loop

configuration of an op-amp is defined as an op-amp circuit without any circuit loops that connect the output to any of the inputs. inputs.

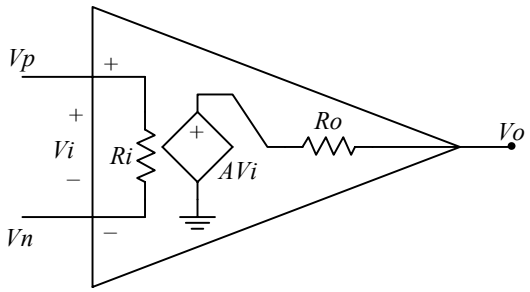


Figure 2. Equivalent circuit model of op-amp device

In the absence of any load at the output, the output voltage is

$$Vo = AVi = A(Vp - Vn) \tag{1.3}$$

Which indicates that the output voltage *Vo* is a function of the difference between the input voltages *Vp* and *Vn*. For this reason op-amps are **difference amplifiers**.

For most practical op-amps the open loop DC gain *A* is extremely high. For example, the popular 741 has a typical open loop gain *A* of 200000 V_o/V_i. Some op-amps have open loop gain values as high as 10^8 V_o/V_i.

The graph that relates the output voltage to the input voltage is called the voltage transfer curve and is fundamental in designing and understanding amplifier circuits. The voltage transfer curve of the op-amp is shown on Figure 3.

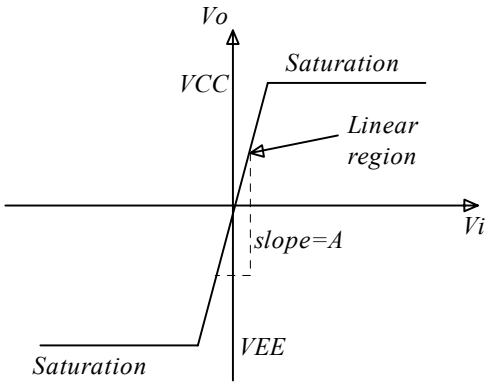


Figure 3. Op-amp voltage transfer characteristics.

Note the two distinct regions of operation: one around $Vi=0V$, the linear region where the output changes linearly with respect to input, and the other at which changes in Vi has little affect on Vo, the saturation region (non-linear behavior).

Circuits with operational amplifiers can be designed to operate in both of these regions. In the linear region the slope of the line relating Vo to Vi is very large, indeed it is equal to the open loop gain A. For a 741 op-amp powered with $VCC= +10V$ and $VEE= -10V$, Vo will saturate (reach the maximum output voltage range) at about $\pm 10\ V$. With an $A=200,000V/V$ saturation occurs with an input differential voltage of $10/200,000 = 50\mu V$, a very small voltage.

The ideal op-amp model

From a practical point of view, an ideal op-amp is a device which acts as an ideal voltage controlled voltage source. Referring to Figure 2, this implies that the device will have the following characteristics:

1. No current flows into the input terminals of the device. This is equivalent to having an infinite input resistance $Ri=\infty$. In practical terms this implies that the amplifier device will make no power demands on the input signal source.
2. Have a zero output resistance ($Ro=0$). This implies that the output voltage is independent of the load connected to the output.

In addition the ideal op-amp model will have infinite open loop gain ($A \to \infty$). The ideal op-amp model is shown schematically on Figure 4.

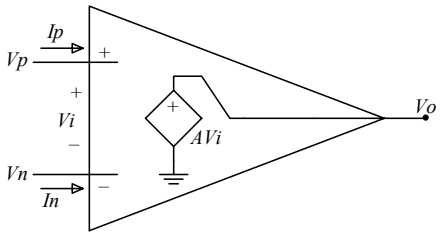


Figure 4. Ideal op-amp model.

In summary, the ideal op-amp conditions are:

$$\left.\begin{array}{ll} I_p = I_n = 0 & \text{No current into the input terminals} \\ R_i \to \infty & \text{Infinite input resistance} \\ R_0 = 0 & \text{Zero output resistance} \\ A \to \infty & \text{Infinite open loop gain} \end{array}\right\} \quad (1.4)$$

Even though real op-amps deviate from these ideal conditions, the ideal op-amp rules are very useful and are used extensively in circuit design and analysis. In the following sections we will see how to use these rules and the typical errors associated with these assumptions.

Note that when using the ideal op-amp rules we should remember that they are limits and so we must perform our analysis by considering them as limits. For example if we consider the equation

$$V_0 = AV_i \Rightarrow V_i = \frac{V_0}{A} \quad (1.5)$$

Which in turn implies that $V_i \to 0$ *as* $A \to \infty$. However, this does not mean that $V_0 \to 0$ but rather that as $A \to \infty$, $V_i \to 0$ in such a way that their product $AV_i = V_0 \neq 0$.

Negative Feedback and Fundamental Op-Amp Configurations.

By connecting the output terminal of the op-amp with the inverting terminal of the device we construct a configuration called the negative feedback configuration as shown on Figure 5. The presence of the biasing voltages of the op-amp, *VCC* and *VEE*, is assumed and will not be shown explicitly in the following circuits. The operational amplifier is assumed to be in the linear region (see Figure 3.)

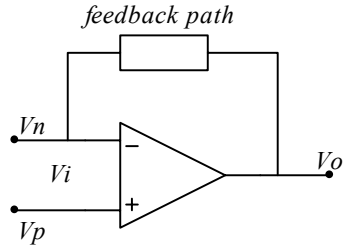


Figure 5. Basic negative feedback configuration.

The closed loop gain of this device is now given by the ratio:

$$G \equiv \frac{V_0}{V_i} \tag{1.6}$$

In negative feedback, a certain fraction of the output signal, voltage *Vo*, is fed back into the inverting terminal via the feedback path.

The block diagram configuration of the negative feedback amplifier is shown on Figure 6. This fundamental feedback circuit contains a basic amplifier with an open-loop gain *A* and a feedback circuit described by the parameter β.

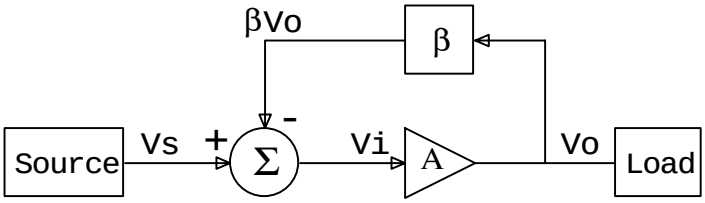


Figure 6. Block diagram of an ideal negative feedback amplifier

The feedback circuit provides a fraction of the output signal, βVo, which is **subtracted** from the input source signal, Vs. The resulting signal, Vi, which is also called the error signal, is the input to the amplifier which in turn produces the output signal Vo = AVi. It is the subtraction of the feedback signal from the source signal that results in the negative feedback.

The gain Vo/Vs of the inverting amplifier is given by

$$G \equiv \frac{Vo}{Vs} = \frac{A}{1+\beta \mathrm{A}} \tag{1.7}$$

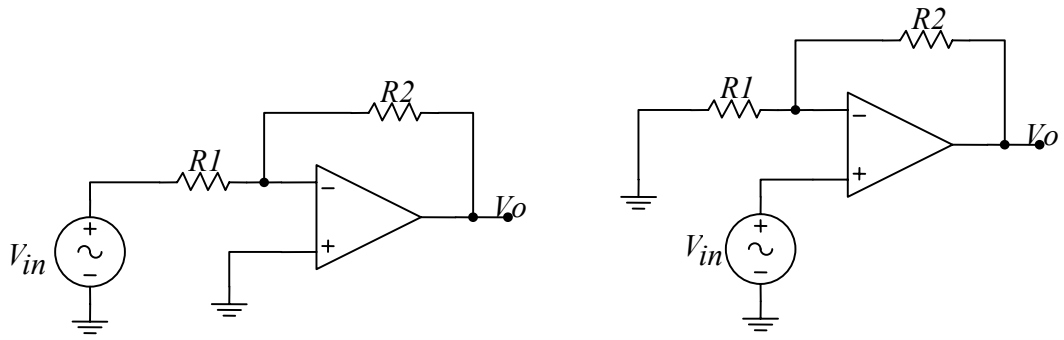
The feedback gain, or closed-loop gain, depends on the open-loop gain, A, of the basic amplifier and the feedback parameter β. The feedback parameter β depends only on the characteristics of the feedback network. For practical operational amplifiers the open-loop gain A is very large. Therefore, in the limit where $A \to \infty$, Equation (1.7) gives

$$G \cong \frac{1}{\beta} \tag{1.8}$$

and so the gain becomes independent of A and it is only a function of the parameter β. The value and "quality" of β depend on the design of the feedback network as well as on the "quality" of the elements used. Therefore, the designer of the feedback amplifier has control over the operational characteristics of the circuit.

Building Negative Feedback Amplifiers.

With two resistors we can construct the fundamental feedback network of a negative feedback amplifier. Depending on the terminal at which the signal is applied, the fundamental negative feedback configuration can be in the **inverting amplifier arrangement**, where the input signal, *Vin*, is applied to the inverting terminal, Figure 7(a), or in the **non-inverting amplifier arrangement**, where the input signal, *Vin*, is applied to the non-inverting terminal, Figure 7(b).



(a) Inverting amplifier (b) Non-inverting amplifier

Figure 7. Basic feedback amplifier configurations: (a) inverting, (b) non-inverting

We will perform the analysis by considering both the effect of finite open loop gain (A is finite) and the ideal op-amp model for which $A \to \infty$.

Inverting Amplifier

The basic inverting amplifier configuration is shown on Figure 8. The input signal, V_{in}, is applied to the inverting terminal and the balance of the circuit consists of resistors *R1* and *R2*.

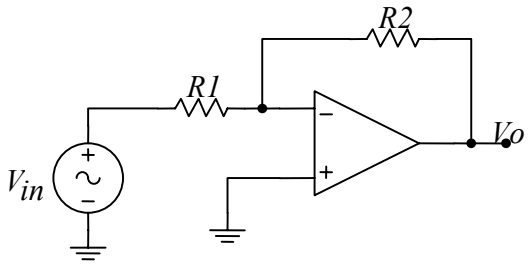


Figure 8. Inverting amplifier circuit

Let's analyze this circuit, i.e determine the output voltage *Vo* as a function of the input voltage *Vin* and the circuit parameters, by assuming infinite input resistance at the inverting and non-inverting terminals, zero output resistance and finite open loop gain *A*. The equivalent circuit of this model is shown on Figure 9.

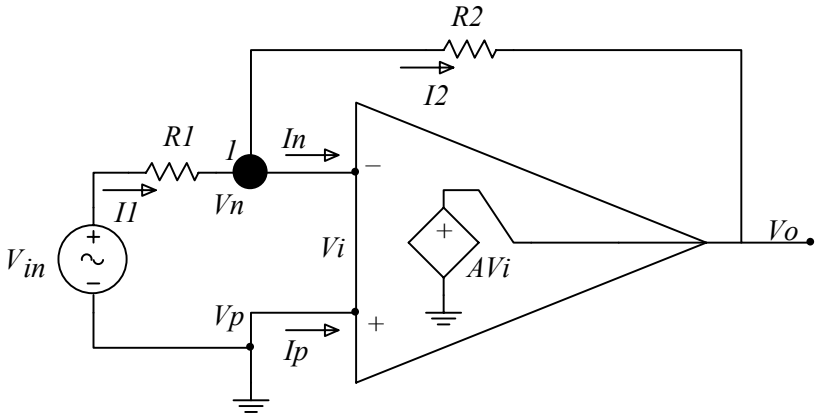
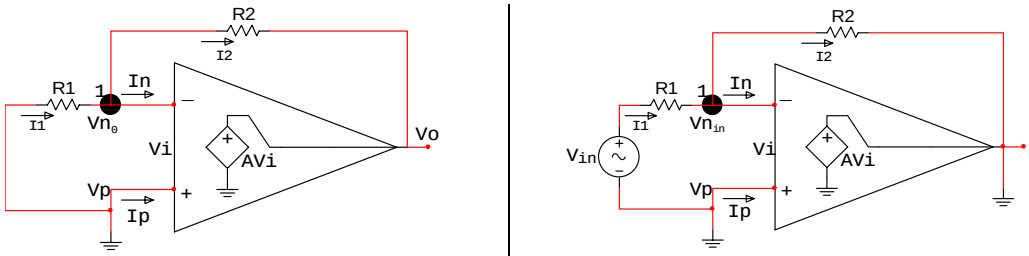


Figure 9. Inverting amplifier circuit model

Since our circuit is linear, the voltage at node 1 can be found by considering the principle of superposition.

Vn is the sum of voltages Vn_o and Vn_{in} as shown on the circuits of Figure 10.
Vn_o is the contribution of *Vo* acting alone and Vn_{in} is the contribution of *Vin* acting alone.



$$V_{n_o} = V_o \frac{R_1}{R_1 + R_2} \qquad V_{n_{in}} = V_{in} \frac{R_2}{R_1 + R_2}$$

Figure 10. Inverting amplifier equivalent circuits considering the property of linearity.

Vn is thus given by

$$V_n = V_{n_o} + V_{n_{in}} = V_o \frac{R_1}{R_1 + R_2} + V_{in} \frac{R_2}{R_1 + R_2} \tag{1.9}$$

The term $V_o \frac{R_1}{R_1 + R_2}$ corresponds to the output voltage that is fed back into the inverting input by the feedback resistor network.

We also know that $Vo = A(Vp - Vn)$ and since $Vp = 0$, $V_n = -\frac{V_o}{A}$. Equation (1.9) becomes

$$-\frac{V_o}{A} = V_o \frac{R_1}{R_1 + R_2} + V_{in} \frac{R_2}{R_1 + R_2} \tag{1.10}$$

By rearranging Equation (1.10) we obtain the voltage gain of the inverting amplifier

$$\begin{aligned} G \equiv \frac{V_0}{V_{in}} &= -\frac{A}{1 + \frac{R1}{R2}(1 + A)} \\ &= -\frac{R2}{R1} \frac{1}{1 + \frac{1}{A}\left(1 + \frac{R2}{R1}\right)} \end{aligned} \tag{1.11}$$

Recall that for an ideal operational amplifier the open loop gain A is infinite. By taking the limit of Equation (1.11) as $A \to \infty$, the "ideal" gain of the inverting amplifier becomes

$$G_{ideal} = \frac{V_0}{V_{in}} = -\frac{R2}{R1} \tag{1.12}$$

By comparing Equation (1.12) to Equation (1.8) we see that the feedback parameter for this amplifier circuit is $\beta = \frac{R1}{R2}$.

Note that the ideal gain depends only on the ratio of resistors *R1* and *R2*. This is a great result. We are now able to design an amplifier with any desirable gain by simply selecting the appropriate ratio of *R1* and *R2*. However, this design flexibility requires a very large value of *A*, the open loop gain of the op-amp. In practice this is not a very difficult requirement to achieve. Op-amp devices have been designed and manufactured with very low cost and are characterized by very high values of *A*.

The negative sign for the gain indicates that the polarity of *Vo* is opposite to the polarity of *Vin*. For example if the input signal *Vin* is a sinusoid of phase 0 degrees, the output signal will also be a sinusoid with a phase shift of 180 degrees. Figure 11 shows the voltages *Vin* and *Vo* for an inverting amplifier with *R2/R1=2*.

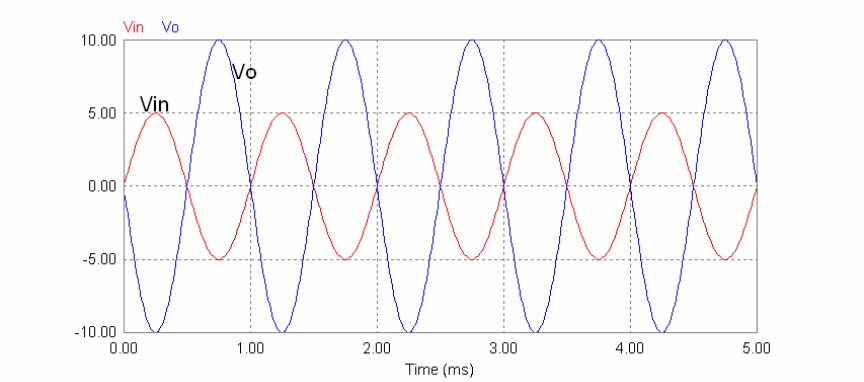


Figure 11. Input and output signals of an inverting amplifier with gain of 2.

It is instructive at this point to investigate the difference between the ideal model represented by Equation (1.12) and the finite open loop gain model represented by Equation (1.11). Let's consider an inverting amplifier design with *R1=10kΩ* and *R2=100kΩ*. In this case, the ideal voltage gain is -10 as given by Equation (1.12). By assuming that *A* ranges in values from 1,000 V/V to 10,000,000V/V, Table I shows the results from Equation (1.11) and the resulting deviation in % from the ideal case.

Table I. The effect of finite A on op-amp gain

A	G	Deviation %
1000	-9.9810	1.088
10000	-9.9890	0.109
100000	-9.9989	0.011
200000	-9.9998	0.0055
1000000	-9.9999	0.0011
10000000	-9.99999	0.00011

The widely used 741 op-amp has a typical open loop gain of 200,000 V/V. With the 741 used in an inverting amplifier circuit, the error introduced in the analysis by considering the ideal gain is less than 0.0055% (55 ppm), a very good value for many applications.

Inverting Amplifier. Ideal op-amp circuit analysis

The ideal op-amp rules are:

1. The differential input voltage is zero. $Vi = 0 \rightarrow Vn = Vp$
2. No current flowing into the input terminals. This is equivalent to infinite input resistance for the op-amp Ri = ∞ $In = Ip = 0$
3. Infinite open loop gain. $A \rightarrow \infty$
4. Output resistance is zero $Ro = 0$

By using these rules we can analyze the inverting amplifier op-amp circuit. From Figure 12 we see that *Vp* is at ground potential (*Vp=0V*). According to the second rule the voltage *Vn* must also be at zero Volts. This does not mean that the inverting terminal is grounded. It simply implies that the inverting terminal is at ground potential (zero volts) but it does not provide a current path to ground. This terminal is said to be at "virtual ground".

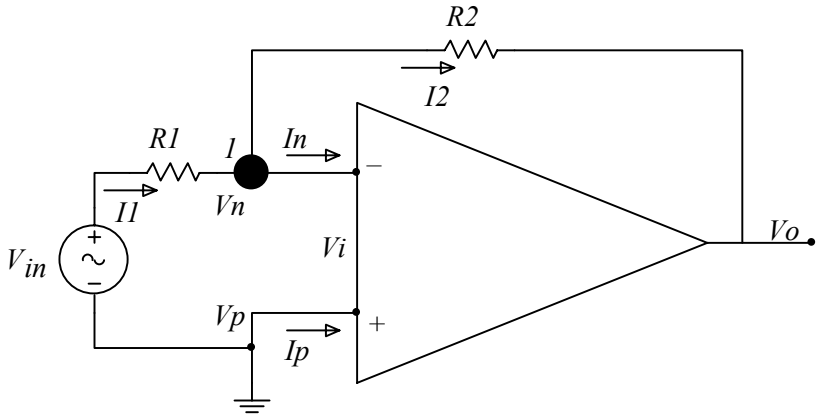


Figure 12. Ideal op-amp inverting amplifier circuit.

Since *In=Ip=0* (rule 2), KCL at node 1 tells us that current *I1* must be equal to current *I2*.

$$I1 = \frac{V_{in} - V1}{R1} = \frac{V_{in}}{R1} = I2 \qquad (1.13)$$

The current *I2*, flowing through *R2*, is related to the voltage drop across *R2*

$$I2 = \frac{Vn - Vo}{R2} \Rightarrow Vo = -I2\,R2 = -Vin\frac{R2}{R1} \tag{1.14}$$

And so the gain of the ideal inverting amplifier is

$$G_{ideal} \equiv \frac{V_0}{V_{in}} = -\frac{R2}{R1} \tag{1.15}$$

Note that the gain given by Equation (1.15) is the same as that obtained in the general case as given by Equation (1.11) as $A \to \infty$.

In order to obtain additional intuition on the operation of this circuit let's consider the two cases for *Vin*.

1. For *Vin >0* the current *I1* will be flowing as indicated on Figure 12. Since *In = 0*, *I2* must also flow as indicated. In order for this to happen, the voltage *Vo* must be at a lower potential than the voltage *Vn*. But since *Vn=0*, this can happen only if *Vo < 0*.

2. For *Vin <0* the direction of the currents will be reversed and the argument follows in a similar way, resulting in *Vo > 0*.

Non-Inverting Amplifier

Figure 13 shows the basic non-inverting amplifier configuration. The negative feedback is maintained and the input signal is now applied to the non-inverting terminal.

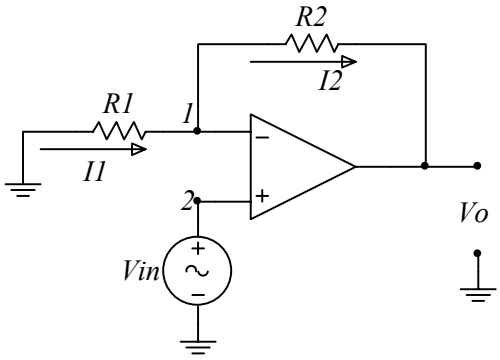


Figure 13. Non-inverting amplifier

The equivalent circuit of the Non-Inverting amplifier with a finite open-loop gain is shown on Figure 14. Here we have assumed an infinite input resistance and a zero output resistance for the op-amp.

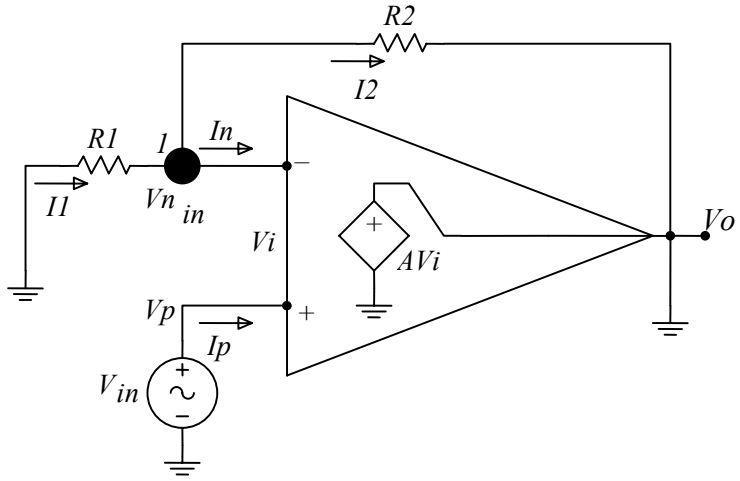


Figure 14. Equivalent circuit of Non-inverting amplifier with finite open loop gain.

Since $In = Ip=0$, we have $I1=I2$ and therefore:

$$\frac{-Vn}{R1}=\frac{Vn-Vo}{R2}\Rightarrow\frac{Vo}{R2}=Vn\left(\frac{1}{R1}+\frac{1}{R2}\right) \tag{1.16}$$

Since the voltage $Vi = Vp\text{-}Vn = Vin\text{-}Vn$, the output voltage is given by:

$$Vo = A(Vin - Vn) \tag{1.17}$$

Combining Equations (1.16) and (1.17), the resulting expression for the closed loop gain, $G \equiv \frac{Vo}{Vin}$, becomes:

$$G \equiv \frac{Vo}{Vin} = \frac{1 + R2/R1}{1 + (1 + R2/R1)/A} \tag{1.18}$$

The gain is positive and unlike the inverting amplifier, the output voltage *Vo* is in phase with the input *Vin* and the gain is always greater than 1.

From Equation (1.18)we see that as $A \to \infty$, the closed loop gain is

$$\underset{A\to\infty}{G} = 1 + \frac{R2}{R1} \tag{1.19}$$

The open-loop gain, *A*, of an op-amp is a parameter with considerable variability. It depends on the characteristics of the various components inside the operational amplifier (transistors, resistors, capacitors, diodes) and so it may be a function of environmental conditions (temperature, humidity) and manufacturing processes. As *A* changes by a certain fraction, $\frac{dA}{A}$, the closed loop gain, *G*, will also change by an amount $\frac{dG}{G}$. By taking the derivative $\frac{dG}{dA}$ of Equation (1.18) and simplifying we obtain:

$$\frac{dG}{G} = \frac{dA}{A}\left[\frac{1 + \frac{R2}{R1}}{1 + \frac{1 + \frac{R2}{R1}}{A}}\right] = \frac{dA}{A}\left(\frac{G}{A}\right) \tag{1.20}$$

From Equation (1.20) we see that the change in *G* due to a change in *A* is modulated by the factor $\frac{G}{A}$.

As an example let's consider the 741 op-amp with a nominal open loop gain of 200 *V/mV*, which is arranged in a non-inverting amplifier configuration with a closed loop gain of 10. If the open loop gain *A* changes by 20%, the change in the closed loop gain as given by Equation (14) is

$$\frac{dG}{G} = 20\left(\frac{10}{2.0\times10^5}\right)\% = 0.001\% \tag{1.21}$$

The advantage of having an op-amp with a large value of A is apparent. Of course by "large" value we mean that the open-loop gain is much larger than the closed loop gain $(A >> G)$.

We have been able, by using a component that is characterized by large uncertainty in its performance, to construct a devise with very high performance. This however can happen only if the open-loop gain A is very large, which can be easily achieved with standard integrated circuit technology.

Non-inverting amplifier: Ideal model

Referring to Figure 13, the ideal model implies the voltages at nodes 1 and 2 are equal: $Vn = Vin$. Also, since no current flows into the terminals of the op-amp, KCL at node 1 gives,

$$\left.\begin{aligned} I1 &= I2 \\ I1 &= -\frac{Vin}{R1} \\ I2 &= \frac{Vin - Vo}{R2} \end{aligned}\right\} \Rightarrow -\frac{Vin}{R1} = \frac{Vin - Vo}{R2} \tag{1.22}$$

Solving for the gain (Vo/Vin) we have,

$$G \equiv \frac{Vo}{Vin} = 1 + \frac{R2}{R1}\bigg|_{ideal} \tag{1.23}$$

Note that Equation (1.23) is the same as Equation (1.19) which was obtained in the limit as $A \to \infty$.

Voltage Follower. Buffer.

By letting $R1 \to \infty$ and $R2 = 0$, Equation (1.23) gives $G = \frac{Vo}{Vin} = 1$. Figure 15 shows the resulting circuit.

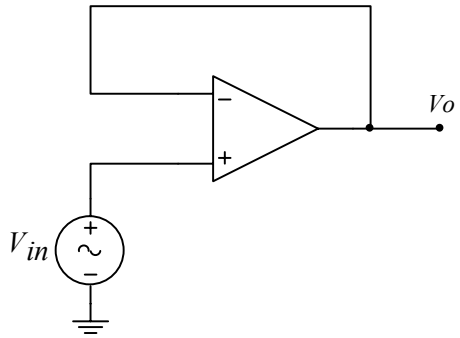


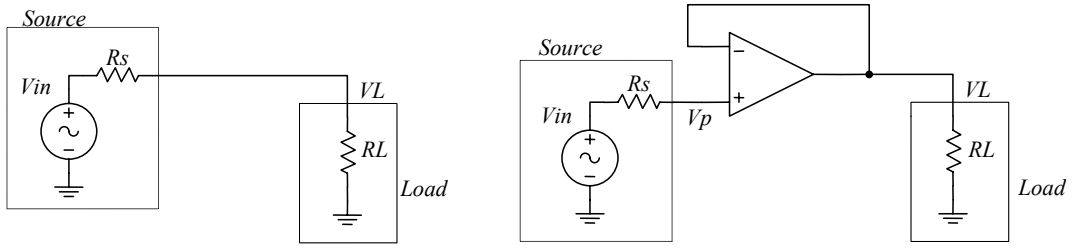
Figure 15. Voltage follower op-amp circuit

The voltage gain of this configuration is 1. The output voltage follows the input.

So what is the usefulness of this op-amp circuit?

Let's look at the input and output resistance characteristics of the circuit. As we have discussed, the resistance at the input terminals of the op-amp is very large. Indeed, for our ideal model we have taken the value of that resistance to be infinite. Therefore the signal *Vin* sees a very large resistance which eliminates any loading of the signal source. Similarly, since the output resistance of the op-amp is very small (zero ideally), the loading is also eliminated at the output of the device. In effect this is a resistance transformer.

In order to see the importance of this **buffer** circuit let's consider the case where the input signal is a source with an output resistance Rs and is connected to a load with resistance RL. In Figure 16(a) the signal source is connected directly to the load RL.



(a) (b)

Figure 16. (a) Source and load connected directly. (b) Source and load connected via a voltage follower.

From Figure 16(a), the voltage divider formed by Rs and RL gives a value for VL which is a fraction of Vin given by

$$VL = Vin\frac{RL}{RL + Rs} \tag{1.24}$$

For example, if $RL = 1k\Omega$ and $Rs = 10\ k\Omega$, then $VL \approx 0.1\ Vin$ which represents a considerable attenuation (loading) of the signal source.

If we now connect the signal source to the load with a buffer amplifier as shown on Figure 16(b). Since the input resistance of the amplifier is very large (no current flows into the terminal), the voltage at the non-inverting terminal, *Vp*, is equal to *Vin*. In addition, since the output resistance of the op-amp is zero, the voltage across the load resistor $VL = Vo = Vin$. The load now sees the input voltage signal but it places no demands on the signal source since it is "buffered" by the operational amplifier circuit.

Example: Non-Inverting amplifier design

Design an amplifier with a gain of 20dB by using standard 5% tolerance resistors. The input signal is in the range -1V to +1V. The amplifier is to drive a resistive load. For your design you may use an op-amp with the ability to deliver a maximum current of 100mA.

Standard 5% resistors are available with values from 10Ω to 10MΩ. The decade values can be found from the following table.

Table I. Standard 5% resistor values

10	11	12	13	15	16	18	20	22
24	27	30	33	36	39	43	47	51
56	62	68	75	82	91			

For example, if we consider the multiplier 11, the possible 5% resistor values corresponding to it are 11Ω, 110Ω, 1.1kΩ, 11kΩ, 110kΩ, 1.1MΩ. For other multipliers, the values may be found by following this example.

Solution:

The non-inverting amplifier circuit is

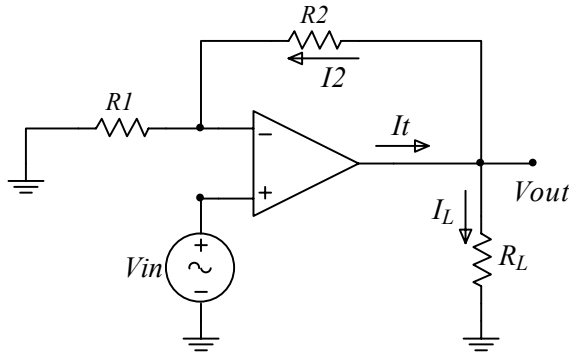


Figure 17. Amplifier circuit.

From the definition of dB we have: $20dB = 20\log\frac{V_{out}}{V_{in}}$ and so $\frac{V_{out}}{V_{in}} = 10$.

The closed loop gain is given by Equation (1.23) and thus for our design

$$10 = 1 + \frac{R2}{R1} \tag{1.25}$$

Our task is now to determine the values for *R1* and *R2* that satisfy the design constraints. We need two resistors whose ratio is 9 (*R2/R1 = 9*). From the values listed on the 5% table we have a few options. Some of our options are:

R2=180Ω and R1=20Ω
R2=1.8kΩ and R1=0.2kΩ
R2=18kΩ and R1=2kΩ
R2=180kΩ and R1=20kΩ
R2=1.8MΩ and R1=200kΩ

The power constraint will now guide us in determining the actual value of resistors *R1* and *R2*. With an input voltage of *+1V* the output voltage *Vo=10V* and thus the current *It* delivered by the op-amp must be less than 100mA.

If all the current is passing through resistor R_L then R_L is limited to *1kΩ*.

Besides the path through R_L current may also flow to ground through *R2* and *R1*. Since no current flows into the terminals of the op-amp, the fraction of the current that flows through *R2* and *R1* is

$$I2 = It\left(\frac{R1+R2}{RL+R1+R2}\right) \tag{1.26}$$

Note that if the resistance value of R_L is comparable to that of *R1+R2*, then a large fraction of the current provided by the op-amp flows through the feedback loop.

Therefore in order to tightly satisfy the current constraint of the op-amp we must also consider the amount of current that flows through the feedback loop. The table below shows some of the many design possibilities.

Table II. Possible designs

R_L	*R1*	*R2*	*IL*	*I2*	*It*
0.1kΩ	20Ω	180Ω	100mA	50mA	150mA
0.1kΩ	0.2kΩ	1.8kΩ	100mA	5mA	105mA
0.1kΩ	2kΩ	18kΩ	100mA	0.5mA	100.5mA
110Ω	*2kΩ*	*18kΩ*	*90.9mA*	*0.5mA*	*91.4mA*
110Ω	*20kΩ*	*180kΩ*	*90.9mA*	*0.05mA*	*90.95mA*
110Ω	*200kΩ*	*1.80MΩ*	*90.9mA*	*0.005mA*	*90.905mA*

If we consider the 5% tolerance of the resistors we conclude that we are limited to the following resistor values:

$$\left.\begin{array}{l} RL > 100\Omega \\ R1 \geq 2k\Omega \\ R2 \geq 18k\Omega \end{array}\right\} \qquad (1.27)$$

Any set of the values in the enclosed dotted box on Table II may be used in this design. In practice we should however avoid extremely large resistance values in the feedback circuit.

Problem:

Consider a signal source with a source output resistance *Rs* connected to the inverting amplifier as shown on Figure P2. Calculate the gain of the amplifier, assuming that the load cannot be ignored. Define the conditions for which the loading can be ignored.

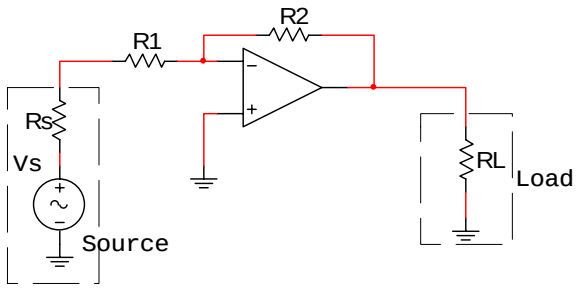


Figure P2

Input and Output Resistance of negative feedback circuits.

(Inverting and Non-Inverting Amplifiers)

As we saw in the example of the buffer amplifier, op-amp amplifier circuits may, besides voltage amplification, provide impedance transformation. It is thus important to be able to determine the input and the output resistance seen by a source or a load connected to an op-amp circuit.

The input impedance of an op-amp circuit with negative feedback may in general be very different from the open loop input/output resistance of an op-amp.

Input resistance

Inverting amplifier

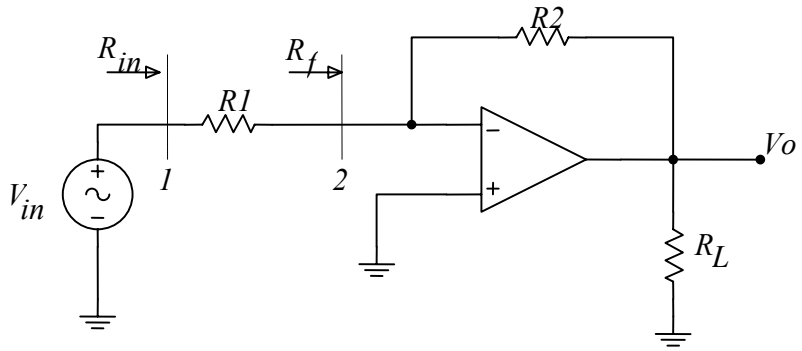


Figure 18. Inverting amplifier showing input resistance.

The input resistance of the inverting amplifier, or equivalently the resistance seen by the source *Vin*, is *Rin* as shown on Figure 18. By designating as *Rf*, the resistance to the right of point 2, we have *Rin = R1 + Rf*. Determining *Rf* and then adding *R1* for the total input resistance is an easier process than performing the calculation together.

The equivalent resistance *Rf* may be determined by considering the circuit shown on Figure 19(a). Here we apply a test current *It* and calculate the resulting voltage *Vt*. The resistance *Rf* is then given by *Rf=Vt/It.*

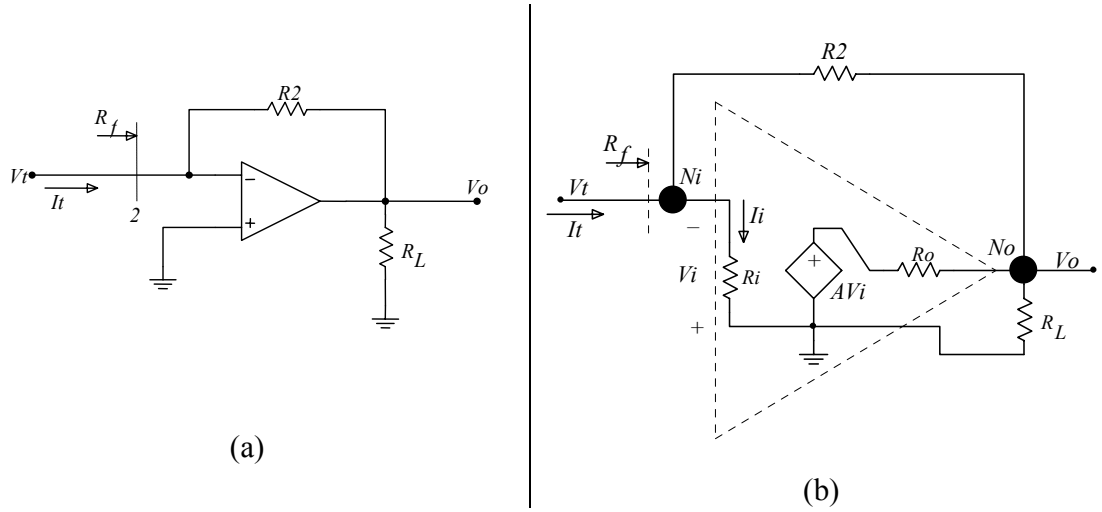


Figure 19. (a) Circuit for the calculation of the input resistance. (b) equivalent circuit for the calculation of input resistance R_f.

By considering the op-amp model with open loop gain *A*, input resistance *Ri* and output resistance *Ro*, the equivalent circuit of interest is shown on Figure 19(b). By applying KCl at the input and output nodes (*Ni* and *No*) we have:

KCL at node *Ni* gives:

$$I_t = \frac{V_t}{Ri} + \frac{V_t - Vo}{R2} \tag{1.28}$$

KCL at node *No* gives:

$$\frac{Vo}{RL} + \frac{Vo - \left(A\left(-V_t\right)\right)}{Ro} + \frac{Vo - V_t}{R2} = 0 \tag{1.29}$$

The ratio *Vt/It* may be obtained from Equations (1.28) and (1.29) by eliminating *Vo*. The input resistance of the inverting amplifier is,

$$\frac{1}{R_f} \equiv \frac{It}{Vt} = \frac{1}{R_i} + \frac{1}{R_2}\left[\frac{1 + A + \frac{R_o}{R_L}}{1 + \frac{R_o}{R_L} + \frac{R_o}{R_2}}\right] \tag{1.30}$$

In the ideal case where $A \to \infty$, the resistance $R_f \to 0$, implying that $Vt \to 0$ and $It \to 0$: the ideal op-amp rules.

For simplicity let's assume that *Ro=0*. Then,

$$\frac{1}{R_f} = \frac{1}{R_i} + \frac{1+A}{R_2} \tag{1.31}$$

For all practical situations $R_2 << R_i$ and Equation 16 gives:

$$R_f \cong \frac{1}{1+A} R_2 \tag{1.32}$$

Which shows that the input resistance R_f is a very strong function of the open loop gain and the input resistance of the op-amp, R_i, has a negligible effect on the resistance R_f.

For the 741 op-amp which has *A=200 V/mV,* R_i *= 2 MΩ* and R_o *= 100Ω* an inverting amplifier with *R2=10 kΩ*, is characterized by R_f *= 0.5 mΩ*. This is a negligible value for all applications of interest.

Therefore, the effective resistance seen by the source is $\approx R1$.

Non-inverting amplifier

Figure 20 shows the equivalent non-inverting amplifier circuit for the calculation of the input resistance R_{in}. We apply a test voltage Vt and calculate the resulting current It. The input resistance is then $R_{in}=Vt/It$.

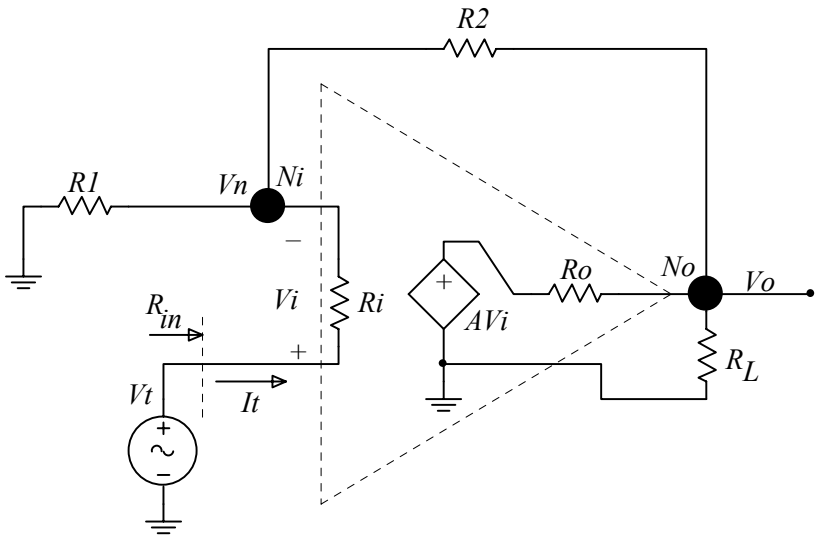


Figure 20. Non-inverting amplifier equivalent circuit for the calculation of the input resistance.

We proceed by applying KCL at nodes *Ni* and *No*.

KCL at node *Ni* gives:

$$It-\frac{Vn}{R1}-\frac{Vn-Vo}{R2}=0 \tag{1.33}$$

KCL at node *No* gives:

$$\frac{Vo}{RL}+\frac{Vo\ -\ \left(A\left(Vi\right)\right)}{Ro}+\frac{Vo\ -\ Vn}{R2}=0 \tag{1.34}$$

Since $Vi = Vt – Vn = I\,Ri$, Equations (1.33) and (1.34) after some algebraic manipulations give

$$\frac{Vt}{It}=Rin=\frac{1+\frac{Ro}{RL}+\frac{Ro}{R2}+\left[\left(\frac{1}{R1}+\frac{1}{R2}\right)\left(1+\frac{Ro}{RL}+\frac{Ro}{R2}\right)-\frac{Ro}{R2^2}+\frac{A}{R2}\right]Ri}{\left(\frac{1}{R1}+\frac{1}{R2}\right)\left(1+\frac{Ro}{RL}+\frac{Ro}{R2}\right)-\frac{Ro}{R2^2}} \tag{1.35}$$

For a simplification of the above expression let's neglect *Ro* which is anyway small compared to other values. Equation (1.35) now becomes

$$Rin = \frac{R2\left(1+\frac{Ri}{R1}\right)+Ri\left(1+A\right)}{1+\frac{R2}{R1}} \tag{1.36}$$

In the limit $A \to \infty$, $Rin \to \infty$. Similarly, in the limit $Ri \to \infty$, $Rin \to \infty$.

Output Resistance

The equivalent circuit for the calculation of the output resistance is shown on Figure 17. Note that this equivalent circuit, which is obtained by suppressing the input sources, is common for both the inverting and the non-inverting amplifiers. We apply a rest voltage V at the output and calculate the resulting current I. The output resistance is Rout=V/I.

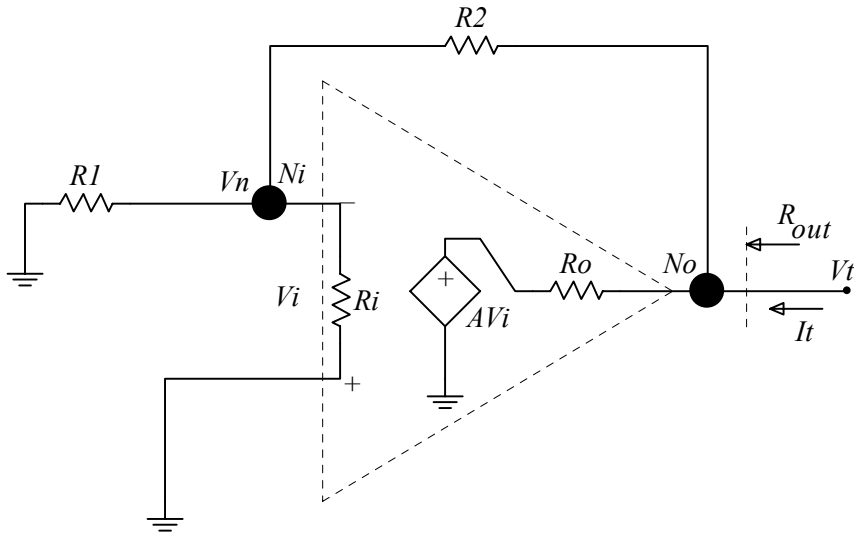


Figure 21. Model for the calculation of output resistance

KCL at node *No* gives:

$$I + \frac{-AVn - Vt}{Ro} + \frac{Vn - Vt}{R2} = 0 \tag{1.37}$$

By noting that resistors *R1* and *Ri* are in parallel, the voltage *Vn* at node *Ni* is

$$Vn = Vt \frac{\frac{R1Ri}{R1+Ri}}{\frac{R1Ri}{R1+Ri} + R2} \tag{1.38}$$

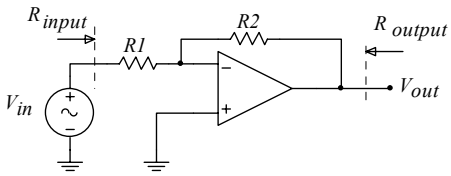
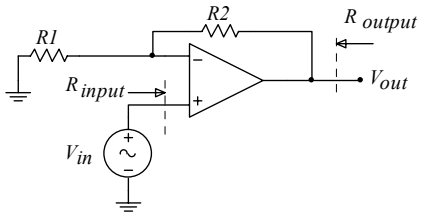
By substituting Equation (1.38) into Equation (1.37) the ratio *Vt/It* becomes

$$\frac{Vt}{It} = Rout = \frac{Ro\left(1 + \frac{R2}{R1} + \frac{R2}{Ri}\right)}{1 + \frac{R2}{R1} + \frac{R2}{Ri} + A + \frac{Ro}{R1} + \frac{Ro}{Ri}} \tag{1.39}$$

In typical circuits $R2 << Ri$, $Ro \cong 100\Omega$ and $A >> 1$. Therefore the output resistance is very small. For our typical 741 op-amp, with $Ro = 100\Omega$, $Ri = 2M\Omega$, and A=200V/mV, arranged as an inverting amplifier of gain -10 the output resistance is 5.5mΩ.

Table III summarizes the results for the input and output resistance of the ideal inverting and non inverting amplifiers. These general results are sufficient for the design of most amplifiers of interest. The non inverting amplifier is the most useful configuration in terms of its ideal coupling characteristics with the signal source. The signal source sees an infinite input resistance and thus the non-inverting amplifier places no loading demands on the source. Furthermore, the input resistance seen by the source does not change as the gain of the amplifier changes. By contrast, when a source is connected to an inverting amplifier, the source sees the resistor R1 as the input resistance of the amplifier.

Table III. Summary of ideal amplifier characteristics.

	Inverting amplifier	Non inverting amplifier
		
Gain: $\left(\frac{Vout}{Vin}\right)$	$-\frac{R2}{R1}$	$1+\frac{R2}{R1}$
Rinput	$R1$	∞
Routput	0	0

Practical op-amp considerations

Input Offset and Input Bias currents

For an ideal op amp no current flows into its input terminals. However, for real op amps there is a small amount of current that flows into the inverting and non inverting terminals as shown on Figure 22.

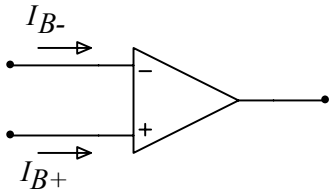


Figure 22. Op-amp symbol with input currents.

The electrical characteristics table of op-amp device data sheets give the values for Input offset current (I_{IO}) and the Input Bias current (I_{IB}), where I_{IO} and I_{IB} are defined by

$$I_{IO} = \left| I_{B+} - I_{B-} \right| \tag{1.40}$$

$$I_{IB} = \frac{I_{B+} + I_{B-}}{2} \tag{1.41}$$

In order to quantify the effect of the currents I_{B+} and I_{B-} lets consider the amplifier configuration of Figure 23 for which all inputs have been set to zero.

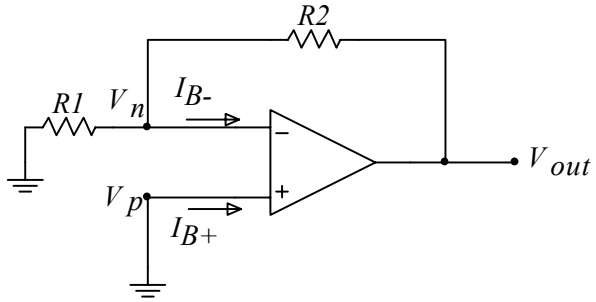


Figure 23. Amplifier for the evaluation of the effect of the input bias currents.

If I_{B+} and I_{B-} are zero then the output voltage V_{out} will also be zero.

The voltage error due to the bias currents I_{B+} and I_{B-} is generated by the flow of these currents through resistor *R2*. For the 741 op amp, the typical room temperature values for

I_{IO} and I_{IB} are: I_{IO}=*20 nA and* I_{IB}=*80 nA*. For an amplifier with R2=100kΩ, the resulting output voltage is $V_{out} = I_{B-}\ R2\ =\ (90nA)\ (100k\Omega)\ =\ 9\ mV$. In some application this might be an unacceptable value.

This "error" voltage may be reduced by simply selecting a smaller resistor *R2*. In some cases this might be sufficient assuming that other circuit characteristics like power consumption is not violated.

In general however the effect of the bias currents may be reduced by employing the appropriate "compensation technique." Such an arrangement is shown on Figure 24, where we have used resistor *Rp* at the non inverting terminal.

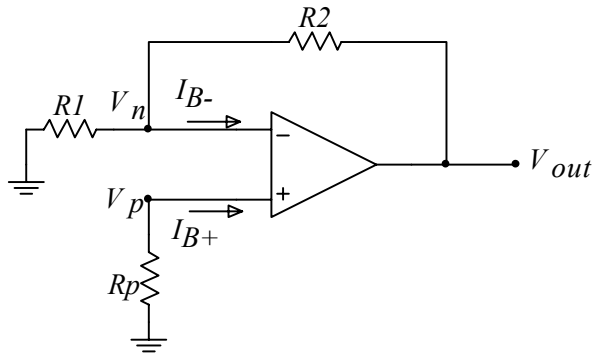


Figure 24. Amplifier circuit with bias current compensating resistor.

Since we have a linear system the effect of the bias currents on V_{out} can be estimated by using the principle of superposition. We have two cases:

1. $I_{B+} = 0$ which gives $V_{out(n)} = I_{B-}R2$
2. $I_{B-} = 0$ which gives $V_{out(p)} = \left(1+\frac{R2}{R1}\right)Vp\ =\ -\ \left(1+\frac{R2}{R1}\right)I_{B+}R3$

And superposition gives

$$Vout\ =\ I_{B-}R2\ -\ \left(1+\frac{R2}{R1}\right)I_{B+}R3 \qquad (1.42)$$

Before we proceed with further algebraic manipulation of Equation (1.42) let's look at the operation of the circuit.

The equivalent resistance of the feedback network seen at node *Vn* is the parallel combination of *R1* and *R2*. By further assuming that $I_{B+} = I_{B-}$, the desired system symmetry can be maintained if the resistance seen at node *Vp* is the same as that seen at node *Vn*. Therefore if *Rp* has a value that is equal to the parallel combination of *R1* and *R2* the differential voltage at the inputs of the op amp balances the effect of the input currents.

Now by manipulating Equation (1.42) for the general case when $I_{B+} \neq I_{B-}$ we obtain

$$Vout = \left(1+\frac{R2}{R1}\right)\left[\underbrace{\left(\frac{R1R2}{R1+R2}-Rp\right)I_{IB}}_{Bias\ Term} - \underbrace{\left(\frac{R1R2}{R1+R2}+Rp\right)\frac{I_{IO}}{2}}_{Offset\ Term}\right] \tag{1.43}$$

For $I_{B+} = I_{B-}$, $I_{IO}=0$ and the "*Offset Term*" of Equation (1.43) is zero. The "*Bias Term*" and thus V_{out} will then become zero when

$$Rp = \frac{R1R2}{R1+R2} \tag{1.44}$$

When $I_{B+} \neq I_{B-}$ and $Rp = R1 // R2 = \frac{R1R2}{R1+R2}$, the "*Bias Term*" becomes zero and V_{out} is

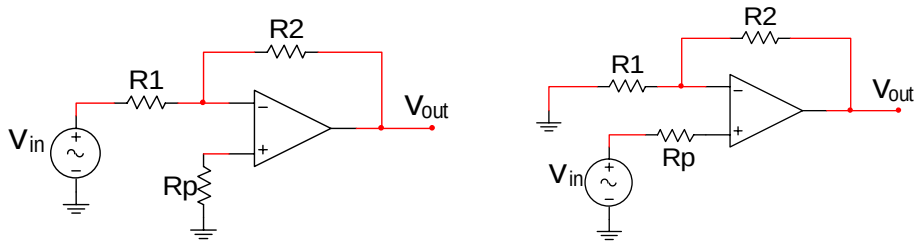
$$Vout = -\left(1+\frac{R2}{R1}\right)\left(\frac{R1R2}{R1+R2}+Rp\right)\frac{I_{IO}}{2} = -R2\ I_{IO} \tag{1.45}$$

The output error is thus proportional to the input offset current which for most op-maps is about an order of magnitude less than the currents I_{B+} and I_{B-}. For the 741 op amp $I_{B+} = 90nA$ and I_{IO}=20nA.

Design Practice (principle)

Always use a resistor Rp from the non inverting input to ground. Make

$$Rp = \frac{R1R2}{R1+R2}$$ Since we want the resistance seen by V- and V+ to be the same.



Input Offset Voltage

Besides the offset current at the inputs there also exists a nonzero difference voltage *Vi* at the input terminals even if we apply the same external voltage inputs. For the circuit of Figure 25 the out put voltage is not zero even though the input pins are grounded. The presence of this error voltage is due to transistor matching issues in the internal op-amp circuit.

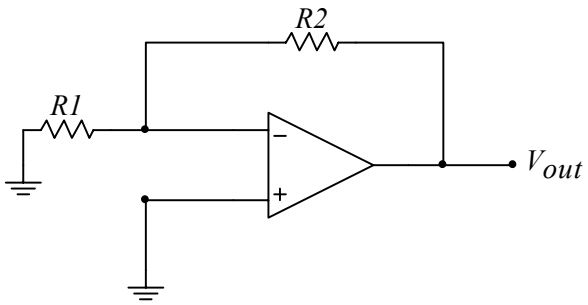


Figure 25. Output offset voltage

In the above figure, *Vo = Voff·(R1+R2)/R1*.

Common Mode Rejection Ratio (CMRR)

As we have seen, the usefulness of the op amp is derived from its ability to amplify differential signals. In fact the ideal op amp has an infinite gain for differential voltage signals. It is desired that signals that are common to both inputs "Common Mode (CM) Signals" be rejected by the amplifier. An ideal op amp has the ability to completely reject those CM signals; thus having infinite Common Mode Rejection (CMR) ability.

For an amplifier subjected to a differential voltage V_D and a common mode voltage V_{CM}, the output voltage is

$$Vo = G_D V_D + G_{CM} V_{CM} \tag{1.46}$$

Where G_D is the differential gain and G_{CM} is the common mode gain of the amplifier. In practice we would like to minimize G_{CM}. The ability of an amplifier to reject the CM signal is expressed by a parameter called the Common Mode Rejection Ratio (CMRR) which is defined as the ratio of the differential gain to common mode gain as follows.

$$\text{CMRR} \equiv 20 \log_{10} \left| \frac{\text{Gain of Differential Signal}}{\text{Gain of Common Mode Signal}} \right| = 20 \log_{10} \left| \frac{G_D}{G_{CM}} \right| \tag{1.47}$$

In the open loop configuration, our standard 741 op amp is characterized by a CMRR of 90dB for signal frequencies less than 100 Hz. At higher frequencies CMRR degrades considerably falling to 40dB at 100 kHz.

In general CMRR is not of concern in the inverting amplifier configuration. Can you see why? explain

Design Principle

Signal frequency is a fundamental parameter that drives circuit design

To see the effects of CMRR, drive a unity gain non-inverting 741 op-amp with a 10V step function; the output should be off 10V by a few hundred microvolts. This error is partially due to the finite open-loop gain of the op-amp and partially due to the CMRR. The inverting configuration leads to minimal common mode error since the amplifier's inputs are both at ground.

Non-linear application in op-amp

- When opamp operated in open-loop configurations, the slightest change in input voltage will force the op-amp into saturation (V_{POS} or V_{NEG})
- Op-amps are sometimes used in non-linear applications as square wave generator.
- By comparing these two input voltages: positive input voltages, V^+ and negative input voltage, V^- where:

$$V_O = V_{CC} \text{ if } V^+ > V^-$$

$$V_O = -V_{CC} \text{ if } V^+ < V^-$$

$$V_O = A(V^+ - V^-) \text{ if } V^- < V_O < V^+$$

- Input current, $I_i = 0$

Comparator

An analog comparator has two inputs one is usually a constant reference voltage V_R and other is a time varying signal v_i and one output v_O. The basic circuit of a comparator is shown in **Fig.1**

When the noninverting voltage is larger than the inverting voltage the comparator produces a high output voltage ($+V_{sat}$). When the non-inverting output is less than the inverting input the output is low ($-V_{sat}$). **Fig. 2** also shows the output of a comparator for a sinusoidal.

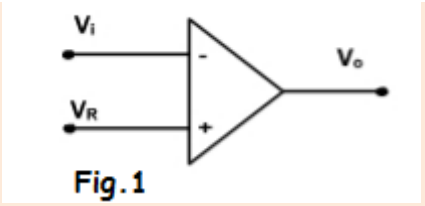
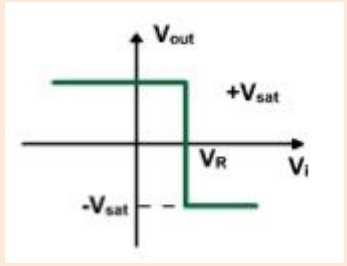


Fig.1



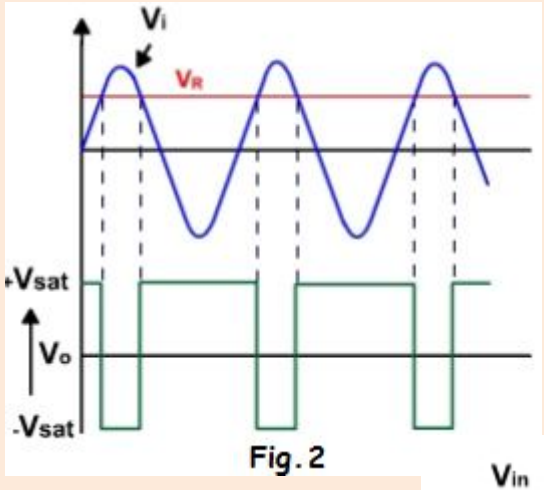


Fig. 2

$$v_O = -V_{sat} \text{ if } v_i > V_R$$

$$= +V_{sat} \text{ if } v\,i < V_R$$

If VR = 0, then slightest input voltage (in mV) is enough to saturate the OPAMP and the circuit acts as zero crossing detector shown in fig .3

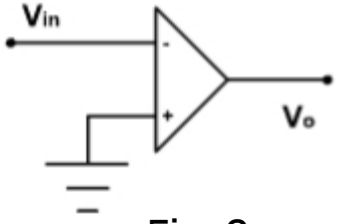
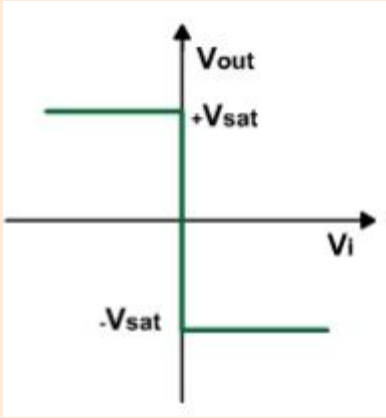


Fig. 3



Regenerative Comparator (Schmitt Trigger)

If the input to a comparator contains noise, the output may be erractive when vin is near a trip point. For instance, with a zero crossing, the output is low when vin is positive and high when vin is negative. If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise. Fig. 1, shows the output of zero crossing detection if the input contains noise.

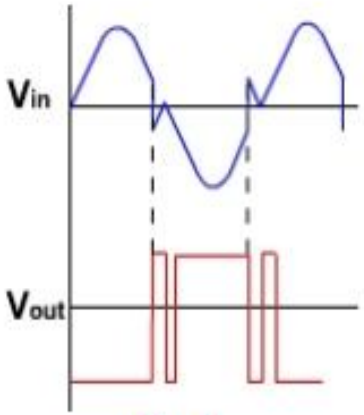


Fig. 1

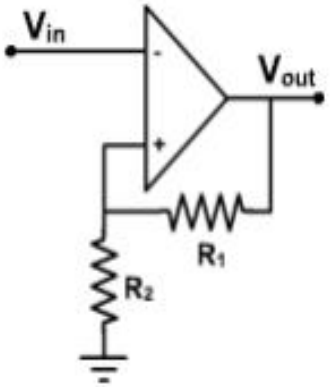


Figure 2

This can be avoided by using a Schmitt trigger, circuit which is basically a comparator with positive feedback. Fig. 2, shows an inverting Schmitt trigger circuit using OPAMP.

Because of the voltage divider circuit, there is a positive feedback voltage. When OPAMP is positively saturated, a positive voltage is feedback to the non-inverting input, this positive voltage holds the output in high stage. (vin< vf). When the output voltage is negatively saturated, a negative voltage feedback to the inverting input, holding the output in low state.

When the output is +Vsat then reference voltage Vref is given by

$$V_{ref} = \frac{R_2}{(R_1+R_2)} * V_{sat} = (+\beta V_{sat})$$

If Vin is less than Vref output will remain +Vsat.

When input vin exceeds Vref = +Vsat the output switches from +Vsat to –Vsat. Then the reference voltage is given by

$$V_{ref} = \frac{-R_2}{(R_1+R_2)} * V_{sat} = (-\beta V_{sat})$$

The output will remain –Vsat as long as vin > Vref.

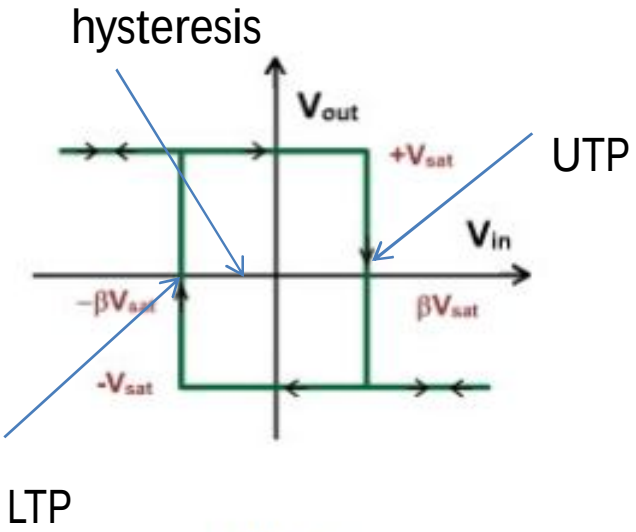


Fig. 3

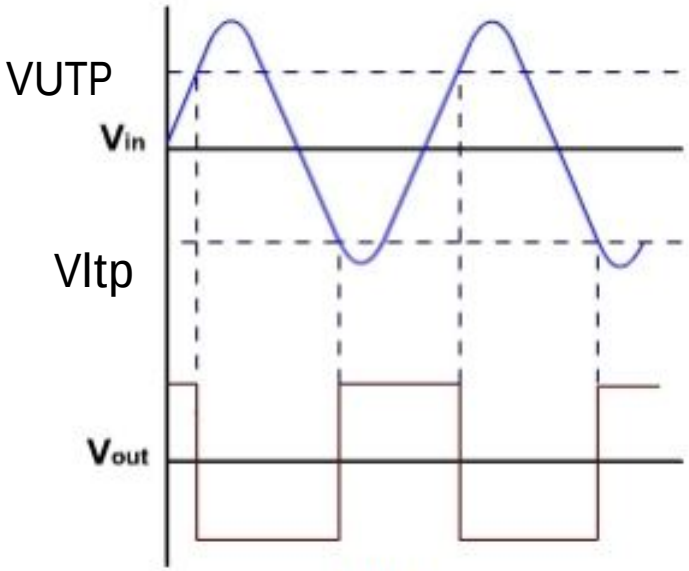


Fig. 4

If vin < Vref i.e. vin becomes more negative than−Vsat then again output switches to +Vsat and so on. The transfer characteristic of Schmitt trigger circuit is shown in fig. 3. The output is also shown in fig. 4 for a sinusoidal wave. If the input is different than sine even then the output will be determined in a same way.

Positive feedback has an unusual effect on the circuit. It forces the reference voltage to have the same polarity as the output voltage, The reference. voltage is positive when the output voltage is high ($+v_{sat}$) and negative when the output is low ($-v_{sat}$).

In a Schmitt trigger, the voltages at which the output switches from $+v_{sat}$ to $-v_{sat}$ or vice versa are called upper trigger point (UTP) and lower trigger point (LTP). the difference between the two trip points is called hysteresis.

$$UTP = \frac{R_2}{R_1 + R_2} V_{sat}$$

$$LTP = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

$$V_{hys} = UTP - LTP$$

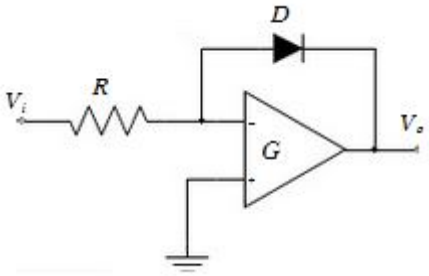
$$= \frac{R_2}{R_1 + R_2} V_{sat} - \frac{R_2}{R_1 + R_2} (-V_{sat})$$

$$= 2\left(\frac{R_2}{R_1 + R_2}\right) V_{sat}$$

$$= 2\beta V_{sat}$$

Logarithmic Amplifier

Figure shows an elementary logarithmic amplifier, i.e. the output is proportional to the logarithm of the input. A BJT as feedback provides a larger input dynamic range.



Because the Op-Amp is mounted as an inverting amplifier, if v_i is positive, then v_o must be negative and the diode is in conduction.

We must have

$$i \simeq I_s e^{-qV_o/k_B T} \qquad I_s \ll 1,$$

where $q < 0$ is the electron charge. Considering that

$$i = \frac{v_i}{R},$$

and after some algebra we finally get

$$v_o = \frac{k_B T}{-q} \left[\ln(v_i) - \ln(RI_s) \right].$$

The constant term $\ln(RI_s)$ is a systematic error that can estimated and subtracted at the output. It is worth to notice that v_i must be positive to have the circuit working.

Anti-Logarithmic Amplifier

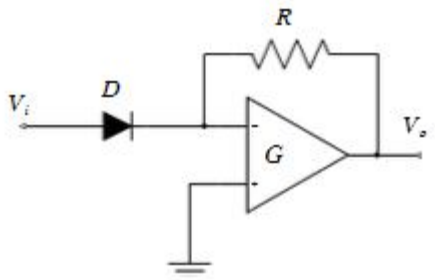


Figure shows an elementary logarithmic amplifier, i.e. the output is proportional to the inverse of logarithm of the input. Same remarks of the logarithmic amplifier about the npn BJT applies to this circuit.

The current flowing through the diode or the BJT is

$$i \simeq I_s e^{-qV_i/k_B T} \qquad I_s \ll 1,$$

where in the argument of the exponential function we have the input voltage. Considering that

$$v_o = -Ri\,,$$

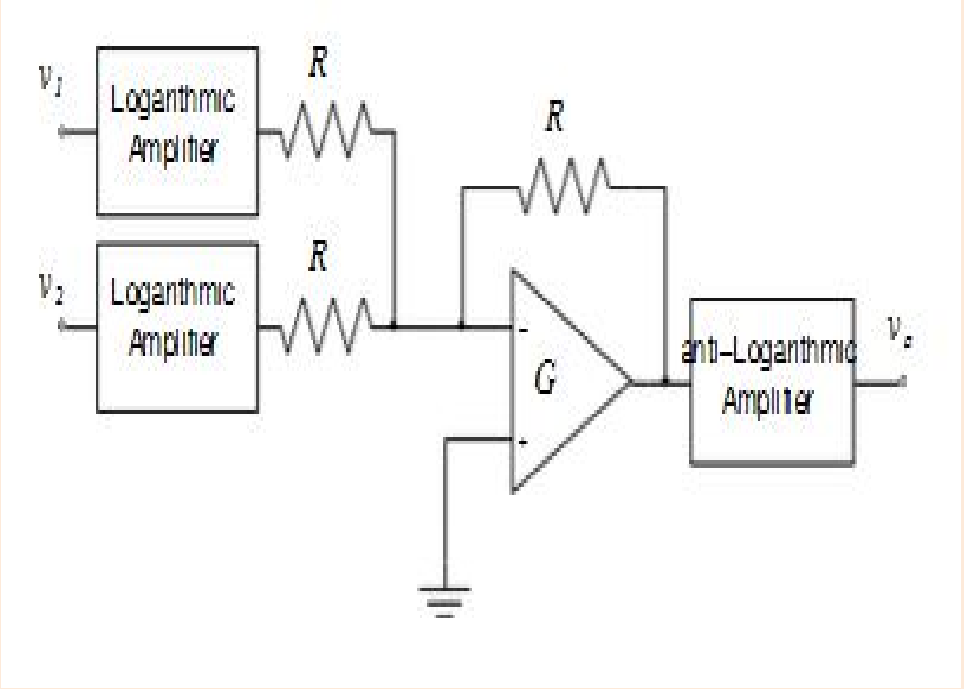
thus

$$v_o \simeq -RI_s e^{-qV_i/k_B T}.$$

If the input v_i is negative, we have to reverse the diode's connection or replace the BJT with a pnp BJT.

Logarithmic Multiplier

Analog multiplier based on a two log one antilog and one adder circuits.



Questions

Flow of electrons is generally termed as __.

A ___is a material which offers very little resistance to theflow of current through it.

A silicon diode measures a low value of resistance with the meter leads in both positions. The trouble, if any, is

The materialswhich behave like perfect insulators at low temperatures & athigher temperatures, they behave like

Under normal conditions a diode conducts current when it is

The movement of free electrons in a conductor is called

An n-type semiconductor material

The boundary between p-type material and n-type material is called

You have an unknown type of diode in a circuit. You measure the voltage across it and find it to be 0.3 V. The diod

What type of impurities are to be added to form a P type semiconductors ?

Doping of a semiconductor material means

What occurs when a conduction-band electron loses energy and falls back into a hole in the valence band?

The term bias in electronics usually means

How many valence electrons does a silicon atom have?

Which capacitance dominates in the forward-bias region?

What is the Cut in volatage of Silicon diode?

Germanium Knee Volage is

Intrinsic Semiconductor means

Under normal conditions a diode conducts current when it is

Reverse breakdown is a condition in which a diode

There is a small amount of current across the barrier of a reverse-biased diode. This current is called

Since diodes are destroyed by excessive current, circuits must have:

Why is heat produced in a diode?

The diode schematic arrow points to the:

The voltage where current may start to flow in areverse-biased pn junction is called the

The area at the junction of p-type and n-type materials that has lost its majority carriersis called the

DC power should be connected to forward bias a diode as follows:

A diode for which you can change the reverse bias, and thus vary the capacitance is called a

Avalanche breakdown results basically due to

The varactor diode is usually

The diode in which impurities are heavily doped is

The depletion region in a Junction Diode contains

Varactor diodes are used in FM receivers to obtain:

As the forward current through a silicon diode increases, the internal resistance

Reverse breakdown is a condition in which a diode

There is a small amount of current across the barrier of a reverse-biased diode. This current is called

What is the state of an ideal diode in the region of nonconduction?

Schottky diodes are also known as

zener breakdown refers to

What kind of diode is formed by joining a doped semiconductor region with a metal?

An intrinsic semiconductor at the absolute zero temperature

A pn junction allows current flow when

The forward characteristics curve of a diode grows in _____ form.

The reverse-saturation current level is typically measured in

Varying the _____ can control the location of the Zener region.

The _____ the current through a diode, the _____ the dc resistance level.
The reverse-bias current _____ with the increase of temperature.
What is the resistor value of an ideal diode in the region of conduction?
Diodes are connected _____ to increase the current-carrying capacity
A Zener diode:
Avalanche breakdown in semiconductor diode occurs when
The varactor diode is usually
Zener diodes are:
The capacitance of a varactor diode increases when the reverse voltage across it
The diode with a forward voltage drop of approximately 0.25 V is the
Since diodes are destroyed by excessive current, circuits must have:
Drift current is influenced by
What type of diode is commonly used in electronic tuners in TVs?
Which diode employs graded doping?
A PNPN diode is a

opt1
Electric current
good conductor
the diode is open.
good conductor
reverse-biased.
voltage.
is intrinsic.
a diode.
a silicon diode.
Trivalent
that a glue-type substance is added to hold the material together.
doping
the value of ac voltage in the signal.

1

Diffusion
0.5V
0.3V
Pure Semicionductor
reverse-biased
is subjected to a large reverse voltage
forward-bias current
higher voltage sources
due to current passing through the diode
trivalent-doped material
breakdown voltage
barrier potential
– anode, + cathode
varactor diode
impact ionisation
Forward biased
Varactor diode
only charge carriers
Automatic frequency control
increases.
is subjected to a large reverse voltage.

forward-bias current.
An open circuit
PIN diodes.
Reverse bias region
laser
behaves like a metallic conductor
the p-type material is more positive than the n-type material
linear
pA
forward current

higher, lower
decreases

0

in series
Has a high forward voltage rating
Reverse bias exceeds a certain value
Forward biased
Specially doped p–n junctions
Decreases
Step-recovery diode
current limiting resistors
magnitude of voltage
varactor
zener
negative resistence device

opt2
electric shock
insulator
the diode is shorted to ground.
insulator
forward-biased.
current.
has trivalent impurity atoms added.
a reverse-biased diode.
a germanium diode.
Pentavalent
that impurities are added to increase the resistance of the material.
recombination
the condition of current through a pn junction.

Transition
0.6V
0.4V
Impure Semiconductor
forward-biased
is reverse-biased and there is a small leakage current
reverse breakdown current
current limiting resistors
due to voltage across the diode
positive axial lead
barrier potential
depletion region
– cathode, – anode
tunnel diode
strong electric field across the junction
reverse biased
PIN diode
no charge at all
Automatic gain control
decreases.
is reverse-biased and there is a small leakage current.
reverse breakdown
current.
A short circuit
hot carrier diodes.
Forward bias region
tunnel
behaves like an insulator
the n-type material is more positive than the p-type material
exponential
μA
doping levels

lower, lower
increases
5 k
in parallel-series
Is useful as an amplifier
Forward bias exceeds a certain value
Reverse biased
Normally doped p–n junctions
Increases
Schottky diode
more dopants
concentration of carriers
Schottky
LED
voltage controllable device

opt3

semiconductor

semiconductor

the diode is internally shorted.

semiconductor

avalanched.

recombination.

has pentavalent impurity atoms added.

a pn junction.

a forward-biased silicon diode.

Octavalent

that impurities are added to decrease the resistance of the material.

generation

the value of dc voltages for the device to operate properly.

3

Depletion

0.7V

0.5V

Non doped Conductor

avalanched

has no current flowing at all

conventional current

more dopants

due to the power rating of the diode

anode lead

forward voltage

n region

+ anode, – cathode

zener diode

emission of electrons

Unbiased

Tunnel diode

vacuum, and no atoms at all

Automatic volume control

remains the same.

has no current flowing at all.

conventional

current.

Unpredictable

step-recovery diodes.

no bias

pin

has a large number of holes

both the n-type and p-type materials have the same potential

logarithmic

mA

forward voltage

lower, higher
remains the same
Undefined
in parallel-series
Has a sharp breakdown at low reverse voltage
Forward current exceeds a certain value
un biased
Lightly doped p–n junctions
Breaks down
Back diode
higher voltage sources
concentration gradient of carriers
LED
tunnel
current controllable negative resistence device

opt4
none of the above
none of the above
the diode is working correctly.
none of the above
saturated.
equilibrium.
requires no doping.
a forward-biased diode.
a reverse-biased germanium diode.
Divalent
that all impurities are removed to get pure silicon.
combination
the status of the diode.

4

None of the above
0.3V
None of these
Both A & C
saturated
is heated up by large amounts of current in the forward direction
reverse leakage current
higher current sources
due to the PN junction of the diode
cathode lead
biasing voltage
p region
+ cathode, + anode
switching diode
rise in temperature
holes and electronics
Zener diode
only ions i.e., immobile charges
None of the above
increases & decreases
is heated up by large amounts of current in the forwarddirection.
reverse leakage
current.
Undefined
tunnel diodes.
depletion region
Schottky
has a large number of electrons
there is no potential on the n-type or p-type materials
sinusoidal
A
dc resistance

higher, higher
None of the above
Infinity
in parallel
None of the above
the potential barrier is reduced to zero
in the breakdown region
None of the above
Stores charges
Constant-current diode
higher current sources
forward-bias current.
Gunn
step-recovery
switching device

opt5

opt6

Answer

Electric current
good conductor
the diode is internally shorted.
semiconductor
forward-biased.
current.
has pentavalent impurity atoms added.
a pn junction.
a germanium diode.
Trivalent
that impurities are added to decrease the resistance of the material.
recombination
the value of dc voltages for the device to operate properly.
4
Diffusion
0.7V
0.3V
Both A & C
forward-biased
is subjected to a large reverse voltage
reverse leakage current
current limiting resistors
due to current passing through the diode
cathode lead
breakdown voltage
depletion region
+ anode, – cathode
varactor diode
impact ionisation
reverse biased
Tunnel diode
only ions i.e., immobile charges
Automatic frequency control
decreases.
is subjected to a large reverse voltage.

reverse leakage current.
An open circuit
hot carrier diodes.
Reverse bias region
Schottky
behaves like an insulator
the p-type material is more positive than the n-type material
exponential
μA
doping levels

lower, higher
increases
0
in parallel
Has a sharp breakdown at low reverse voltage
Reverse bias exceeds a certain value
Reverse biased
Specially doped p–n junctions
Decreases
Schottky diode
current limiting resistors
magnitude of voltage
varactor
step-recovery
switching device

Questions

When transistors are used in digital circuits they usually operate in the

A transistor has a of 250 and a base current, IB, of 20 A. The collector current, IC, equals:

A current ratio of IC/IE is usually less than one and is called:

In a C-E configuration, an emitter resistor is used for:

To operate properly,a transistor's base-emitter junction must be forward biased with reverse bias applied to which

the C-B configuration is used to

provide which type of gain?

A transistor may be used as a switching device or as a:

If an input signal ranges from 20–40 A (microamps), with an output signal ranging from .5–1.5 mA (milliamps), wh

Which is beta's current ratio?

A collector characteristic curve is a graph showing:

With low-power transistor packages, the base terminal is usually the:

When a silicon diode is forward biased, what is V BE for a C-E configuration?

What is the current gain for a common-base configuration where IE = 4.2 mA and IC = 4.0 mA?

With a PNP circuit, the most positive voltage is probably:

If a 2 mV signal produces a 2 V output, what is the voltage gain?

The term BJT is short for

Most of the electrons in the base of an NPN transistor flow:

In a transistor, collector current is controlled by:

Total emitter current is:

Often a common-collector will be the last stage before the load; the main function(s) of this stage is to:

For a C-C configuration to operate properly, the collector-base junction should be reverse biased, while forward b

The input/output relationship of the common-collector and common-base amplifiers is:

At saturation the value of VCE is nearly _____, and IC = _____.

In which operation region(s) does the Ebers-Moll model describe a bipolar transistor?

Transistor act as a?

The part of the transistor which is heavily doped to produce large number of majority carriers is

A BJT is a _____-controlled device.

In a transistor

The principal advantage(s) of BJTs over MOSFETs is (are) that

What is the ratio of IC to IB?

For normal operation of a pnp BJT, the base must be _____ with respect to the emitter and _____ with res

The term BJT is short for

For a silicon transistor, when a base-emitter junction is forward-biased, it has a nominal voltage drop of

What are the two types of bipolar junction transistors?

What is the order of doping, from heavily to lightly doped, for each region?

in what range of voltages is the transistor in the linear region of its operation?

What is (are) common fault(s) in a BJT-based circuit?

The dc load line on a family of collector characteristic curves of a transistor shows the

How many layers of material does a transistor have?

In which region are both the collector-base and base-emitter junctions forward-biased?

Which of the following is (are) the terminal(s) of a transistor?

Transistors are _____-terminal devices.

How many carriers participate in the injection process of a unipolar device?

In what decade was the first transistor created?

Which component of the collector current IC is called the leakage current?

Clipping is the result of
In a NPN transistors Collector is
In a NPN transistors emitter is
In a NPN transistors base is
When a transistor is used as a switch, it is stable in which two distinct regions?
At which of the following condition(s) is the depletion region uniform?
Clipping is the result of
alpha refers to
Beta refers to
gamma refers to
In a transistor, collector current is controlled by:
How much is the base-to-emitter voltage of a transistor in the "on" state?
Which of the following equipment can check the condition of a transistor?
For what kind of amplifications can the active region of the common-emitter configuration be used?
A transistor can be checked using a(n) _____.

opt1
active region
500 A
beta
stabilization
collector-emitter

voltage
fixed resistor
0.05
IC/IB
emitter current (IE) versus collector-emitter voltage (VCE) with (VBB) base bias voltage held constant
tab end
voltage-divider bias
16.8
ground
0.001
base junction transistor
out of the base lead
collector voltage
IE – IC
provide voltage gain
collector-emitter
270 degrees
zero, zero
Forward active.
conductor
emitter
current
$\beta = \alpha / (\alpha + 1)$
voltage drop across the transistor is important.
DC
positive, negative
base junction transistor
0.7 V.
npn and pnp
base, collector, emitter
0 < VCE
opens or shorts internal to the transistor
saturation region.
1
Active
Emitter
2
1
1930s
Majority

the input signal being too large
Heavily doped
Heavily doped
Heavily doped
saturation and active
No bias
the input signal being too large.
Ic/Ib
Ic/Ib
1+alfha
collector voltage
0 V
Current tracer
Voltage
curve tracer

opt2
breakdown region
5 mA
theta
ac signal bypass
base-collector

current
tuning device
20
VCC
collector current (IC) versus collector-emitter volt
middle
0.4 V
1.05
VC
0.004
binary junction transistor
into the collector
base current
IC + IE
provide phase inversion
base-emitter
180 degrees
VCC, IC(sat)
Saturation.
semi-conductor
base
voltage
$\beta = \alpha / (1 - \alpha)$
they are not as prone to ESD.
hFE
positive, positive
binary junction transistor
0.3 V.
pnn and nnp
emitter, collector, base
0.7 < VCE < VCE(max)
open bias resistor(s)
cutoff region.
2
Cutoff
Base
3
2
1940s
Independent

the transistor being driven into saturation.
moderately doped
moderately doped
moderately doped
active and cutoff
VDS > 0 V
the transistor being driven into saturation
Ic/Ie
Ic/Ie
1-alpha
base current
0.7 V
Digital display meter (DDM)
Current
digital meter

opt3
saturation and cutoff regions
50 mA
alpha
collector bias
base-emitter

resistance
rectifier
50
IB/IE
collector current (I C) versus collector-emitter voltage (VC) with (VBB) base bi
right end
0.7 V
0.2
VBE
100
both junction transistor
into the emitter
collector resistance
IB + IC
provide a high-frequency path to improve the frequency response
collector-base
90 degrees
zero, I(sat)
Cut-off.
insulator
collector
-
α = β/ (β-1)
both of the above
DC
negative, positive
both junction transistor
0.2 V.
ppn and nnp
emitter, base, collector
VCE(max) > VCE
external opens and shorts on the circuit board
active region.
3
Saturation
Collector
4
3
1950s
Minority

the transistor being driven into cutoff.
lightly doped
lightly doped
lightly doped
saturation and cutoff
VDS = VP
the transistor being driven into cutoff.
Ie/Ic
Ie/Ic
1/alpha
collector resistance
0.7 mV
Ohmmeter (VOM)
Power
ohmmeter

opt4
linear region
0.208333333
omega
higher gain
collector-base

power
variable resistor
500
IE/IB
collector current (I C) versus collector-emitter voltage (VCC) with (VBB) base bias voltage held constant
stud mount
emitter voltage
0.95
VCC
1000
bipolar junction transistor
into the base supply
all of the above
IB – IC
buffer the voltage amplifiers from the low-resistance load and provide impedance matching for maximum power t
cathode-anode
0 degrees
VCC, zero
All of the above.
thermionic valve
any of the above depending upon the nature of transistor
-
α = (β+1)/β
none of the above
either DC or hFE, but not DC
negative, negative
bipolar junction transistor
VCC.
pts and stp
collector, emitter, base
none of the above
all of the above
all of the above
4
All of the above
All of the above
5
0
1960s
None of the above

all of the above
none of the these
none of the these
none of the these
none of the above
None of the above
all of the above
Ib/Ic
Ib/Ic
1/(1-alpha)
all of the above
Undefined
All of the above
All of the above
Any of the above

opt5

transfer

opt6

Answer

saturation and cutoff regions
5 mA
alpha
stabilization
collector-base

voltage
variable resistor
50
IC/IB
collector current (IC) versus collector-emitter voltage (V CE) with (VBB) base bias voltage held constant
middle
0.7 V
0.95
ground
1000
bipolar junction transistor
into the collector
base current
IB + IC
buffer the voltage amplifiers from the low-resistance load and provide impedance matching for maximum power t
collector-emitter
0 degrees
zero, I(sat)
All of the above.
thermionic valve
emitter
current
$\alpha = \beta/(\beta-1)$
both of the above
either DC or hFE, but not DC
negative, positive
bipolar junction transistor
0.7 V.
npn and pnp
emitter, collector, base
0.7 < VCE < VCE(max)
all of the above
all of the above
3
Saturation
All of the above
3
1
1940s
Minority

all of the above
moderately doped
Heavily doped
lightly doped
saturation and cutoff
No bias
all of the above
Ic/Ie
Ic/Ib
1+alfha
base current
0.7 V
All of the above
All of the above
Any of the above

transfer

Questions

When an input delta of 2 V produces a transconductance of 1.5 mS, what is the drain current delta?
When not in use, MOSFET pins are kept at the same potential through the use of:
D-MOSFETs are sometimes used in series to construct a cascode high-frequency amplifier to overcome the loss of
A MOSFET has how many terminals?
IDSS can be defined as:
With the E-MOSFET, when gate input voltage is zero, drain current is:
With a 30-volt VDD, and an 8-kilohm drain resistor, what is the E-MOSFET Q point voltage, with ID = 3 mA?
When an input signal reduces the
channel size, the process is called:
When applied input voltage varies the resistance of a channel, the result is called:
When is a vertical channel E-MOSFET used?
How will a D-MOSFET input impedance change with signal frequency?
What is the transconductance of an FET when ID = 1 mA and VGS = 1 V?
Which component is considered to be an "OFF" device?
For what value of ID is gm equal to 0.5 gm0?
Where do you get the level of gm and rd for an FET transistor?
The class D amplifier uses what type of transistors?
What is (are) the function(s) of the coupling capacitors C1 and C2 in an FET circuit?
What is the typical value for the input impedance Zi for JFETs?
MOSFETs make better power switches than BJTs because they have
MOSFET digital switching is used to produce which digital gates?
Which FET amplifier(s) has (have) a phase inversion between input and output signals?
MOSFET can be used as a
What limits the signal amplitude in an analog MOSFET switch?
Input resistance of a common- drain amplifier is
E-MOSFETs are generally used in switching applications because
For an FET small-signal amplifier, one could go about troubleshooting a circuit by _____.
The E-MOSFET is quite popular in _____ applications.
Material used for design of MESFET is
Secondary breakdown occurs in
CMOS is widely used in
In the transfer characteristics of a MOSFET, the threshold voltage is the measure of the
Input impedance of MOSFET is
MOSFET uses the electric field of
In MOSFET devices the N-channel type is better the P-channel type in the following respects
In a MOSFET, the polarity of the inversion layer is the same as that of the
Which of the following is expected to have highest input impedance?
Most small - signal E - MOSFETs are found in
Which insulating layer used in Fabrication of MOSFET?
What is used to higher the speed of operation in MOSFET fabrication?
A power MOSFET has three terminals called
MESFET can be operated on
The arrow on the symbol of MOSFET indicates
The operation of CCD is
What limits the signal amplitude in an analog MOSFET switch?
Input resistance of a common- drain amplifier is

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Which insulating layer used in Fabrication of MOSFET?
What is used to higher the speed of operation in MOSFET fabrication?
When an input delta of 2 V produces a transconductance of 1.5 mS, what is the drain current delta?
When not in use, MOSFET pins are kept at the same potential through the use of:
D-MOSFETs are sometimes used in series to construct a cascode high-frequency amplifier to overcome the loss of
A MOSFET has how many terminals?
IDSS can be defined as:
What is (are) the function(s) of the coupling capacitors C1 and C2 in an FET circuit?

opt1
666 mA
shipping foil
low output impedance
2 or 3
the minimum possible drain current
at saturation
6 V

enhancement
saturization
for high frequencies
As frequency increases input impedance increases.
1 kS
transistor
0 mA
from the dc biasing arrangement
JFETs
to create an open circuit for dc analysis
100 k
lower turn-off times.
inverters
common-gate
Current controlled capacitor
the switch input capacitance
RG || RIN(gate).
of their very low input capacitance.
viewing the circuit board for poor solder joints
digital circuitry
Gallium arsenide (GaAs)
MOSFET but not in BJT
Digital wrist watches
minimum voltage to induce a n-channel/p-channel for conduction
less than of FET but more than BJT.
gate capacitance to control the channel current.
it has better noise immunity.
charge on the gate electrode
MOSFET.
heavy - current applications.
Aluminium oxide
Ceramic gate
Collector, emitter and gate.
Enhancement mode (normally OFF) only
that it is a N-channel MOSFET
captures light and converts it to digital data
the switch input capacitance
RG || RIN(gate).

of their very low input capacitance.
the minimum possible drain current
at saturation
6 V

enhancement
saturization
heavy - current applications.
Aluminium oxide
Ceramic gate
666 mA
shipping foil
low output impedance
2 or 3
the minimum possible drain current
to create an open circuit for dc analysis

opt2
3 mA
nonconductive foam
capacitive reactance
3
the maximum possible current with VGS held at –4 V
zero
10 V
substrate
connecting
polarization
for high voltages
As frequency increases input impedance is constant.
1 mS
JFET
0.25 IDSS
from the specification sheet
BJTs
to isolate the dc biasing arrangement from the applied signal and load
1 M
lower on-state resistance.
NOR gates
common-drain
Voltage controlled capacitor
VGS(th)
RG + RIN(gate).
of their threshold characteristic (VGS(th)).
using a dc meter
high-frequency
Germanium
Both MOSFET and BJT
analogue circuits
minimum voltage till which temperature is constant
more than that of FET and BJT.
barrier potential of p-n junction to control the channel current.
it is faster.
minority carriers in the drain
JEFT amplifier.
discrete circuits.
Silicon Nitride
Silicon dioxide
Drain, source and gate.
Depletion mode only (normally ON) only
the direction of electrons
converts digital data
VGS(th)
RG + RIN(gate).

of their threshold characteristic (VGS(th)).
the maximum possible current with VGS held at –4 V
zero
10 V
substrate
connecting
polarization
discrete circuits.
Silicon Nitride
Silicon dioxide
3 mA
nonconductive foam
capacitive reactance

3

the maximum possible current with VGS held at –4 V
to isolate the dc biasing arrangement from the applied signal and load

opt3
0.75 mA
conductive foam
high input impedance

4

the maximum possible current with VGS held at 0 V
IDSS
24 V

gate charge
cutoff
for high currents
As frequency decreases input impedance increases.
1 k
D-MOSFET
0.5 IDSS
from the characteristics
MOSFETs
to create a short-circuit equivalent for ac analysis
10 M
a positive temperature coefficient.
NAND gates
common-source
Current controlled inductor
the switch's power handling
RG
of their high-frequency response capabilities.
applying a test ac signal
buffering
Silicon
BJT but not in MOSFET
high power circuits
minimum voltage to turn off the device
more than that of FET but less than BJT.
both (A) and (B).
it is TTL compatible.
majority carries in the substrate.
CE bipolar transistor.
disk drives.
Silicon dioxide
Silicon nitride
Drain, source and base.
Both Enhancement mode and Depletion mode
the direction of conventional current flow
project the data on screen
the switch's power handling
RG

of their high-frequency response capabilities.
the maximum possible current with VGS held at 0 V
IDSS
24 V

gate charge
cutoff
disk drives.
Silicon dioxide
Silicon nitride
0.75 mA
conductive foam
high input impedance

the maximum possible current with VGS held at 0 V
to create a short-circuit equivalent for ac analysis

opt4
0.5 mA
a wrist strap
inductive reactance
3 or 4
the maximum drain current with the source shorted
widening the channel
30 V

depletion
field effect
for high resistances
As frequency decreases input impedance is constant.
1 m Ω
E-MOSFET
IDSS
All of the above
any of the above
All of the above
1000 MΩ
all of the above
all of the above
all of the above
Voltage controlled inductor
VDS
RIN(gate).
of their power handling.
All of the above
All of the above
Zinc arsenide
None of these
all of the above
none of the above mentioned is true
less than that of FET and BJT.
none of these.
it has better drive capability.
majority carries in the source .
Common collector bipolar transistor
integrated circuit.
None of the mentioned
Poly silicon gate
Collector, emitter and base.
None of the above
that it is a P-channel MOSFET
Captures light
VDS
RIN(gate).

of their power handling.
the maximum drain current with the source shorted
widening the channel
30 V

depletion
field effect
integrated circuit.
None of the mentioned
Poly silicon gate
0.5 mA
a wrist strap
inductive reactance
3 or 4
the maximum drain current with the source shorted
All of the above

opt5 **opt6**

Answer

3 mA
conductive foam
high input impedance
3 or 4
the maximum possible current with VGS held at 0 V
zero
6 V

depletion
field effect
for high currents
As frequency decreases input impedance increases.
1 mS
E-MOSFET
0.25 IDSS
All of the above
MOSFETs
All of the above
1000 MΩ
all of the above
all of the above
common-source
Voltage controlled capacitor
VGS(th)
RG || RIN(gate).
of their threshold characteristic (VGS(th)).
All of the above
All of the above
Gallium arsenide (GaAs)
BJT but not in MOSFET
Digital wrist watches
minimum voltage to induce a n-channel/p-channel for conduction
more than that of FET and BJT.
gate capacitance to control the channel current.
it is faster.
majority carries in the source .
MOSFET.
integrated circuit.
Silicon dioxide
Poly silicon gate
Drain, source and gate.
Both Enhancement mode and Depletion mode
the direction of electrons
captures light and converts it to digital data
VGS(th)
RG || RIN(gate).

of their threshold characteristic (VGS(th)).
the maximum possible current with VGS held at 0 V
zero
6 V

depletion
field effect
integrated circuit.
Silicon dioxide
Poly silicon gate
3 mA
conductive foam
high input impedance
3 or 4
the maximum possible current with VGS held at 0 V
All of the above

Questions

A differential amplifier
When a differential amplifier is operated single-ended,
In differential-mode
In the common-mode
The common-mode gain is
The differential gain is
If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is
With zero volts on both inputs, an OPamp ideally should have an output
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is
The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is
A common-mode signal is applied to
The common-mode voltage gain is
The input stage of an OP-amp is usually a
Current cannot flow to ground through
Which of the following electrical characteristics is not exhibited by an ideal op-amp?
An ideal op-amp requires infinite bandwidth because
Ideal op-amp has infinite voltage gain because
Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages
How will be the output voltage obtained for an ideal op-amp?
Which is not the ideal characteristic of an op-amp?
Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
Which factor determine the output voltage of an op-amp?
The opamp can amplify
In a nonlinear op-amp circuit, the
The input signal for an instrumentation amplifier usually comes from
In a differential amplifier, the CMRR is limited mostly by the
A common - mode signal is applied to
The common-mode voltage gain is
The input stage of an op amp is usually a
The common - mode rejection ratio is
A 741 C has
The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
The voltage gain of a loaded differential amp is
At the unity-gain frequency, the open-loop voltage gain is
The tail current in a differential amplifier equals
A common - mode signal is applied to
An instrumentation amplifier has a high
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
An ideal op-amp requires infinite bandwidth because
With zero volts on both inputs, an OPamp ideally should have an output
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is

The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is
A common-mode signal is applied to
The common-mode voltage gain is
The input stage of an OP-amp is usually a
Current cannot flow to ground through
Which of the following electrical characteristics is not exhibited by an ideal op-amp?
An ideal op-amp requires infinite bandwidth because
The common-mode gain is
The differential gain is
If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is
With zero volts on both inputs, an OPamp ideally should have an output
The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
Current cannot flow to ground through

opt1

is a part of an OP-amp
the output is grounded
opposite polarity signals are applied to the inputs
both inputs are grounded
very high
very high
1225
equal to the positive supply voltage
1
700 nA
90 V/ µs
the non-inverting in
smaller than differential voltage gain
differential amplifier
a mechanical ground
Infinite voltage gain
Signals can be amplified without attenuation
To control the output voltage
$V_O = V_1 - V_2$
Amplifies the difference between the two input voltages
Input Resistance –> 0
8v
Both positive and negative saturation voltage
AC signals only
opamp never saturates
an inverting amplifier.
CMRR of the opamp
the non - inverting input.
smaller than the voltage gain.
differential amp.
very low.
a voltage gain of 100,000.
single - ended input and single-ended output
less than the input bias current.
input offset current.
large than the unloaded voltage gain.
1
difference between two emitter currents
the non - inverting input.
output impedance
1
Signals can be amplified without attenuation
equal to the positive supply voltage
1
700 nA

90 V/ µs
the non-inverting in
smaller than differential voltage gain
differential amplifier
a mechanical ground
Infinite voltage gain
Signals can be amplified without attenuation
very high
very high
1225
equal to the positive supply voltage
single - ended input and single-ended output
less than the input bias current.
input offset current.
a mechanical ground

opt2

has one input and one output
one input is grounded and signal is applied to the other
the gain is one
the outputs are connected together
very low
very low
10,000
equal to the negative supply voltage
2000
99.3 μA
0.67 V/ μs
the inverting input
equal to differential voltage gain
class B push-pull amplifier
an a.c. ground
Infinite bandwidth
Output common-mode noise voltage is zero
To obtain finite output voltage
$V_O = A \times (V_1 - V_2)$
Amplifies individual voltages input voltages
Output impedance –> 0
4v
Positive saturation
DC signals only.
feedback loop is never opened
resistor
gain - bandwidth product.
the inverting input.
equal to the voltage gain.
class B push-pull amplifier.
as high as possible.
an input impedance of 2 MΩ.
single - ended input and differential output.
equal to zero.
input bias current.
equal to R_C / r_e.
$A_{V(mid)}$.
sum of two emitter currents
the inverting input.
power gain.
2000
Output common-mode noise voltage is zero
equal to the negative supply voltage
2000
99.3 μA

0.67 V/ µs
the inverting input
equal to differential voltage gain
class B push-pull amplifier
an a.c. ground
Infinite bandwidth
Output common-mode noise voltage is zero
very low
very low
10,000
equal to the negative supply voltage
single - ended input and differential output.
equal to zero.
input bias current.
an a.c. ground

opt3

has two outputs
both inputs are connected together
the outputs are of different amplitudes
an identical signal appears on both inputs
always unity
dependent on input voltage
80 dB
equal to zero
80 dB
49.7 μA
1.5 V/ μs
both inputs
greater than differential voltage gain
CE amplifier
a virtual ground
Infinite output resistance
Output voltage occurs simultaneously with input voltage changes
To receive zero noise output voltage
$V_O = A \times (V_1 + V_2)$
Amplifies products of two input voltage
Bandwidth –> ∞
-4v
Negative saturation
both AC and DC signals
output shape is the same as the input shape.
differential amplifier.
supply voltages
both inputs.
greater than the voltage gain.
CE amplifier.
equal to the voltage gain.
an output impedance of 75 Ω
differential input and single - ended output.
less than the input offset voltage.
input offset voltage.
smaller than the unloaded voltage gain.
zero.
collector current divided by current gain
both inputs.
CMMR.
80 dB
Output voltage occurs simultaneously with input voltage changes
equal to zero
80 dB
49.7 μA

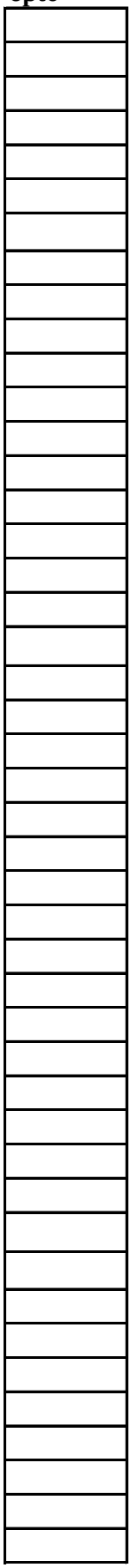
1.5 V/ µs
both inputs
greater than differential voltage gain
CE amplifier
a virtual ground
Infinite output resistance
Output voltage occurs simultaneously with input voltage changes
always unity
dependent on input voltage
80 dB
equal to zero
differential input and single - ended output.
less than the input offset voltage.
input offset voltage.
a virtual ground

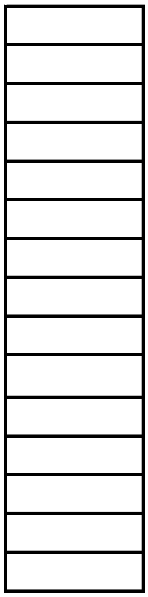
opt4
answers a and c
the output is not inverted
only one supply voltage is used
the output signals are in-phase
unpredictable
about 100
answers b and c
equal to the CMRR
100,000
none of these
none of these
top of the tail resistor
none of the above
swamped amplifier
an ordinary ground
Infinite slew rate.
Output can drive infinite number of device
None of the mentioned
$V_O = V_1 \times V_2$
None of the mentioned
Open loop voltage gain –> ∞
-2v
Supply voltage
neither AC not DC signals.
opamp may saturate.
Wheatstone bridge.
tolerance of the resistors
he top of the tail resistor
none of the above.
swamped amplifier.
equal to the common-mode voltage gain.
all of the above.
differential input and differential output
unimportant when a base resistor is used.
β.
impossible to determine.
very large
collector voltage divided by collector resistance
he top of the tail resistor
supply voltage.
100,000
Output can drive infinite number of device
equal to the CMRR
100,000
none of these

none of these
top of the tail resistor
none of the above
swamped amplifier
an ordinary ground
Infinite slew rate.
Output can drive infinite number of device
unpredictable
about 100
answers b and c
equal to the CMRR
differential input and differential output
unimportant when a base resistor is used.
β.
an ordinary ground

opt5

opt6





Answer

a and c
one input is grounded and signal is applied to the other
opposite polarity signals are applied to the inputs
an identical signal appears on both inputs
very low
very low
answers b and c
equal to zero
100,000
700 nA
0.67 V/ µs
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
To obtain finite output voltage
$V_O = A \times (V_1 - V_2)$
Amplifies the difference between the two input voltages
Input Resistance –> 0
-2v
Both positive and negative saturation voltage
both AC and DC signals
opamp may saturate.
Wheatstone bridge.
gain - bandwidth product.
both inputs.
greater than the voltage gain.
differential amp.
as high as possible.
all of the above.
differential input and single - ended output.
less than the input bias current.
input offset voltage.
equal to R_C / r_e.
1
sum of two emitter currents
both inputs.
CMMR.
100,000
Signals can be amplified without attenuation
equal to zero
100,000
700 nA

0.67 V/ µs
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
very low
very low
answers b and c
equal to zero
differential input and single - ended output.
less than the input bias current.
input offset voltage.
a virtual ground

Questions

A summing amplifier can have
An averaging amplifier has five inputs . The ratio R_f/R_i must be
In a scaling adder, the input resistors are
In an integrator , the feed back element is a
For step - in put , the out put of an integrator is a
In a differentiator , the feed back element is a
The output of the differentiator is proportional to
The voltage follower has a:
The ratio between differential gain and common-mode gain is called:
In an analog multiplier, the reference Voltage V_{ref} is internally set to ____
In one quadrant multiplier, the polarity of the input voltage V_x is _____ and V_y is_____
If $V_s = V_s \sin(2*pi*f_s*t)$ and $V_o = V_o \sin((2*pi*f_o*t) +\theta)$ are applied to a switch type phase detector, then the output consists of a DC term and the other term is _____
Division can be accomplished by placing the multiplier circuit in the _____ of the operational amplifier.
The input stage of Phase Locked Loop is_____
The Voltage Controlled Oscillator is also called as _____
The Voltage Controlled Oscillator is designed such that at zero voltage, it is oscillating at some initial frequency called _____ frequency.
Analog Multiplier produces an output which is a
The function of phase detector is to compare the _____ of the incoming signal to that of the output V_0 of Voltage Controlled Oscillator.
Phase detector is basically a _____.
The output of phase detector is _____.
The signal V_c shifts the frequency in a direction to reduce the difference between f_s and $f_{0.}$ Now the signal is in _____ range.
The VCO continues to change the frequency till its output frequency is _____the input signal frequency.
The range of frequencies over which the PLL can maintain the lock with the incoming signal is called _____ range.
The range of frequencies over which the PLL can acquire the lock with the incoming signal is called _____ range
The output frequency of Voltage Controlled Oscillator f_0 is _____
Voltage Controlled Oscillator is otherwise called as _____.
In PLL, the high frequency component (f_s+f_0) is removed by_____
Which of the following are the stages of PLL? i) free running ii) capture iii) tracking iv) pull in
Which of the following are the problems associated with the switch type phase detector? i) since the output voltage Ve is directly proportional to Vs, the phase detector gain and loop gain becomes dependent on the input signal amplitude. ii) output is proportional to cosΦ which makes it non linear. iii) the circuit becomes unstable iv) full wave detector
In switch type phase detector, at the locked state ($f_s = f_0$) the phase shift should be _____ in order to get zero error signal.
In balanced modulator type phase detector, the transistors act as _____.
In balanced modulator type phase detector, the phase angle to voltage transfer co-efficient KΦ is _____

The Voltage to Frequency conversion factor of VCO is _____.
The output from a Phase Locked Loop system is _____.
If a divide by N - network is inserted between VCO output and phase comparator input of PLL, then in the locked state f0 is _____.
When PLL is used as AM demodulator, the AM signal is shifted in phase by _____ before being fed to the multiplier.
The other name for capture range is _____ range.
The other name for lock in range is _____ range.
The range of modulating input voltage applied to a VCO is _____.
Lock in range of a PLL is _____ the capture range.
Which of the following is the drawback of variable transconductance multiplier?
The time taken for a PLL to capture the incoming signal is called _____ time.
If the voltage at the modulation input of VCo is biased at 7/8 Vcc then the output frequency of VCO in PLL is given by f0 = _____.
The maximum operated range of PLL 565 is_____.
The Lock in range of Phase Locked Loop is _____.
If the offset frequency f_1 is applied to the phase detector of frequency translator circuit, then at the locked state f0 is given by _____.
_____ filter controls the capture range and lock in range of PLL.
The operating voltage range of IC 565 is _____.
An external capacitor connected across IC 565 will act as _____.
If V_c shifts the VCO frequency from the free running frequency f_0 to a frequency f, then the new frequency shift from VCO in a PLL is _____.
A _____ is an electronic system which generates any range of frequencies from a single fixed time base or oscillator.
Phase detector is basically a _____.
In PLL, the output of the error amplifier is equal to the _____.
Select correct statement of PLL.
The Voltage to Frequency Converter of VCO is defined as ____
IC 566 functions as_____.
The total time taken by PLL to establish the lock is called _____.
If the frequency of the carrier wave is varied in accordance with the modulating signal, then the modulation refers to _____ modulation
The capture range of PLL is defined as _____.
The lock in range of PLL is defined as _____.

opt1	opt2
only one input	only two inputs
5	0.2
all of the same value	all of different values
resistor	capacitor
pulse	triangular wave form
resistor	capacitor
the RC time constant	the rate at which the input is changing
closed-loop voltage gain of unity	small open-loop voltage gain
Amplitude	differential-mode rejection
15V	5V
positive, negative.	positive, positive
f_o	$2* f_o$
feedback loop	inverting input terminal
Low Pass Filter	Error Amplifier
relaxation oscillator	free running multivibrator
free running	cut off
product of two input signals divided by a reference voltage.	product of two input signals and reference voltage.
phase and frequency	phase
summer	subtractor
f_s+f_0	f_s-f_0
lock-in	capture
less than	exactly the same as
tracking	capture
tracking	capture
$(V_{cc}-v_c)/(R_T*C_T*V_{cc})$	$v_c/(R_T*C_T*V_{cc})$
voltage to frequency converter	voltage to time converter
high pass filter	low pass filter
only i and ii	only ii and iv
i and ii	i,ii and iii
0º	180º
switch	amplifier
$(I_Q*R_L)/ pi$	$V_0/(2*pi)$

f_0 / V_{CC}	$8*f_0 / V_{CC}$
voltage or frequency	only voltage
f_s /N	$N*f_s$
0º	180º
tracking	lock in
tracking	acquisition
0.5 V_{CC} to V_{CC}	0.75 V_{CC} to V_{CC}
greater than	equal to
inaccurate	costly
pull out	capture
$0.25/ (R_T*C_T)$	$(R_T*C_T)/4$
0 to 500 kHz	0.001 to 500 kHz
$\Delta f_L = 7.8 f_0/v$	$\Delta f_L = +/- (7.8 f_0/v)$
fs	fs * f_1
high pass filter	low pass filter
+/- 6V to +/-12V	+/- 10V to +/-12V
passive device	low pass filter
$f_0 + k_v*Vc$	$f_0 - k_v*Vc$
frequency multiplier	frequency synthesizer
summer	subtractor
error voltage	applied voltage
capture range is smaller than lock in range	capture range is greater than lock in range
$\Delta V_c /\Delta f_0$	Δf_0
phase detector	low pass filter
pull in time	pull out time
frequency shift keying	frequency
$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10\text{^}3))\}^{1/2}$	$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C)\}^{1/2}$
$\Delta f_L = +/- (K_v*K_\Phi)$	$\Delta f_L = +/- (K_v*K_\Phi*A$

opt3	opt4
only three inputs	any number of inputs
1	2
each proportional to the weight of its input	related by a factor of two
zener diode	voltage divider
spike	ramp
zener diode	voltage divider
the amplitude of the input	both a and b
closed-loop bandwidth of zero	large closed-loop output impedance
common-mode rejection	phase
20V	10V
negative, negative	negative positive
$f_o/ 2$	$3* f_o$
output	non inverting terminal
Voltage Controlled Oscillator	Phase Detector
monostable multivibrator	phase shift oscillator
capture	free cycle
product of three input signals.	product of two input signals.
frequency	amplitude
multiplier	divider
f_s*f_0	f_s+/ f_0
free running	unlocked
greater than	twice that of
free running	pull in
free running	pull in
$2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})$	$1/(R_T*C_T)$
voltage to current converter	frequency to voltage converter
band pass filter	band reject filter
i, ii and iii	only iv
ii,iii	only i
270º	90º
oscillator	modulator
$(4*I_Q*R_L)/pi$	$(I_Q*R_L)/2*pi$

$2*f_0 / V_{CC}$	$4*f_0 / V_{CC}$
only frequency	only phase.
f_s+N	f_s –N
270º	90º
free running	acquisition
free running	capture
0 V_{CC} to V_{CC}	0.25 V_{CC} to V_{CC}
lesser than	less than or equal to
difficult to integrate in IC	scale factor depends on temperature which affects the output
lock in	pull in
$4(R_T*C_T)$	$(R_T*C_T)/0.25$
100 to 400 kHz	10 to 400 kHz
$\Delta f_L = +/- (8.7 f_0/v)$	$\Delta f_L = 8.7 f_0/v$
fs + f_1	fs - f_1
band pass filter	band reject filter
+/- 8V to +/-12V	+/- 12V
charging device	discharging device
k_v*Vc	Vc
frequency doubler	frequncy translator
multiplier	divider
control voltage	power supply voltage
capture range is equal to lock in range	capture range is not equal to lock in range
ΔV_c	$\Delta f_0/\Delta V_c$
VCO	PLL
rise time	hold time
amplitude	phase
$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10\^3))\}$	$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C)\}$
$\Delta f_L = +/- (K_v*K_\Phi)/(A*(pi/2))$	$\Delta f_L = +/- (K_v*K_\Phi*A*(pi/2))$

opt5	opt6	Answer
		any number of inputs
		0.2
		each proportional to the weight of its input
		capacitor
		ramp
		resistor
		both a and b
		closed-loop voltage gain of unity
		common-mode rejection
		10V
		positive, positive
		$2* f_o$
		feedback loop
		Phase Detector
		free running multivibrator
		free running
		product of two input signals divided by a reference voltage.
		phase and frequency
		multiplier
		f_s+/ f_0
		capture
		exactly the same as
		tracking
		capture
		$2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})$
		voltage to frequency converter
		low pass filter
		i, ii and iii
		i and ii
		90º
		switch
		$(4*I_Q*R_L)/pi$

		$8*f_0 / V_{CC}$
		voltage or frequency
		$N*f_s$
		90^o
		acquisition
		tracking
		$0.75\ V_{CC}$ to V_{CC}
		greater than
		scale factor depends on temperature which affects the output
		capture
		$0.25/ (R_T*C_T)$
		0.001 to 500 kHz
		$\Delta f_L = +/- (7.8 f_0/v)$
		$fs + f_1$
		low pass filter
		+/- 6V to +/-12V
		low pass filter
		$f_0 + k_v*Vc$
		frequency synthesizer
		multiplier
		control voltage
		capture range is smaller than lock in range
		$\Delta f_0/\Delta V_c$
		VCO
		pull in time
		frequency
		$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10\text{^}3))\}^{1/2}$
		$\Delta f_L = +/- (K_v*K_\Phi*A*(pi/2))$