KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University Established Under Section 3 of UGC Act 1956)

Pollachi Main Road, Eachanari Post,

Coimbatore – 641 021

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LECTURE PLAN

NAME OF THE STAFF : Dr.K.G.Dharani

DESIGNATION : ASSOCIATE PROFESSOR

CLASS : B.E-IV YEAR ECE

SUBJECT : ASIC DESIGN

SUBJECT CODE : 16BEEC8E04

S.No	TOPICS TO BE COVERED	TIME DURATION	SUPPORTING MATERIALS	TEACHING AIDS
UNIT-I INTRODUCTION TO ASICs				
1	Introduction to ASICs	2	T1,Pg :No-1 to 4	PPT , BB
2	Full-custom	1	T1,Pg :No-5 to 10	PPT , BB
3	Semi-custom	1	T1,Pg :No-10 to 16	PPT , BB
4	ASIC Design	1	T1,Pg :No-16 to 35	PPT , BB
5	CMOS logic	2	T1,Pg :No-39 to 60	PPT , BB
6	ASIC library design	2	T1,Pg :No-117 to 130	PPT , BB
Introduction		**02**		
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-II PROGRAMMABLE ASICs				
7	Programmable ASICs	1	T1,Pg :No-169 to 170	PPT , BB
8	Anti fuse	1	T1,Pg :No-170 to 172	PPT , BB
9	Static RAM	1	T1,Pg :No-174	PPT , BB
10	EPROM and Technology	1	T1,Pg :No-174	PPT , BB
11	Actel ACT–Xilinx LCA	1	T1,Pg :No-191 to 193	PPT , BB
12	Altera flex	1	T1,Pg :No-209	PPT , BB
13	Altera MAX Logic cells	1	T1,Pg :No-209	PPT , BB
14	I/O cells–Interconnects	1	T1,Pg :No-232 to 240	PPT , BB
15	Low level design entry: Schematic entry.	1	T1,Pg :No-327	PPT , BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-III SIMULATION AND SYNTHESIS				
16	Logic synthesis: A comparator MUX	01	T1,Pg :No-561	BB, PPT
17	Inside a logic synthesizer	01	T1,Pg :No-569	BB, PPT
18	VHDL	01	T1,Pg :No-593	BB, PPT
19	Logic synthesis	01	T1,Pg :No-594 to 600	PPT ,BB
20	FSM synthesis	01	T1,Pg :No-605	PPT ,BB
21	Memory synthesis	01	T1,Pg :No-611,612	PPT ,BB
22	Simulation	01	T1,Pg :No-641	BB, PPT
23	Types of simulation	01	T1,Pg :No-641 to 647	BB, PPT
24	Logic systems	01	T1,Pg :No-656	BB, PPT
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-IV ASIC TESTING				
25	Boundary scantest	01	T1,Pg :No-714 to 724	BB, PPT
26	Faults–Fault simulation	01	T1,Pg :No-736 to 741	BB, PPT
27	Automatic test pattern generation algorithm	02	T1,Pg :No-755 to 756	BB, PPT
28	D- algorithm	02	T1,Pg :No-755	BB, PPT
29	PODEM	01	T1,Pg :No-759	BB, PPT
30	Built in self-test	02	T1,Pg :No-766	BB, PPT
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT-V ASIC CONSTRUCTION				
37	System partitioning	01	T1,Pg :No-809	BB, PPT
38	power dissipation	02	T1,Pg :No-816	BB, PPT
39	partitioning methods	02	T1,Pg :No-824	BB, PPT
40	floor planning and placement	02	T1,Pg :No-853 to 856, 873	BB, PPT
41	Routing: Global routing, detailed routing, special routing	01	T1,Pg :No- 910,922,935	BB, PPT
42	Introduction to SOC	01	T1,Pg :No-939	BB, PPT
Total Lecture Hours		**09**		
Total Hours		**09**		

Total No of Hours for Introduction: 02Hrs

Total No of Lecture Hours Planned: 45 Hrs

Total No of Hours Planned : 45 Hours

TEXT BOOKS:

S.NO.	Author(s) Name	Title of the book	Publisher	Year of the publication
1	M.J.S.SMITH	"Application Specific Integrated Circuits"	Pearson Education	2006
2.	Wolf Wayne	FPGA based system design	Pearson Education	2005

REFERENCE BOOKS:

S.NO.	Author(s) Name	Title of the book	Publisher	Year of the publication
1.	M. Sarafzadehand C.K.Wong	An Introduction to VLSI Physical Design	McGraw Hill	1996
2.	JanM.Rabaey. Anantha Chandra kasan, Borivoje Nikolic	Digital Integrated Circuits	Prentice-Hall Publication	2002

STAFF IN-CHARGE **HOD/ECE**

ASIC Design

Objectives:

- To focus on the IC Design and the various design
- To understand the principles of design logic cells, I/O cells and interconnect architecture
- To explore the Application Specific Integrated Circuits (ASIC) design flow from the circuit and layout design point of view.
- To study about logic synthesis, placement and routing

Outcomes:

After completing this course the student will be able to

- Gain knowledge on various types of ASIC design
- Gain knowledge in the circuit design aspects at various levels of abstractions.
- Understand various architecture and its purpose in different application
- Understand placement, routing concepts in optimized IC design

Unit I Introduction To ASIC, CMOS Logic And ASIC Library Design

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

Unit II Programmable Asics, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

Unit III Programmable ASIC Architecture

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

Unit IV Logic Synthesis, Placement And Routing

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

Unit V High Performance Algorithms for ASIC / SOCs

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. Case Studies: Digital camera, SDRAM, High speed data standards.

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Suggested Readings:

1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.

2. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003

3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.

4. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008

5. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.

Weblinks:

https://www.electronics-notes.com/articles/electronic_components/programmable-logic/what-is-an-asic-application-specific-integrated-circuit.php

https://www.tce.edu/sites/default/files/PDF/14EC770-ASIC-DESIGN-K.Kalyani.pdf

ASIC LIBRARY DESIGN

3

Key concepts: Tau, logical effort, and the prediction of delay • Sizes of cells, and their drive strengths • Cell importance • The difference between gate-array macros, standard cells, and datapath cells

ASIC design uses predefined and precharacterized cells from a library—so we need to design or buy a cell library. A knowledge of ASIC library design is not necessary but makes it easier to use library cells effectively.

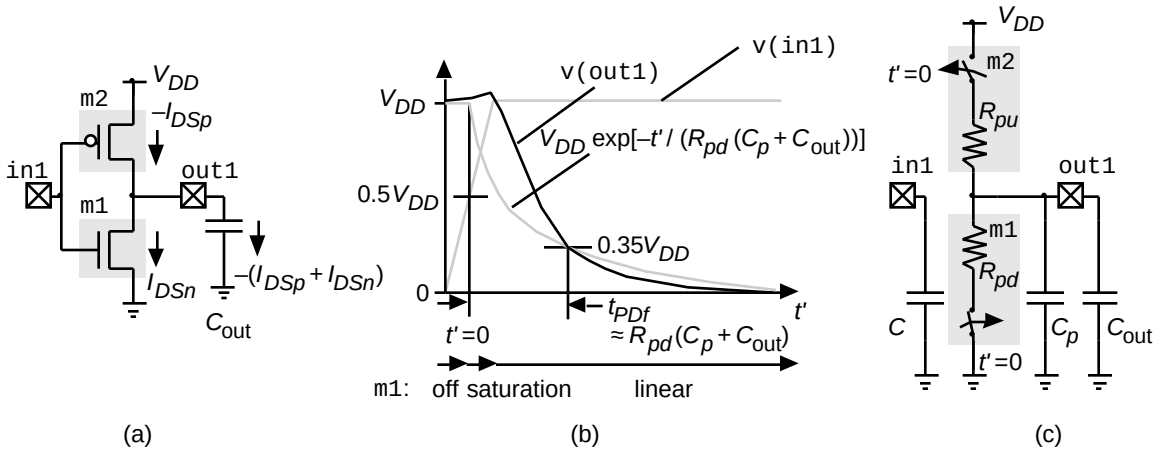
3.1 Transistors as Resistors

$$0.35V_{DD} = V_{DD} \exp \frac{-t_{PDf}}{R_{pd}(C_{out} + C_p)}$$

An output trip point of 0.35 is convenient because $\ln(1/0.35)=1.04 \approx 1$ and thus

$t_{PDf} = R_{pd}(C_{out} + C_p) \ln(1/0.35) \approx R_{pd}(C_{out} + C_p)$

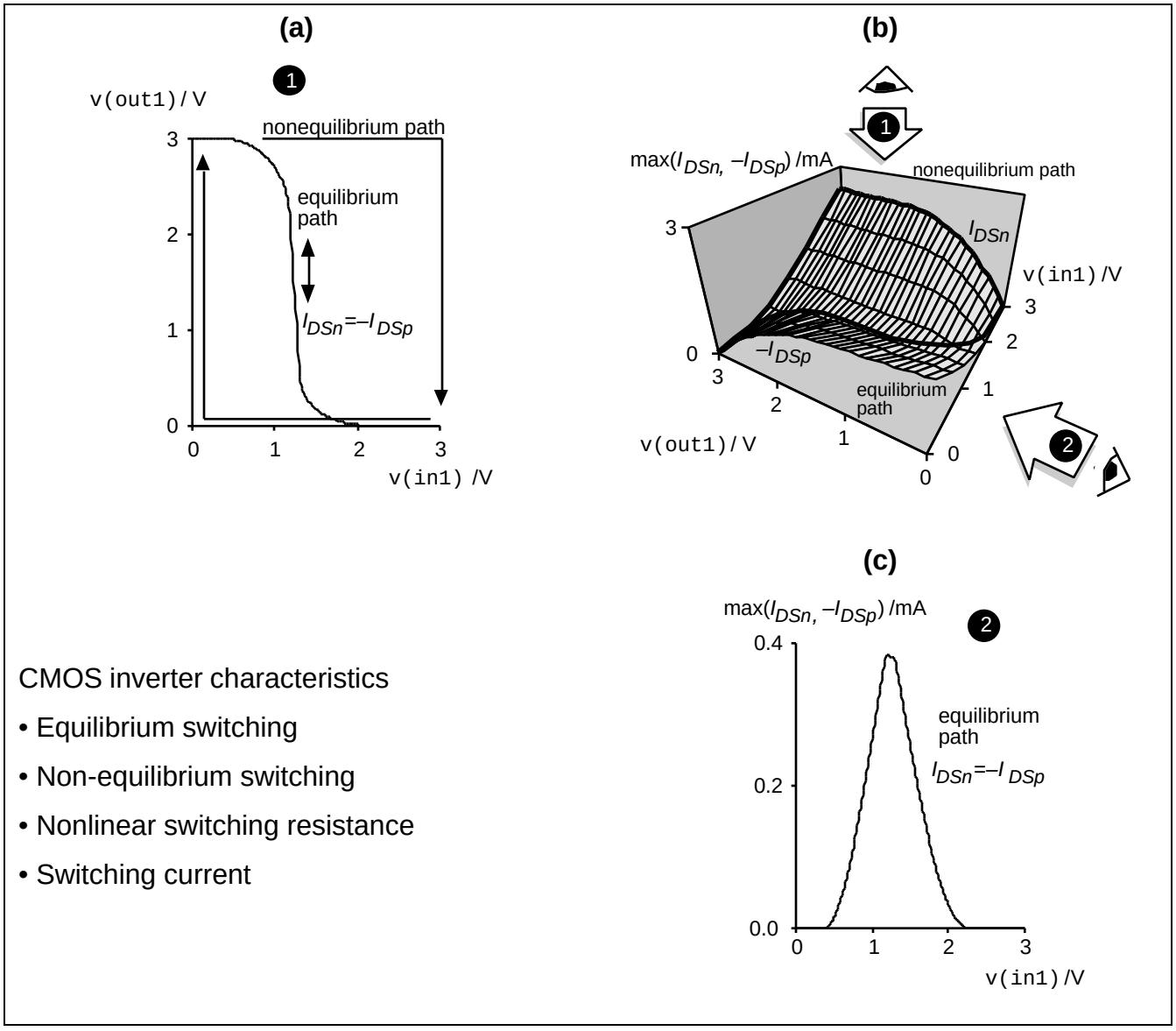
For output trip points of 0.1/0.9 we multiply by $-\ln(0.1) = 2.3$, because $\exp(-2.3) = 0.100$



(a) (b) (c)

A linear model for CMOS logic delay

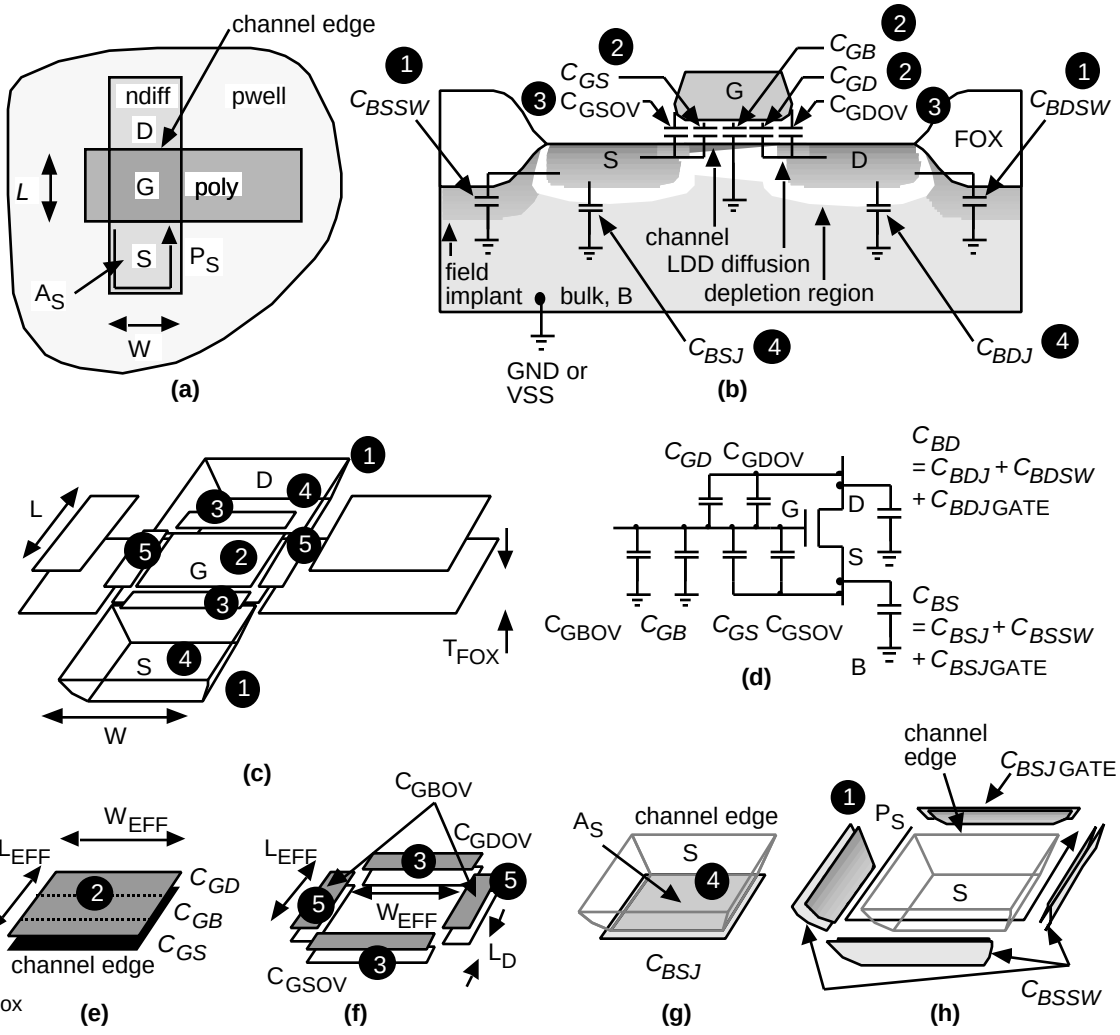
- Ideal switches = no delay • Resistance and capacitance causes delay
- Load capacitance, C_{out} • parasitic output capacitance, C_p • input capacitance, C
- Linearize the switch resistance • Pull-up resistance, R_{pu} • pull-down resistance, R_{pd}
- Measure and compare the input, `v(in1)` and output, `v(out1)`
- Input trip point of 0.5 • output trip points are 0.35 (falling) and 0.65 (rising)
- The linear prop–ramp model: falling propagation delay, $t_{PDf} \approx R_{pd}(C_p + C_{out})$



CMOS inverter characteristics

- Equilibrium switching
- Non-equilibrium switching
- Nonlinear switching resistance
- Switching current

3.2 Transistor Parasitic Capacitance



Transistor parasitic capacitance

- Constant overlap capacitances C_{GSOV}, C_{GDOV}, and C_{GBOV}
- Variable capacitances C_{GS}, C_{GB}, and C_{GD} depend on the operating region
- C_{BS} and C_{BD} are the sum of the area (C_{BSJ}, C_{BDJ}), sidewall (C_{BSSW}, C_{BDSW}), and channel edge (C_{BSJ}GATE, C_{BDJ}GATE) capacitances
- L_D is the lateral diffusion • T_{FOX} is the field-oxide thickness

```
NAME          m1           m2
MODEL         CMOSN        CMOSP
ID            7.49E-11    -7.49E-11
VGS           0.00E+00    -3.00E+00
VDS           3.00E+00    -4.40E-08
VBS           0.00E+00     0.00E+00
VTH           4.14E-01    -8.96E-01
VDSAT         3.51E-02    -1.78E+00
GM            1.75E-09     2.52E-11
GDS           1.24E-10     1.72E-03
GMB           6.02E-10     7.02E-12
CBD           2.06E-15     1.71E-14
CBS           4.45E-15     1.71E-14
CGSOV         1.80E-15     2.88E-15
CGDOV         1.80E-15     2.88E-15
CGBOV         2.00E-16     2.01E-16
CGS           0.00E+00     1.10E-14
CGD           0.00E+00     1.10E-14
CGB           3.88E-15     0.00E+00
```

- `ID` (I_{DS}), `VGS`, `VDS`, `VBS`, `VTH` (V_t), and `VDSAT` ($V_{DS(sat)}$) are DC parameters
- `GM`, `GDS`, and `GMB` are small-signal conductances (corresponding to $\partial I_{DS}/\partial V_{GS}$, $\partial I_{DS}/\partial V_{DS}$, and $\partial I_{DS}/\partial V_{BS}$, respectively)

Calculations of parasitic capacitances for an n-channel MOS transistor.		
PSpice	**Equation**	**Values[1] for V_{GS}=0V, V_{DS}=3V, V_{SB}=0V**
CBD	$C_{BD} = C_{BDJ} + C_{BDSW}$ $C_{BDJ} + A_D C_J (1 + V_{DB}/\varphi_B)^{-mJ}$ (φ_B = PB) $C_{BDSW} = P_D C_{JSW} (1 + V_{DB}/\varphi_B)^{-mJSW}$ (P_D may or may not include channel edge)	$C_{BD} = 1.855 \times 10^{-13} + 2.04 \times 10^{-16} = 2.06 \times 10^{-13}$ F $C_{BDJ} = (4.032 \times 10^{-15})(1 + (3/1))^{-0.56} = 1.86 \times 10^{-15}$ F $C_{BDSW} = (4.2 \times 10^{-16})(1 + (3/1))^{-0.5} = 2.04 \times 10^{-16}$ F
CBS	$C_{BS} = C_{BSJ} + C_{BSSW}$ $C_{BSJ} + A_S C_J (1 + V_{SB}/\varphi_B)^{-mJ}$ $C_{BSSW} = P_S C_{JSW} (1 + V_{SB}/\varphi_B)^{-mJSW}$	$C_{BS} = 4.032 \times 10^{-15} + 4.2 \times 10^{-16} = 4.45 \times 10^{-15}$ F $A_S C_J = (7.2 \times 10^{-15})(5.6 \times 10^{-4}) = 4.03 \times 10^{-15}$ F $P_S C_{JSW} = (8.4 \times 10^{-6})(5 \times 10^{-11}) = 4.2 \times 10^{-16}$ F
CGSOV	$C_{GSOV}=W_{EFF}C_{GSO}$; $W_{EFF}=W-2W_D$	$C_{GSOV} = (6 \times 10^{-6})(3 \times 10^{-10}) = 1.8 \times 10^{-16}$ F
CGDOV	$C_{GDOV}=W_{EFF}C_{GSO}$	$C_{GDOV} = (6 \times 10^{-6})(3 \times 10^{-10}) = 1.8 \times 10^{-15}$ F
CGBOV	$C_{GBOV}=L_{EFF}C_{GBO}$; $L_{EFF}=L-2L_D$	$C_{GDOV} = (0.5 \times 10^{-6})(4 \times 10^{-10}) = 2 \times 10^{-16}$ F
CGS	C_{GS}/C_O = 0 (off), 0.5 (lin.), 0.66 (sat.) C_O (oxide capacitance) = $W_{EF} L_{EFF} \varepsilon_{ox} / T_{ox}$	$C_O = (6 \times 10^{-6})(0.5 \times 10^{-6})(0.00345) = 1.03 \times 10^{-14}$ F C_{GS} = 0.0 F
CGD	C_{GD}/C_O = 0 (off), 0.5 (lin.), 0 (sat.)	C_{GD} = 0.0 F
CGB	C_{GB} = 0 (on), = C_O in series with C_{GS} (off)	$C_{GB} = 3.88 \times 10^{-15}$ F, C_S=depletion capacitance

[1]Input	`.MODEL CMOSN NMOS LEVEL=3 PHI=0.7 TOX=10E-09 XJ=0.2U TPG=1 VTO=0.65 DELTA=0.7`
	`+ LD=5E-08 KP=2E-04 UO=550 THETA=0.27 RSH=2 GAMMA=0.6 NSUB=1.4E+17 NFS=6E+11`
	`+ VMAX=2E+05 ETA=3.7E-02 KAPPA=2.9E-02 CGDO=3.0E-10 CGSO=3.0E-10 CGBO=4.0E-10`
	`+ CJ=5.6E-04 MJ=0.56 CJSW=5E-11 MJSW=0.52 PB=1`
	`m1 out1 in1 0 0 cmosn W=6U L=0.6U AS=7.2P AD=7.2P PS=8.4U PD=8.4U`	

3.2.1 Junction Capacitance

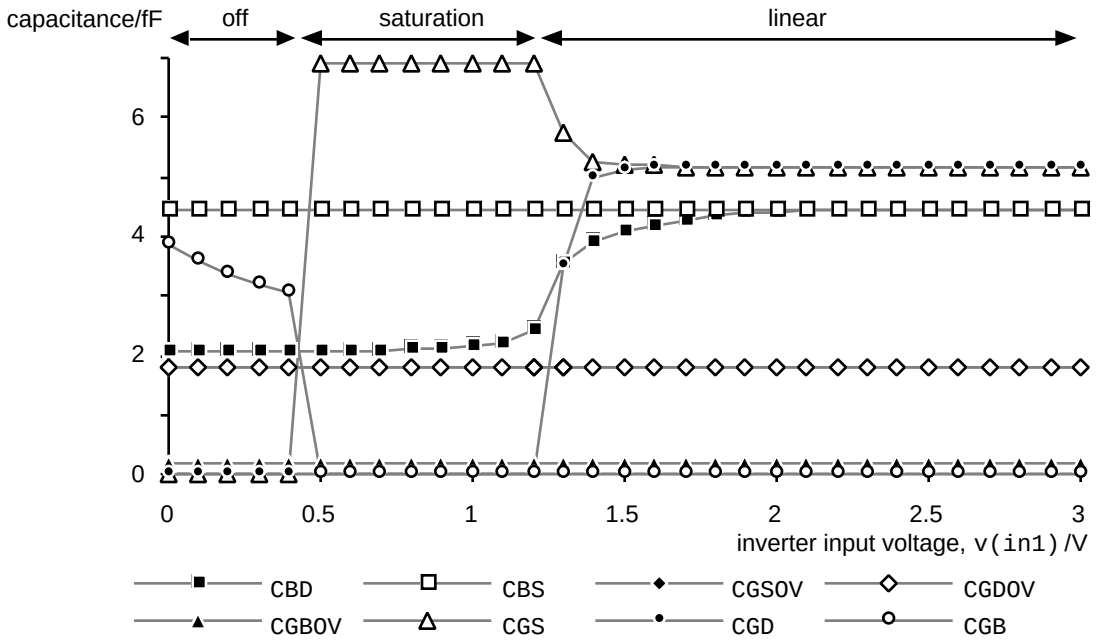
- Junction capacitances, C_{BD} and C_{BS}, consist of two parts: junction area and sidewall
- Both C_{BD} and C_{BS} have different physical characteristics with parameters: `CJ` and `MJ` for the junction, `CJSW` and `MJSW` for the sidewall, and `PB` is common
- C_{BD} and C_{BS} depend on the voltage across the junction (V_{DB} and V_{SB})
- The sidewalls facing the channel (C_{BSJ}GATE and C_{BDJ}GATE) are different from the sidewalls that face the field
- It is a mistake to exclude the gate edge assuming it is in the rest of the model—it is not
- In HSPICE there is a separate mechanism to account for the channel edge capacitance (using parameters `ACM` and `CJGATE`)

3.2.2 Overlap Capacitance

- The overlap capacitance calculations for C_{GSOV} and C_{GDOV} account for lateral diffusion
- SPICE parameter `LD=5E-08` or L_D=0.05µm
- Not all SPICE versions use the equivalent parameter for width reduction, `WD`, in calculating C_{GDOV}
- Not all SPICE versions subtract W_D to form W_{EFF}

3.2.3 Gate Capacitance

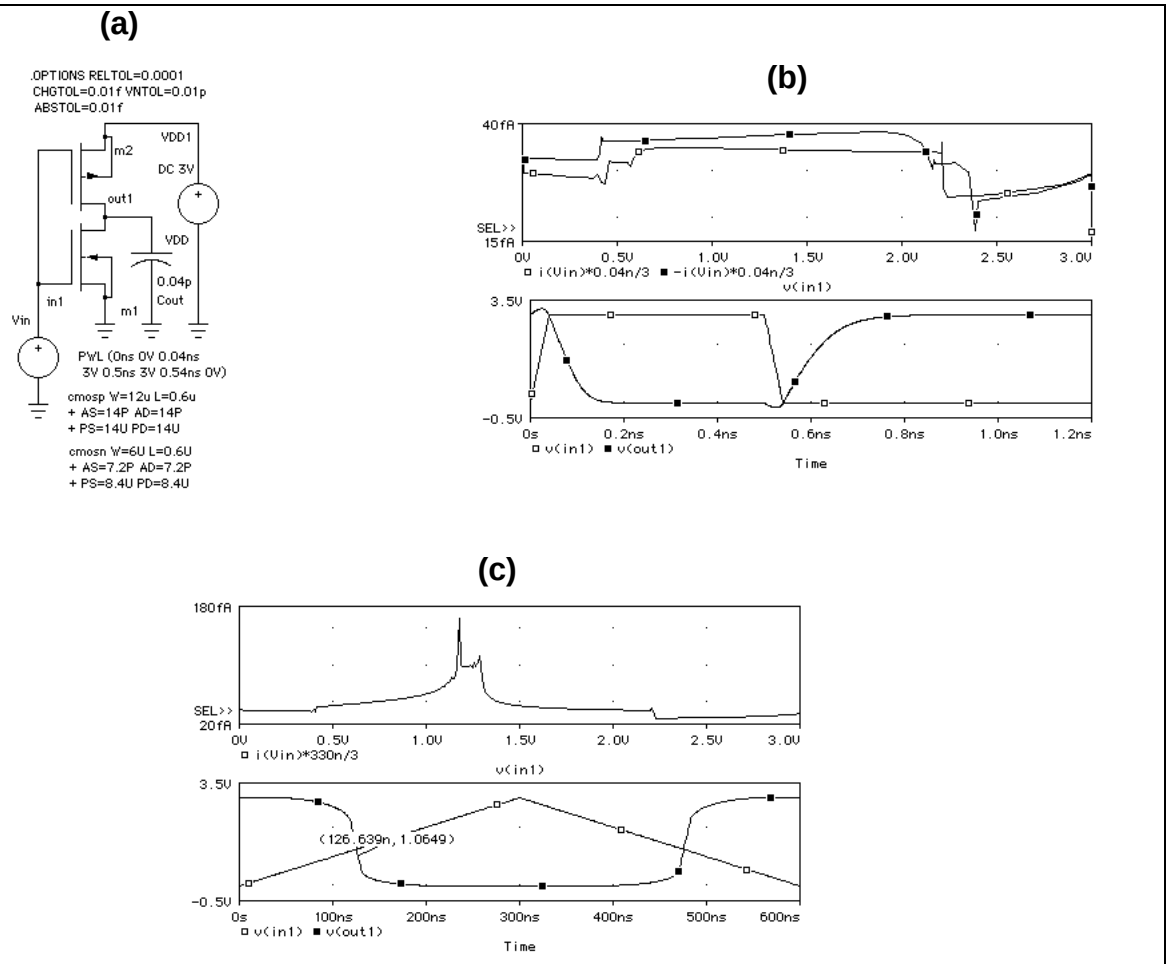
- The gate capacitance depends on the operating region
- The gate–source capacitance C_{GS} varies from zero (off) to $0.5C_O$ in the linear region to $(2/3)C_O$ in the saturation region
- The gate–drain capacitance C_{GD} varies from zero (off) to $0.5C_O$ (linear region) and back to zero (saturation region)
- The gate–bulk capacitance C_{GB} is two capacitors in series: the fixed gate-oxide capacitance, C_O, and the variable depletion capacitance, C_S
- As the transistor turns on the channel shields the bulk from the gate—and C_{GB} falls to zero
- Even with V_{GS}=0V, the depletion width under the gate is finite and thus C_{GB} is less than C_O



The variation of n-channel transistor parasitic capacitance

- PSpice v5.4 (LEVEL=3)
- Created by varying the input voltage, v(in1), of an inverter
- Data points are joined by straight lines
- Note that CGSOV=CGDOV

3.2.4 Input Slew Rate



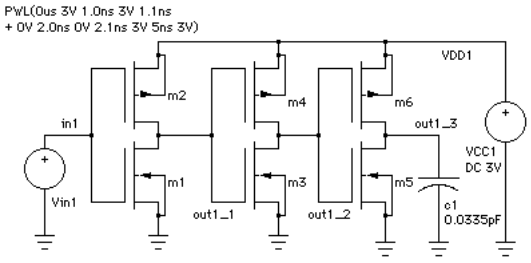
Measuring the input capacitance of an inverter

(a) Input capacitance is measured by monitoring the input current to the inverter, `i(Vin)`

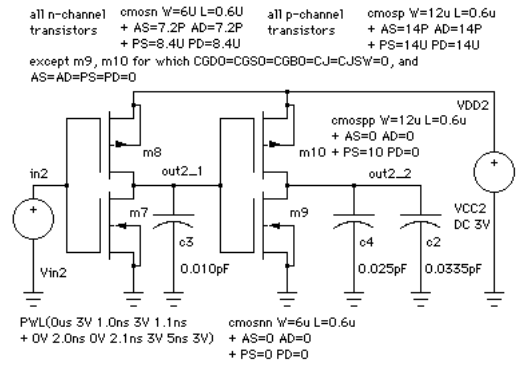
(b) Very fast (non-equilibrium) switching: input current of 40fA = input capacitance of 40fF

(c) Very slow (equilibrium) switching: input capacitance is now equal for both transitions

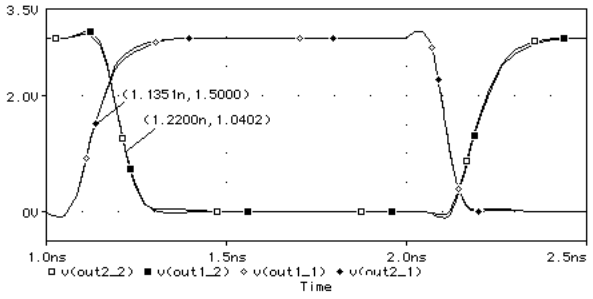
(a)



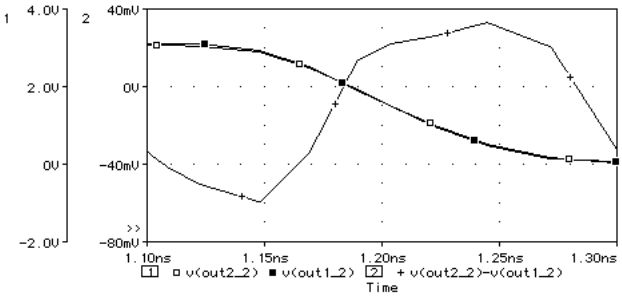
(b)



(c)



(d)



Parasitic capacitance measurement

(a) All devices in this circuit include parasitic capacitance

(b) This circuit uses linear capacitors to model the parasitic capacitance of `m9/10`.

• The load formed by the inverter (`m5` and `m6`) is modeled by a 0.0335pF capacitor (`c2`)

• The parasitic capacitance due to the overlap of the gates of `m3` and `m4` with their source, drain, and bulk terminals is modeled by a 0.01pF capacitor (`c3`)

• The effect of the parasitic capacitance at the drain terminals of `m3` and `m4` is modeled by a 0.025pF capacitor (`c4`)

(c) Comparison of (a) and (b). The delay (1.22–1.135=0.085ns) is equal to t_{PDf} for the inverter `m3/4`

(d) An exact match would have both waveforms equal at the 0.35 trip point (1.05V).

3.3 Logical Effort

We extend the prop–ramp model with a "catch all" term, t_q, that includes:

- delay due to internal parasitic capacitance
- the time for the input to reach the switching threshold of the cell
- the dependence of the delay on the slew rate of the input waveform

$t_{PD} = R(C_{out} + C_p) + t_q$

We can **scale** any logic cell by a scaling factor s: $t_{PD} = (R/s)\cdot(C_{out} + sC_p) + st_q$

$$t_{PD} = RC\frac{C_{out}}{C_{in}} + RC_p + st_q$$

Normalizing the delay: $$d = \frac{(RC)\,(C_{out} / C_{in}) + RC_p + st_q}{\tau} = f + p + q$$

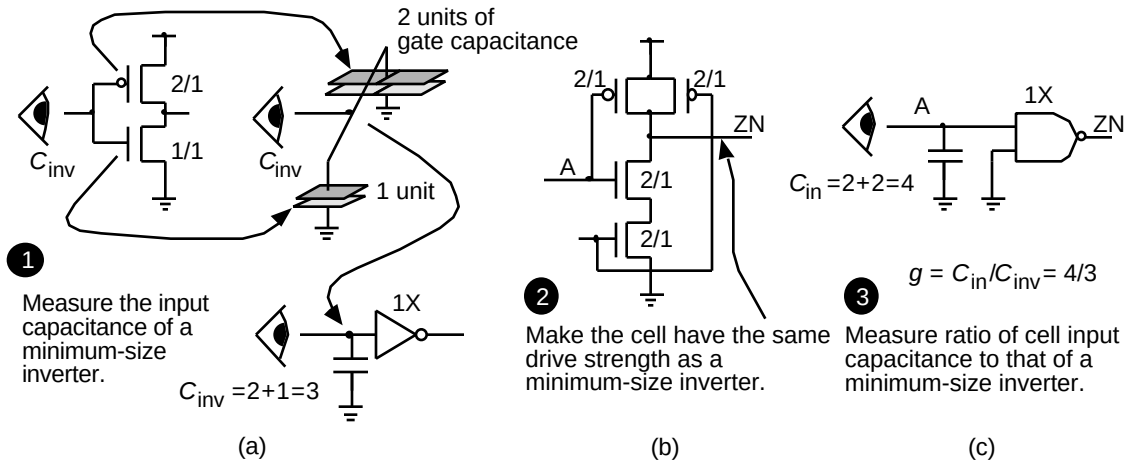
The time constant **tau**, $\tau = R_{inv} C_{inv}$, is a basic property of any CMOS technology

The delay equation is the sum of three terms, $d = f + p + q$ or
delay = **effort delay** + **parasitic delay** + **nonideal delay**

The effort delay f is the product of **logical effor**t, g, and **electrical effort**, h: $f = gh$

Thus, delay = logical effort × electrical effort + parasitic delay + nonideal delay

- R and C will change as we scale a logic cell, but the RC product stays the same
- Logical effort is independent of the size of a logic cell
- We can find logical effort by scaling a logic cell to have the same drive as a 1X minimum-size inverter
- Then the logical effort, g, is the ratio of the input capacitance, C_{in}, of the 1X logic cell to C_{inv}



Logical effort • For a two-input NAND cell, the logical effort, g=4/3

(a) Find the input capacitance, C_{inv}, looking into the input of a minimum-size inverter in terms of the gate capacitance of a minimum-size device

(b) Size a logic cell to have the same drive strength as a minimum-size inverter (assuming a logic ratio of 2). The input capacitance looking into one of the logic-cell terminals is then C_{in}

(c) The logical effort of a cell is C_{in}/ C_{inv}

The h depends only on the load capacitance C_{out} connected to the output of the logic cell and the input capacitance of the logic cell, C_{in}; thus

electrical effort $h = C_{out}/C_{in}$

parasitic delay $p = RC_p/\tau$ (the parasitic delay of a minimum-size inverter is: $p_{inv} = C_p/C_{inv}$)

nonideal delay $q = st_q/\tau$

Cell effort, parasitic delay, and nonideal delay (in units of τ) for single-stage CMOS cells				
Cell	**Cell effort (logic ratio=2)**	**Cell effort (logic ratio=r)**	**Parasitic delay/τ**	**Nonideal delay/τ**
inverter	1 (by definition)	1 (by definition)	p_{inv} (by definition)	q_{inv} (by definition)
n-input NAND	$(n+2)/3$	$(n+r)/(r+1)$	np_{inv}	nq_{inv}
n-input NOR	$(2n+1)/3$	$(nr+1)/(r+1)$	np_{inv}	nq_{inv}

3.3.1 Predicting Delay

- Example: predict the delay of a three-input NOR logic cell
- 2X drive
- driving a net with a fanout of four
- 0.3pF total load capacitance (input capacitance of cells we are driving plus the interconnect)
- $p=3p_{inv}$ and $q=3q_{inv}$ for this cell
- the input gate capacitance of a 1X drive, three-input NOR logic cell is equal to gC_{inv}
- for a 2X logic cell, $C_{in} = 2gC_{inv}$

$$gh = g\,\frac{C_{out}}{C_{in}} = \frac{g\cdot(0.3\text{ pF})}{2gC_{inv}} = \frac{(0.3\text{ pF})}{(2)\cdot(0.036\text{ pF})}$$ (Notice g cancels out in this equation)

The delay of the NOR logic cell, in units of τ, is thus

$$d = gh + p + q = \frac{0.3\times10^{-12}}{(2)\cdot(0.036\times10^{-12})} + (3)\cdot(1) + (3)\cdot(1.7)$$

$= 4.1666667 + 3 + 5.1$

$= 12.266667\ \tau$ equivalent to an absolute delay, $t_{PD}\approx12.3\times0.06\text{ns}=0.74\text{ns}$

The delay for a 2X drive, three-input NOR logic cell is $t_{PD} = (0.03 + 0.72C_{out} + 0.60)$ ns

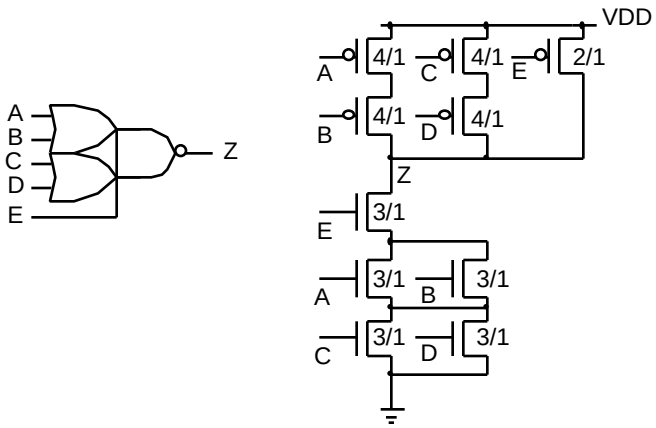
With C_{out}=0.3pF, $t_{PD} = 0.03 + (0.72)\cdot(0.3) + 0.60 = 0.846$ ns compared to our prediction of 0.74ns

3.3.2 Logical Area and Logical Efficiency

An OAI221 logic cell

• **Logical-effort vector g**=(7/3, 7/3, 5/3)

• The **logical area** is 33 **logical squares**

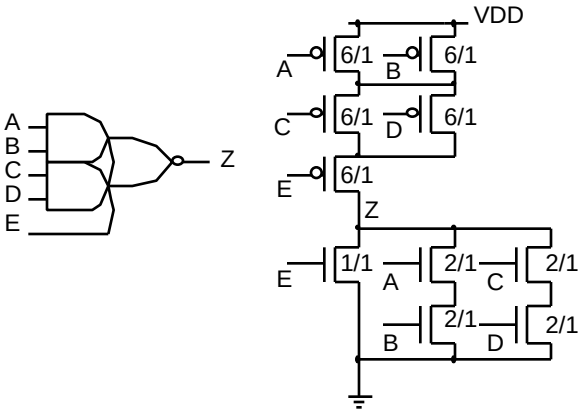


An AOI221 logic cell

• **g**=(8/3, 8/3, 7/3)

• Logical area is 39 logical squares

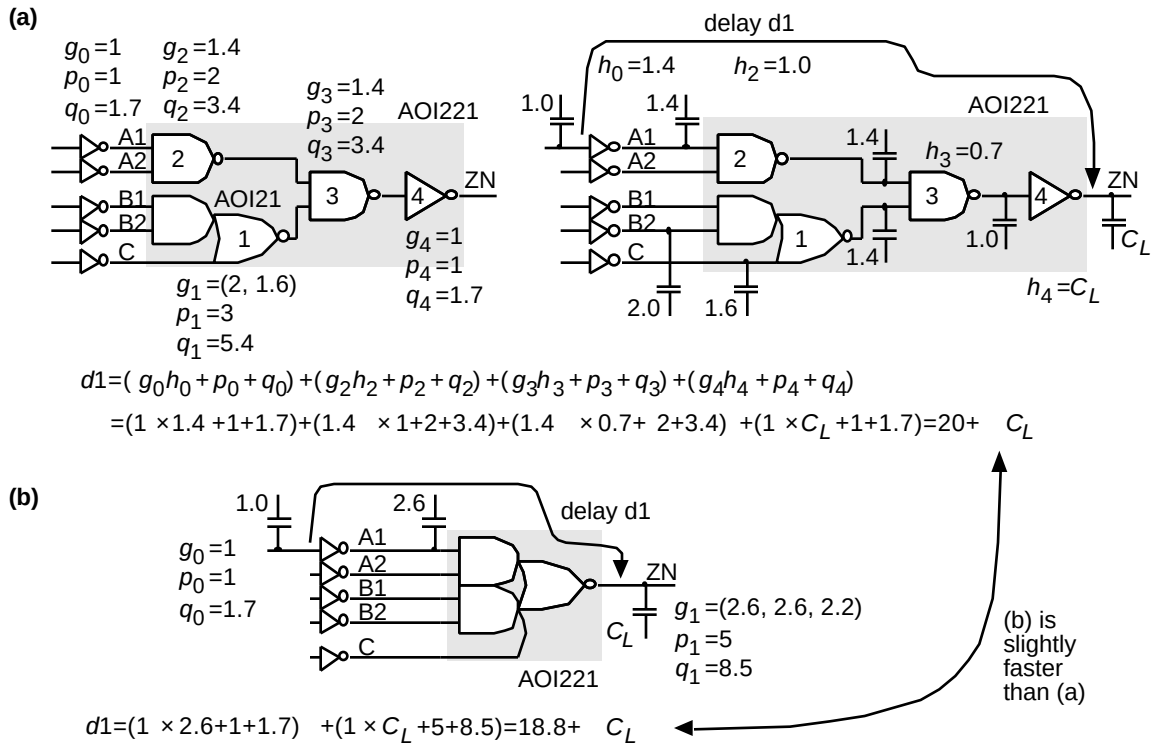
• Less **logically efficient** than OAI221



3.3.3 Logical Paths

$$\textbf{path delay } D = \sum_{i \text{ path}} g_i h_i + \sum_{i \text{ path}} (p_i + q_i)$$

3.3.4 Multistage Cells



Logical paths • Comparison of multistage and single-stage implementations

(a) An AOI221 logic cell constructed as a multistage cell, $d1 = 20 + C_L$

(b) A single-stage AOI221 logic cell, $d1 = 18.8 + C_L$

3.3.5 Optimum Delay

path logical effort $G = \prod_{i \text{ path}} g_i$

path electrical effort $H = \prod_{i \text{ path}} h_i \frac{C_{out}}{C_{in}}$

C_{out} is the load and C_{in} is the first input capacitance on the path

path effort $F = GH$

optimum effort delay $f\hat{}_i = g_i h_i = F^{1/N}$

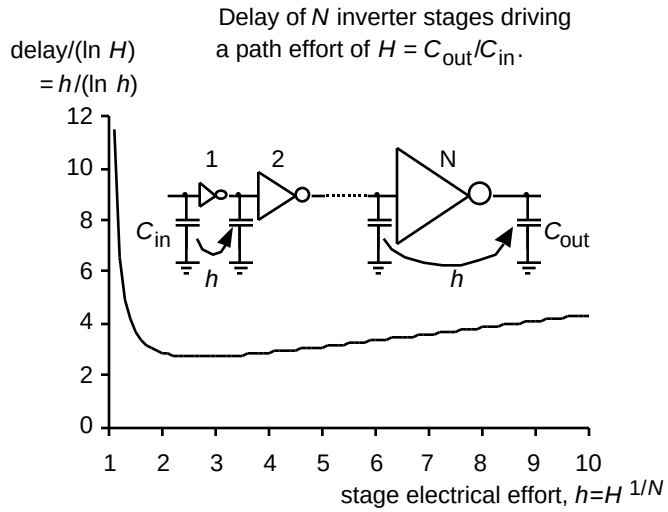
optimum path delay $D\hat{} = NF^{1/N} = N(GH)^{1/N} + P + Q$

$$P + Q = \sum_{i \text{ path}} p_i + h_i$$

3.3.6 Optimum Number of Stages

Stage effort

h	h/(ln h)
1.5	3.7
2	2.9
2.7	2.7
3	2.7
4	2.9
5	3.1
10	4.3



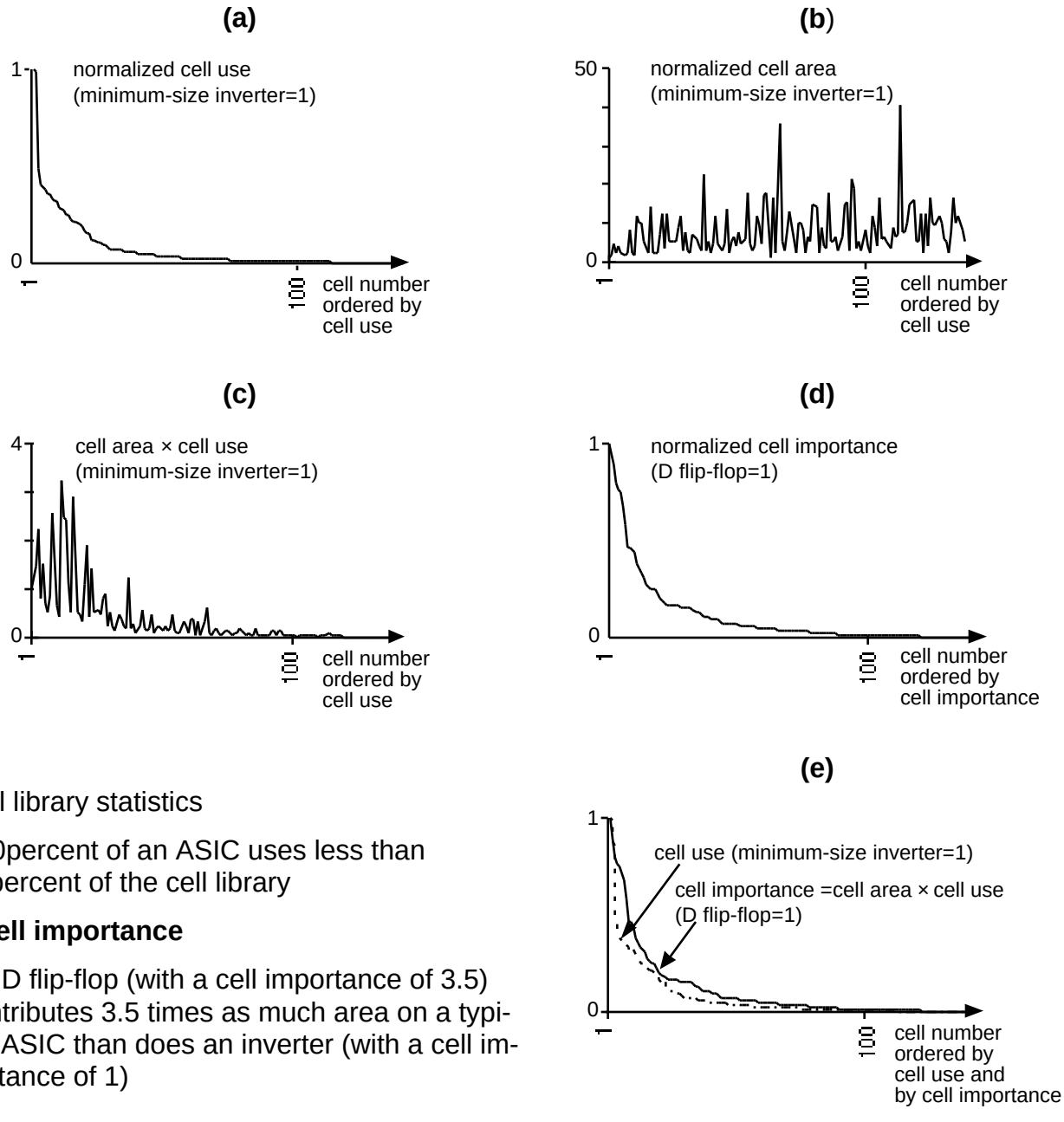
- Chain of N inverters each with equal stage effort, $f=gh$
- Total path delay is $Nf=Ngh=Nh$, since $g=1$ for an inverter

- To drive a path electrical effort H, $h^N = H$, or $N \ln h = \ln H$
- Delay, $Nh = h \ln H / \ln h$
- Since $\ln H$ is fixed, we can only vary $h/\ln(h)$
- $h/\ln(h)$ is a shallow function with a minimum at $h = e \approx 2.718$
- Total delay is $Ne = e \ln H$

3.4 Library-Cell Design

- A big problem in library design is dealing with design rules
- Sometimes we can **waive** design rules
- **Symbolic layout**, **sticks** or **logs** can decrease the library design time (9 months for Virtual Silicon–currently the most sophisticated standard-cell library)
- Mapping symbolic layout uses 10–20 percent more area (5–10 percent with compaction)
- Allowing 45° layout decreases silicon area (some companies do not allow 45° layout)

3.5 Library Architecture



Cell library statistics

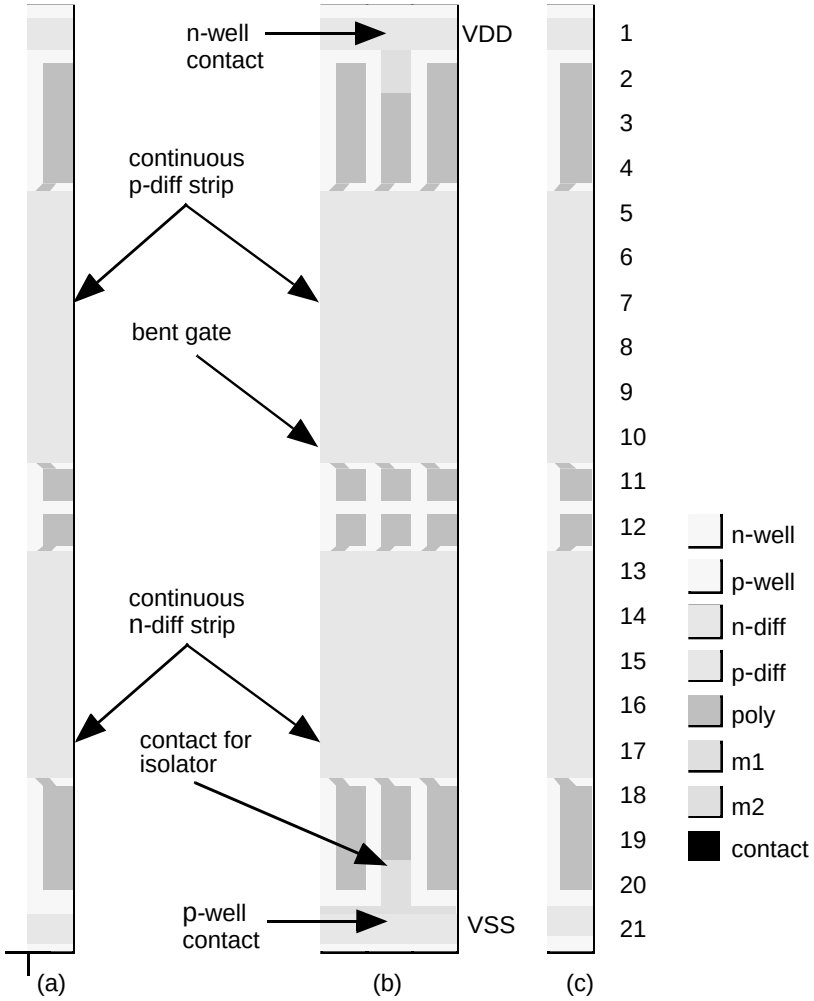
• 80percent of an ASIC uses less than 20percent of the cell library

• **Cell importance**

• A D flip-flop (with a cell importance of 3.5) contributes 3.5 times as much area on a typical ASIC than does an inverter (with a cell importance of 1)

3.6 Gate-Array Design

Key words: gate-array base cell (or base cell) • gate-array base (or base) • horizontal tracks • vertical track • gate isolation • isolator transistor • oxide isolation • oxide-isolated gate array

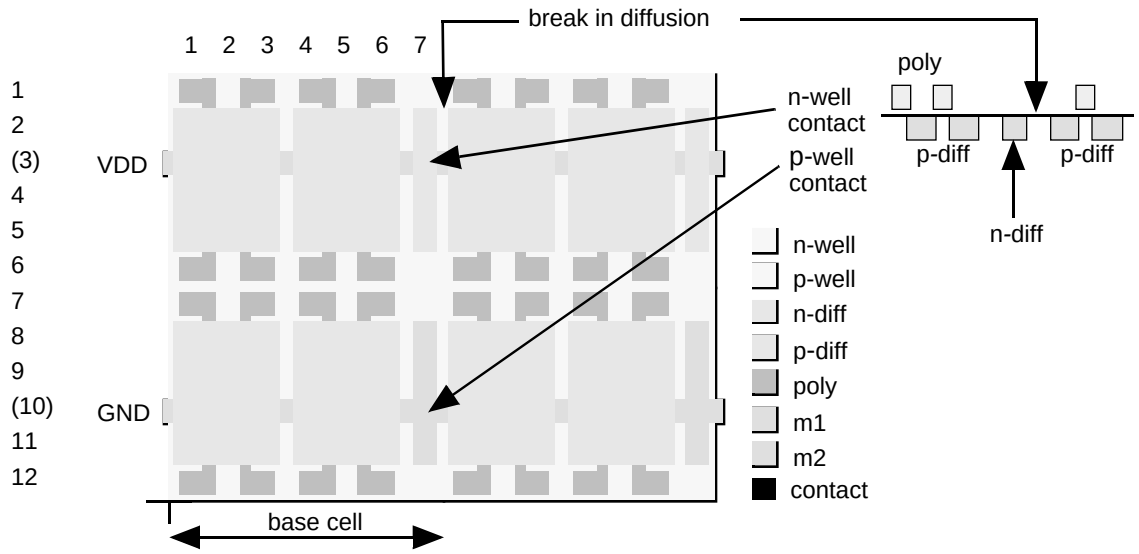


The construction of a gate-isolated gate array

(a) The one-track-wide base cell containing one p-channel and one n-channel transistor

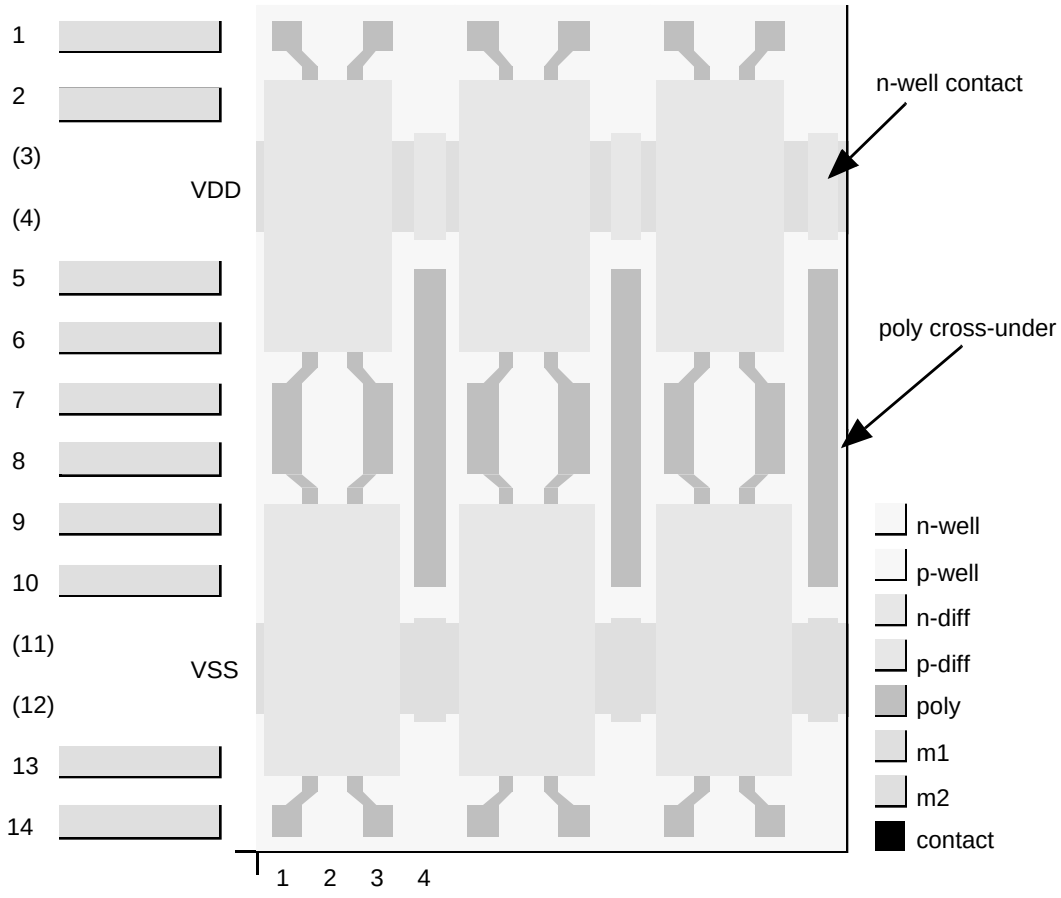
(b) The center base cell is isolating the base cells on either side from each other

(c) The base cell is 21 tracks high (high for a modern cell library)



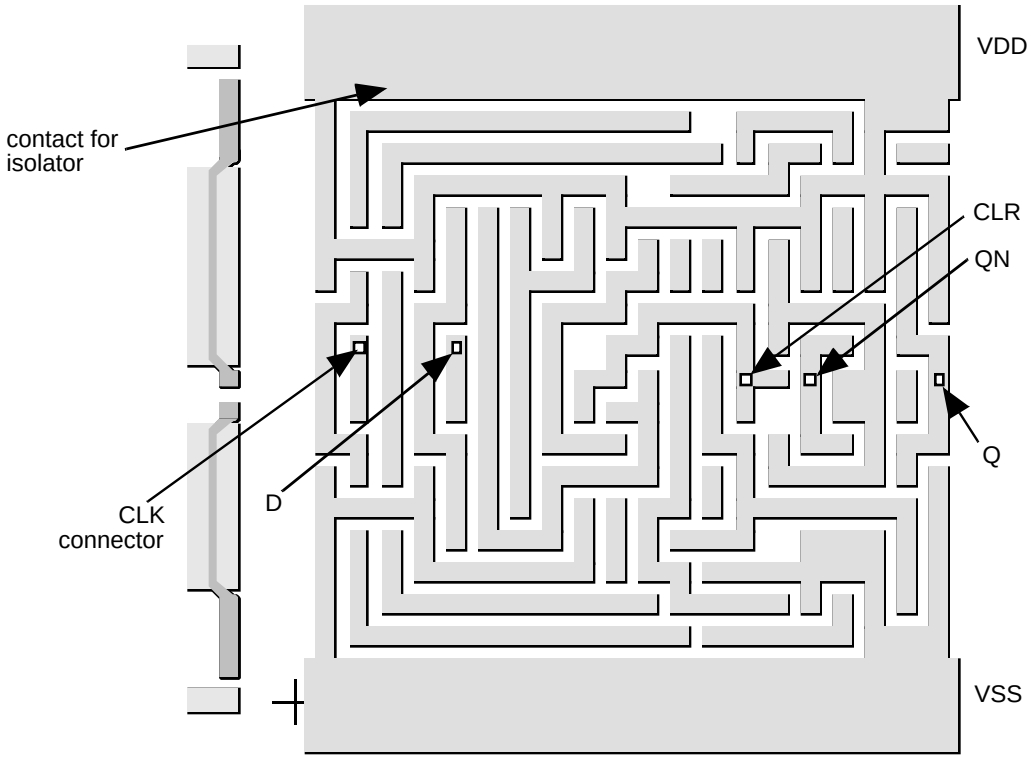
An oxide-isolated gate-array base cell

- Two base cells, each contains eight transistors and two well contacts
- The p-channel and n-channel transistors are each 4 tracks high
- The cell is 12 tracks high (8–12 is typical for a modern library)
- The base cell is 7 tracks wide



An oxide-isolated gate-array base cell

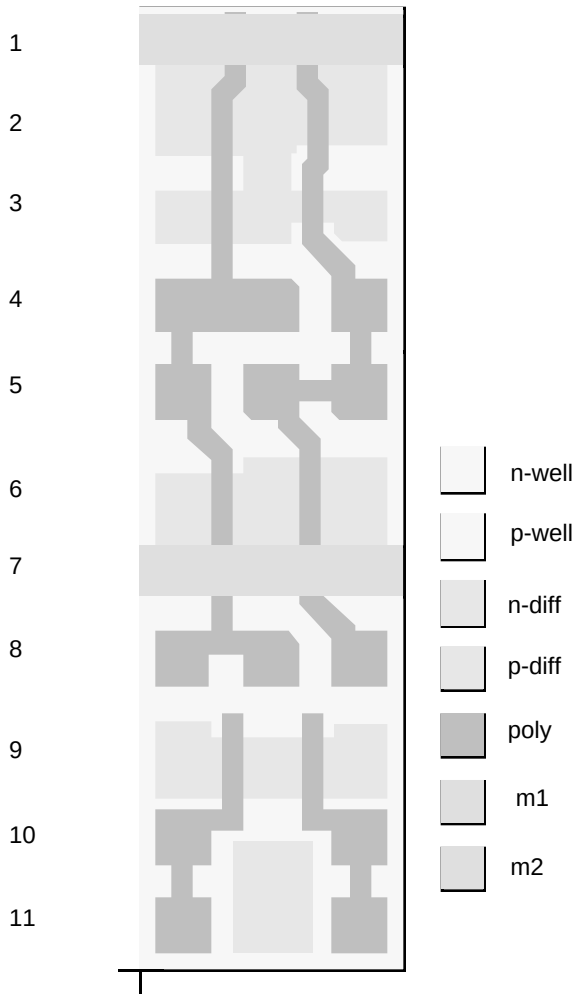
- 14 tracks high and 4 tracks wide
- VDD (tracks 3 and 4) and GND (tracks 11 and 12) are each 2 tracks wide
- 10 horizontal routing tracks (tracks 1, 2, 5–10, 13, 14)—unusually large number for modern cells
- p-channel and n-channel polysilicon **bent gates** are tied together in the center of the cell
- The well contacts leave room for a **poly cross-under** in each base cell.



Flip-flop macro in a gate-isolated gate-array library

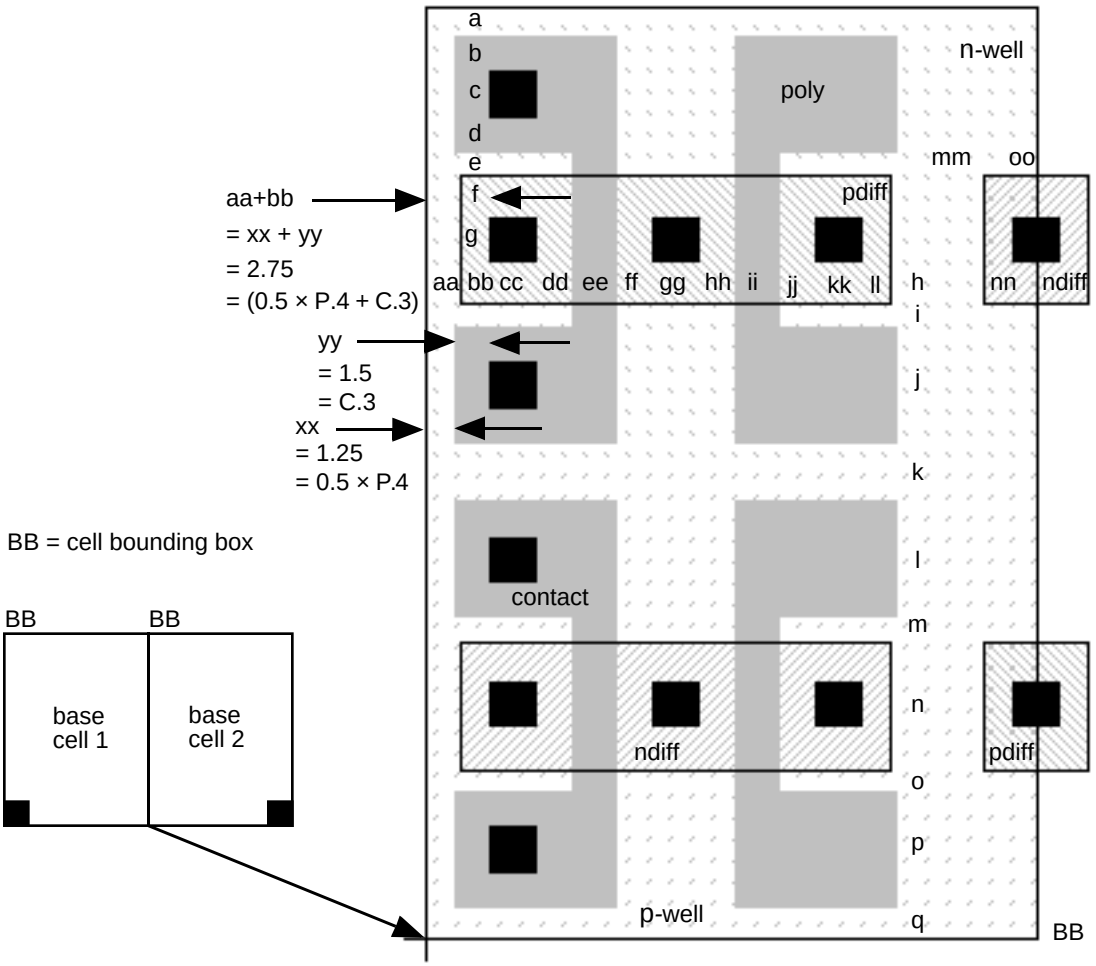
• Only the first-level metallization and contact pattern, the **personalization**, is shown, but this is enough information to derive the schematic

• This is an older topology for 2LM (cells for 3LM are shorter in height)



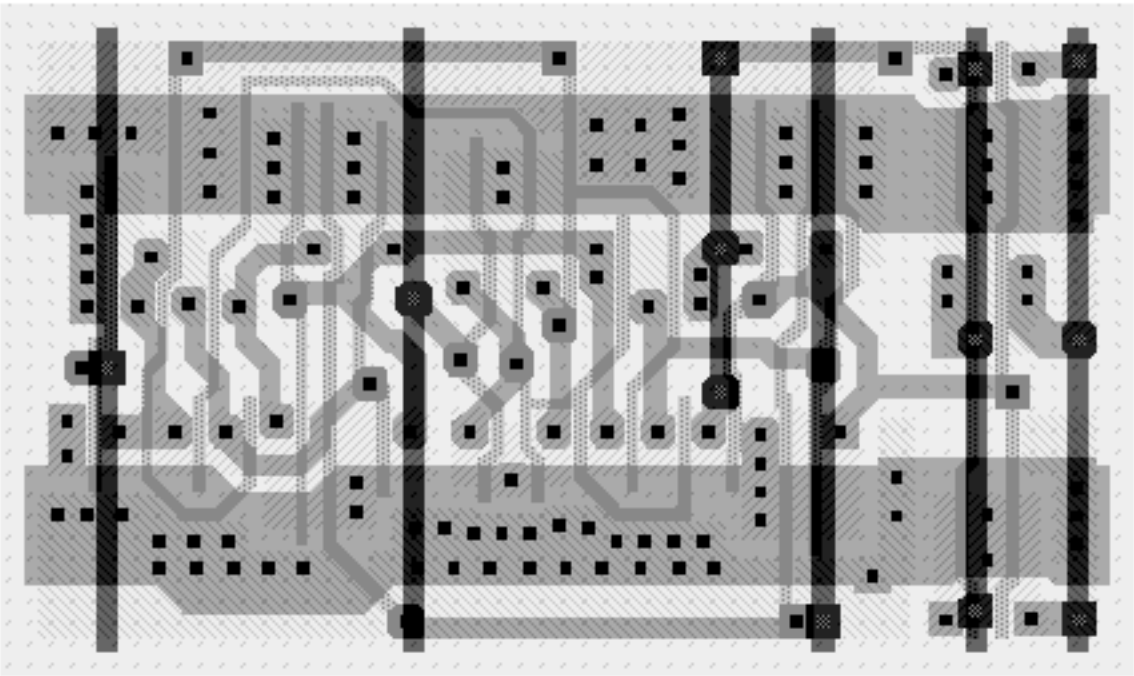
The SiARC/Synopsys cell-based array (CBA) basic cell

- This is CBA I for 2LM (CBA II is intended for 3LM and salicide proceses)



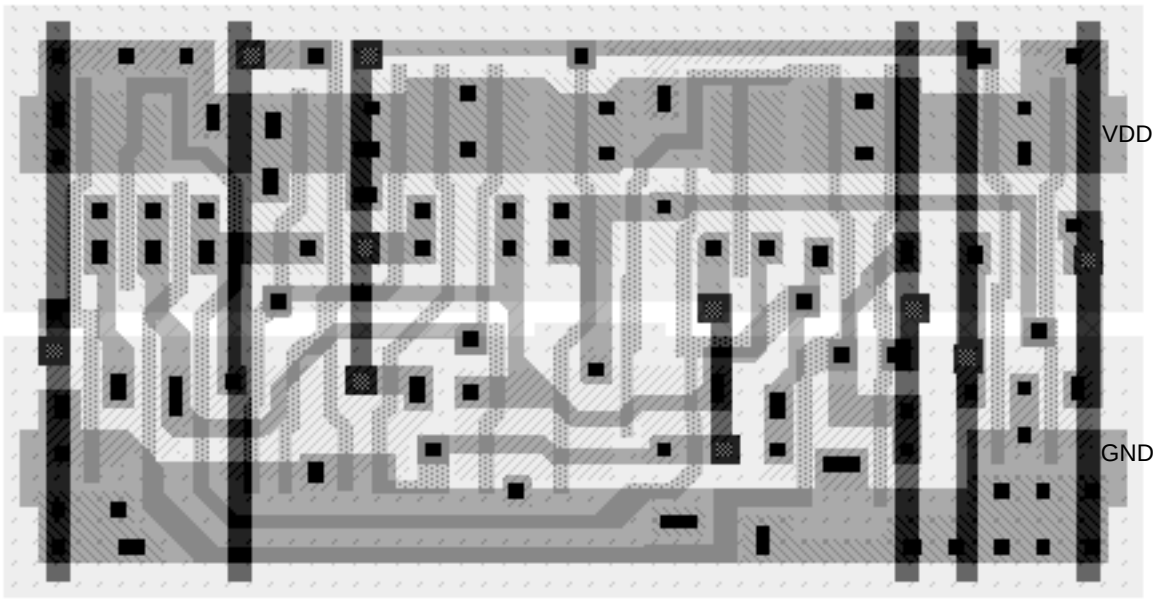
A simple gate-array base cell

3.7 Standard-Cell Design

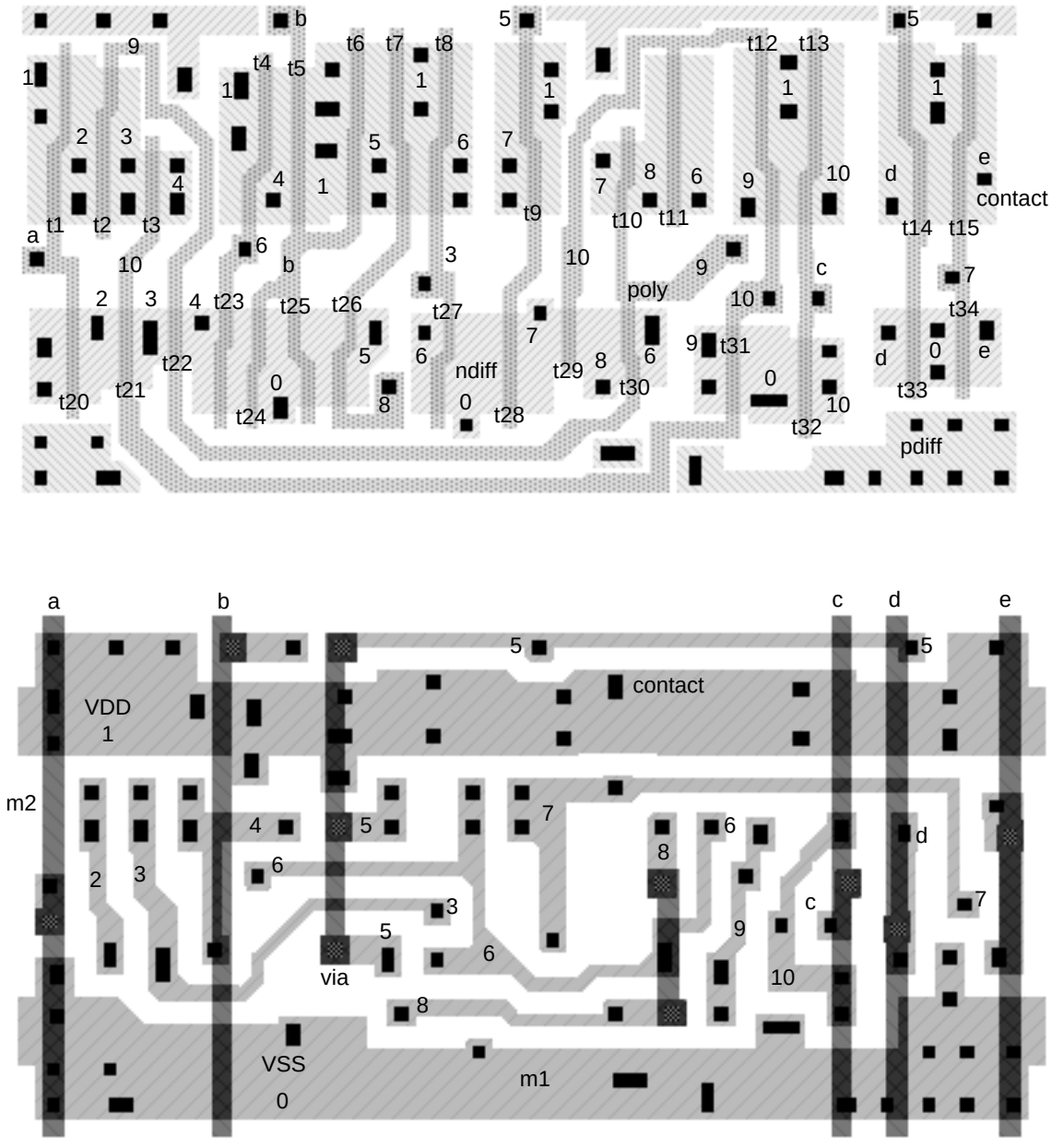


A D flip-flop standard cell

- **Performance-optimized library** • **Area-optimized library**
- Wide **power buses** and transistors for a performance-optimized cell
- **Double-entry cell** intended for a 2LM process and channel routing
- Five **connectors** run vertically through the cell on m2
- The extra short vertical metal line is an internal **crossover**
- **bounding box** (BB) • **abutment box** (AB) • **physical connector** • **abut**



A D flip-flop from a 1.0µm standard-cell library

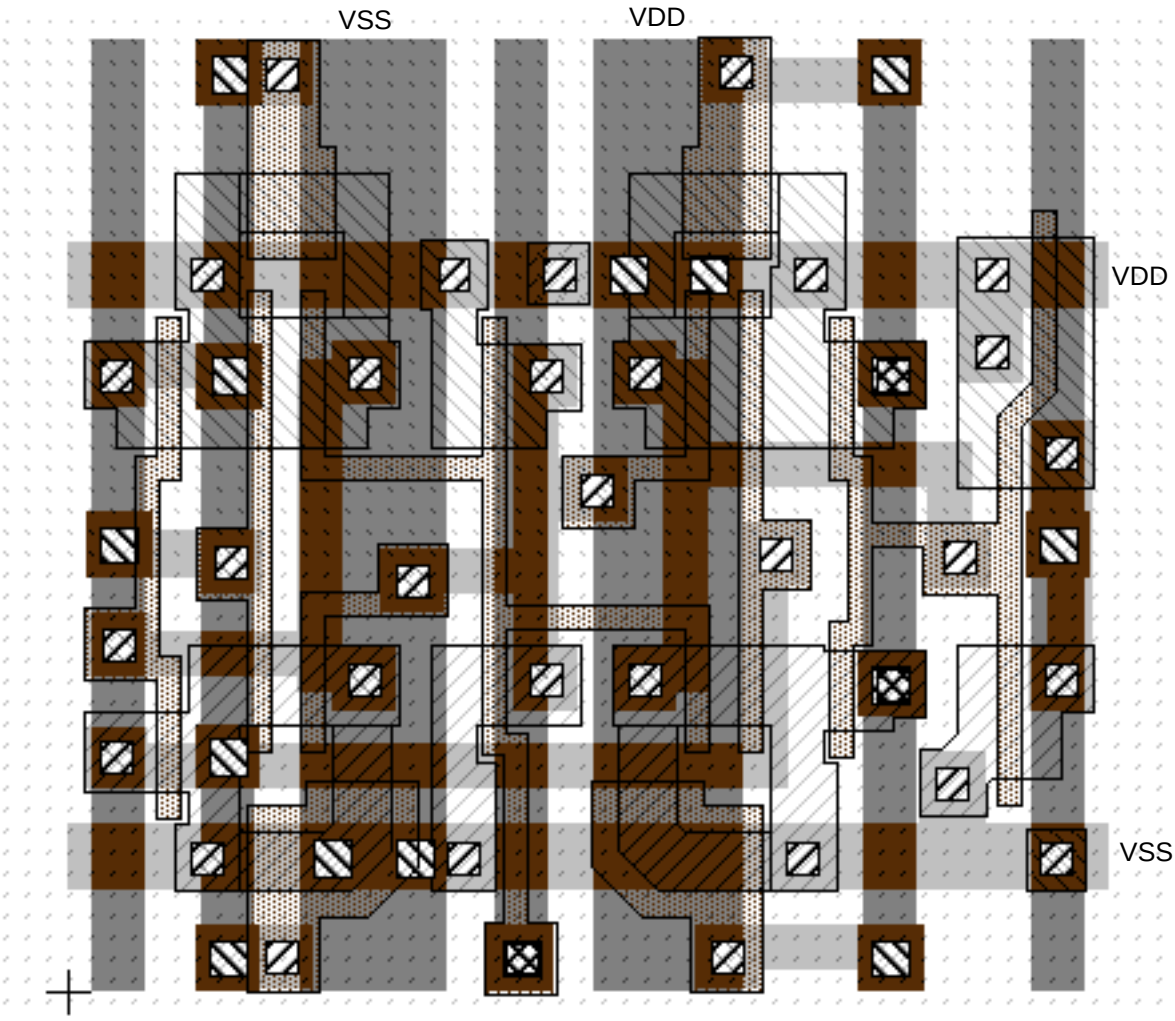


D flip-flop

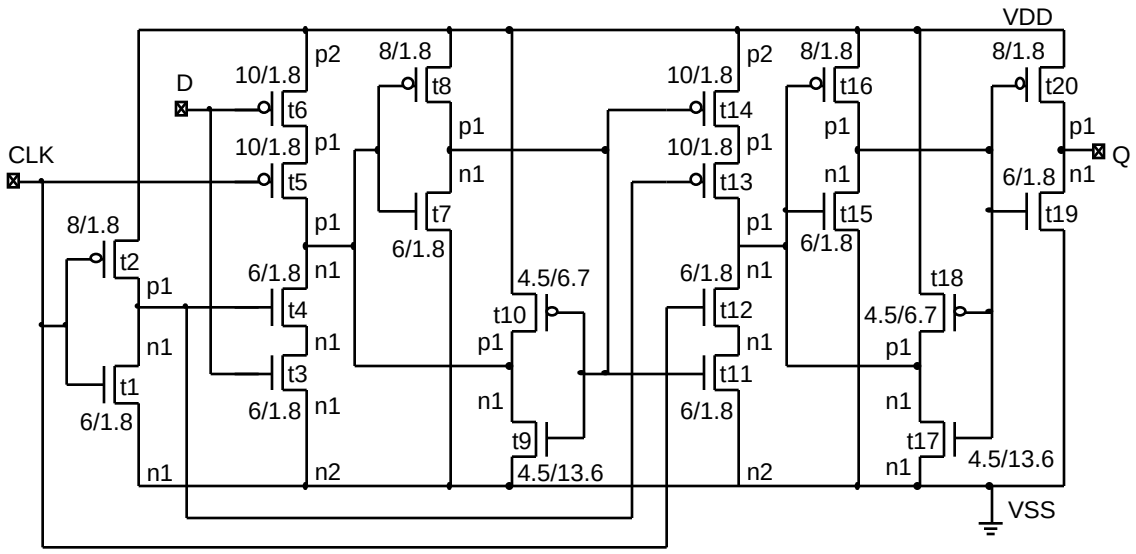
(Top) n-diffusion, p-diffusion, poly, contact (n-well and p-well are not shown)

(Bottom) m1, contact, m2, and via layers

3.8 Datapath-Cell Design



A datapath D flip-flop cell



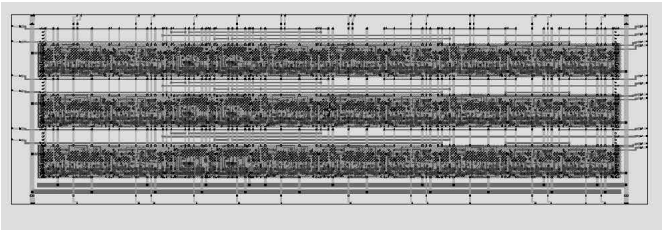
The schematic of a datapath D flip-flop cell

A narrow datapath

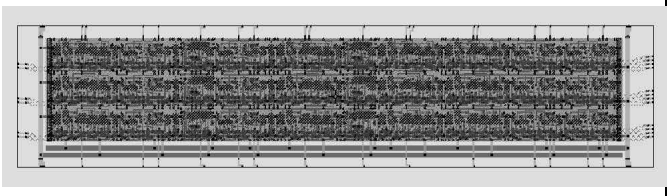
(a) Implemented in a two-level metal process

(b) Implemented in a three-level metal process

(a)



(b)



3.9 Summary

Key concepts:

- Tau, logical effort, and the prediction of delay
- Sizes of cells, and their drive strengths
- Cell importance
- The difference between gate-array macros, standard cells, and datapath cells

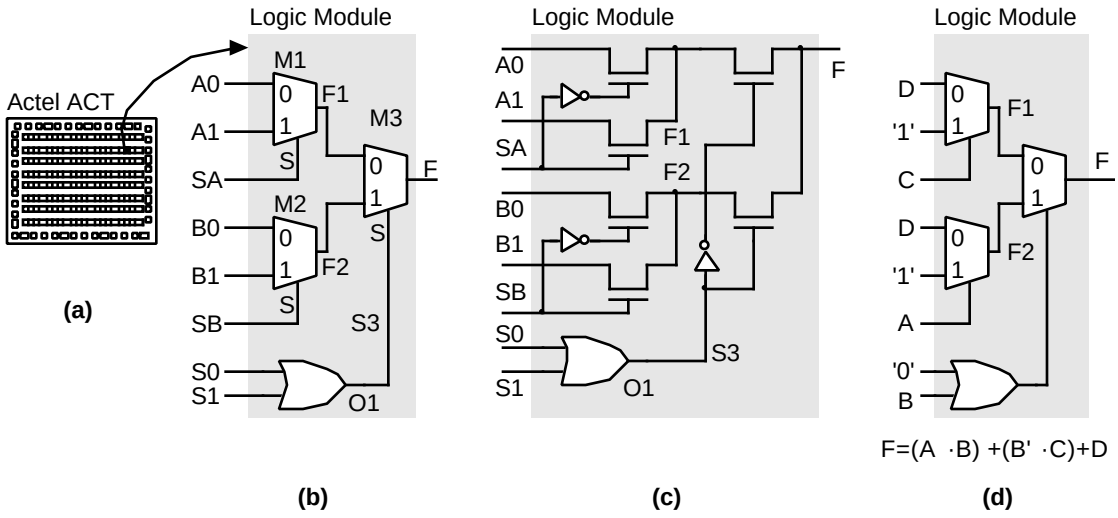
PROGRAMMABLE ASIC LOGIC CELLS

5

Key concepts: basic logic cell • multiplexer-based cell • look-up table (LUT) • programmable array logic (PAL) • influence of programming technology • timing • worst-case design

5.1 Actel ACT

5.1.1 ACT 1 Logic Module



The Actel ACT architecture

(a) Organization of the **basic logic cells**

(b) The ACT 1 **Logic Module** (LM, the Actel basic logic cell). The ACT 1 family uses just one type of LM. ACT 2 and ACT 3 FPGA families both use two different types of LM

(c) An example LM implementation using pass transistors (without any buffering)

(d) An example logic macro. Connect logic signals to some or all of the LM inputs, the remaining inputs to VDD or GND

5.1.2 Shannon's Expansion Theorem

- We can use the **Shannon expansion theorem** to **expand** F =A·F(A='1') + A'·F(A='0')

Example: F =A'·B + A·B·C' + A'·B'·C = A·(B·C') + A'·(B + B'·C)

- F(A='1')=B·C' is the **cofactor** of F with respect to (**wrt**) A or F_A
- If we expand F *wrt* B, F =A'·B + A·B·C' + A'·B'·C = B·(A' + A·C') + B'·(A'·C)
- Eventually we reach the unique **canonical form**, which uses only minterms
- (A **minterm** is a **product term** that contains all the variables of F—such as A·B'·C)

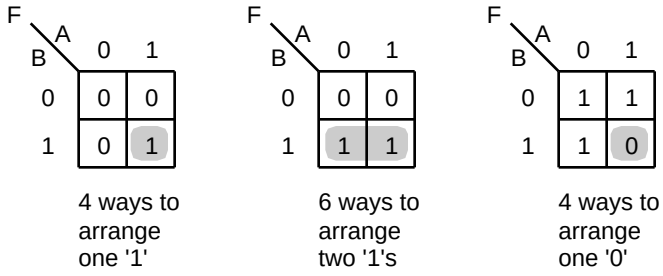
Another example: F=(A·B) + (B'·C) + D

- Expand F *wrt* B: F=B·(A + D) + B'·(C + D) =B·F2 + B'·F1
- F = 2:1 MUX, with B selecting between two inputs: F(A='1') and F(A='0')
- F also describes the output of the ACT 1 LM
- Now we need to split up F1 and F2
- Expand F2 *wrt* A, and F1 *wrt* C: F2=A + D=(A·1) + (A'·D); F1=C + D=(C·1) + (C'·D)
- A, B, C connect to the select lines and '1' and D are the inputs of the MUXes in the ACT 1 LM
- Connections: A0=D, A1='1', B0=D, B1='1', SA=C, SB=A, S0='0', and S1=B

5.1.3 Multiplexer Logic as Function Generators

The 16 logic functions of 2 variables:

- 2 of the 16 functions are not very interesting (F='0', and F='1')
- There are 10 functions that we can implement using just one 2:1 MUX
- 6 functions are useful: INV, BUF, AND, OR, AND1-1, NOR1-1



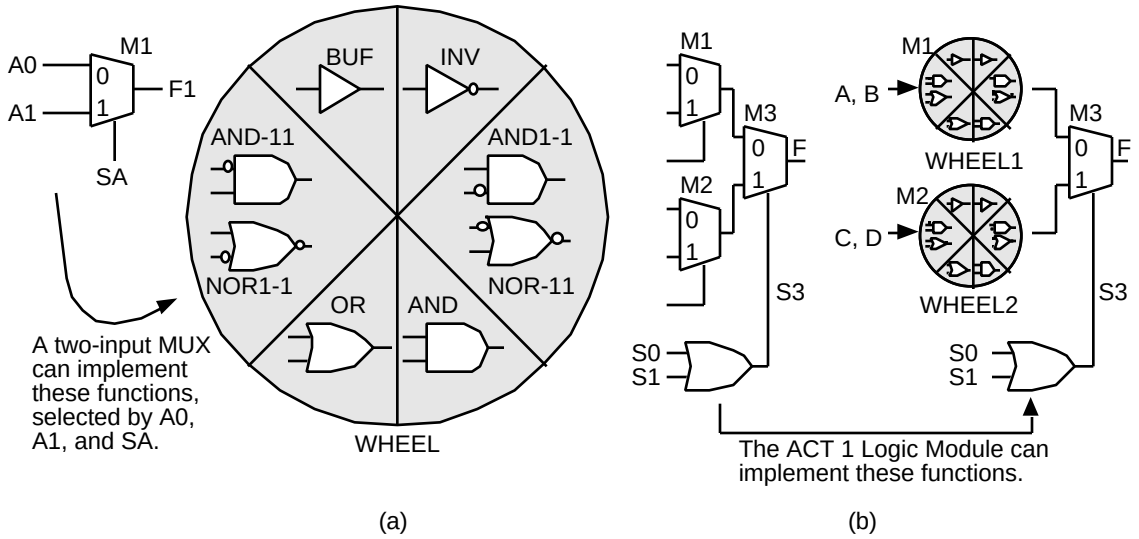
14 functions of 2 variables (and F='0', F ='1' makes 16)

Boolean functions using a 2:1 MUX

	Function, F	F=	Canonical form	Min-terms	Min-term code	Function number	M1		
							A0	A1	SA
1	'0'	'0'	'0'	none	0000	0	0	0	0
2	NOR1-1(A, B)	(A+B')	A'·B	1	0010	2	B	0	A
3	NOT(A)	A'	A'·B' + A'·B	0, 1	0011	3	0	1	A
4	AND1-1(A, B)	A·B'	A·B'	2	0100	4	A	0	B
5	NOT(B)	B'	A'·B' + A·B'	0, 2	0101	5	0	1	B
6	BUF(B)	B	A'·B + A·B	1, 3	1010	6	0	B	1
7	AND(A, B)	A·B	A·B	3	1000	8	0	B	A
8	BUF(A)	A	A·B' + A·B	2, 3	1100	9	0	A	1
9	OR(A, B)	A+B	A'·B + A·B' + A·B	1, 2, 3	1110	13	B	1	A
10	'1'	'1'	A'·B' + A'·B + A·B' + A·B	0, 1, 2, 3	1111	15	1	1	1

Example of using the WHEEL functions to implement F=NAND(A, B)=(A·B)'

- 1. First express F as the output of a 2:1 MUX: we do this by expanding F *wrt* A (or *wrt* B; since F is symmetric) F=A·(B') + A'·('1')
- 2. Assign WHEEL1 to implement INV(B), and WHEEL2 to implement '1'
- 3. Set the select input to the MUX connecting WHEEL1 and WHEEL2, S0+S1=A. We can do this using S0=A, S1='1'



The ACT 1 Logic Module as a Boolean function generator

(a) A 2:1 MUX viewed as a **function wheel**

(b) The ACT 1 Logic Module is two function wheels, an OR gate, and a 2:1 MUX

• A 2:1 MUX is a function wheel that can generate BUF, INV, AND-11, AND1-1, OR, AND

• WHEEL(A, B) =MUX(A0, A1, SA)

• MUX(A0, A1, SA)=A0·SA' + A1·SA

• The inputs (A0, A1, SA) ={A, B, '0', '1'}

• Each of the inputs (A0, A1, and SA) may be A, B, '0', or '1'

• The ACT 1 LM is built from two function wheels, a 2:1 MUX, and a two-input OR gate

• ACT 1 LM =MUX [WHEEL1, WHEEL2, OR(S0, S1)]

5.1.4 ACT 2 and ACT 3 Logic Modules

• ACT 1 requires 2 LMs per flip-flop: with unknown interconnect capacitance

• ACT 2 and ACT 3 use two types of LMs, one includes a D flip-flop

• ACT 2 **C-Module** is similar to the ACT 1 LM but can implement five-input logic functions

• *combinatorial* module implements *combinational* logic (blame MMI for the misuse of terms)

• ACT 2 **S-Module** (**sequential module**) contains a C-Module and a **sequential element**

5.1.5 Timing Model and Critical Path

Keywords and concepts: timing model • deals only with internal logic • estimates delays • before place-and-route step • nondeterministic architecture • find slowest register–register delay or critical path

Example of timing calculations (a rather complex examination of internal module timing):

- The setup and hold times, measured *inside* (not outside) the S-Module, are t'_{SUD} and t'_{H} (a prime denotes parameters that are measured inside the S-Module)
- The clock–Q propagation delay is t'_{CO}
- The parameters t'_{SUD}, t'_{H}, and t'_{CO} are measured using the *internal* clock signal CLKi
- The propagation delay of the combinational logic *inside* the S-Module is t'_{PD}
- The delay of the combinational logic that drives the flip-flop clock signal is t'_{CLKD}
- From *outside* the S-Module, with reference to the outside clock signal CLK1:

$t_{SUD}=t'_{SUD} + (t'_{PD} - t'_{CLKD})$, $t_{H}=t'_{H} + (t'_{PD} - t'_{CLKD})$, $t_{CO}=t'_{CO} + t'_{CLKD}$

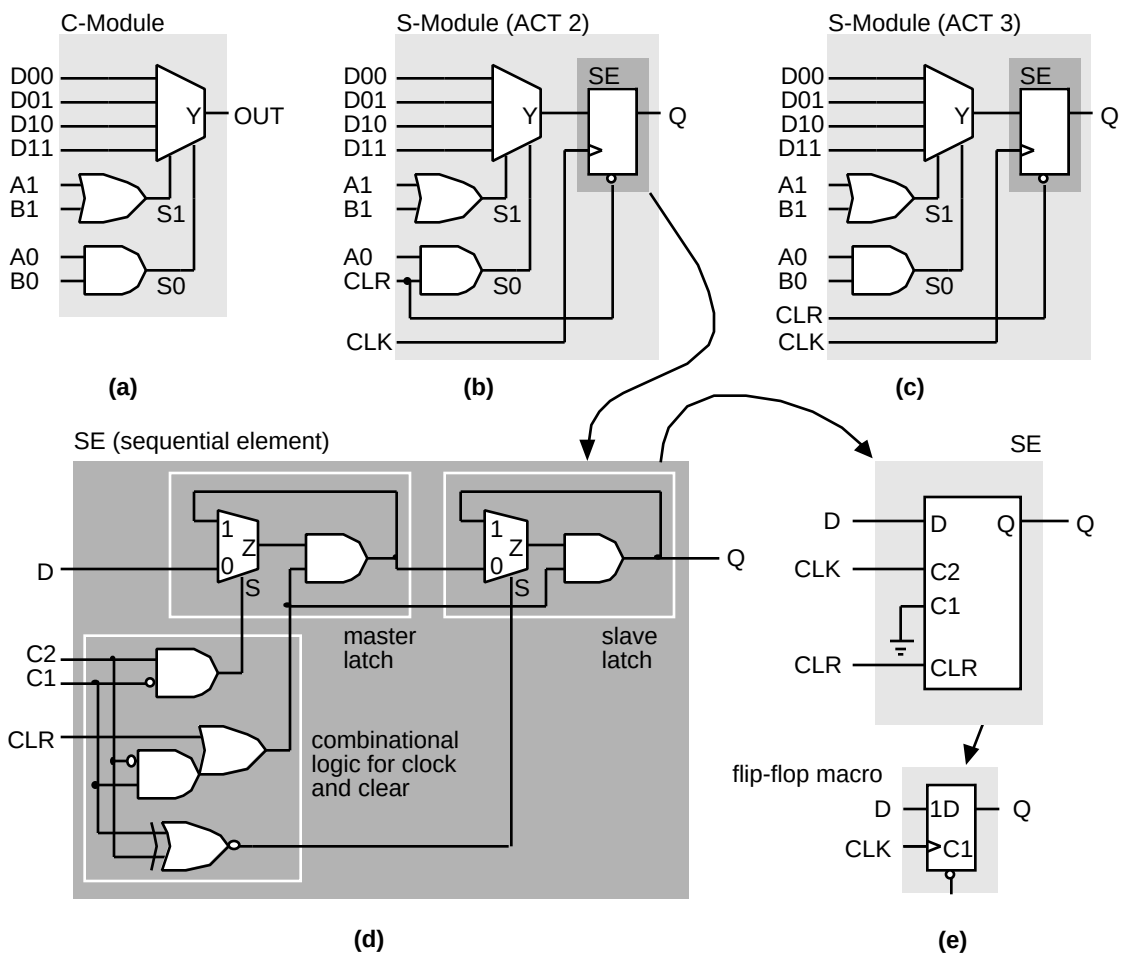
- We do not know the *internal* parameters t'_{SUD}, t'_{H}, and t'_{CO}, but assume reasonable values:

$t'_{SUD}=0.4ns$, $t'_{H}=0.1ns$, $t'_{CO}=0.4ns$.

- t'_{PD} (combinational logic inside the S-Module) is equal to the C-Module delay, so $t'_{PD}=3ns$ for the ACT 3
- We do not know t'_{CLKD}; assume a value of $t'_{CLKD}=2.6ns$ (the exact value does not matter)
- Thus the *external* S-Module parameters are: $t_{SUD}=0.8ns$, $t_{H}=0.5ns$, $t_{CO}=3.0ns$
- These are the same as the ACT 3 S-Module parameters (I chose t'_{CLKD} so they would be)
- Of the 3.0ns combinational logic delay: 0.4ns increases the setup time and 2.6ns increases the clock–output delay, t_{CO}
- Actel says that the combinational logic delay is *buried* in the flip-flop setup time. But this is borrowed money—you have to pay it back.

5.1.6 Speed Grading

- **Speed grading** (or **speed binning**) uses a **binning circuit**
- Measure $t_{PD}=(t_{PLH} + t_{PHL})/2$ — and use the fact that properties match across a chip
- Actel speed grades are based on 'Std' speed grade



Actel ACT 2 and ACT 3 Logic Modules

(a) The C-Module for combinational logic

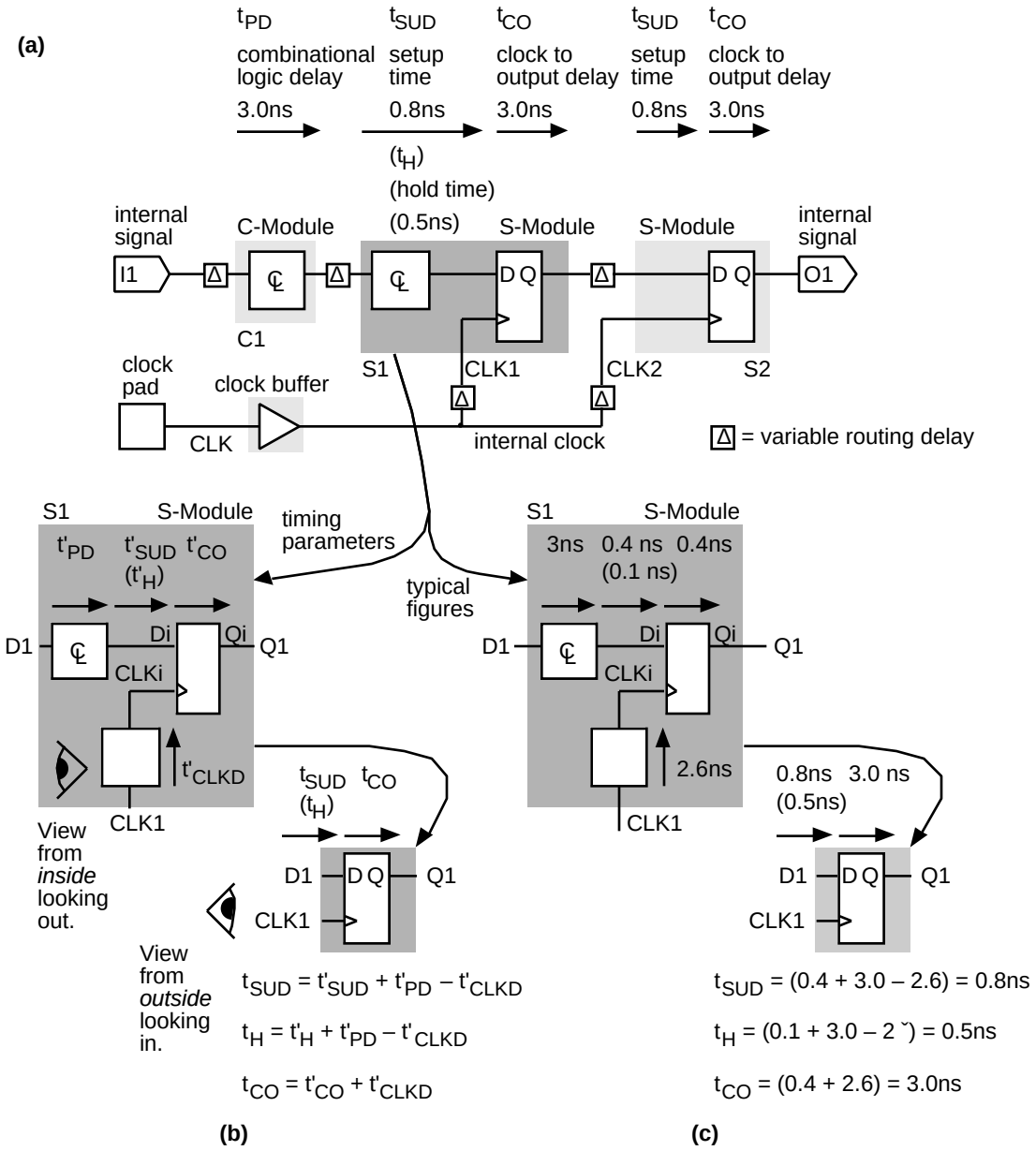
(b) The ACT 2 S-Module

(c) The ACT 3 S-Module

(d) The equivalent circuit (without buffering) of the SE (sequential element)

(e) The SE configured as a positive-edge–triggered D flip-flop

- '1' speed grade is approximately 15 percent faster than 'Std'
- '2' speed grade is approximately 25 percent faster than 'Std'
- '3' speed grade is approximately 35 percent faster than 'Std'.



Timing views from inside and outside the Actel ACT S-module

(a) Timing parameters for a 'Std' speed grade ACT 3

(b) Flip-flop timing

(c) An example of flip-flop timing based on ACT 3 parameters

5.1.7 Worst-Case Timing

Keywords and concepts: Using synchronous design you worry about how slow your circuit may be—not how fast • **ambient temperature**, T_A • package **case temperature**, T_C (military) • temperature of the chip, the **junction temperature**, T_J • nominal operating conditions: V_{DD}=5.0V, and T_J=25°C • **worst-case commercial** conditions: V_{DD}=4.75V, and T_J=+70°C • always design using **worst-case timing** • **derating factors** • **critical path delay** between registers • **process corner** (slow–slow • fast–fast • slow–fast • fast–slow) • Commercial. V_{DD}=5V ± 5%, T_A (ambient)=0 to +70°C • Industrial. V_{DD}=5V ± 10%, T_A (ambient)=–40 to +85°C • Military: V_{DD}=5V ± 10%, T_C (case)=–55 to +125°C • Military: Standard MIL-STD-883C Class B • Military extended: unmanned spacecraft

ACT 3 timing parameters

		Fanout				
Family	**Delay**	**1**	**2**	**3**	**4**	**8**
ACT 3-3 (data book)	t_{PD}	2.9	3.2	3.4	3.7	4.8
ACT3-2 (calculated)	t_{PD}/0.85	3.41	3.76	4.00	4.35	5.65
ACT3-1 (calculated)	t_{PD}/0.75	3.87	4.27	4.53	4.93	6.40
ACT3-Std (calculated)	t_{PD}/0.65	4.46	4.92	5.23	5.69	7.38

ACT 3 derating factors

	Temperature T_J (junction)/°C						
V_{DD}/V	**–55**	**–40**	**0**	**25**	**70**	**85**	**125**
4.5	0.72	0.76	0.85	0.90	1.04	1.07	1.17
4.75	0.70	0.73	0.82	0.87	1.00	1.03	1.12
5.00	0.68	0.71	0.79	0.84	0.97	1.00	1.09
5.25	0.66	0.69	0.77	0.82	0.94	0.97	1.06
5.5	0.63	0.66	0.74	0.79	0.90	0.93	1.01

5.1.8 Actel Logic Module Analysis

- Actel uses a **fine-grain architecture** which allows you to use almost all of the FPGA
- Synthesis can map logic efficiently to a fine-grain architecture

- Physical symmetry simplifies place-and-route (swapping equivalent pins on opposite sides of the LM to ease routing)
- Matched to small antifuse programming technology
- LMs balance efficiency of implementation and efficiency of utilization
- A simple LM reduces performance, but allows fast and robust place-and-route

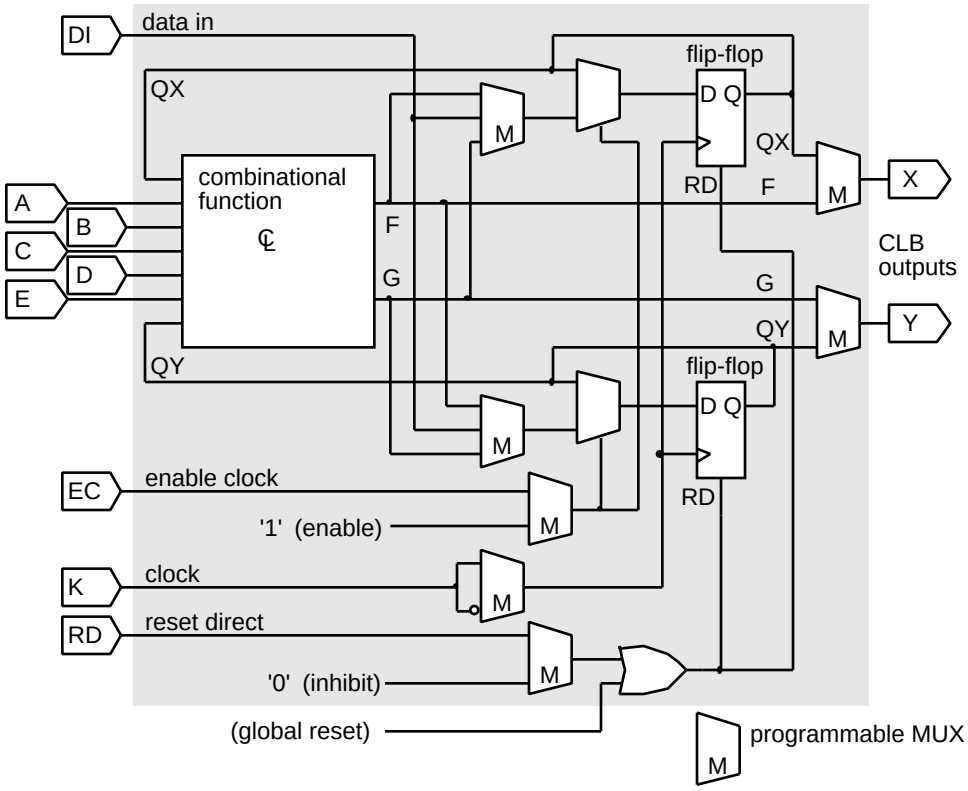
5.2 Xilinx LCA

Keywords and concepts: Xilinx LCA (a trademark, logic cell array) • **configurable logic block** • **coarse-grain architecture**

5.2.1 XC3000 CLB

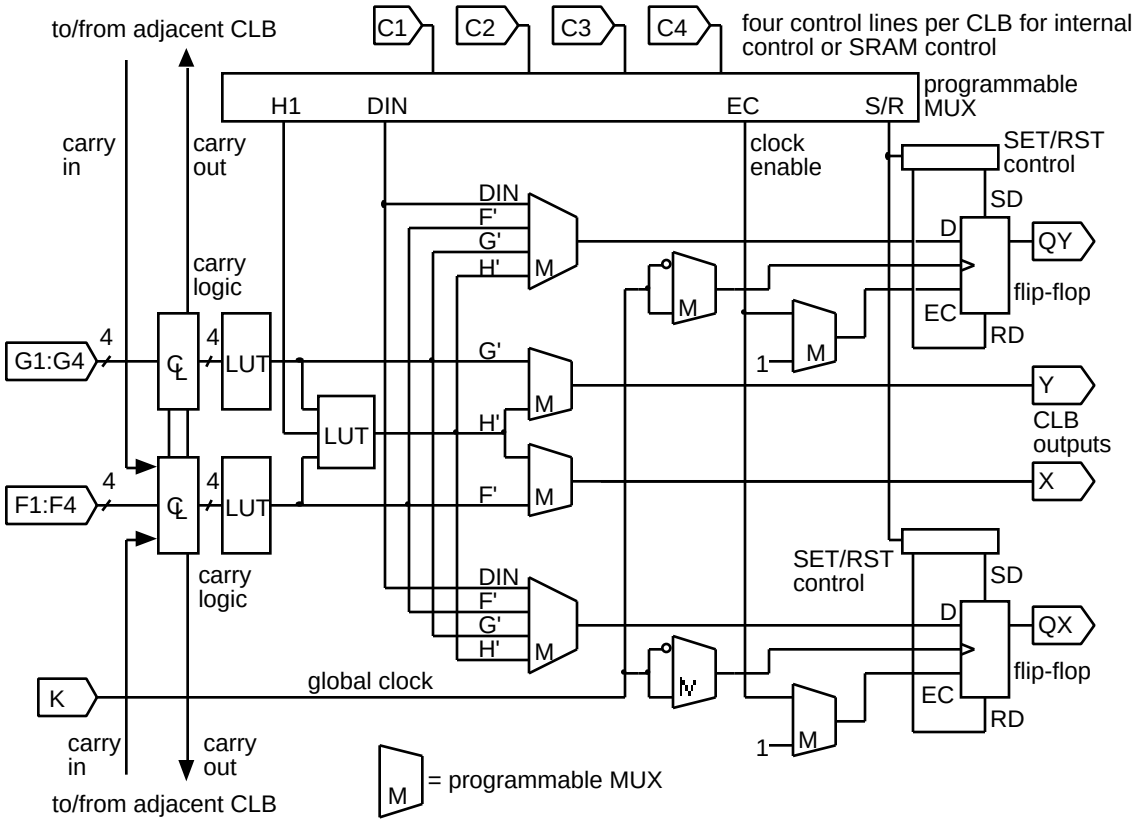
- A 32-bit **look-up table** (LUT)
- CLB propagation delay is fixed (the LUT access time) and independent of the logic function
- 7 inputs to the XC3000 CLB: 5 CLB inputs (A–E), and 2 flip-flop outputs (QX and QY)
- 2 outputs from the LUT (F and G). Since a 32-bit LUT requires only five variables to form a unique address ($32=2^5$), there are several ways to use the LUT:
- Use 5 of the 7 possible inputs (A–E, QX, QY) with the entire 32-bit LUT (the CLB outputs (F and G) are then identical)
- Split the 32-bit LUT in half to implement 2 functions of 4 variables each; choose 4 input variables from the 7 inputs (A–E, QX, QY).You have to choose 2 of the inputs from the 5 CLB inputs (A–E); then one function output connects to F and the other output connects to G.
- You can split the 32-bit LUT in half, using one of the 7 input variables as a select input to a 2:1 MUX that switches between F and G (to implemen some functions of 6 and 7 variables).

5.2.2 XC4000 Logic Block



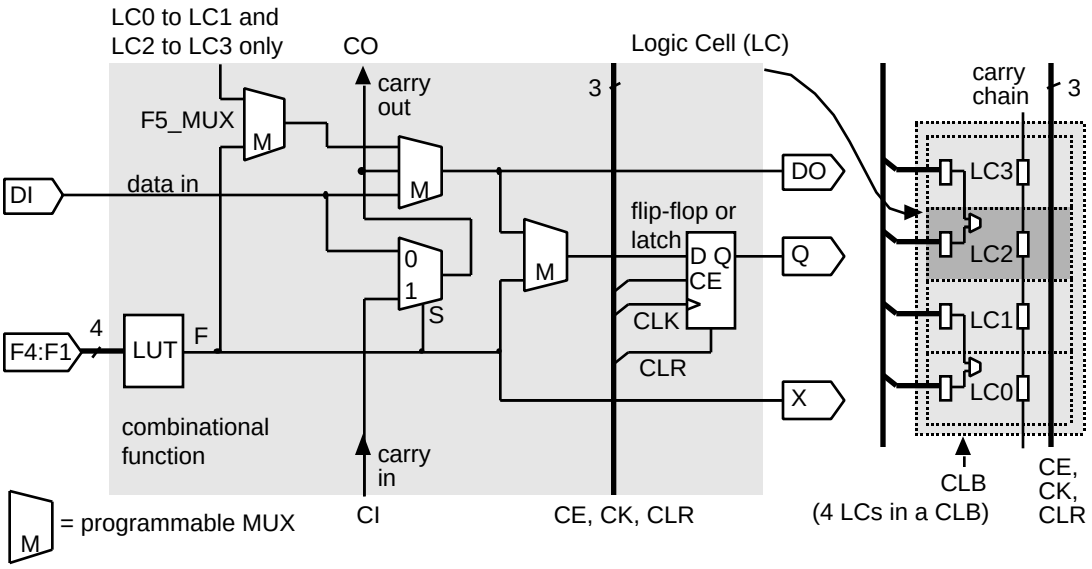
The Xilinx XC3000 CLB (configurable logic block)

(Source: Xilinx.)



The Xilinx XC4000 family CLB (configurable logic block). (*Source:* Xilinx.)

5.2.3 XC5200 Logic Block



The Xilinx XC5200 family **Logic Cell** (LC) and configurable logic block (CLB).(*Source:* Xilinx.)

5.2.4 Xilinx CLB Analysis

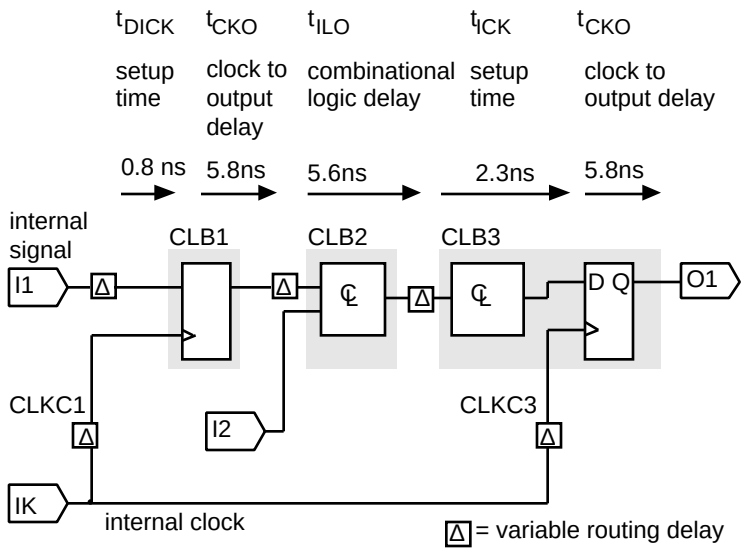
The use of a LUT has advantages and disadvantages:

- An inverter is as slow as a five-input NAND
- A LUT simplifies timing of synchronous logic
- Matched to large SRAM programming technology

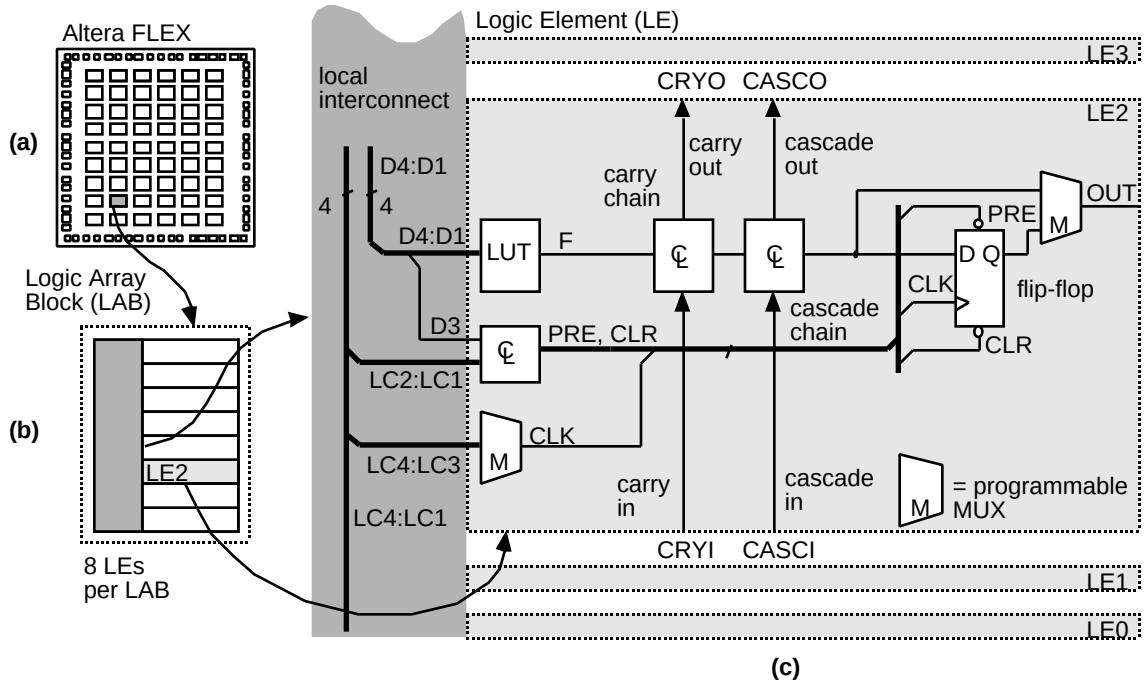
Xilinx uses two speed-grade systems:

- Maximum guaranteed toggle rate of a CLB flip-flop (in MHz) as a suffix—higher is faster
- Example: Xilinx XC3020-125 has a toggle frequency of 125MHz
- Delay time of the combinational logic in a CLB in ns—lower is faster
- Example: XC4010-6 has t_{ILO}=6.0ns
- Correspondence between grade and t_{ILO} is fairly accurate for the XC2000, XC4000, and XC5200 but not for the XC3000

Xilinx LCA timing model (XC5210-6)
(*Source:* Xilinx.)



5.3 Altera FLEX



The Altera FLEX architecture

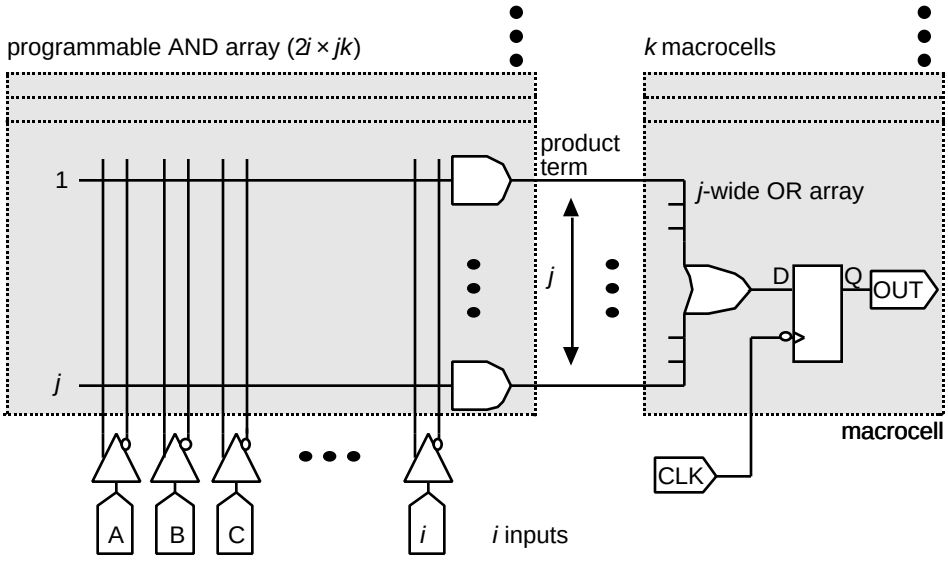
(a) Chip floorplan

(b) Logic Array Block (LAB)

(c) Details of the **Logic Element** (LE)

(*Source:* Altera (adapted with permission).)

5.4 Altera MAX

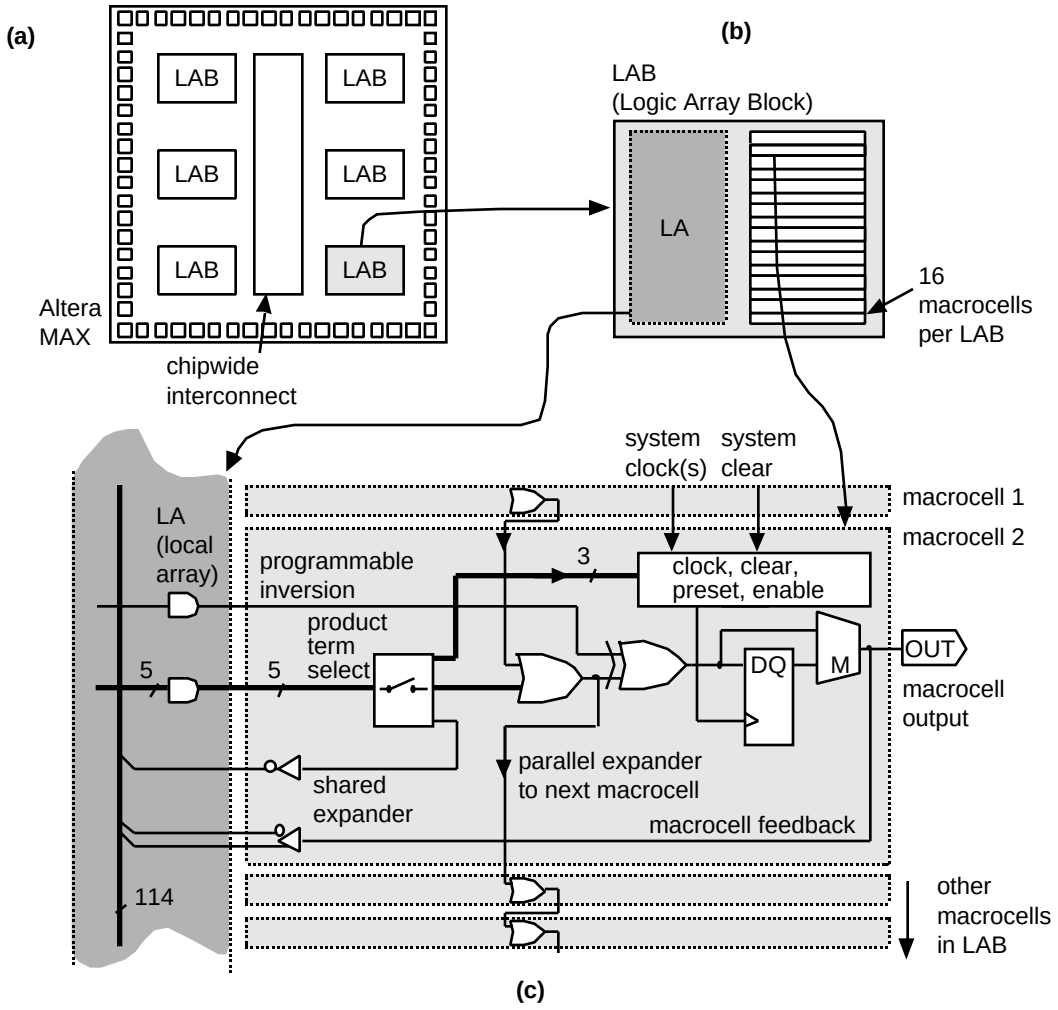


A registered PAL with *i* inputs, *j* product terms, and *k* macrocells. (*Source:* Altera (adapted with permission).)

Features and keywords:

- product-term line
- programmable array logic
- bit line
- word line
- programmable-AND array (or product-term array)
- pull-up resistor
- wired-logic
- wired-AND
- macrocell
- 22V10 PLD

5.4.1 Logic Expanders

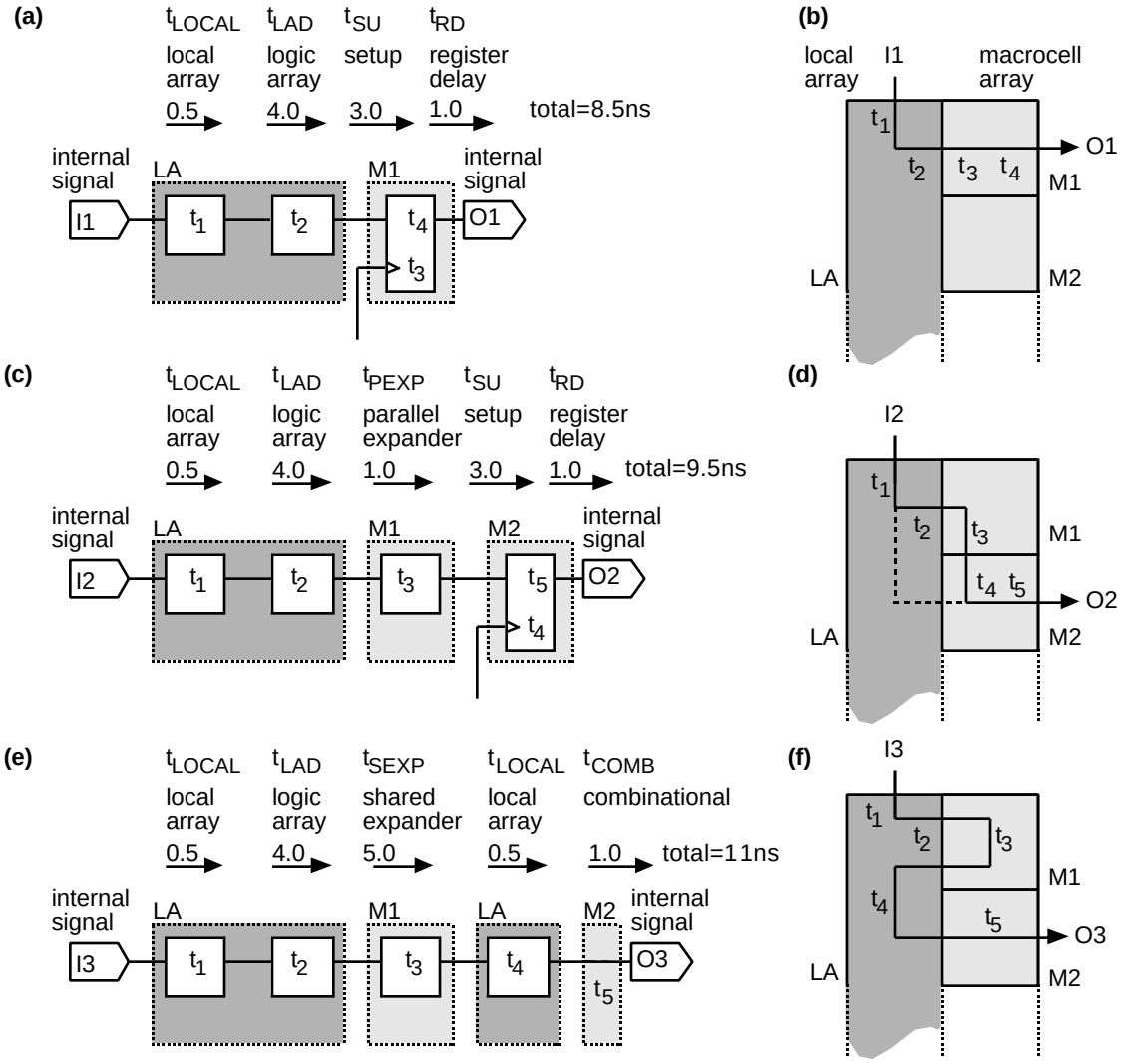


The Altera MAX architecture (the macrocell details vary between the MAX families—the functions shown here are closest to those of the MAX 9000 family macrocells) (*Source:* Altera (adapted with permission).) **(a)** Organization of logic and interconnect **(b)** LAB (Logic Array Block) **(c)** Macrocell

Features:

- Logic expanders and expander terms (helper terms) increase term efficiency
- Shared logic expander (shared expander, intranet) and parallel expander (internet)
- Deterministic architecture allows deterministic timing before logic assignment
- Any use of two-pass logic breaks deterministic timing
- Programmable inversion increases term efficiency

5.4.2 Timing Model



Altera MAX timing model (ns for the MAX 9000 series, '15' speed grade) (*Source:* Altera .)

(a) A direct path through the logic array and a register

(b) Timing for the direct path

(c) Using a parallel expander

(d) Parallel expander timing

(e) Making two passes through the logic array to use a shared expander

(f) Timing for the shared expander (there is no register in this path)

5.4.3 Power Dissipation in Complex PLDs

Key points: **static power • Turbo Bit**

5.5 Summary

Key points: The use of multiplexers, look-up tables, and programmable logic arrays • The difference between fine-grain and coarse-grain FPGA architectures • Worst-case timing design • Flip-flop timing • Timing models • Components of power dissipation in programmable ASICs • Deterministic and nondeterministic FPGA architectures

5.6 Problems

PROGRAMMABLE ASIC I/O CELLS

6

Key concepts:

Input/output cell (I/O cell) • I/O requirements • DC output • AC output • DC input • AC input • Clock input • Power input

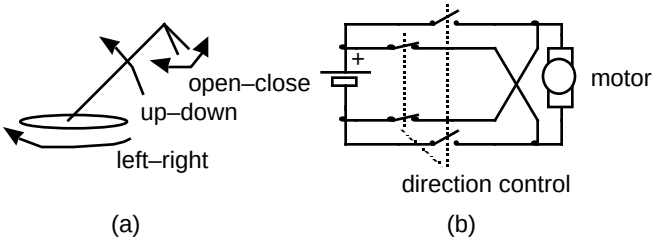
6.1 DC Output

A robot arm example

To design a system work from the outputs back to the inputs

(a) Three small DC motors drive the arm

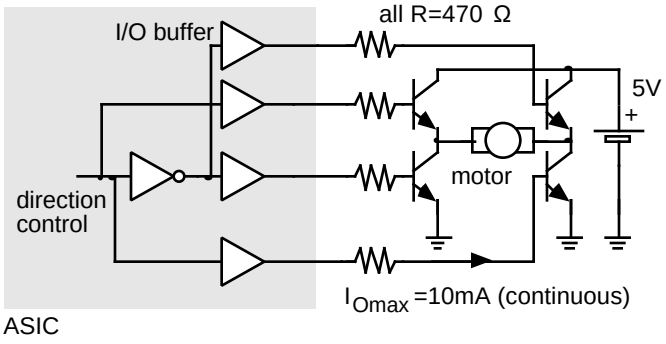
(b) Switches control each motor

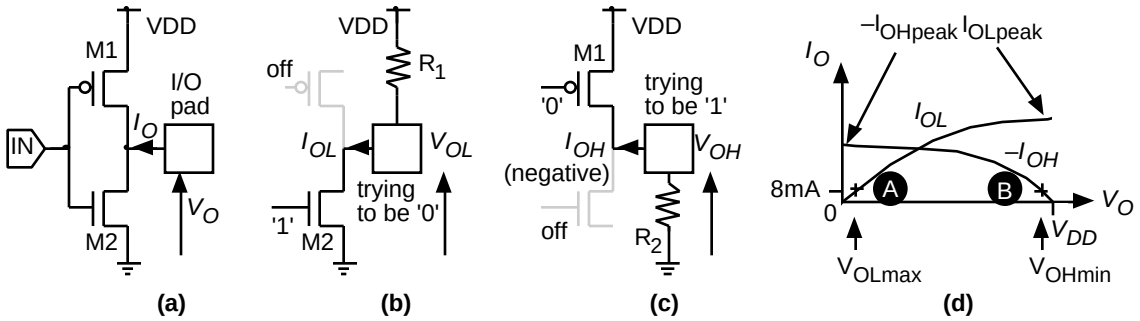


A circuit to drive a small electric motor (0.5A) using ASIC I/O buffers

Work from the outputs to the inputs

The 470Ω resistors drop up to 5V if an output buffer current approaches 10mA, reducing the drive to the output transistors





CMOS output buffer characteristics

(a) A CMOS complementary output buffer

(b) Transistor M2 (M1 off) sinks (to GND) a current I_{OL} through a pull-up resistor, R_1

(c) Transistor M1 (M2 off) sources (from VDD) a current $-I_{OH}$ (I_{OH} is negative) through a pull-down resistor, R_2

(d) Output characteristics:

• Data books specify characteristics at two points, A (V_{OHmin}, I_{OHmax}) and B (V_{OLmax}, I_{OLmax})

Example (Xilinx XC5200):

V_{OLmax}=0.4V, **low-level output voltage** at I_{OLmax}=8.0mA

V_{OHmin}=4.0V, **high-level output voltage** at I_{OHmax}=–8.0mA

• **Output current**, I_O, is positive if it flows into the output

• Input current, if there is any, is positive if it flows into the input

• Output buffer can force the output pad to 0.4V or lower and **sink** no more than 8mA

• When the output is 4V, the buffer can **source** 8mA

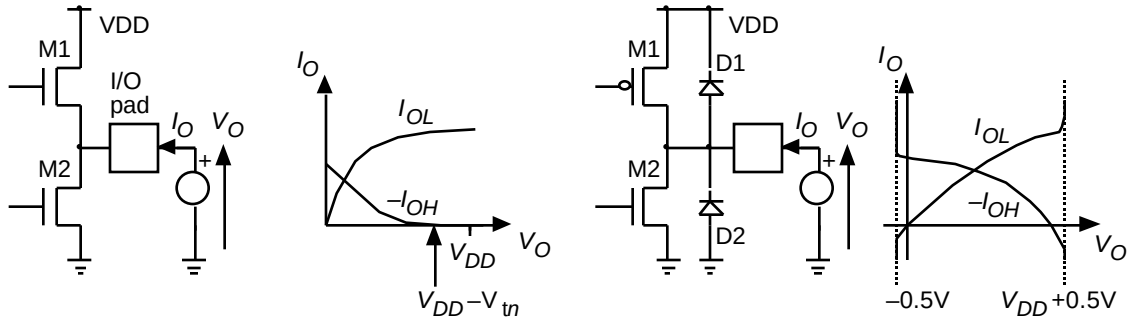
• Specifying only V_{OLmax}=0.4V and V_{OHmin}=4.0V for a technology is strictly incorrect

• We do not know the value of I_{OLpeak} or I_{OHpeak} (typical values are 50–200mA)

6.1.1 Totem-Pole Output

Keywords: totem-pole output buffer • similar to TTL totem-pole output • two n-channel transistors in a stack • reduced output voltage swing

6.1.2 Clamp Diodes



(a) **(b)** **(c)** **(d)**

Output buffer characteristics

(a) A CMOS totem-pole output stage (both M1 and M2 are n-channel transistors)

(b) Totem-pole output characteristics (notice the reduced signal swing)

(c) Clamp diodes, D1 and D2, in an output buffer (totem-pole or complementary) prevent the I/O pad from voltage excursions greater than V_{DD} and less than V_{SS}

(d) The clamp diodes conduct as the output voltage exceeds the supply voltage bounds

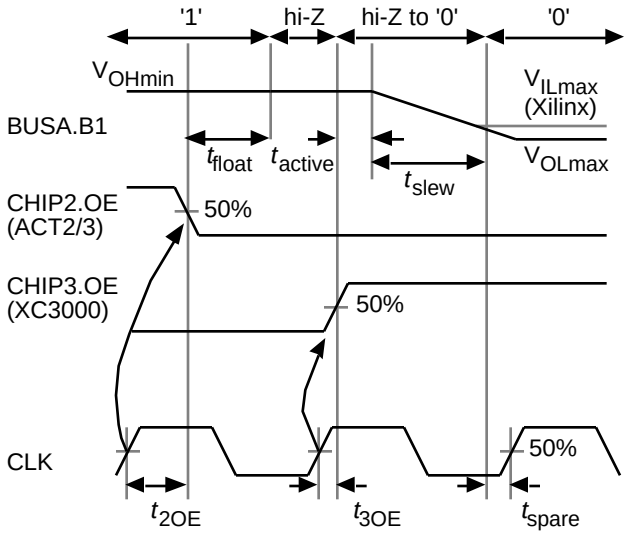
6.2 AC Output

Keywords: bus transceivers • bus transaction (a sequence of signals on a bus) • floating a bus • bus keeper • trip points • three-stated (high-impedance or hi-Z) • time to float • disable time, time to begin hi-Z, or time to turn off • slew • sustained three-state (s/t/s) • turnaround cycle

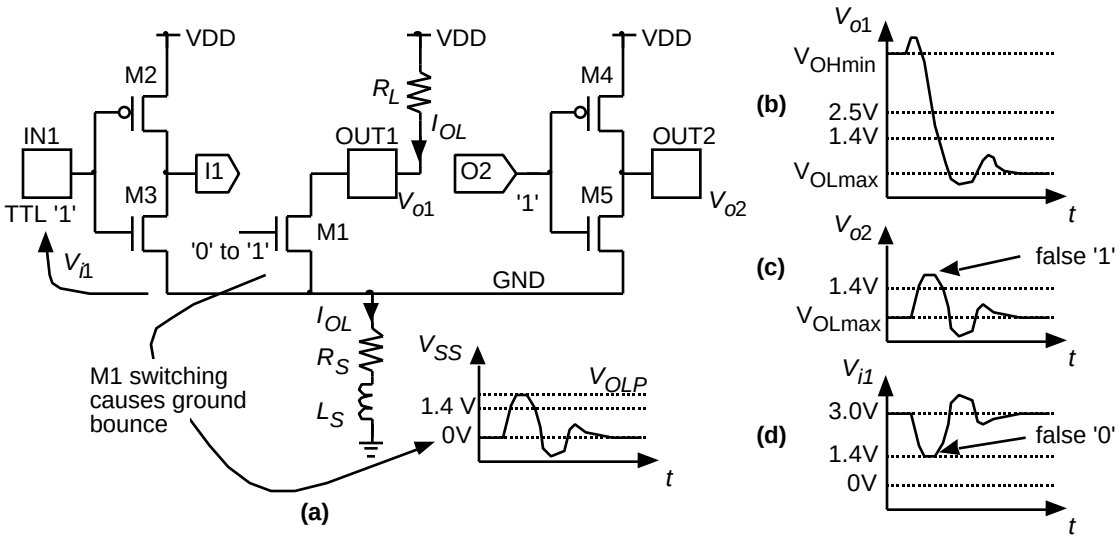
Three-state bus timing

The on-chip delays, t_{2OE} and t_{3OE}, for the logic that generates signals CHIP2.E1 and CHIP3.E1 are derived from the timing models

(The minimum values for each chip would be the clock-to-Q delay times)



6.2.1 Supply Bounce



Supply bounce

A substantial current I_{OL} may flow in the resistance, R_S, and inductance, L_S, that are between the on-chip GND net and the off-chip, external ground connection

(a) As the pull-down device, M1, switches, it causes the GND net (value V_{SS}) to **bounce**

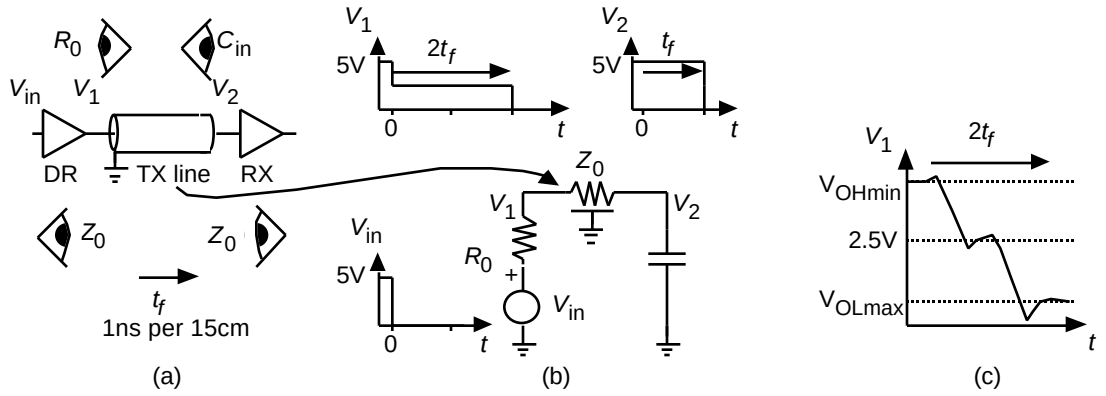
(b) The **supply bounce** is dependent on the output slew rate

(c) Ground bounce can cause other output buffers to generate a **logic glitch**

(d) Bounce can also cause errors on other inputs

Keywords: simultaneously-switching outputs (SSOs) • quiet I/O • slew-rate control • I/O management • packaging • PCB layout • ground planes • inductance

6.2.2 Transmission Lines



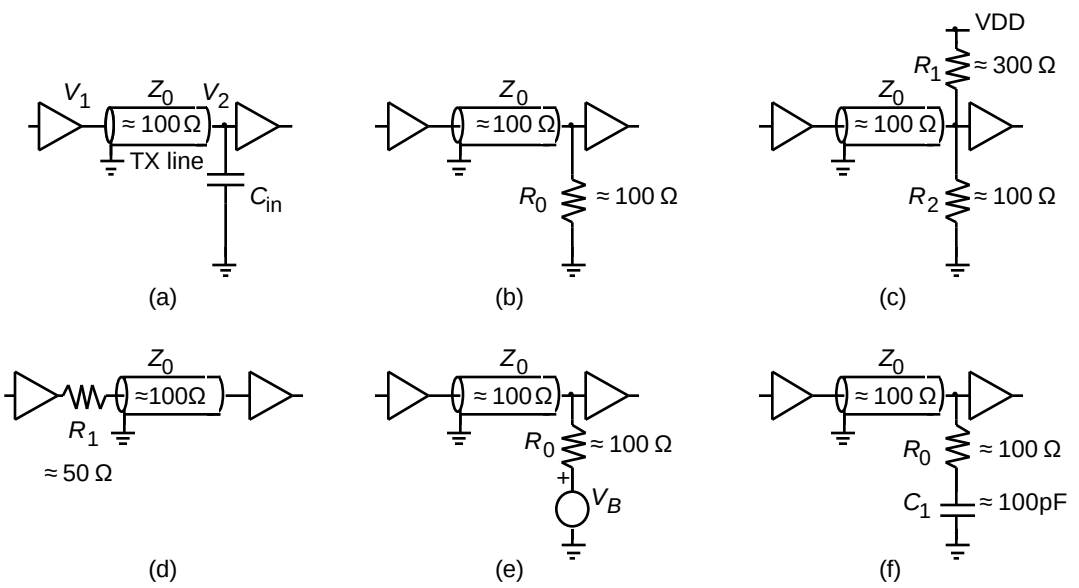
Transmission lines

(a) A printed-circuit board (PCB) trace is a transmission (TX) line (Z_0 = 50Ω–100Ω)

(b) A driver launches an incident wave, which is reflected at the end of the line

(c) A connection starts to look like a TX line when the rise time is about 2 × line delay ($2t_f$)

6.3 DC Input



Transmission line termination

(a) Open-circuit or capacitive termination

(b) Parallel resistive termination

(c) Thévenin termination

(d) Series termination at the source

(e) Parallel termination using a voltage bias

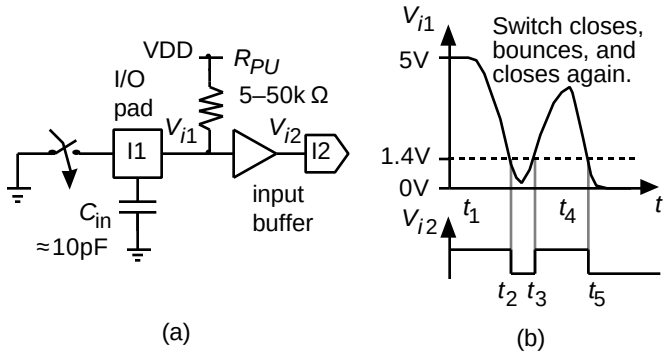
(f) Parallel termination with a series capacitor

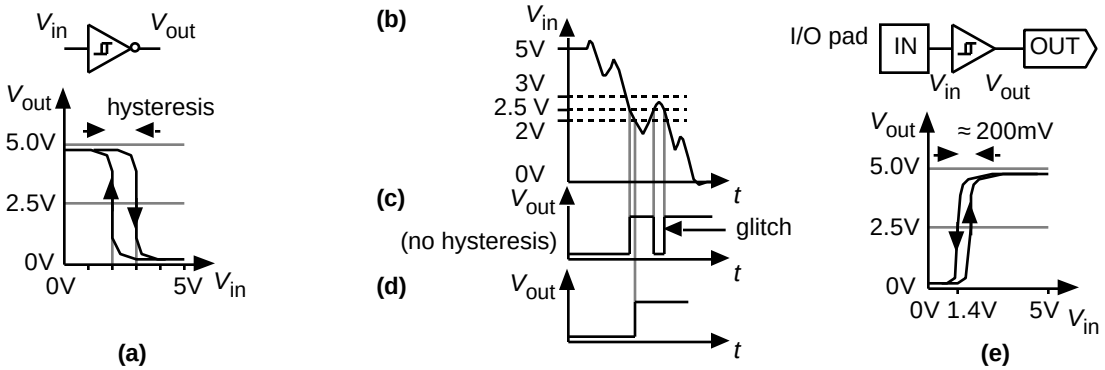
A switch input

(a) A pushbutton switch connected to an input buffer with a pull-up resistor

(b) As the switch bounces several pulses may be generated

We might have to **debounce** this signal using an SR flip-flop or small state machine





DC input

(a) A **Schmitt-trigger inverter** • lower switching threshold • upper switching threshold • difference between thresholds is the **hysteresis**

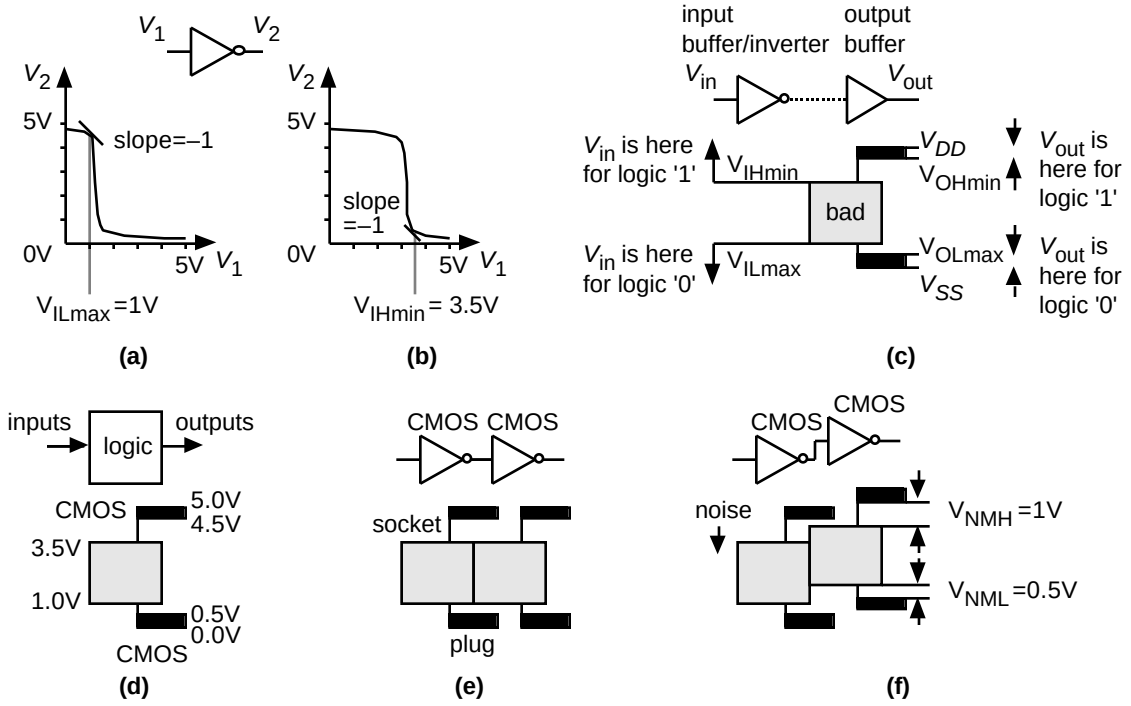
(b) A noisy input signal

(c) Output from an inverter with no hysteresis

(d) Hysteresis helps prevent **glitches**

(e) A typical FPGA input buffer with a hysteresis of 200mV and a threshold of 1.4V

6.3.1 Noise Margins



Noise margins

(a) Transfer characteristics of a CMOS inverter with the lowest switching threshold

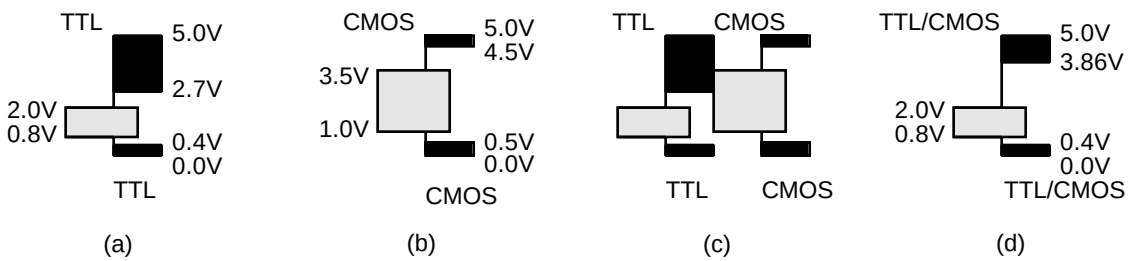
(b) The highest switching threshold

(c) A graphical representation of CMOS **logic thresholds**

(d) Logic thresholds at the inputs and outputs of a logic gate or an ASIC

(e) The switching thresholds viewed as a plug and socket

(f) CMOS plugs fit CMOS sockets and the clearances are the **noise margins**



TTL and CMOS logic thresholds

(a) TTL logic thresholds

(b) Typical CMOS logic thresholds

(c) A TTL plug will not fit in a CMOS socket

(d) Raising V_{OHmin} solves the problem

6.3.2 Mixed-Voltage Systems

FPGA logic thresholds

	I/O options		Input levels		Output levels (high current)				Output levels (low current)			
XC3000	TTL		2.0	0.8	3.86	–4.0	0.40	4.0				
	CMOS		3.85	0.9	3.86	–4.0	0.40	4.0				
XC3000L			2.0	0.8	2.40	–4.0	0.40	4.0	2.80	–0.1	0.2	0.1
XC4000			2.0	0.8	2.40	–4.0	0.40	12.0				
XC4000H	TTL	TTL	2.0	0.8	2.40	–4.0	0.50	24.0				
	CMOS	CMOS	3.85	0.9	4.00	–1.0	0.50	24.0				
XC8100	TTL	R	2.0	0.8	3.86	–4.0	0.50	24.0				
	CMOS	C	3.85	0.9	3.86	–4.0	0.40	4.0				
ACT 2/3			2.0	0.8	2.4	–8.0	0.50	12.0	3.84	–4.0	0.33	6.0
FLEX10k		3V/5V	2.0	0.8	2.4	–4.0	0.45	12.0				

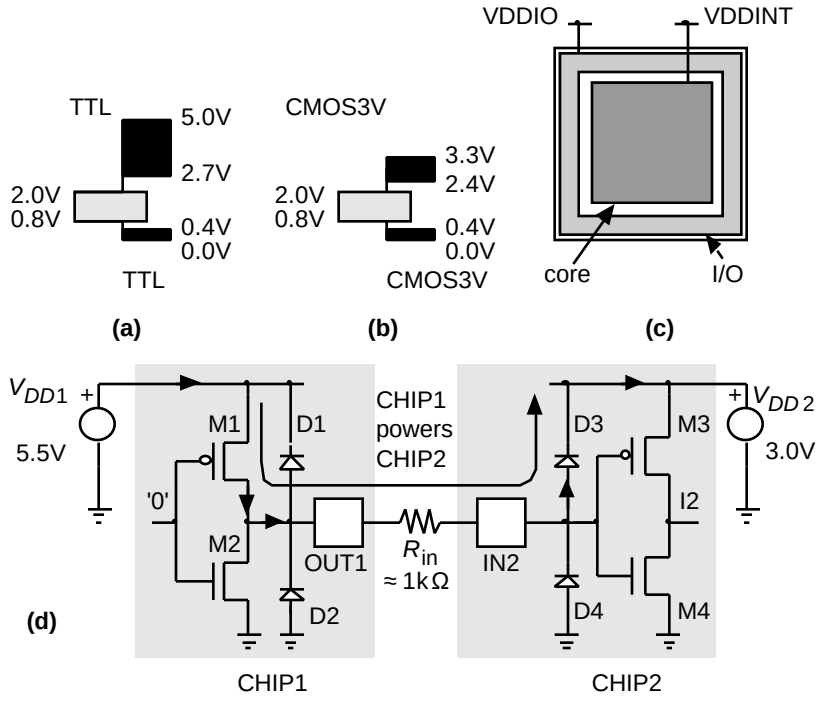
Mixed-voltage systems

(a) TTL levels

(b) Low-voltage CMOS levels • JEDEC 8 • 3.3±0.3V

(c) Mixed-voltage ASIC • 5V-tolerant I/O • V_{DDint} and $V_{DDI/O}$

(d) A problem when connecting two chips with different supply voltages—caused by the input clamp diodes



6.4 AC Input

Keywords and concepts: input bus • sampled data • clock frequency of 100kHz • FPGA • system clock • 10MHz • Data should be at the flip-flop input at least the flip-flop setup time before the clock edge. Unfortunately there is no way to guarantee this; the data clock and the system clock are completely independent

6.4.1 Metastability

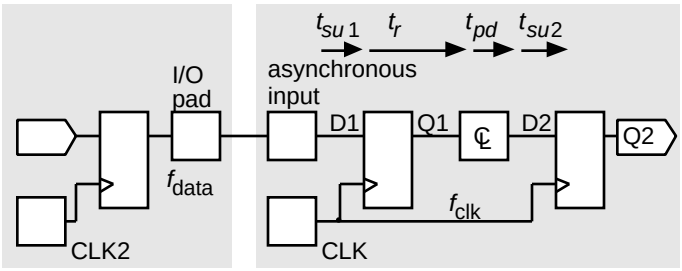
Metastability

(a) Data coming from one clocked system is an **asynchronous** input to another

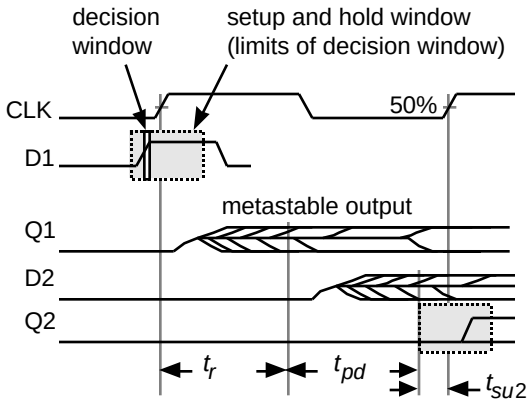
(b) A flip-flop (or latch, a **sampler**) has a very narrow decision window bounded by the setup and hold times to **resolve** the input

If the data input changes inside the decision window (a setup or hold-time **violation**) the output may be **metastable**—neither '1' or '0'—an **upset**

(a)



(b)



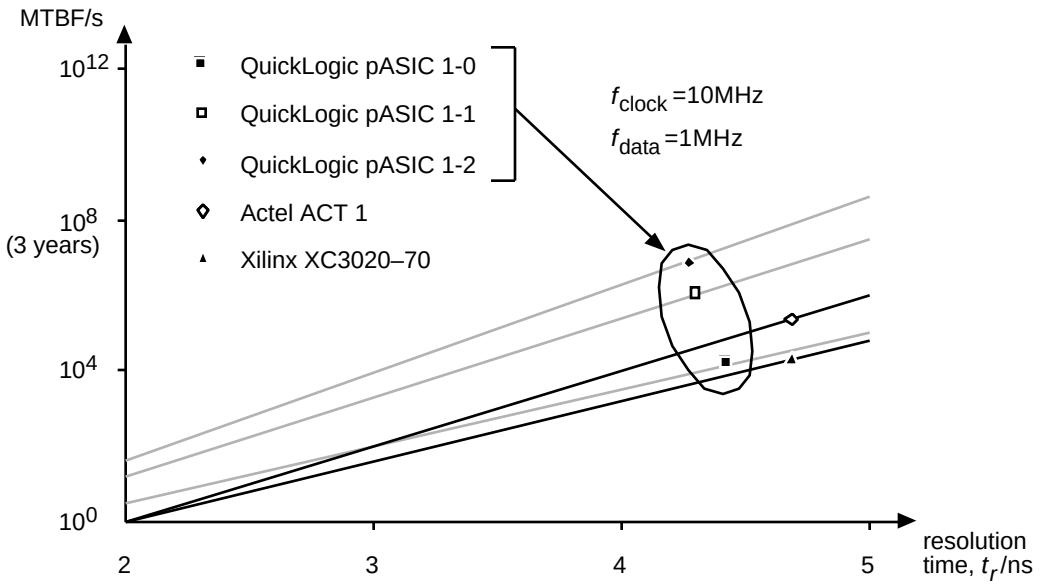
Metastability parameters for FPGA flip-flops (not guaranteed by the vendors)		
FPGA	**T_0/s**	**τ_c/s**
Actel ACT 1	1.0E–09	2.17E–10
Xilinx XC3020-70	1.5E–10	2.71E–10
QuickLogic QL12x16-0	2.94E–11	2.91E–10
QuickLogic QL12x16-1	8.38E–11	2.09E–10
QuickLogic QL12x16-2	1.23E–10	1.85E–10
Altera MAX 7000	2.98E–17	2.00E–10
Altera FLEX 8000	1.01E–13	7.89E–11

The **mean time between upsets** (**MTBU**) or MTBF is

$$\text{MTBU} = \frac{1}{p f_{\text{clock}} f_{\text{data}}} = \frac{\exp t_r/\tau_c}{f_{\text{clock}}\, f_{\text{data}}}$$

where f_{clock} is the clock frequency and f_{data} is the data frequency

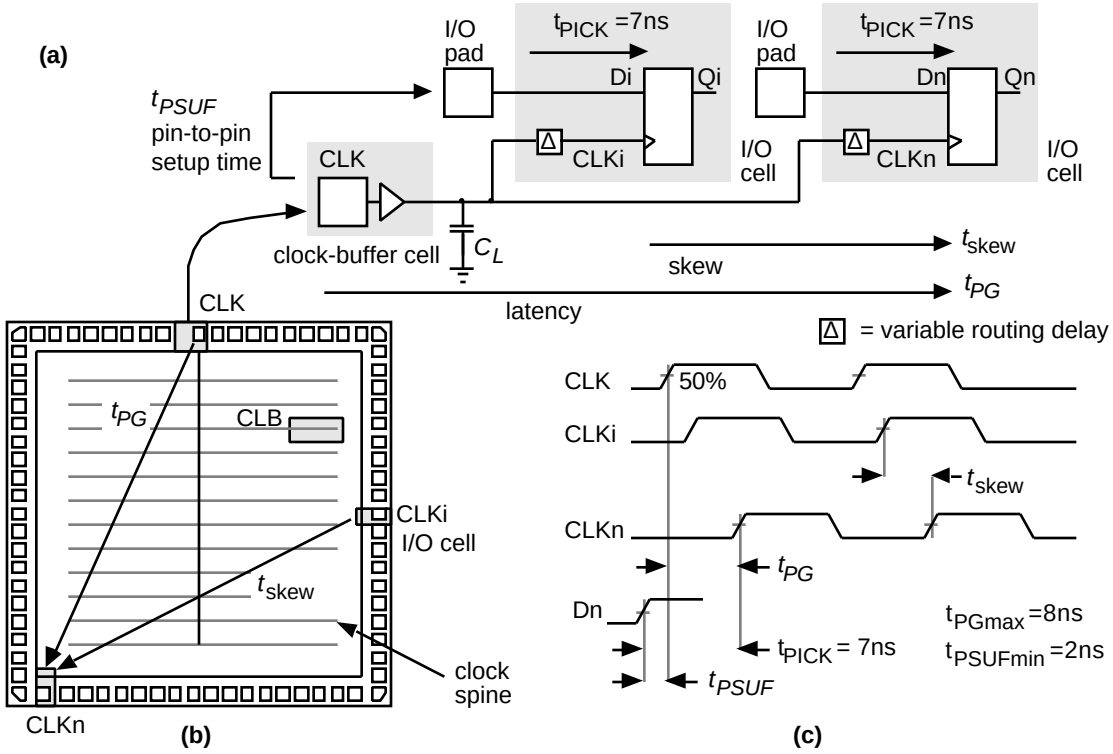
A **synchronizer** is built from two flip-flops in cascade, and greatly reduces the effective values of τ_c and T_0 over a single flip-flop. The penalty is an extra clock cycle of latency.



Mean time between failure (MTBF) as a function of resolution time

The data is from FPGA vendors' data books for a single flip-flop with clock frequency of 10MHz and a data input frequency of 1MHz

6.5 Clock Input



Clock input

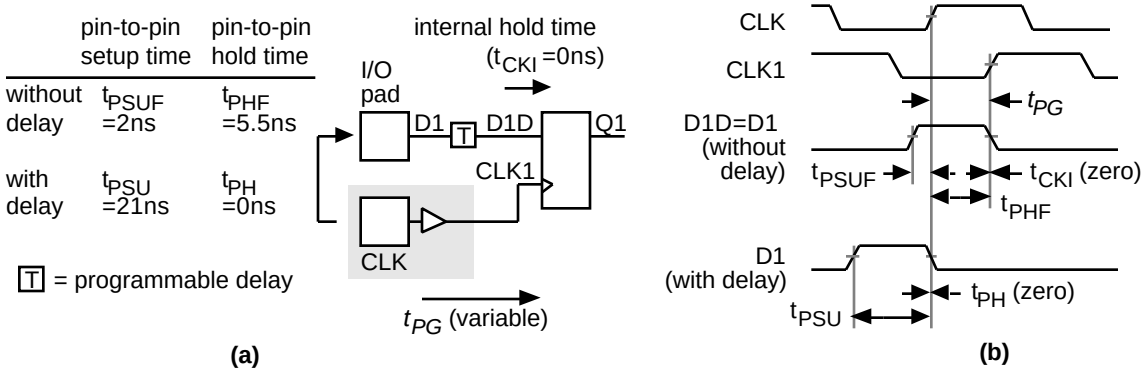
(a) Timing model (Xilinx XC4005-6)

(b) A simplified view of clock distribution • **clock skew** • **clock latency**

(c) Timing diagram

(Xilinx eliminates the variable internal delay t_{PG}, by specifying a **pin-to-pin setup time**, $t_{PSUFmin}$=2ns)

6.5.1 Registered Input



Programmable input delay

(a) Pin-to-pin timing model (XC4005-6) with pin-to-pin timing parameters

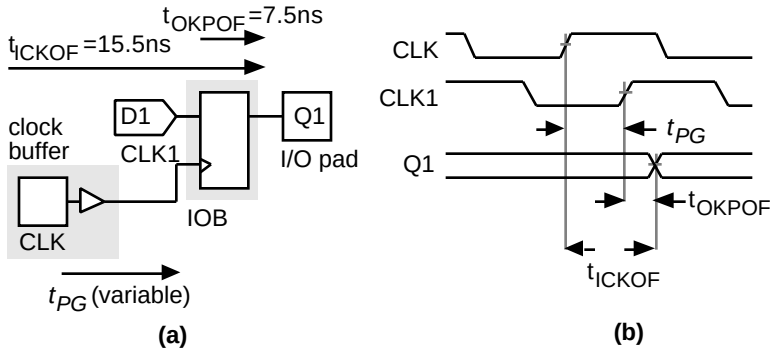
(b) Timing diagrams with and without programmable delay

Notice $t_{PSUFmin}$ = 2 ns ≠ t_{PICK} – t_{PGmax} = –1 ns

Registered output

(a) Timing model with values for an XC4005-6 programmed with the fast slew-rate option

(b) Timing diagram



6.6 Power Input

6.6.1 Power Dissipation

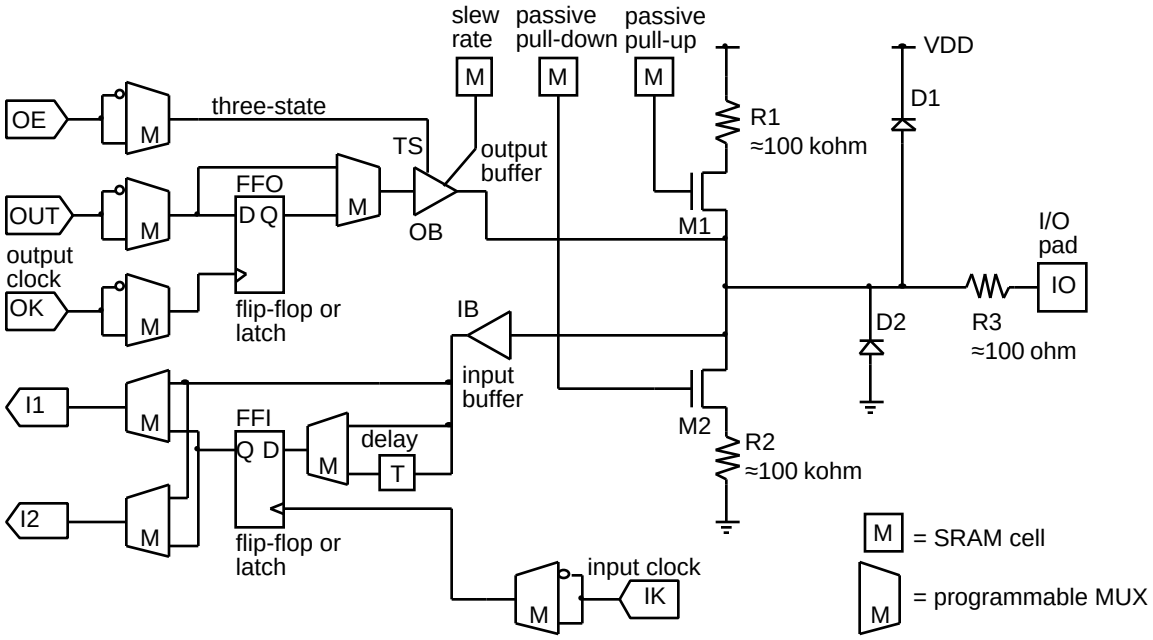
Thermal characteristics of ASIC packages

Package	Pin count	Max. power P_{max}/W	θ_{JA} /°CW^{-1} (still air)	θ_{JA} /°CW^{-1} (still air)
CPGA	84		33	32–38
CQFP	84		40	
CQFP	172		25	
VQFP	80		68	

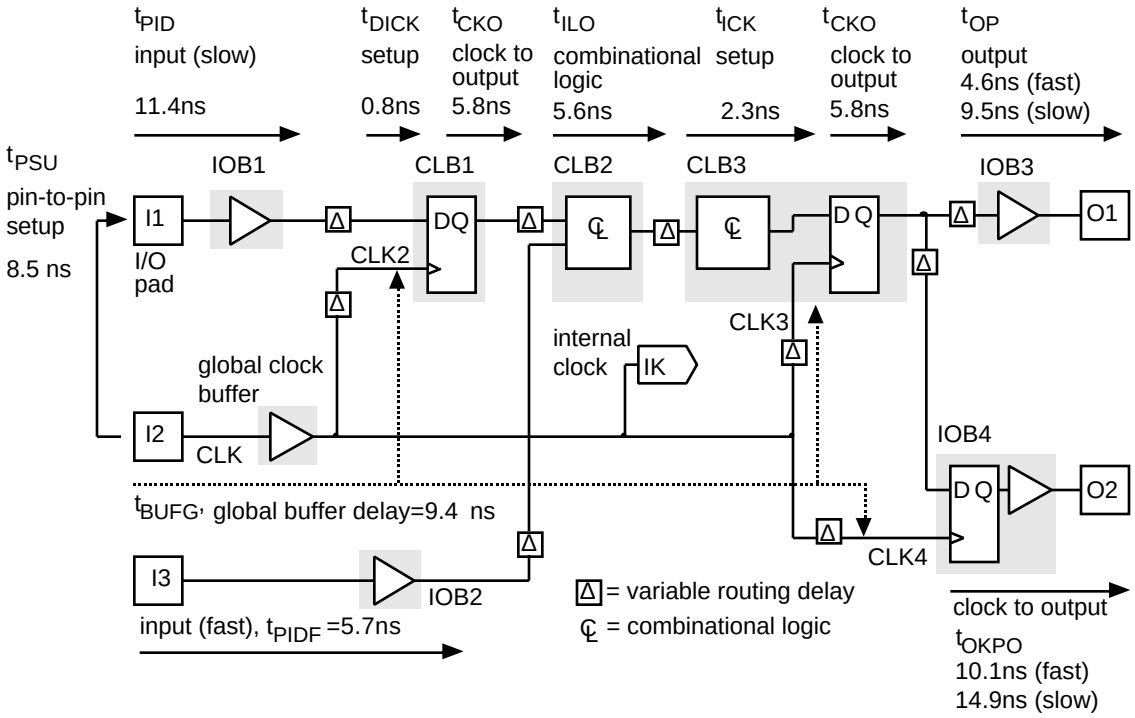
6.6.2 Power-On Reset

Key concepts: Power-on reset sequence • Xilinx FPGAs configure all flip-flops (in either the CLBs or IOBs) as either SET or RESET • after chip programming is complete, the global SET/RESET signal forces all flip-flops on the chip to a known state • this may determine the initial state of a state machine, for example

6.7 Xilinx I/O Block



The Xilinx XC4000 family IOB (input/output block). (*Source:* Xilinx.)



The Xilinx LCA (Logic Cell Array) timing model (XC5210-6). (*Source:* Xilinx.)

6.7.1 Boundary Scan

Key concepts: IEEE boundary-scan standard 1149.1 • Many FPGAs contain a standard boundary-scan test logic structure with a four-pin interface • **in-system programming** (ISP)

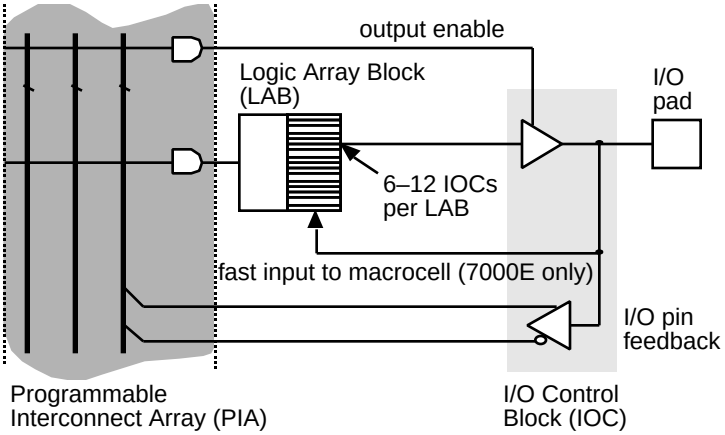
6.8 Other I/O Cells

A simplified block diagram of the Altera **I/O Control Block** (IOC) used in the MAX 5000 and MAX 7000 series

The **I/O pin feedback** allows the I/O pad to be isolated from the macrocell

It is thus possible to use a LAB without using up an I/O pad (as you often have to do using a PLD such as a 22V10)

The **PIA** is the chipwide interconnect

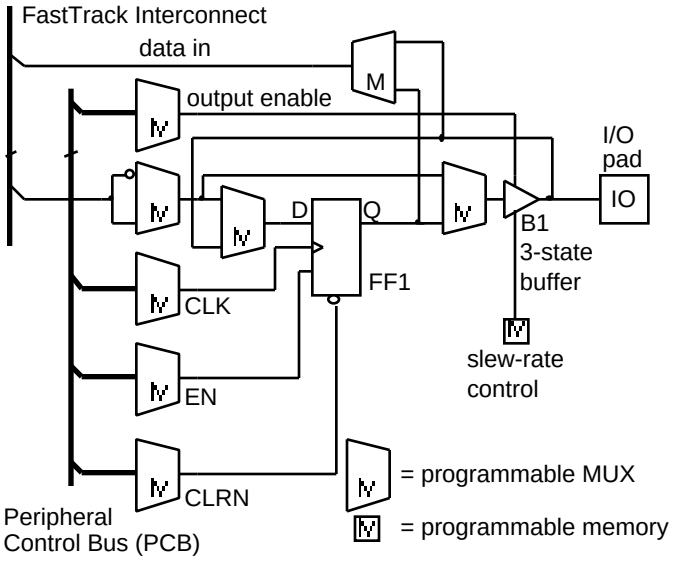


A simplified block diagram of the Altera **I/O Element** (IOE), used in the FLEX 8000 and 10k series

The MAX 9000 IOC (I/O Cell) is similar

The FastTrack Interconnect bus is the chipwide interconnect

The **Peripheral Control Bus** (PCB) is used for control signals common to each IOE



6.9 Summary

Key concepts:

Outputs can typically source or sink 5–10mA continuously into a DC load

Outputs can typically source or sink 50–200mA transiently into an AC load

Input buffers can be CMOS (threshold at $0.5V_{DD}$) or TTL (1.4V)

Input buffers normally have a small hysteresis (100–200mV)

CMOS inputs must never be left floating

Clamp diodes to GND and VDD are present on every pin

Inputs and outputs can be registered or direct

I/O registers can be in the I/O cell or in the core

Metastability is a problem when working with asynchronous inputs

Questions	opt1	opt2	opt3	opt4	opt 5	opt 6	Answer
In which design all circuitry and all interconnections are designed?	full custom design.	semi-custom design	gate array design	transistor design			full custom design.
Which design contains only the interconnections designed?	full custom design	semi-custom design	gate array design .	transistor design			gate array design .
In which method regularity is used to reduce complexity?	random approach	hierarchical approach.	algorithmic approach	semi-design approach			hierarchical approach.
Size of the die is determined using	transistor size	inverter size	area of the circuitry .	length of the circuitry			area of the circuitry
Which design is faster?	full custom design	semi-custom design	gate array design .	transistor design			gate array design .
Which has relatively low-level capabilities?	hand-crafted designs	computer assisted textual entry .	compute r assisted graphical entry	silicon compiler-based design			computer assisted textual entry .
Computer-assisted graphical entry is done through	monochrom e .	grayscale graphics	bichrome	trichrome			monochro me .
Which method is used for verification along with generation?	hand-crafted designs	computer assisted textual entry	compute r assisted graphical entry.	silicon compiler-based design			computer assisted graphical entry.
Whih method uses high level programming language?	hand-crafted designs	computer assisted textual entry	compute r assisted graphical entry	silicon compiler-based design .			silicon compiler-based design .
The set of design rules does not give	widths	spacing	colours .	overlaps			colours .
When setting the voltage for an external device that must interface with an FPGA, you must	VCCIO .	VDDIN	VDDiO	VCCIN			VCCIO .
Which of the following digital IC logic families is most susceptible to static discharge?	RTL	ECL	MOS.	TTL			MOS.
Which of the following is a	mechanical shock	electrostatic	fan out	under voltage			electrostati c

concern when using CMOS type devices?		discharge .			discharge .
Which of the following is not a solution to interface problems between CMOS and TTL?	pull- up resistor	pull- down resistor .	level- shifter	buffer	pull- down resistor .
Which of the following is not a common logic family used today?	RTL .	ECL	TTL	CMOS	RTL .
The output current for a LOW output is called a(n)	exit current	sink current.	ground current	fan- out.	sink current.
Which of the following are not characteristics of TTL logic gates?	Totem- pole output	Bipolar transistors	CMOS transistor s .	Multiemitt er transistors	CMOS transistors .
) Which of the following output levels would not be a valid LOW for a TTL gate?	0.3	0.5	0.2	All are valid .	All are valid .
A family of logic devices designed for extremely high speed applications is called	NMOS	ECL .	PMOS	TTL	ECL .
) Unused inputs on TTL, AND, and NAND gates	degrade the gate's noise immunity.	if left open will have the same effect as HIGH inputs.	should be tied HIGH.	All of the above are correct .	All of the above are correct .
) The lower transistor of a totem- pole output is OFF when the gate output is	HIGH.	malfunctioni ng	LOW	over driven	HIGH.
) The input transistor on a TTL circuit is unusual in that it has	multiple bases.	no collector.	no base	multiple emitters .	multiple emitters .
) The 54XX TTL IC series is the military version and has	a wider temperatur e range.	more stringent power supply requirement s.	higher current output capability .	all of the above	a wider temperatur e range.

Which potential problem must be overcome when interfacing TTL to CMOS?	The HIGH output voltage may be too low.	The LOW output voltage may be too high.	The HIGH output voltage may be too high.	The output current may not be sufficient	The HIGH output voltage may be too low.
Typical TTL LOW level output voltage is	0.3V.	0.0V	3.4V	4.0V	0.3V.
When the outputs of several open-collector TTL gates are connected together, the gate outputs	produce more fan-out.	usually burn out.	are ANDed together .	produce more voltage.	are ANDed together .
) The abbreviated designation for output current with a LOW output is	OOL	IOL .	iOH	IIH	IOL
The input transistor (Q 1) of a TTL gate acts like	NAND	NOR.	AND..	OR	AND
The unused input for a NOR gate should be tied to	HIGH.	ground..	another unused input.	both B and C	ground.
Which of the following output levels would be a valid HIGH for a TTL gate?	3.0V	2.6V	5.1	All are valid .	All are valid.

The noise margin for a standard TTL gate is	1.0V	0.4V .	1.4V	0.8V	0.4V .
) When a TTL gate output connects to a CMOS gate, what must be added to the circuit?	a decoupling capacitor	a pull- up resistor .	a pull-down resistor	an open-collector gate	a pull- up resistor .
Which of the following levels would <u>not</u> be a valid LOW for a TTL gate?	0.1V	0.7V	1.0V .	All are valid	1.0V .
) What advantage does the 74HXX series device have over standard TTL?	reduced propagation delay .	higher propagation delay	low power consumption	lower voltage requirements	reduced propagation delay .
The CMOS series that is pin compatible with the TTL family is the	74C00 series.	4000 series.	5400 series.	7400 series	74C00 series.
) The propagation delay of standard TTL gates is approximately	2 µsec	10 nsec .	4 nsec.	1 µsec	10 nsec .
) Which alteration is made in the manufacture of a TTL gate to create	The output transistors are replaced by	The input transistor is replaced by a	The output transistors	The top output transistor is	The top output transistor is

an open- collector output?	diodes.	diode.	are missing.	missing..	missing..
) One advantage that MOSFET transistors have over bipolar transistors is	reduced propagation delay.	higher switching speed.	high input impedance.	low input impedance	high input impedance.
The original CMOS line of circuits is the	5400 series.	4000 series..	74C00 series	74HCOO series.	4000 series.

Questions	opt1	opt2	opt3	opt4	opt 5	opt 6	Answer
new generation of_____a re emerging that could add flexibility and investment protection for networks.	FPGA	programmable ASICs	ASIC	logic cell			programmable ASICs
ASIC stands for_____ ___	Application-specific integrated circuit	Application-specific integrated circuit	Application-specific intermodulated circuit	Application-specific inter circuit			Application-specific integrated circuit
FPGAs may be more_____ ___ than an ASIC design	costly	low cost	cost effective	effective			cost effective
The programming technology in an FPGA determines the type of scheme	logic cell	basic logic cell and the interconnect	interconnection	basic cell			basic logic cell and the interconnect
programming technologies are classified into	3	4	5	2			3
Antifuse PLDs have advantages over SRAM based PLDs. they do not need to be configured each	applied time	time power is applied.	power speed	applied power			time power is applied.
Each bit contains_____ _____ is programmed by triggering one of the two.	fuse	none	both a fuse and an antifuse	antifused conductor and semi conductor			both a fuse and an antifuse
antifuses employ a very thin oxide barrier between_____ ____.	semi conductor	a pair of conductors	conductor				a pair of conductors
SRAM is a type of semiconductor	bistable latching	flip flop	stable	unstable			bistable latching

memory that uses_____ to store each bit.	circuitry (flip-flop)				circuitry (flip-flop)
Types of SRAM is_____.	NV-SRAM	PS-SRAM	BOTH	none	BOTH
The power consumption of _____ varies widely depending on frequently it is accessed.	RAM	SRAM	ROM	EPROM	SRAM
EEPROM cells consist of one, one-and-a-half, or two transistor. then EPROM cells consist of _____ ___.	one transistor	two transistor	three transistor	four transistor	one transistor
_____ ___is a special type of ROM that is programmed electrically and erasable under UV light.	SRAM	EPROM	RAM	ROM	EPROM
The EPROM device is programmed by forcing an electrical charge on a small piece of_____located in the memory cell.	silicon	silicon metal	polysilicon material	monosilicon	polysilicon material
EPROM floating gate transistor characteristic theory also applies to_____ .	flash devices	EEPROM and flash devices.	EPROM	none	EEPROM and flash devices.
EPROMs were created in the_____	1980s	1960s	1970s	1990s	1970s

and have long been the cornerstone of the non-volatile memory market					
Actel FPGA is very similar to that of a _____array	non conventional gate	none	conventional gate	all the above	conventional gate
the logic core is the interface to the_____of the devices	output pads	I/O pads	all the above	none	I/O pads
The first Actel logic module was the Simple Logic Module is used in _____	the ACT 2 family	the ACT 4 family	the ACT 1 family	none	the ACT 1 family
core module of the act 3 is_____	sequential order	enhanced sequential	combinatorial	Combinatorial and Enhanced Sequential Modules	Combinatorial and Enhanced Sequential Modules
The storage element can be either a_____	register or a latch.	register	latch	none	register or a latch.
the 3200DX family has a number of special logic modules optimized for implementing _____functions directly driving device outputpads.	output	input and output	wide-inputcombinatorial logic	all the above	wide-inputcombinatorial logic
_____ used in the ACT 3 family is a refinement of the Sequential Logic Module	logic module	The Enhanced Sequential Logic Module	sequential logic	all the above	The Enhanced Sequential Logic Module

the hierarchical Xilinx LCA interconnect architecture_____	The vertical and horizontal lines run between CLBs.	cross section	vertical lines	horizontal lines	The vertical lines and horizontal lines run between CLB
Xilinx 8th employee Bill Carter hired in 1984 as _____					
suggested that this concept required many precious transistors	the second IC designer	the third IC designer	the fourth IC designer	the first IC designer	the first IC designer
_____is a special implementation strategy was elaborated for the microprocessor's RAM and ALU blocks	20KA technology	Altera FLEX 10KA technology	none	all the above	Altera FLEX 10KA technology
Altera FLEX 10K family contains up to_____of embedded memory;	100K gates and 24,576 bits	10,000 bits	1240 bits	1856 bits and 200k bits	100K gates and 24,576 bits
The Altera Max 10 has _____ and user memory the routing switches are based SRAM.	programmable	reprogrammable flash configuration	flash configuration	none	reprogrammable flash configuration
Each clock source can come from any of_____ located on the same side of the device as the PLL.	the two or four clock pins	the one or 2 clock pins	the two or five clock pins	only 6 clock pins	the two or four clock pins
The MAX 10 device family supports_____	low speed	high-speed LVDS	speed LVDS	high LVDS	high-speed LVDS

__protocols through the LVDS I/O banks The MAX 10 solution uses shift registers, internal PLLs, and I/O elements to perform _____	serial	parallel	serial-to-parallel and parallel-to-serial	serial to parallel	serial-to-parallel and parallel-to-serial
FPGA logic thresholds of xc3000 input level is___	1.0,2.0	2.0,0.8	5.0,0.1	0.6,4.0	2.0,0.8
FPGA logic thresholds of ACT 2/3 output (low level) is_____	9.0,3.11,5.7	6.45,0.08	3.84 ,–4.0 ,0.33 ,6.0	1.67,2.63	3.84 ,–4.0, 0.33, 6.0
I/O cells handle driving signals off chip		conditioning			conditioning external inputs
Receiving and _____	internal input	external inputs	internal output	external output	
Design Entry - Description of a microelectronic system to _____.	a set of ASIC tools	a set of EDA tools	none	all the above	a set of EDA tools
_____ _ is the most common method of design entry for ASICs	systematic entry	none	Schematic entry	all the above	Schematic entry
HDLs are replacing the conventional____ _____ schematic entry	gate-level	sequential level	combinatorial	enhanced sequential level	gate-level
A second problem with ASIC schematic libraries is that there are_____for	standards	no standards	sequential standards	all the above	no standards

cell behavior.

Schematics can be a very effective way to convey design information because pictures are such _____	a set of medium	a sequential medium	a powerful medium	none	a powerful medium

Questions	opt1	opt2	opt3	opt4	opt5	Answer
Which of the following HDLs are IEEE standards?	a) VHDL and Verilog	b) C and C++	c) Altera and Xilinx	d) Quartus II and MaxPlus II		a) VHDL and Verilog
VHDL is based on which of the following programming languages?	a) ADA programming language	b) C	c) Assembly	d) PHP		a) ADA programming language
What is the advantage of using VHDL instead of any other HDL?	a) Week typing	b) Based on ADA	c) Portability	d) Easy to code		c) Portability
Which of the following is a characteristic of Verilog HDL?	a) Strongly typed language	b) Case sensitive	c) Better library	d) Not portable		b) Case sensitive
The most basic form of behavioral modeling in VHDL is_____	a) IF statements	b) Assignment statements	c) Loop statements	d) WAIT statements		b) Assignment statements
The main problem with behavioral modeling is _____	a) Asynchronous delays	b) Simulation	c) No delay	d) Supports single driver only		a) Asynchronous delays
What is the use of simulation deltas in VHDL code?	a) To create delays in simulation	b) To assign values to signals	c) To order some events	d) Evaluate assignment statements		c) To order some events
Which function is used to create a single value for multiple driver signals?	a) Resolution function	b) Package	c) Concurrent assignments	d) Sequential assignments		a) Resolution function
The utilization of CAD tools for drawing timing waveform diagram and transforming it into a network	a. Waveform Editor	b. Waveform Estimator	c. Waveform Simulator	d. Waveform Evaluator		a. Waveform Editor

of logic gates is known as _____.					
Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?	a. Simulation	b. Optimization	c. Synthesis	d. Verification	c. Synthesis
_____ is the fundamental architecture block or element of a target PLD.	a. System Partitioning	b. Pre-layout Simulation	c. Logic cell	d. Post-layout Simulation	c. Logic cell
Among the VHDL features, which language statements are executed at the same time in parallel flow?	a. Concurrent	b. Sequential	c. Net-list	d. Test-bench	a. Concurrent
In Net-list language, the net-list is generated _____synthesizing VHDL code.	a. Before	b. At the time of (during)	c. After	d. None of the above	c. After
In VHDL, which object/s is/are used to connect entities together for the model formation?	a. Constant	b. Signal	c. Variable	d. All of the above	b. Signal
Which type of simulation mode is used to check the timing performance of a design?	a. Behavioural	b. Switch-level	c. Transistor-level	d. Gate-level	d. Gate-level
In the simulation process, which	a. Compilation	b. Elaboration	c. Initialization	d. Execution	b. Elaboration

step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?					
Which type of simulator/s neglect/s the intra-cycle state transitions by checking the status of target signals periodically irrespective of any events?	a. Event-driven Simulator	b. Cycle-based Simulator	c. Both a and b	d. None of the above	
Which among the following is not a characteristic of 'Event-driven Simulator'?	a. Identification of timing violations	b. Storage of state values & time information	c. Time delay calculation	d. No event scheduling	d. No event scheduling
Which among the following is an output generated by synthesis process?	a. Attributes & Library	b. RTL VHDL description	c. Circuit constraints	d. Gate-level net list	d. Gate-level net list
Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?	a. Combinational System	b. Sequential system	c. Both a and b	d. None of the above	b. Sequential system

Questions	opt1	opt2	opt3	opt4	opt5	Answer
The serial shift register is driven using	a) one over-lapping clock	b) two over-lapping clock	c) one non over-lapping clock	d) two non over-lapping clock		d) two non over-lapping clock
Which is used to control the scan path movement?	a) clock signals	b) input signals	c) output signals	d) delay signals		a) clock signals
The circuit operation is independent of	a) rise time	b) fall time	c) propogation delays	d) all of the mentioned above		d) all of the mentioned above
Boundary scan test is used to test	a) pins	b) multipliers	c) boards	d) wires		c) boards
The boundary scan path is provided with	a) serial input pads	b) parallel input pads	c) parallel output pads	d) buffer pads		a) serial input pads
The boundary scan path tests the	a) input nodes	b) output nodes	c) buffer nodes	d) interconnection points		d) interconnection points
In scan/set method, _____ is used to implement a scan path	a) serial registers	b) storage elements	c) parallel registers	d) separate register		d) separate register
The automatic test pattern generator method has ____ phases	a) two	b) three	c) four	d) five		a) two
Faults which produce same faulty behaviour are known as	a) similar faults	b) equivalent faults	c) correlative faults	d) ambigious faults		b) equivalent faults
The process of removing equivalent faults is called as	a) equivalent removing	b) bulk damaging	c) fault collapsing	d) fault reduction		c) fault collapsing
The stuck-at model is a _____ fault model	a) recurring	b) equivalent	c) simple	d) logical		d) logical
The _____ between two signal is called as bridging fault	a) open circuit	b) break	c) connection	d) short circuit		d) short circuit
The sum of all propogation delays along a simgle path is given as	a) gate delay fault	b) transition fault	c) path delay fault	d) propogation fault		c) path delay fault
_____ of the area is dedicated for testability	a) 20%	b) 10%	c) 30%	d) 25%		c) 30%
Partitioning into subsystems are done at	a) design stage	b) prototype stage	c) testing stage	d) fabrication stage		b) prototype stage
In prototype testing, the circuits are	a) open circuited	b) short circuited	c) tested as a whole circuit	d) programmed		a) open circuited
What are the dominant faults in diffusion layers?	a) short circuit faults	b) open circuit faults	c) short and open circuit faults	d) power supply faults		a) short circuit faults

Test pattern generation is assisted using	a) automatic test pattern generator	b) exhaustive pattern generator	c) repeated pattern generator	d) loop pattern generator	a) automatic test pattern generator
_____ of faults are easier to detect	a) 50%	b) 60%	c) 70%	d) 80%	d) 80%
Observability is the process of	a) checking all inputs	b) checking all outputs	c) checking all possible inputs	d) checking errors and performance	b) checking all outputs
Exhaustive testing is suitable when N is	a) large	b) small	c) any value for N	d) very large	b) small
To propogate the fault along the selected path to primary output, setting _____ is done	a) OR to 1	b) NOR to 1	c) AND to 1	d) NAND to 0	a) AND to 1
In D-algorithm, a particular _____ fault is detected by examining the _____ conditions	a) internal, output	b) internal, input	c) external, output	d) external, input	a) internal, output
D-algorithm is based on	a) existence of one fault machine	b) existence of one good machine	c) existence of one fault and one good machine	d) existence of two fault machines alone	
In D-algorithm, discrepency is driven to _____ and observed and thus detected	a) all inputs	b) particular inputs	c) output	d) end of the circuit	c) output
Primary objective of testing is to guarantee	(A) Fault-free products	(B) Detection of design error	(C) Reduction of product cost Ans: A	(D) All of these	(A) Fault-free products
Verification targets	(A) Design errors	(B) Manufacturing errors	(C) Both (A) and (B)	(D) None of these	(A) Design errors
Testing targets	(A) Design errors	(B) Manufacturing errors	(C) Both (A) and (B)	(D) None of these	(B) Manufacturing errors
In a certain batch of 10000 chips produced 100 are detected faulty at the manufacturing site while 10 more fails in the field. The yield of the process is	(A) 99%	(B) 98.5%	(C) 90%	(D) None of these	(A) 99%

Applying all possible test patterns to a CUT is called	(A) Exhaustive testing	(B) Complete testing	(C) Functional testing	(D) None of these	(A) Exhaustive testing
A quantity to measure quality of a test set is	(A) Fault coverage	(B) Test coverage	(C) Total coverage	(D) None of these	(A) Fault coverage
PODEM stands for	a) Peak Output Decision Making	b) Path Oriented Decision Making	c) Path Output Decision Making	d) Peak Oriented Decision Making	(b) Path Oriented Decision Making

Questions	opt1	opt2	opt3	opt4	opt5	Answer
In floorplanning, placement and routing are _____ tools.	**a.** Front end	**b.** Back end	**c.** Both a and b	**d.** None of the above		**b.** Back end
In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?	**a.** Floorplanning	**b.** Placement & Routing	**c.** Testing	**d.** Extraction		**d.** Extraction
In floorplanning, which plays a crucial role in minimizing the ASIC area and the interconnection density?	**a.** Placement	**b.** Global Routing	**c.** Detailed Routing	**d.** All of the above		**a.** Placement
Timing analysis is more efficient with synchronous systems whose maximum operating frequency is evaluated by the _____path	**a.** shortest	**b.** average	**c.** longest	**d.** unpredictable		**c.** longest
delay between consecutive flip-flops.						
Maze routing is also known	**a.** Viterbi's algorithm	**b.** Lee/Moore	**c.** Prim's algorithm	**d.** Quine-McCluskey		**b.** Lee/Moore

as _____		algorithm		algorithm	algorithm
Maze routing is used to determine the _____path for a single wire between a set of points, if any path exists.	**a.** Shortest	**b.** Average	**c.** Longest	**d.** None of the above	**a.** Shortes t

	low cost basic logic cell and the interconnect	cost effective interconnection	effective basic cell
	4	5	2
applied time	time power is applied.	power speed	applied power
fuse	none	both a fuse and an antifuse	antifused conductor
semi conductor	a pair of conductors	conductor	and semi conductor
bistable latching circuitry (flip-flop)	flip flop	stable	unstable
NV-SRAM	PS-SRAM	BOTH	none
RAM	SRAM	ROM	EPROM
one transistor	two transistor	three transistor	four transistor
SRAM	EPROM	RAM	ROM
silicon	silicon metal	polysilicon material	monosilicon
flash devices	EEPROM and flash devices.	EPROM	none
1980s	1960s	1970s	1990s
non	none	conventional	all the

conventional gate		gate	above
output pads	I/O pads	all the above	none
the ACT 2 family	the ACT 4 family	the ACT 1 family	none
sequential	enhanced		Combinatorial and Enhanced Sequential
order	sequential	combinatorial	Modules
register or a latch.	register	latch	none
output	input and output	wide-inputcombinatorial logic	all the above
logic module	The Enhanced Sequential Logic Module	sequential logic	all the above
The vertical and horizontal lines run between CLBs.	cross section	vertical lines	horizontal lines
the second IC designer	the third IC designer	the fourth IC designer	the first IC designer
20KA technology	Altera FLEX 10KA technology	none	all the above
100K gates and 24,576 bits	10,000 bits	1240 bits	1856 bits and 200k bits
programmable	reprogrammable flash configuration	flash configuration	none
the two or four clock pins	the one or 2 clock pins	the two or five clock pins	only 6 clock pins
low speed	high-speed LVDS	speed LVDS	high LVDS
serial	parallel	serial-to-parallel and parallel-to-	serial to parallel

		serial	
1.0,2.0	2.0,0.8	5.0,0.1	0.6,4.0
9.0,3.11,5.7	6.45,0.08	3.84 ,–4.0 ,0.33 ,6.0	1.67,2.63
internal	conditionin g external	internal	external
input	inputs	output	output
a set of ASIC tools	a set of EDA tools	none	all the above
systematic entry	none	Schematic entry	all the above
gate-level	sequential level	combinatorial	enhanced sequential level
standards	no standards	sequential standards	all the above
a set of medium	a sequential medium	a powerful medium	none