16BEEC401 LINEAR INTEGRATED CIRCUITS L T P C 3 0 0 3

OBJECTIVES

- To introduce the basic building blocks of linear integrated circuits.
- To teach the linear and non-linear application s of operational amplifiers.
- To introduce the theory and applications of analog multipliers and P LL.
- To introduce the concepts of waveform generation and introduce some special function ICs.
- To teach the theory of ADC and DAC

INTENDED OUTCOMES:

- Knowledge about the basic building blocks of linear integrated circuits.
- Knowledge about the linear and non-linear applications of operational amplifiers.
- Knowledge about the theory and applications of analog multipliers and P LL.
- Knowledge about the theory of ADC and DAC
- Knowledge about a few special function integrated circuits

UNIT I-OPERATIONAL AM PLIFIER CHARACTERISTIC

Op-amp symbol, terminals, packages and specifications - Block diagram Representation of op-amp- Ideal op-amp & practical op-amp - Open loop & closed loop configurations – DC & AC performance characteristics of op-amp – Frequency compensation - Noise – Differential amplifiers -Electrical Characteristics and internal schematic of 741 op - amps.

UNIT II-OP–AMP APPLICATIONS

Basic op-amp circuits: Inverting & Non-inverting voltage amplifiers -Voltage follower -Summing, scaling & averaging amplifiers - AC amplifiers.Linear Applications: Instrumentation Amplifiers-V-to-I and I-to-V converters-Differentiators and Integrators.

Non-linear Applications: Precision Rectifiers – Wave Shaping Circuits (Clipper and Clampers) – Log and Antilog Amplifiers – Analog voltage multiplier circuit and its applications - Comparators and its applications.

UNIT III- WAVEFORM GENERATORS AND PLL

Waveform Generators: Sine-wave Generators – Square / Triangle / Sawtooth Wave generators. IC 555 Timer: Monostable operation and its applications, Astable operation and its applications

P LL: Operation of the Basic P LL-Closed loop analysis of P LL-Voltage Controlled Oscillator-P LL

Applications

UNIT IV-ACTIVE FILTERS & VOLTAGE REGULATOR

Filters: Comparison betweenPassive and Active Networks-Active Network Design – Filter

Approximations-Design of LPF, HPF, BPF and Band Reject Filters – State Variable Filters

Voltage Regulators: Basics of Voltage Regulator – Linear Voltage Regulators using Op-amp – IC Regulators (78x x, 79xx, LM 317, 723)-Switching Regulators.

UNIT V-DATA CONVERSION DEVICES

Digital to Analog Conversion: DAC Specifications – DAC circuits – Weighted Resistor DAC-R-2R Ladder DAC-Inverted R-2R Ladder DAC Monolithic DAC

Analog to Digital conversion:ADC specifications-ADC circuits-Ramp Type ADC-Successive

Approximation ADC-Dual Slope ADC-Flash Type ADC.

TEXT BOOKS:

S.NO.	Author(s) Name	Title of the book	Publisher	Year of publication
1	Roy Choudhur y and Shail Jain	Linear Integrated Circuits	New Age International Publishers	2003
2	Ramakant A.Ga yakwad	Op-Amps and Linear Integrated Circuits	Prentice Hall of India, New Delhi	2000

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2	Sergio Franco	Design with operational amplifier and analog integrated circuits	McGraw Hill	2015

KARPAGAM ACADEMY OF HIGHER EDUCATION
(Deemed to be University Established Under Section 3 of UGC Act 1956)
Pollachi Main Road, Eachanari Post,
Coimbatore – 641 021
FACULTY OF ENGINEERING
Linear integrated circuits - LECTURE PLAN

S.No	TOPICS TO BE COVERED	TIME DURATION	SUPPORTING MATERIALS	TEACHING AIDS
	UNIT I OPERATIONAL AMPLIFIER CHARACTERISTICS			
1	Introduction to fabrication of IC and Various linear IC Components and their applications	0	R3- Page.no 2-12	BB
2	Op-amp symbol, terminals packages and specifications– General Description,	01	R3- Page.no 2-12 R1 Page.no 23-42	BB
3	Block diagram Representation of op-amp	01	R2 Page.no 71-81	BB
4	Ideal op-amp & practical op-amp - Open loop & closed loop configurations	01	R3- Page.no.56	BB
5	DC performance characteristics of op-amp	01	T1 Page.no 104-110	BB
6	AC performance characteristics of op-amp	01	T1 page.no 111-126	BB
7	Frequency compensation	01	T1 Page.no 119-123	BB
8	Noise – Differential amplifiers	01	T1 page.no 53-55	BB
9	Manufacturer's Specification, Electrical Characteristics and internal schematic of 741 op-amps.	01	T1 page.no127-128	BB
Introduction		**02**		
Total Lecture Hours		**08**		
Total Hours		**10**		

	UNIT II OP–AMP APPLICATIONS			
10	Basic op-amp circuits: Inverting & Non-inverting voltage amplifiers	01	T1 Page.no43-48	BB
11	Voltage follower - Summing, scaling amplifiers	01	T1 Page.no 49	BB
12	Averaging amplifiers - AC amplifiers.	01	T1 Page.no 139-144	BB
13	Linear Applications: Instrumentation Amplifiers	01	T1 Page.no 141-144	BB
14	V-to-I and I-to-V converters-Differentiators and Integrators.	01	T1 Page.no 146-147	BB
15	Non-linear Applications: Precision Rectifiers – Wave Shaping Circuits (Clipper and Clampers)	01	T1 Page.no 164-171	BB
16	Log and Antilog Amplifiers –	01	T1 Page.no 148-153	BB

17	Analog voltage multiplier circuit and its applications Operational Trans- Conductance Amplifier (OTA)	01	T1 Page.no 155-156	BB
18	Comparators and its applications – Sample and Hold circuit	01	T1 Page.no 159-160	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT III WAVEFORM GENERATORS AND PLL				
19	Waveform Generators: Sine-wave Generators	01	T1 Page.no 222-224	BB
20	Waveform Generators: – Square Wave generators.	01	T1 Page.no 216-218	BB
21	Waveform Generators: Triangle and Sawtooth Wave generators.	01	T1 Page.no 220-222	BB
22	IC 555 Timer: Monostable operation and its applications,	01	T1 Page.no 311-312	BB
23	IC 555 Timer: Astable operation and its applications	01	T1 Page.no 318-324	BB
24	PLL: Operation of the Basic PLL	01	T1 Page.no327-329	BB
25	Closed loop analysis of PLL	01	T1 Page.no 311-324	BB
26	Voltage Controlled Oscillator	01	T1 Page.no 334	BB
27	PLL Applications	01	T1 Page.no 342-345	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT IV ACTIVE FILTERS & VOLTAGE REGULATOR				
28	Filters: Comparison between Passive and Active Networks	01	T1 Page.no 262-263	BB
29	Active Network Design	01	T1 Page.no 262-264	BB
30	Filter. Approximations	01	T1 Page.no 264-265	BB
31	Design of LPF, HPF Filters	01	T1 Page.no 264-272	BB
32	Design of BPF and Band Reject Filters	01	T1 Page.no 272-277	BB
33	State Variable Filters – All Pass Filters – Switched Capacitor Filters	01	T1 Page.no 283-284	BB
34	Voltage Regulators: Basics of Voltage Regulator	01	T1 Page.no 240-241	BB
35	Linear Voltage Regulators using Op-amp – IC Regulators (78x x, 79xx, LM 317, LM 337,723	01	T1 Page.no 241-245	BB
36	Switching Regulators.	01	T1 Page.no 255-288	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

UNIT V DATA CONVERSION DEVICES				
37	Digital to Analog Conversion: DAC Specifications	01	T1 Page.no 349-350	BB

38	DAC circuits - Weighted Resistor DAC- R-2R Ladder DAC	01	T1 Page.no 349-353	BB
39	Inverted R-2R Ladder DAC Monolithic DAC	01	T1 Page.no 353-3555	BB
40	Analog to Digital Conversion: ADC specifications	01	T1 Page.no 357-366	BB
41	ADC circuits-Ramp Type ADC	01	T1 Page.no356-357	BB
42	Dual Slope ADC	01	T1 Page.no 363-364	BB
43	Flash Type ADC	01	T1 Page.no 358 35859	BB
44	Successive Approximation ADC	01	T1 Page.no 361-362	BB
45	Monolithic ADC	01	T1 Page.no 367	BB
Total Lecture Hours		**09**		
Total Hours		**09**		

Total No of Hours for Introduction: 02 Hrs

Total No of Lecture Hours Planned: 44 Hrs

Total No of Hours Planned : 46 Hours

TEXT BOOKS:

S.NO	Author(s) Name	Title of the book	Publisher	Year of publication
1	Roy Choudhury and Shail Jain	Linear Integrated Circuits	New Age International Publishers	2003
2	Ramakant A.Gayakwad	Op-Amps and Linear Integrated Circuits	Prentice Hall of India, New Delhi	2000

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2	Sergio Franco	Design with operational amplifier and analog integrated circuits	McGraw Hill	2015

Staff In-Charge **HOD/ECE**

17BEBME402 – LINEAR INTEGRATED CIRCUITS

Name : Mrs.P.SASIKALA

Designation: Assistant Professor

Department: Electronics and Communication Engineering

College: Karpagam Academy of Higher Education

UNIT-I

OPERATIONAL AMPLIFIER CHARACTERISTICS

- Op-amp symbol, terminals, packages & specifications –
- Block diagram Representation of op-amp-
- Ideal op-amp & practical op-amp –
- Open loop & closed loop configurations –
- DC & AC performance characteristics of op-amp
- Frequency compensation
- Noise
- Differential amplifiers – General Description, Manufacturer's Specification, Electrical Characteristics and internal schematic of 741 op - amps.

INTEGRATED CIRCUITS

An integrated circuit (IC) is a miniature ,low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

ADVANTAGES OF INTEGRATED CIRCUITS

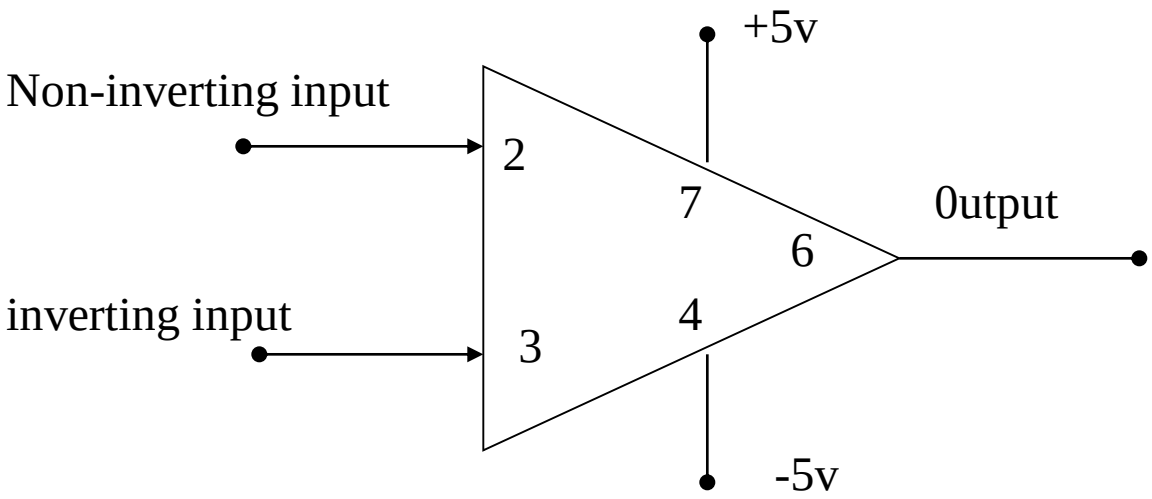
1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

OPERATION AMPLIFIER

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.

It is a versatile device that can be used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

OP-AMP SYMBOL



IDEAL CHARACTERISTICS OF OPAMP

1. Open loop gain infinite
2. Input impedance infinite
3. Output impedance zero
4. Bandwidth infinite
5. Zero offset, ie, Vo=0 when V1=V2=0
6. Infinite CMRR
7. Infinite Slew Rate

DC CHARACTERISTICS

Input offset current

The difference between the bias currents at the input terminals of the op- amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents

DC CHARACTERISTICS

Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

DC CHARACTERISTICS

Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage

DC CHARACTERISTICS

Input bias current

Input bias current IB as the average value of the base currents entering into terminal of an op-amp

$$I_B = \frac{I_B^+ + I_B^-}{2}$$

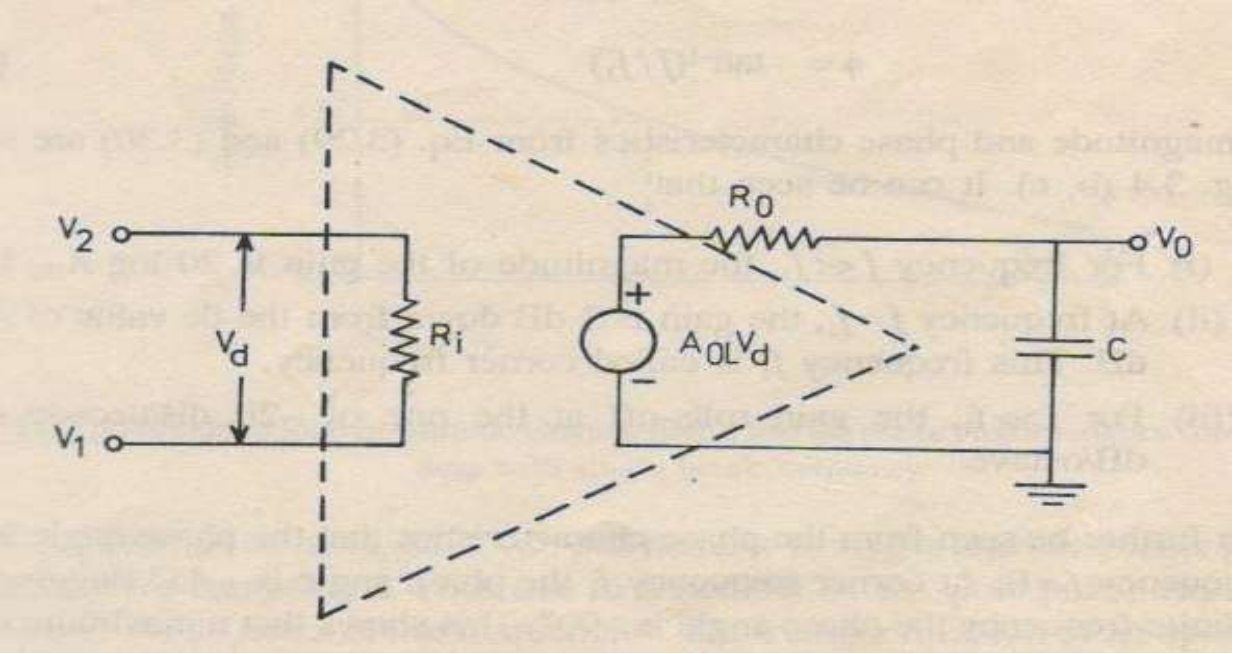
DC CHARACTERISTICS

THERMAL DRIFT

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25^{o}c may not remain so when the temperature rises to 35^{o}c. This is called drift.

AC CHARACTERISTICS

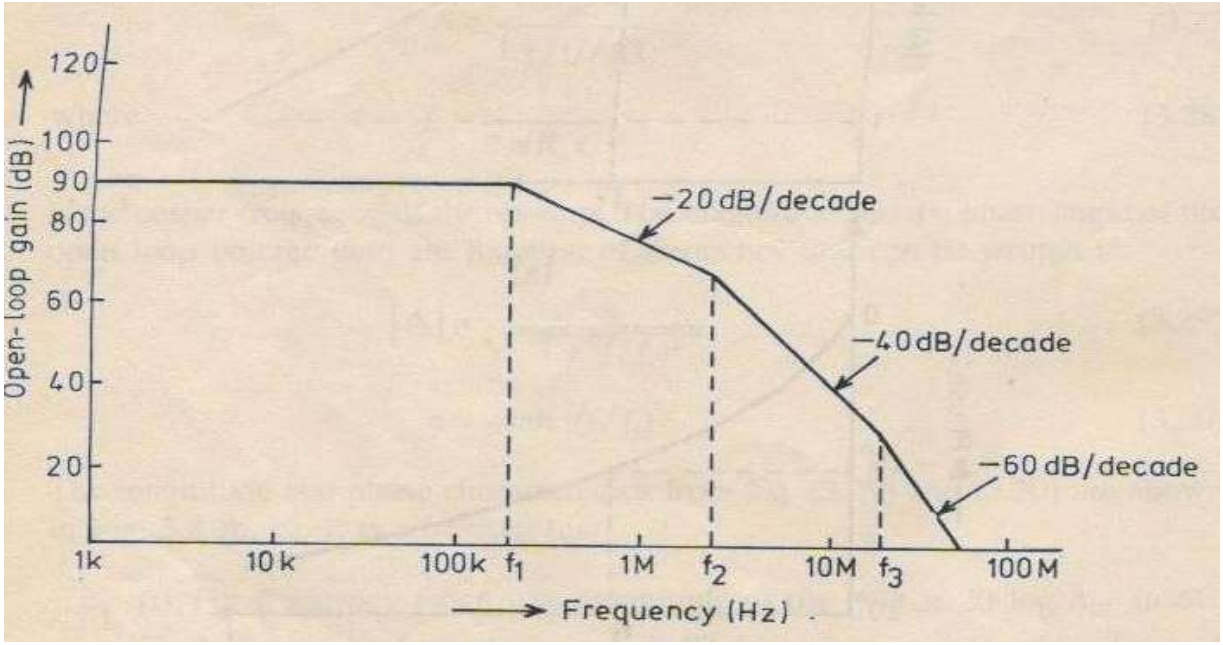
Frequency Response



HIGH FREQUENCY MODEL OF OPAMP

AC CHARACTERISTICS

Frequency Response



OPEN LOOP GAIN VS FREQUENCY

NEED FOR FREQUENCY COMPENSATION IN PRACTICAL OP-AMPS

- Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.
- Compensating networks are used to control the phase shift and hence to improve the stability

FREQUENCY COMPENSATION METHODS

- Dominant- pole compensation
- Pole- zero compensation

SLEW RATE

- The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage.

- An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage

IC PACKAGES AVAILABLE

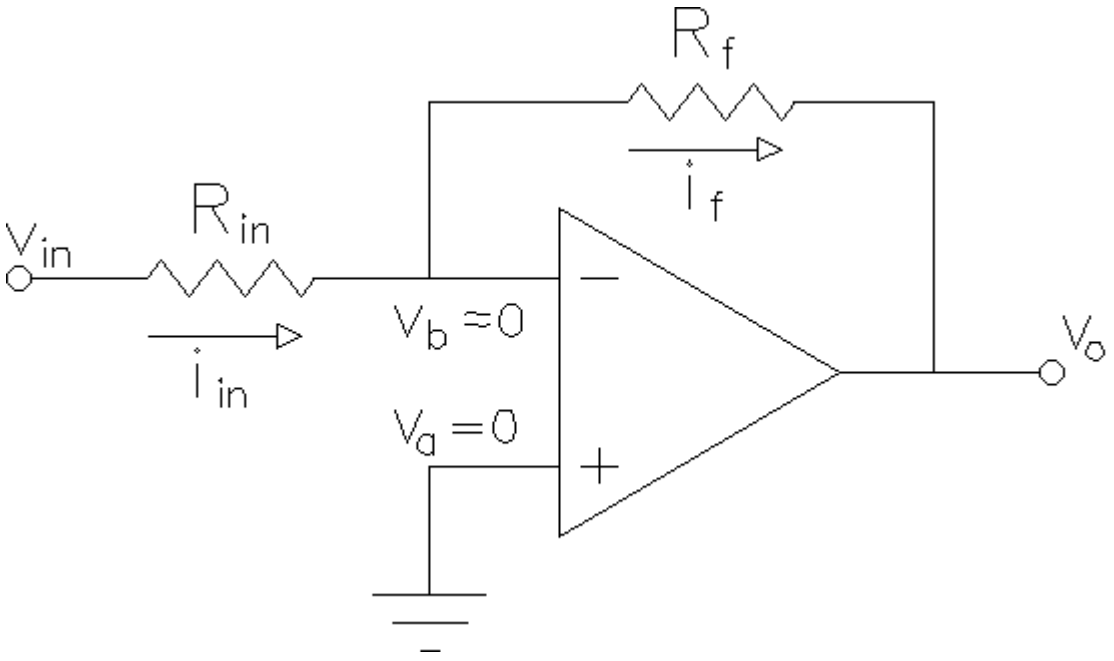
1. Metal can package.
2. Dual-in-line package.
3. Ceramic flat package.

UNIT-II

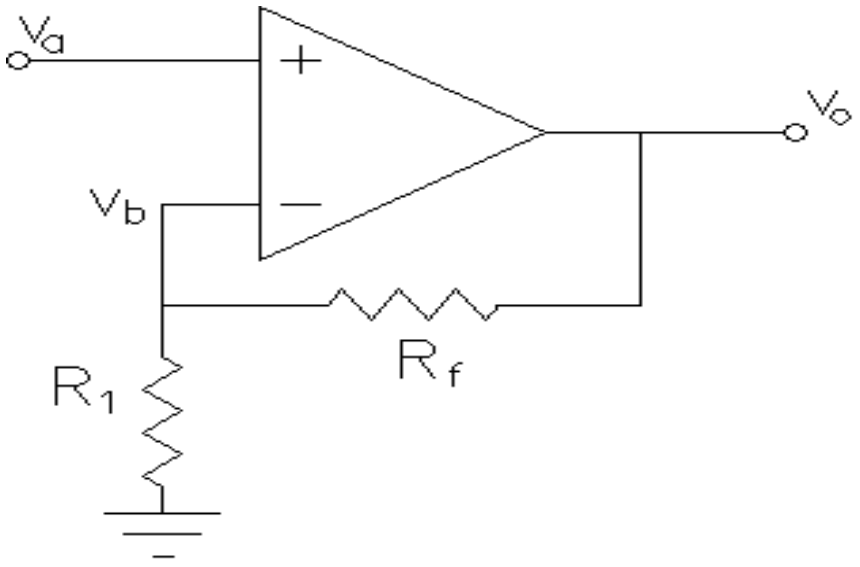
Op-Amp Applications

- Inverting & Non-inverting voltage amplifiers - Voltage follower - Summing, scaling & averaging amplifiers - AC amplifiers.
- Linear Applications: Instrumentation Amplifiers-V-to-I and I-to-V converters- Differentiators and Integrators.
- Non-linear Applications: Precision Rectifiers – Wave Shaping Circuits (Clipper and Clampers) – Log and Antilog Amplifiers – Analog voltage multiplier circuit and its applications – Operational Trans- Conductance Amplifier (OTA) - Comparators and its applications – Sample and Hold circuit.

INVERTING OP-AMP

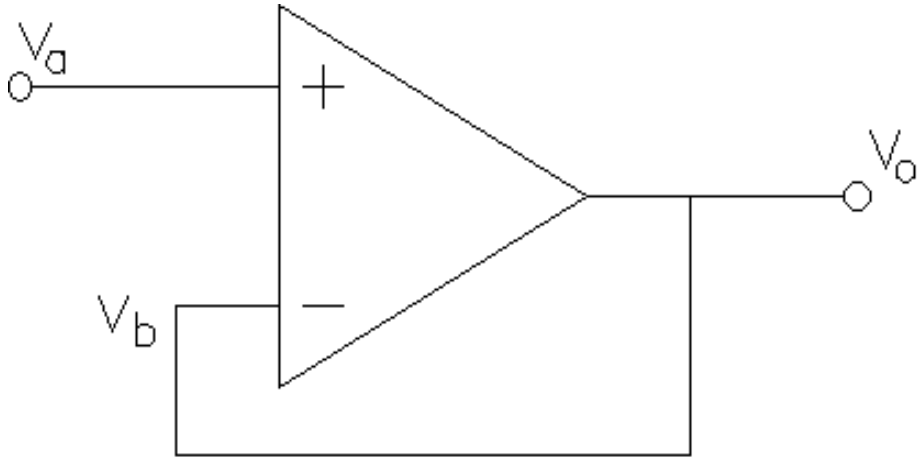


NON-INVERTING AMPLIFIER



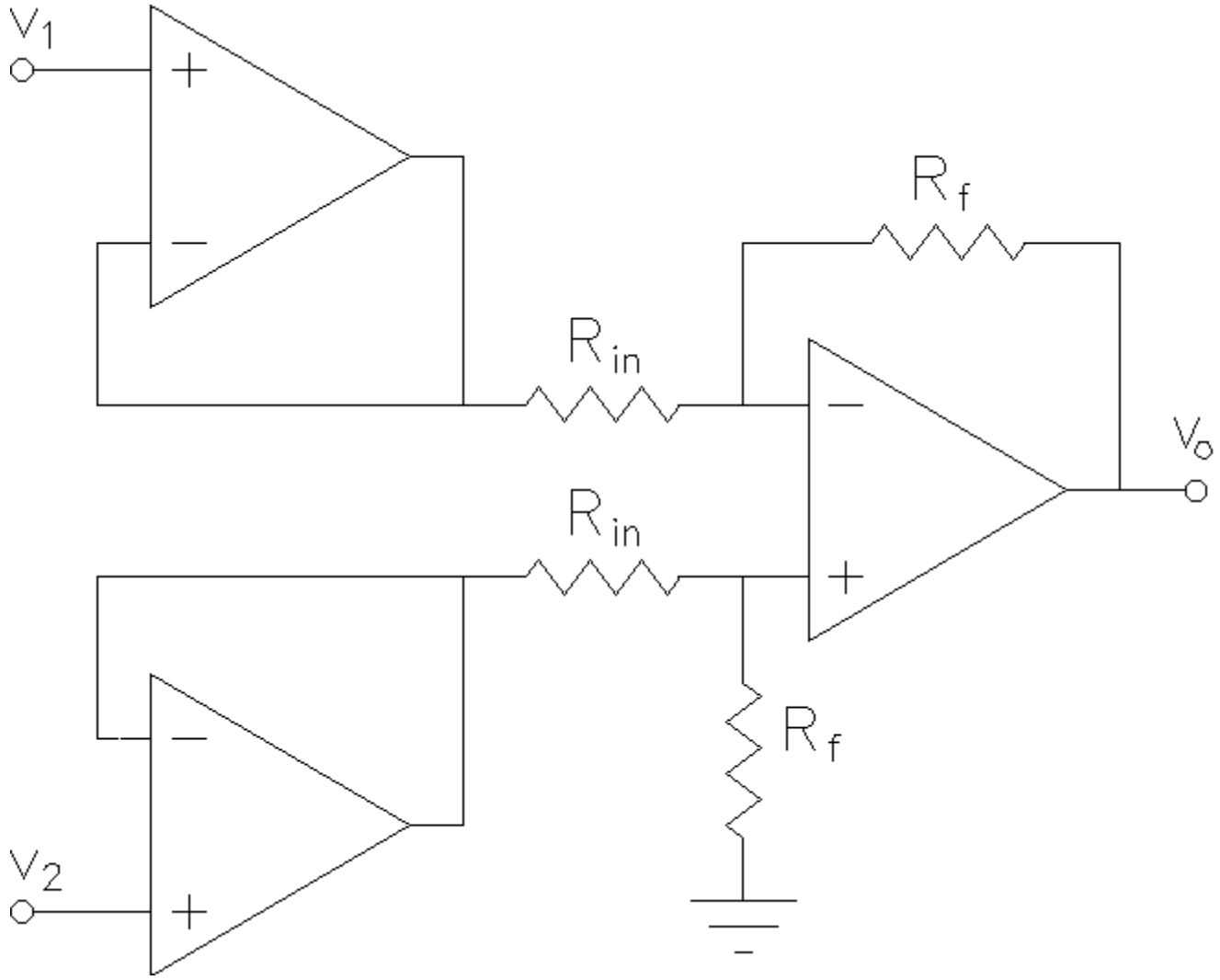
$$V_{out} = (1 + R_f / R_1) V_{in}$$

VOLTAGE FOLLOWER



$$V_{OUT} = V_{IN}$$

INSTRUMENTATION AMPLIFIER



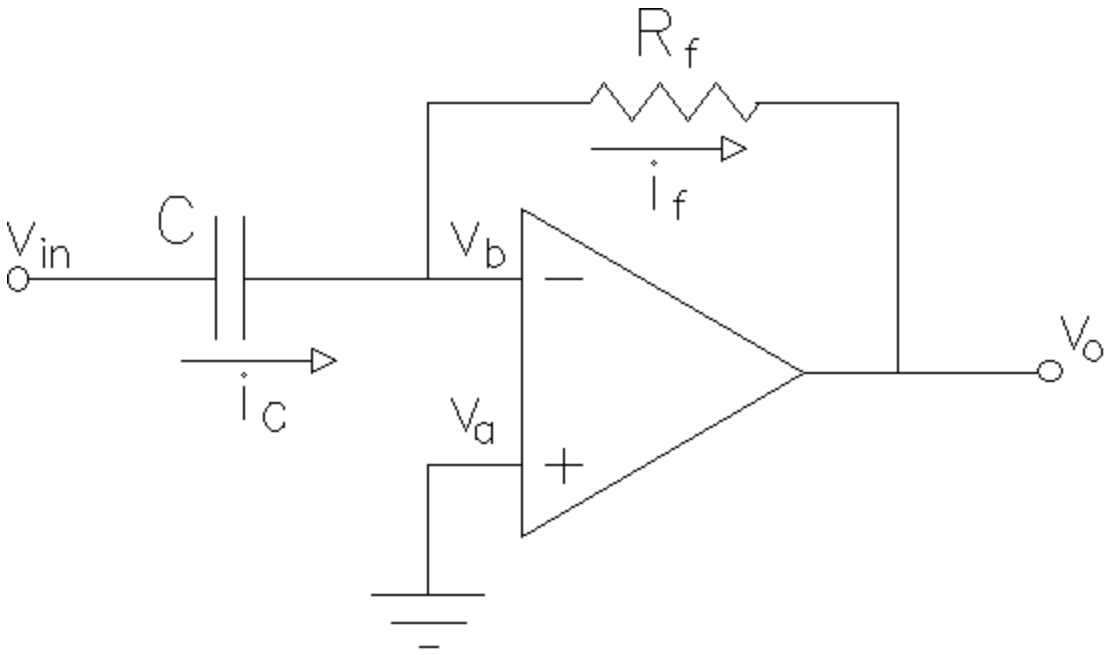
INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier

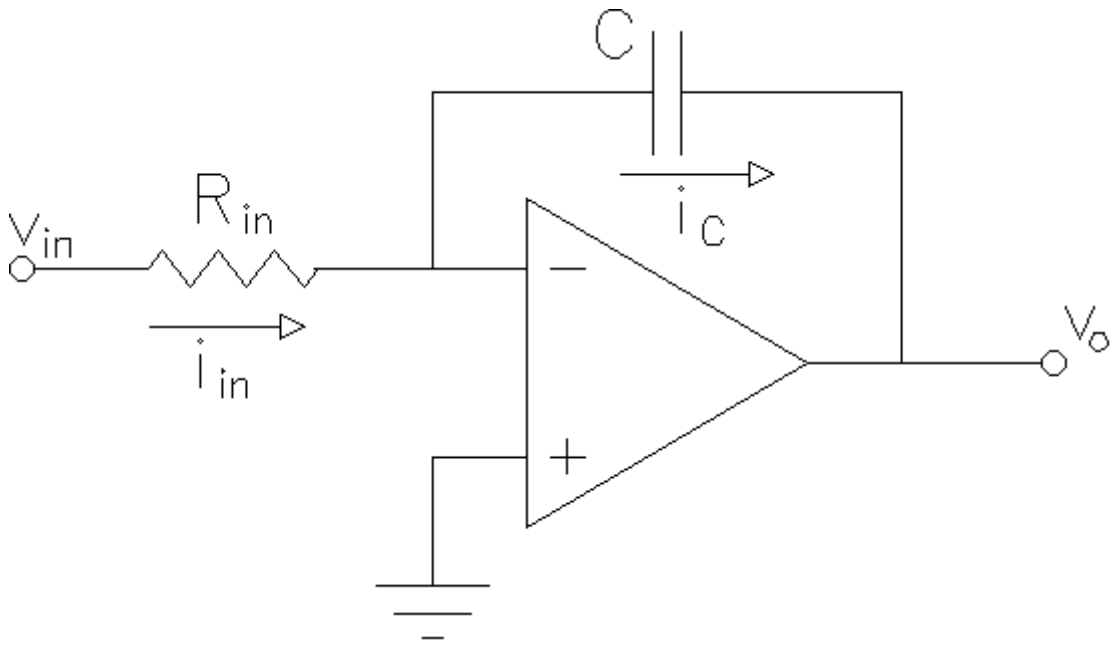
FEATURES OF INSTRUMENTATION AMPLIFIER

1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

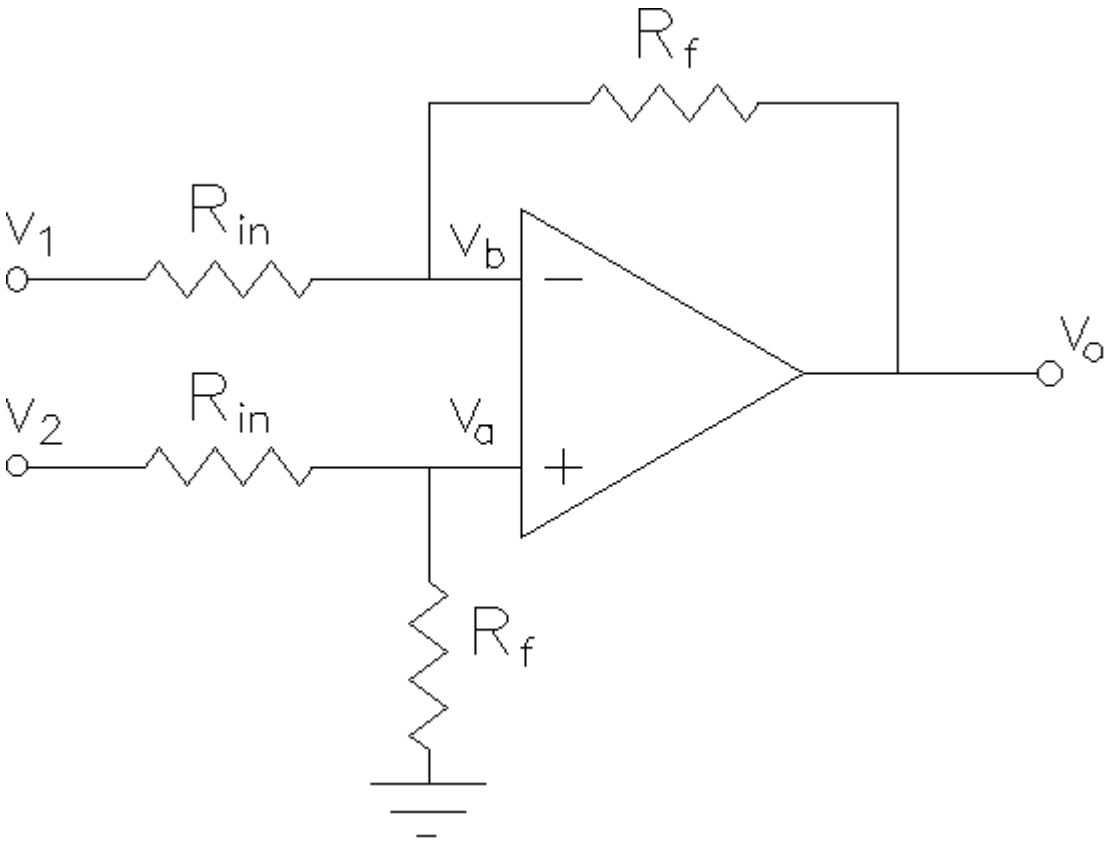
DIFFERENTIATOR



INTEGRATOR



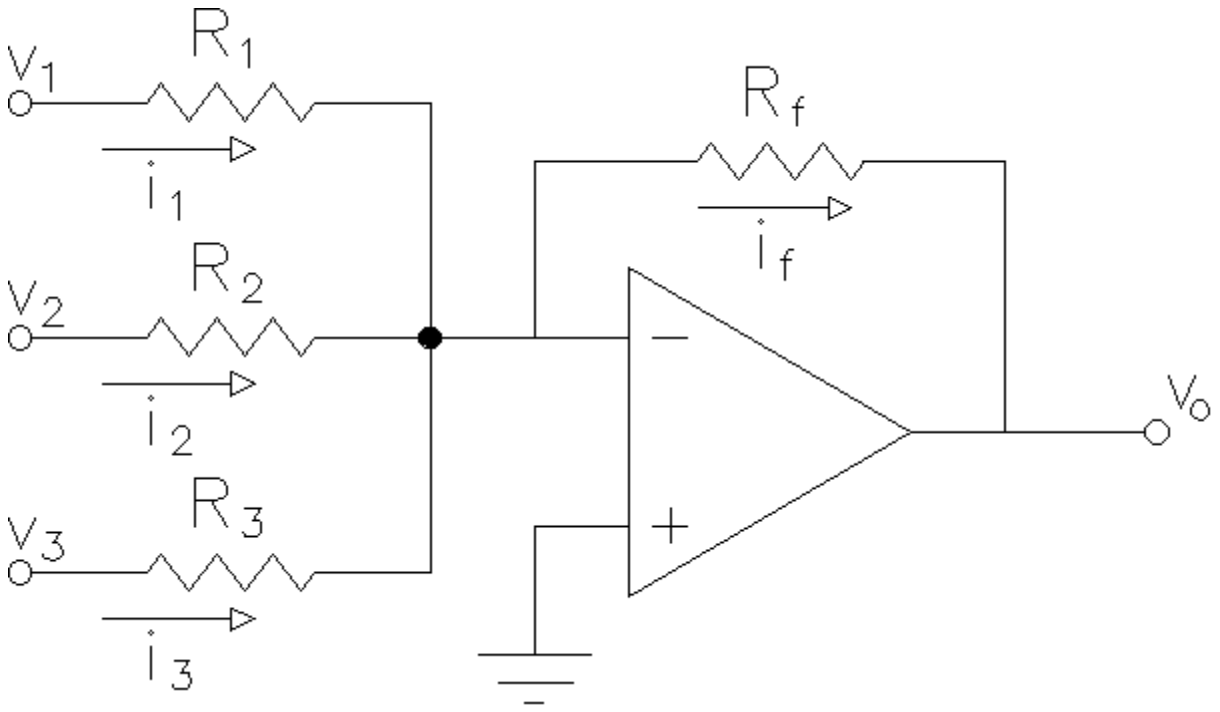
DIFFERENTIAL AMPLIFIER



DIFFERENTIAL AMPLIFIER

This circuit amplifies only the difference between the two inputs. In this circuit there are two resistors labeled R_{IN} Which means that their values are equal. The differential amplifier amplifies the difference of two inputs while the differentiator amplifies the slope of an input

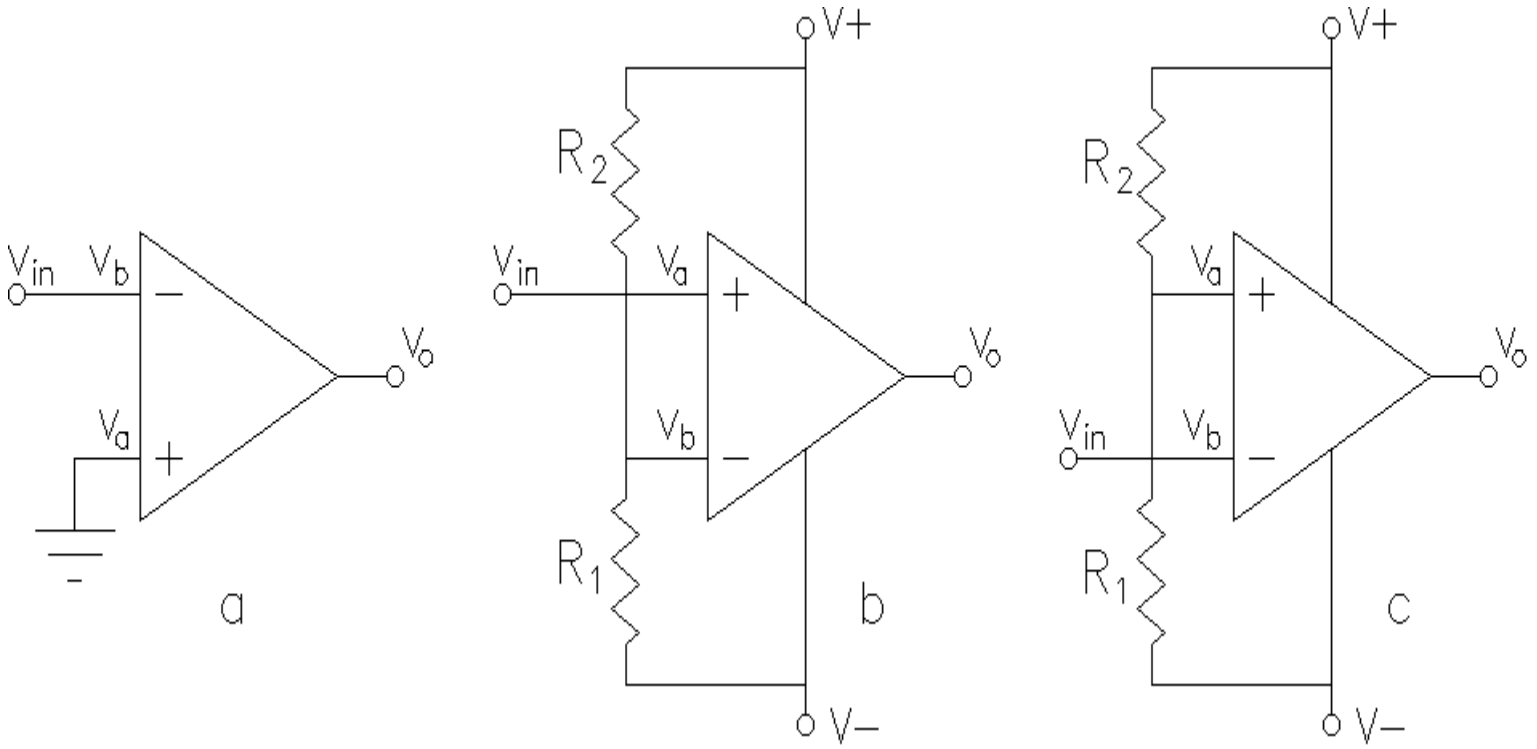
SUMMER



COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output + Vsat

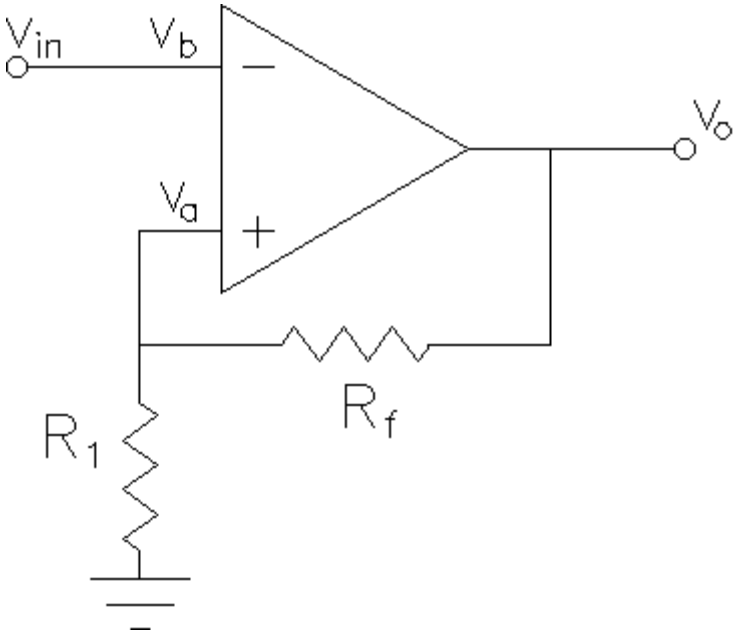
COMPARATOR



APPLICATIONS OF COMPARATOR

1. Zero crossing detector
2. Window detector
3. Time marker generator
4. Phase detector

SCHMITT TRIGGER



SCHMITT TRIGGER

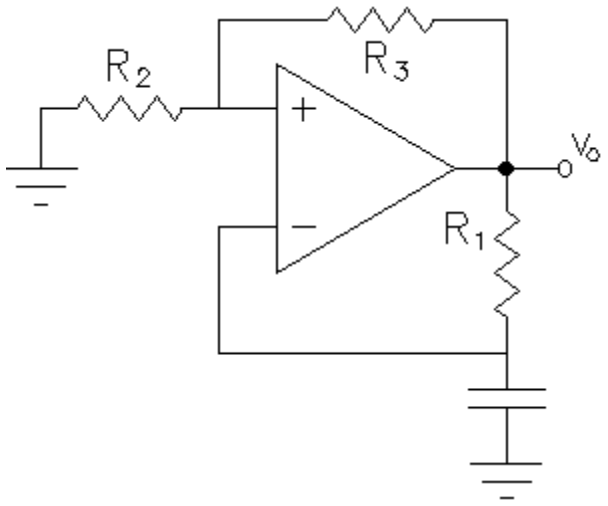
Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform

UNIT-III

Waveform Generators and PLL

- Sine-wave Generators –
- Square / Trian gle / Sawtooth Wave generators. IC 555 Timer: Monostable operation and its applications, Astable operation and its applications
- P LL: Operation of the Basic P LL-Closed loop analysis of P LL-Voltage Controlled Oscillator-
- P LL applications.

SQUARE WAVE GENERATOR



MULTIVIBRATOR

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi-stable depending on the type of multivibrator

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi- stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state

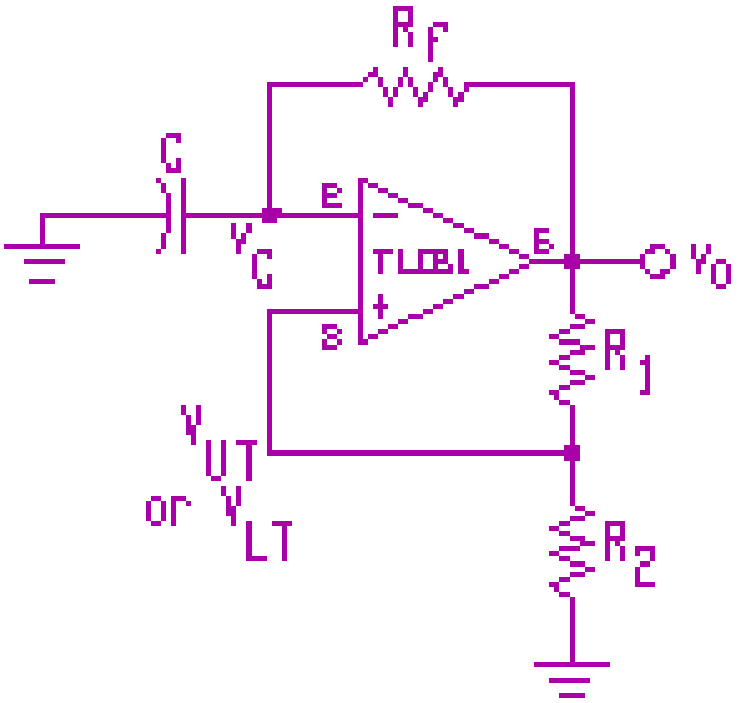
ASTABLE MULTIVIBRATOR

Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state

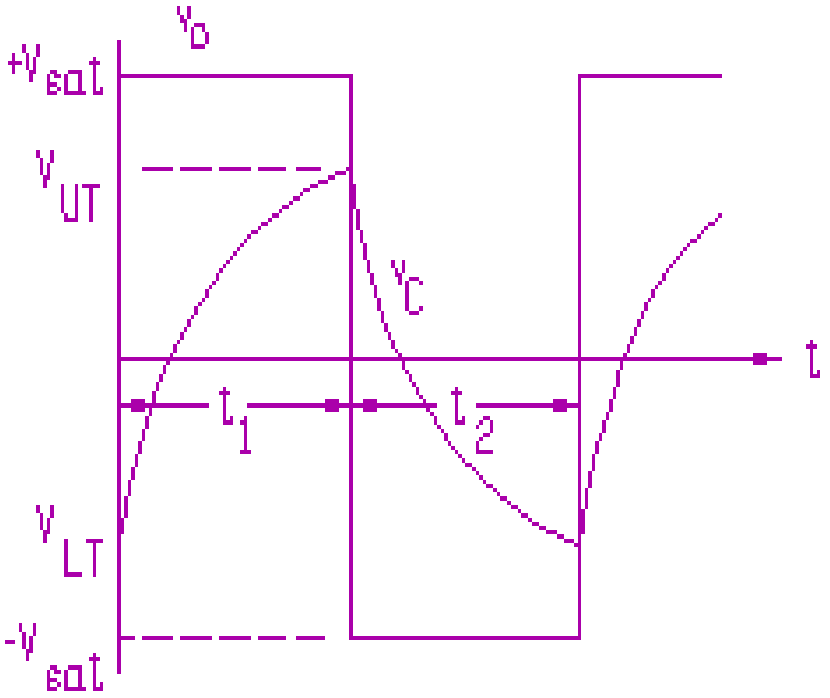
BISTABLE MULTIVIBRATOR

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied . Thus, it requires two external triggers before it returns to its initial state

ASTABLE MULTIVIBRATOR OR RELAXATION OSCILLATOR



Circuit



Output waveform

EQUATIONS FOR ASTABLE MULTIVIBRATOR

$$V_{UT} = \frac{+V_{sat}R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat}R_2}{R_1 + R_2}$$

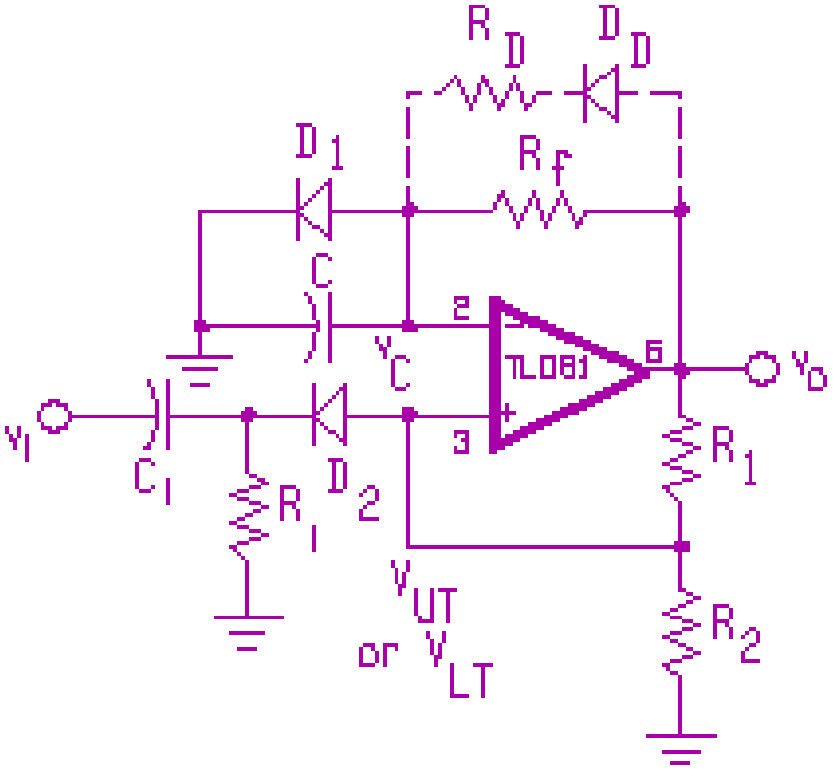
Assuming $|+V_{sat}| = |-V_{sat}|$

$$T = t_1 + t_2 = 2\tau \ln\left(\frac{R_1 + 2R_2}{R_1}\right)$$

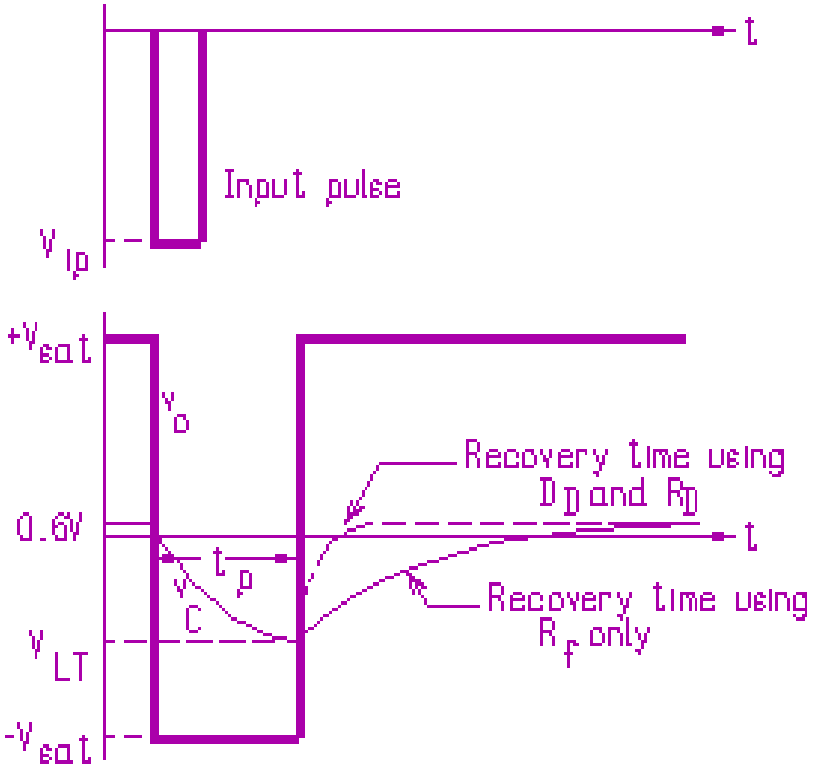
If R_2 is chosen to be $0.86R_1$, then $T = 2R_fC$ and

$$f = \frac{1}{2R_fC}$$

MONOSTABLE (ONE-SHOT) MULTIVIBRATOR



Circuit



Waveforms

NOTES ON MONOSTABLE MULTIVIBRATOR

- Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V
- Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select $R_iC_i \leq 0.1R_fC$.
- Timing state: C charges n
  0.6 V through R_f. Width c
  is:

$$t_p = R_f C \ln\left(\frac{|V_{sat}| + 0.6}{|V_{sat}| + V_{LT}}\right)$$

  - If we pick $R_2 = R_1/5$, then $t_p = R_fC/5$.
  - Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. The *recovery time* $\geq t_p$. To speed up the recovery time, R_D (= $0.1R_f$) & C_D can be added.

UNIT-IV

Active filters & Voltage regulators

- Filters: Comparison between Passive and Active Networks-
- Active Network Design – Filter. Approximations-
- Design of LPF, HPF, BPF and Band Reject Filters – State Variable Filters – All Pass Filters –
- Switched Capacitor Filters.
- Voltage Regulators: Basics of Voltage Regulator – Linear Voltage Regulators using Op-amp – IC Regulators (78x x, 79xx, LM 317, LM 337,723)- Switching Regulators.

FILTER

Filter is a frequency selective circuit that passes signal of specified Band of frequencies and attenuates the signals of frequencies outside the band

Type of Filter

1. Passive filters
2. Active filters

PASSIVE FILTERS

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation

ACTIVE FILTERS

Active filters used op- amp as the active element and resistors and capacitors as passive elements. By enclosing a capacitor in the feed back loop , inductor less active filters can be obtained

SOME COMMONLY USED ACTIVE FILTERS

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter

ACTIVE FILTERS

- Active filters use op-amp(s) and RC components.
- Advantages over passive filters:
  - op-amp(s) provide gain and overcome circuit losses
  - increase input impedance to minimize circuit loading
  - higher output power
  - sharp cutoff characteristics can be produced simply and efficiently without bulky inductors
- Single-chip universal filters (e.g. switched-capacitor ones) are available that can be configured for any type of filter or response.

REVIEW OF FILTER TYPES & RESPONSES

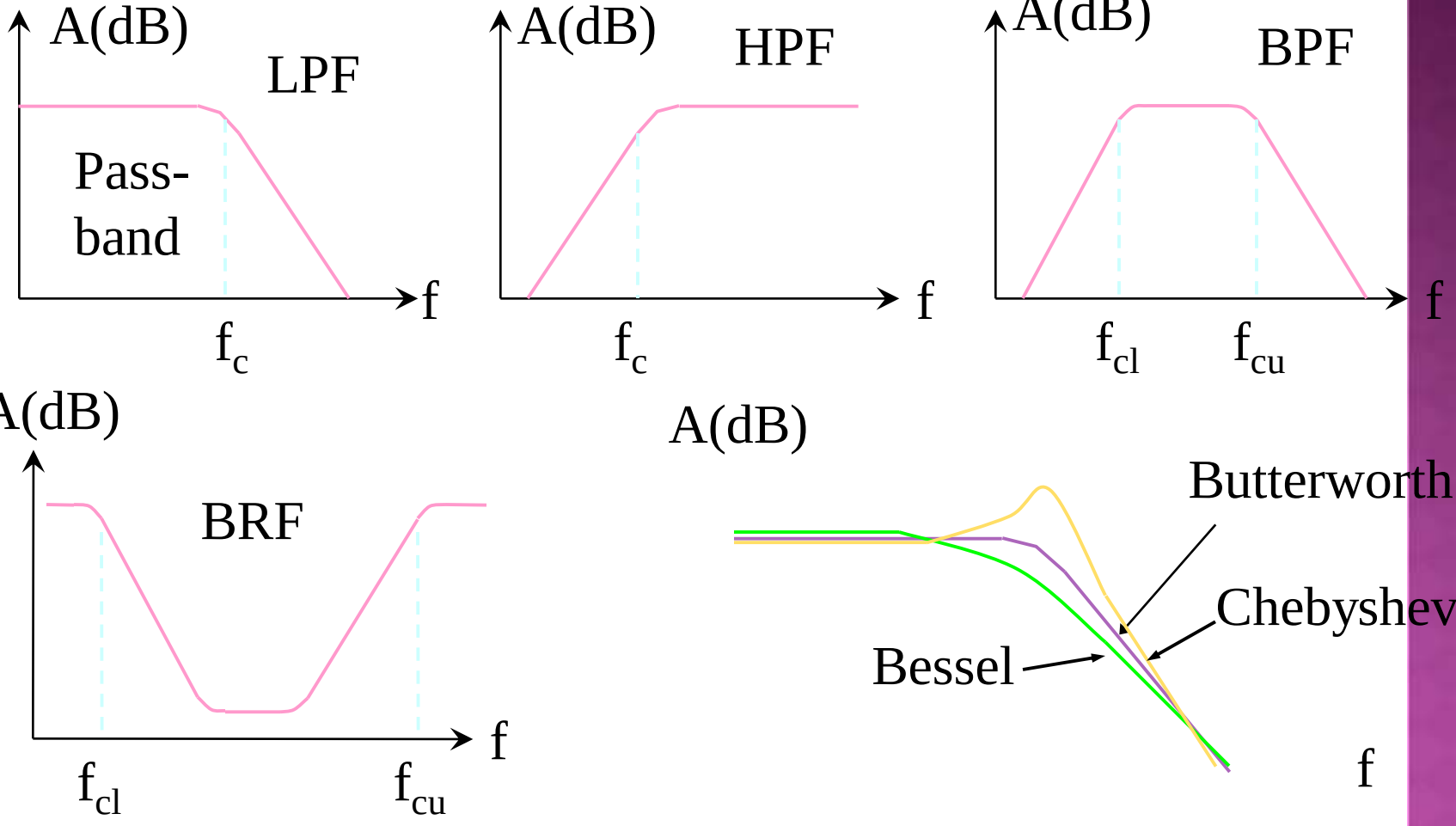
- 4 major types of filters: low-pass, high-pass, band pass, and band-reject or band-stop
- 0 dB attenuation in the passband (usually)
- 3 dB attenuation at the *critical* or *cutoff frequency*, f_c (for Butterworth filter)
- Roll-off at 20 dB/dec (or 6 dB/oct) per *pole* outside the passband (# of poles = # of reactive elements). Attenuation at any frequency, f, is:

$$atten.(dB)\,at\ f = \log\left(\frac{f}{f_c}\right) x\, atten.(dB)\,at\ f_{dec}$$

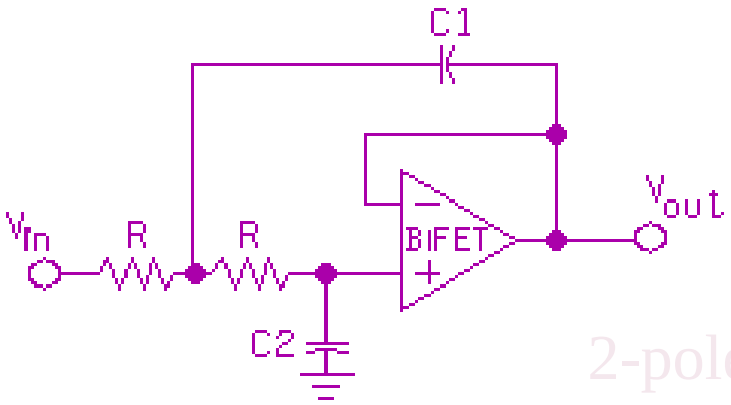
REVIEW OF FILTERS (CONT'D)

- Bandwidth of a filter: BW = f_{cu} - f_{cl}
- Phase shift: 45^o/pole at f_c; 90^o/pole at >> f_c
- 4 types of filter responses are commonly used:
  - Butterworth - maximally flat in passband; highly non-linear phase response with frequecny
  - Bessel - gentle roll-off; linear phase shift with freq.
  - Chebyshev - steep initial roll-off with ripples in passband
  - Cauer (or elliptic) - steepest roll-off of the four types but has ripples in the passband and in the stopband

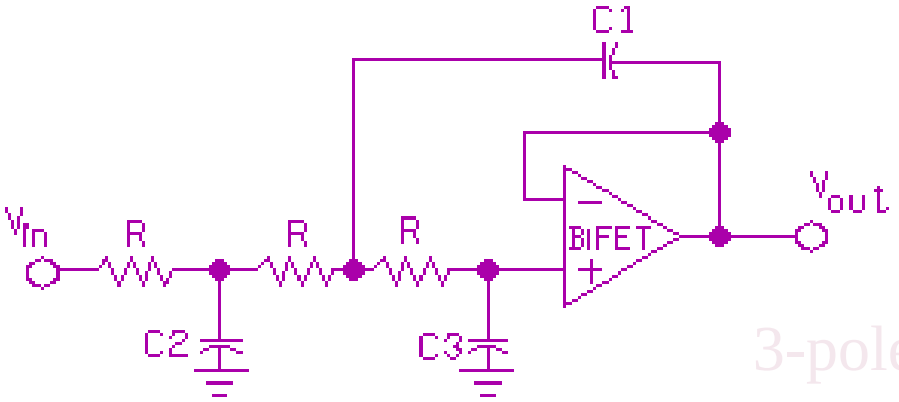
FREQUENCY RESPONSE OF FILTERS



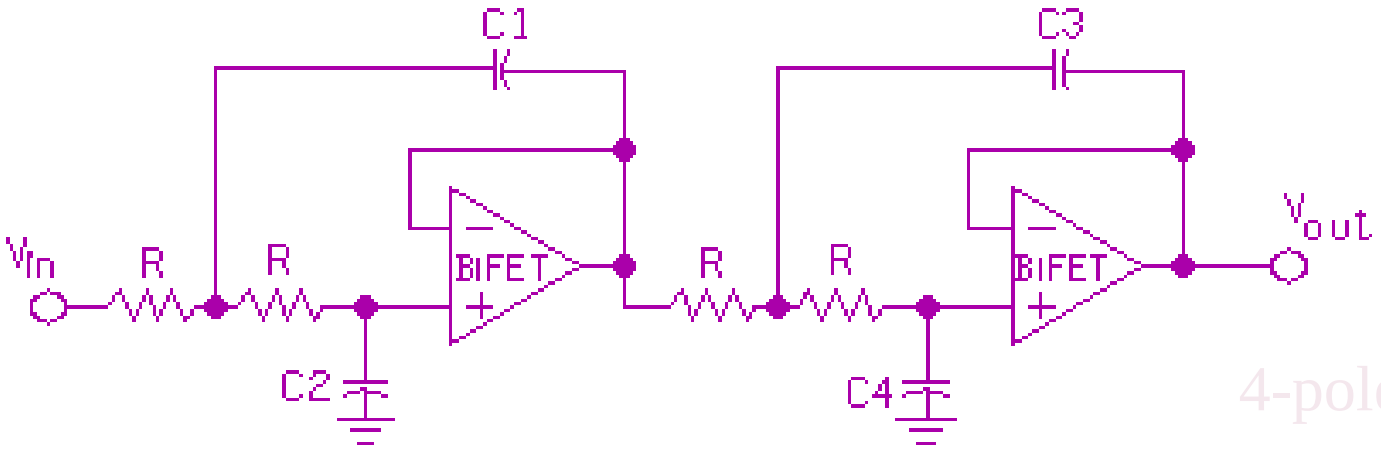
UNITY-GAIN LOW-PASS FILTER CIRCUITS



2-pole



3-pole



4-pole

DESIGN PROCEDURE FOR UNITY-GAIN LPF

- Determine/select number of poles required.
- Calculate the frequency scaling constant, $K_f = 2\pi f$
- Divide normalized C values (from table) by K_f to obtain frequency-scaled C values.
- Select a desired value for one of the frequency-scaled C values and calculate the impedance scaling factor

$$K_x = \frac{frequency - scaled\ C\ value}{desired\ C\ value}$$

  - Divide all frequency-scaled C values by K_x
  - Set $R = K_x\ \Omega$

AN EXAMPLE

Design a unity-gain LP Butterworth filter with a critical frequency of 5 kHz and an attenuation of at least 38 dB at 15 kHz.

The attenuation at 15 kHz is 38 dB

⑧ the attenuation at 1 decade (50 kHz) = 79.64 dB.

We require a filter with a roll-off of at least 4 poles.

K_f = 31,416 rad/s. Let's pick C_1 = 0.01 μF (or 10 nF). Then

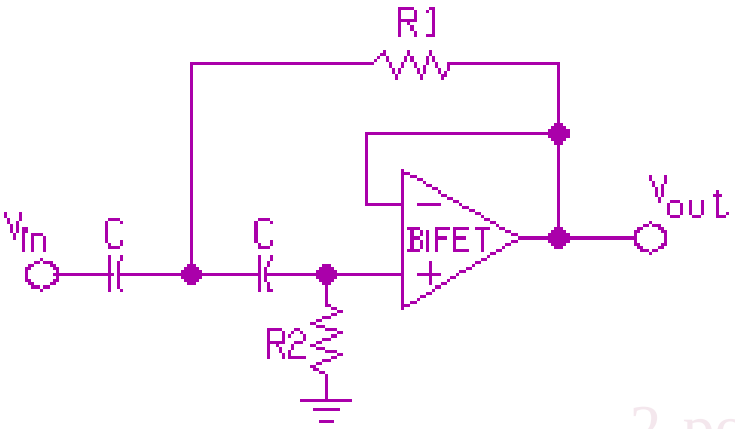
C_2 = 8.54 nF, C_3 = 24.15 nF, and C_4 = 3.53 nF.

Pick standard values of 8.2 nF, 22 nF, and 3.3 nF.

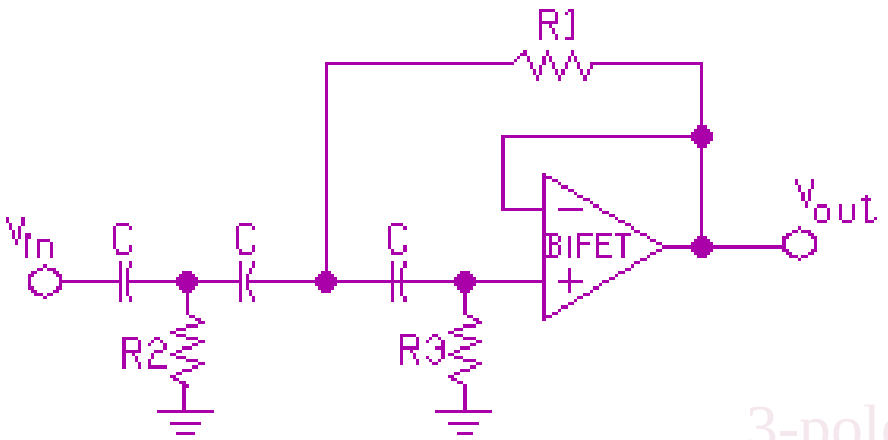
K_x = 3,444

Make all R = 3.6 kΩ (standard value)

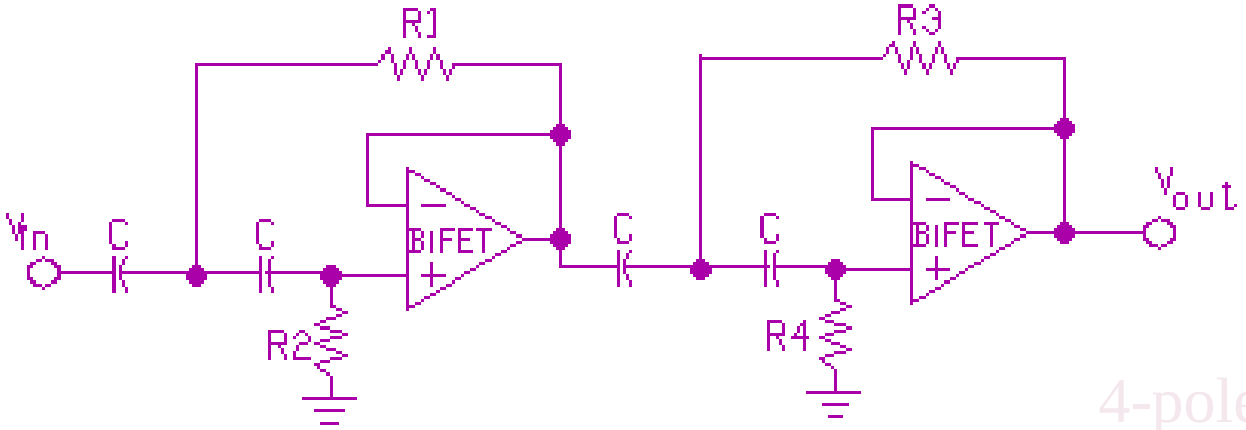
UNITY-GAIN HIGH-PASS FILTER CIRCUITS



2-pole



3-pole



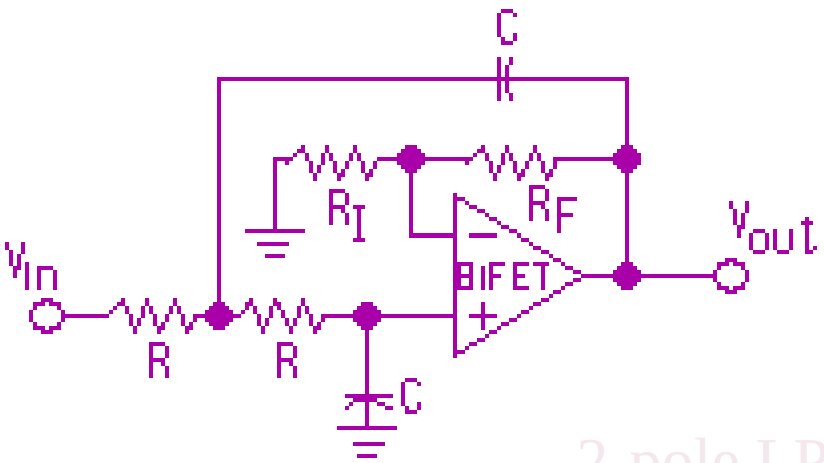
4-pole

DESIGN PROCEDURE FOR UNITY-GAIN HPF

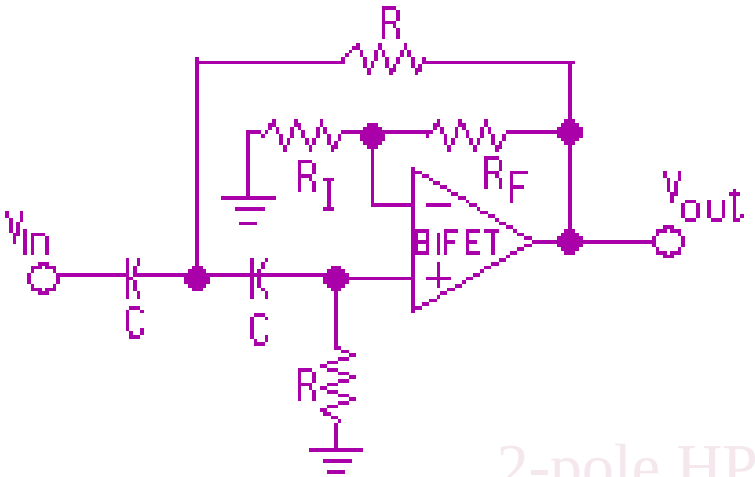
- The same procedure as for LP filters is used except for step #3, the normalized C value of 1 F is divided by K_f. Then pick a desired value for C, such as 0.001 μF to 0.1 μF, to calculate K_x. (Note that all capacitors have the same value).
- For step #6, multiply all normalized R values (from table) by K_x.

E.g. Design a unity-gain Butterworth HPF with a critical frequency of 1 kHz, and a roll-off of 55 dB/dec. (Ans.: C = 0.01 μF, R_1 = 4.49 kΩ, R_2 = 11.43 kΩ, R_3 = 78.64 kΩ.; pick standard values of 4.3 kΩ, 11 kΩ, and 75 kΩ).

EQUAL-COMPONENT FILTER DESIGN



2-pole LPF



2-pole HPF

Same value R & same value C are used in filter.

Select C (e.g. 0.01 μF), then:

A_v for # of poles is given in a table and is the same for LP and HP filter design.

$$A_v = \frac{R_F}{R_I} + 1$$

EXAMPLE

Design an equal-component LPF with a critical frequency of 3 kHz and a roll-off of 20 dB/oct.

Minimum # of poles = 4

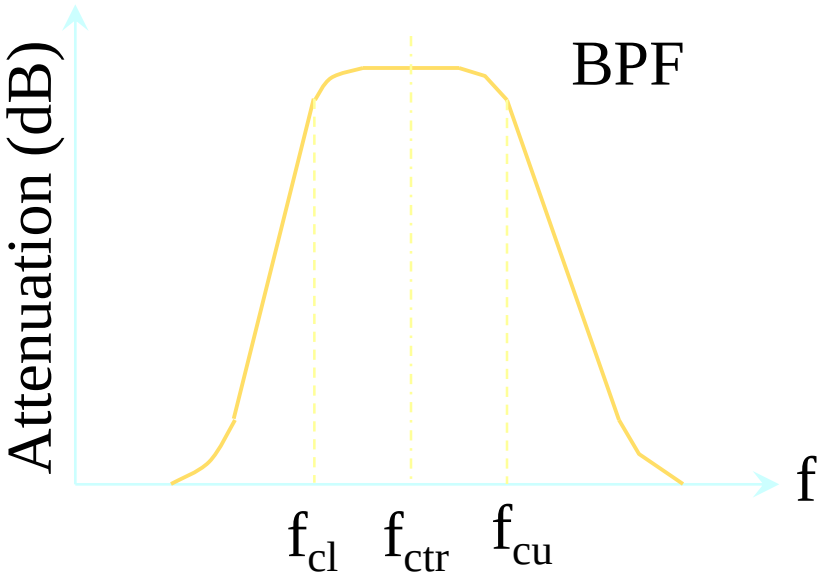
Choose C = 0.01 μF; ⊛ R = 5.3 kΩ

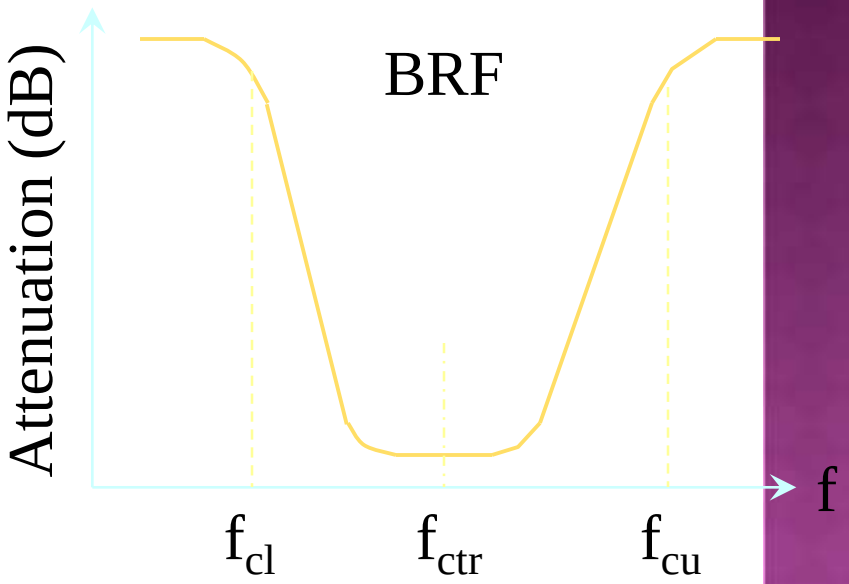
From table, A_{v1} = 1.1523, and A_{v2} = 2.2346.

Choose $R_{I1} = R_{I2}$ = 10 kΩ; then R_{F1} = 1.5 kΩ, and R_{F2} = 12.3 kΩ .

Select standard values: 5.1 kΩ, 1.5 kΩ, and 12 kΩ.

BANDPASS AND BAND-REJECTION FILTER





The quality factor, Q, of a filter is given by:

$$Q = \frac{f_{ctr}}{BW}$$

where BW = $f_{cu} - f_{cl}$ and

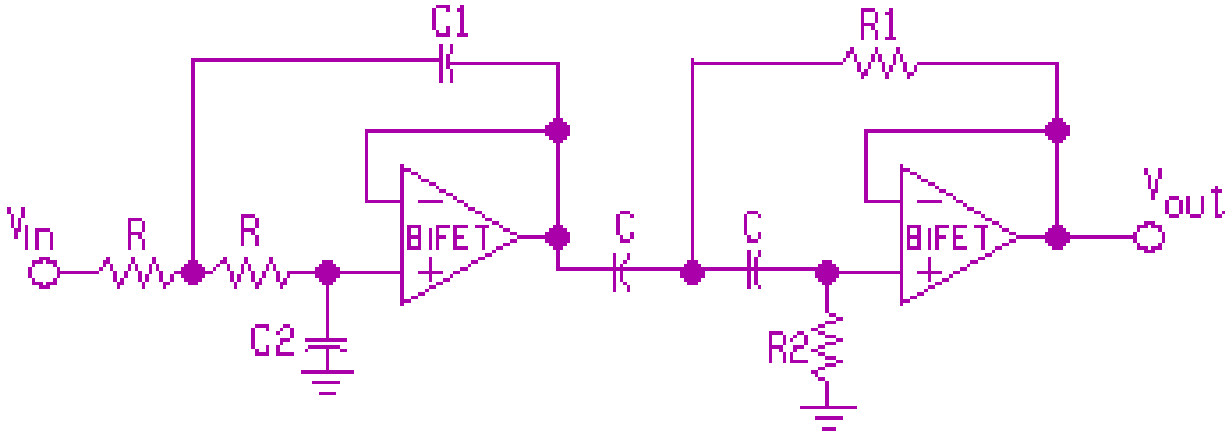
$$f_{ctr} = \sqrt{f_{cu} f_{cl}}$$

MORE ON BANDPASS FILTER

If BW and f_{centre} are given, then:

$$f_{cl} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} - \frac{BW}{2}\,;\; f_{cu} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} + \frac{BW}{2}$$

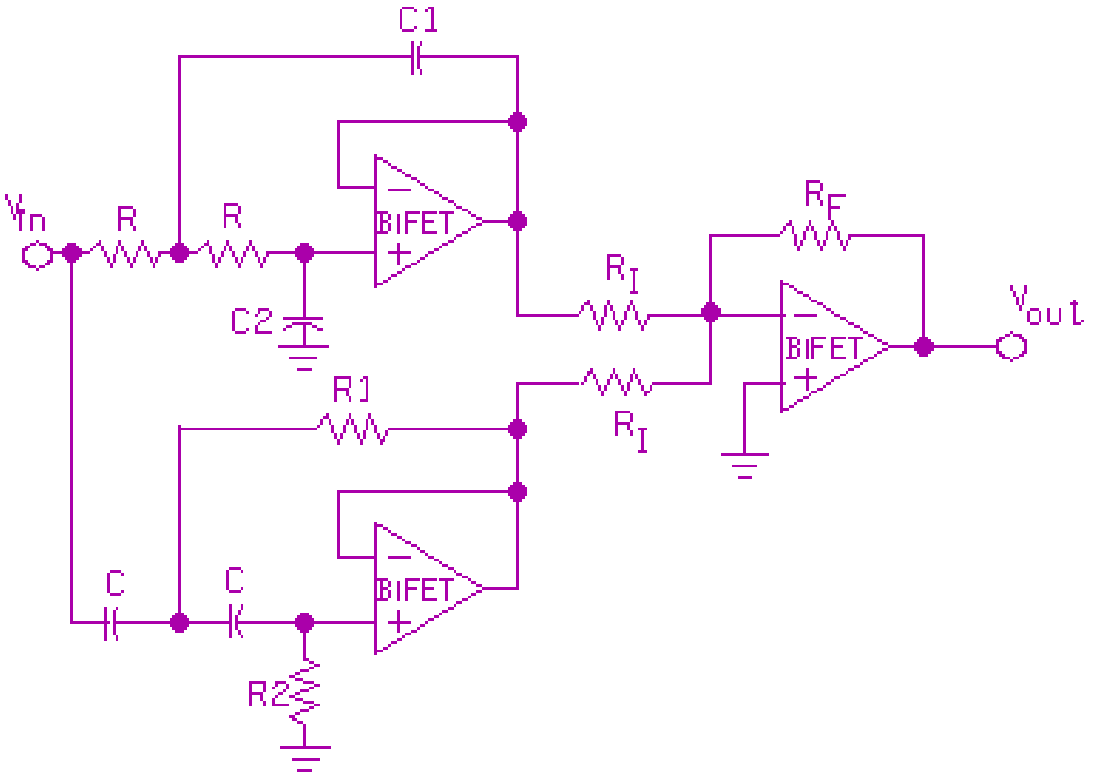
A *broadband* BPF can be obtained by combining a LPF and a HPF:



The Q of this filter is usually > 1.

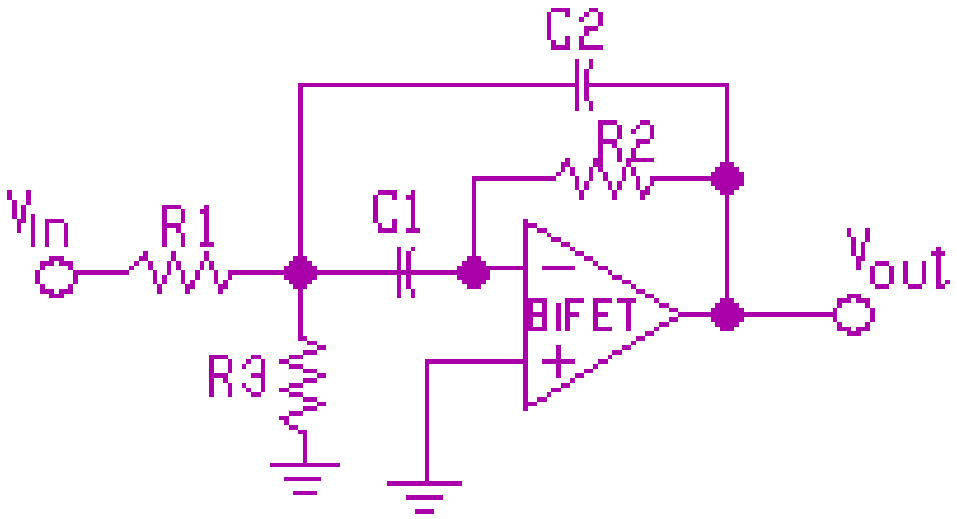
BROADBAND BAND-REJECT FILTER

A LPF and a HPF can also be combined to give a broadband BRF:



2-pole band-reject filter

NARROW-BAND BANDPASS FILTER



$$BW = \frac{f_{ctr}}{Q} = \frac{1}{2\pi R_1 C}$$

C1 = C2 = C

$R_2 = 2\,R_1$

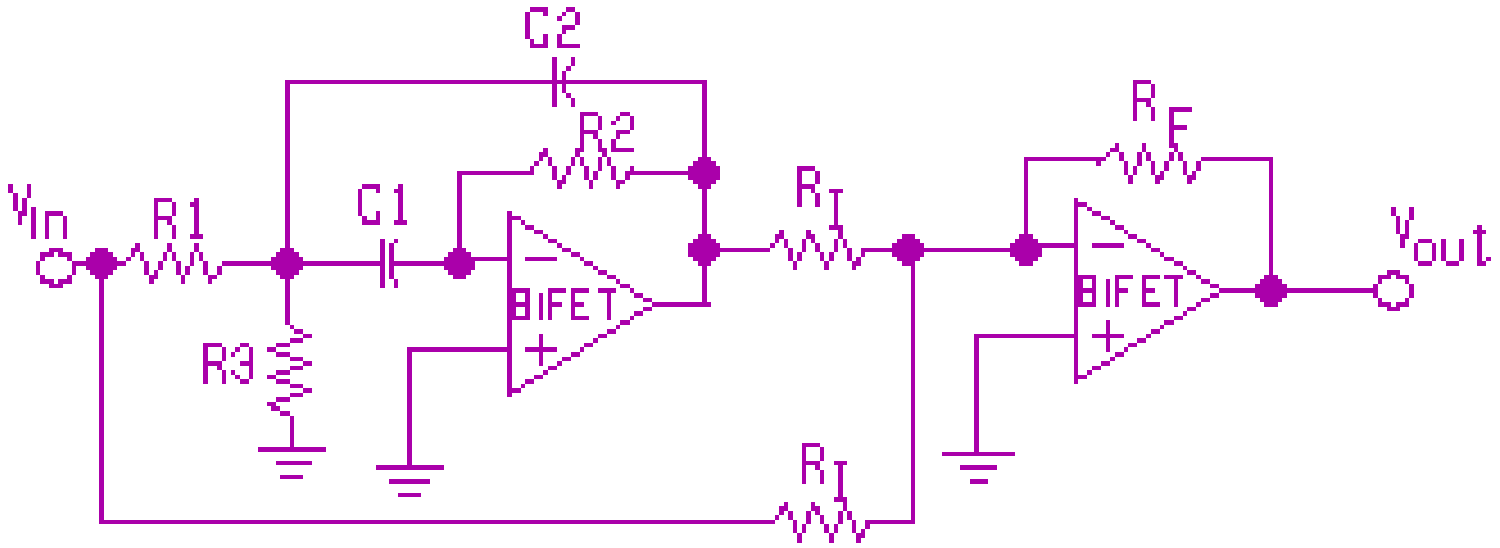
$$R_3 = \frac{R_1}{2Q^2 - 1}$$

$$f_{ctr} = \frac{1}{2\sqrt{2}\pi R_1 C}\sqrt{1 + \frac{R_1}{R_3}}$$

R_3 can be adjusted or trimmed to change f_{ctr} without affecting the BW. Note that Q < 1.

NARROW-BAND BAND-REJECT FILTER

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal:



The equations for R1, R2, R3, C1, and C2 are the same as before.
$R_I = R_F$ for unity gain and is often chosen to be >> R1.

CLASSIFICATION OF ADCS

1. Direct type ADC.
2. Integrating type ADC

Direct type ADCs

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter.
4. Successive approximation type converter

INTEGRATING TYPE CONVERTERS

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter

SAMPLE AND HOLD CIRCUIT

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

SAMPLE AND HOLD CIRCUIT

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period.The time period during which the voltage across the capacitor is held constant is called hold period

555 IC

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.

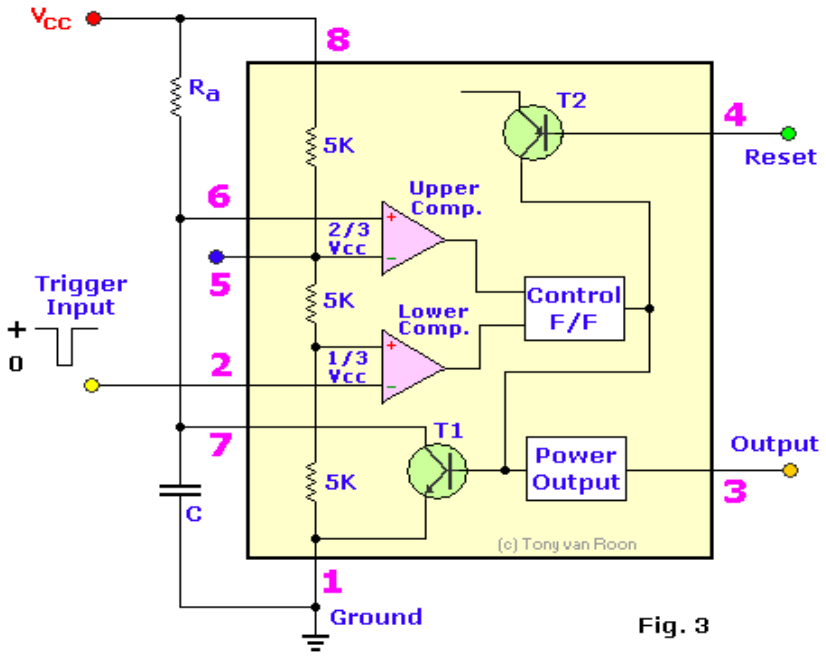


Fig. 3

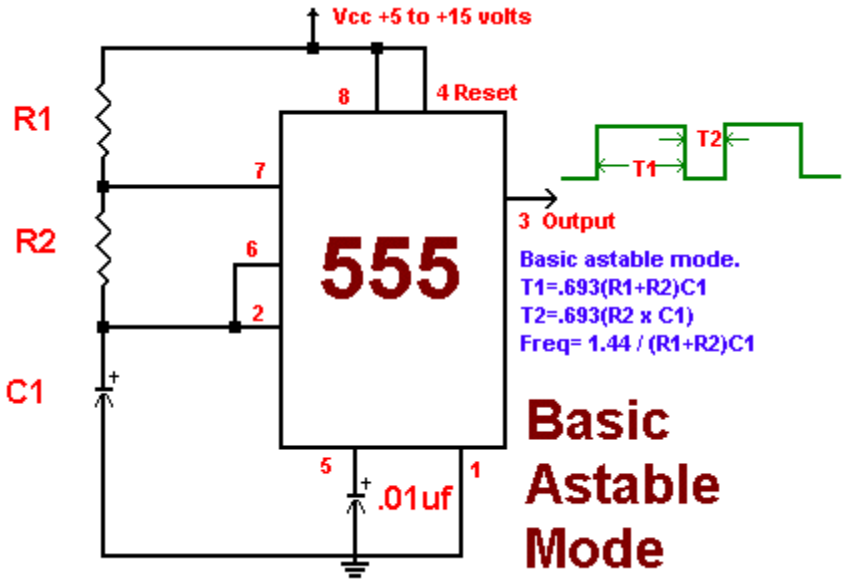
FEATURES OF 555 TIMER BASIC BLOCKS

1. It has two basic operating modes: monostable and astable
2. It is available in three packages. 8 pin metal can , 8 pin dip, 14 pin dip.
3. It has very high temperature stability

APPLICATIONS OF 555 TIMER

1. astable multivibrator
2. monostable multivibrator
3. Missing pulse detector
4. Linear ramp generator
5. Frequency divider
6. Pulse width modulation
7. FSK generator
8. Pulse position modulator
9. Schmitt trigger

ASTABLE MULTIVIBRATOR



ASTABLE MULTIVIBRATOR

- When the voltage on the capacitor reaches (2/3)Vcc, a switch is closed at pin 7 and the capacitor is discharged to (1/3)Vcc, at which time the switch is opened and the cycle starts over

MONOSTABLE MULTIVIBRATOR

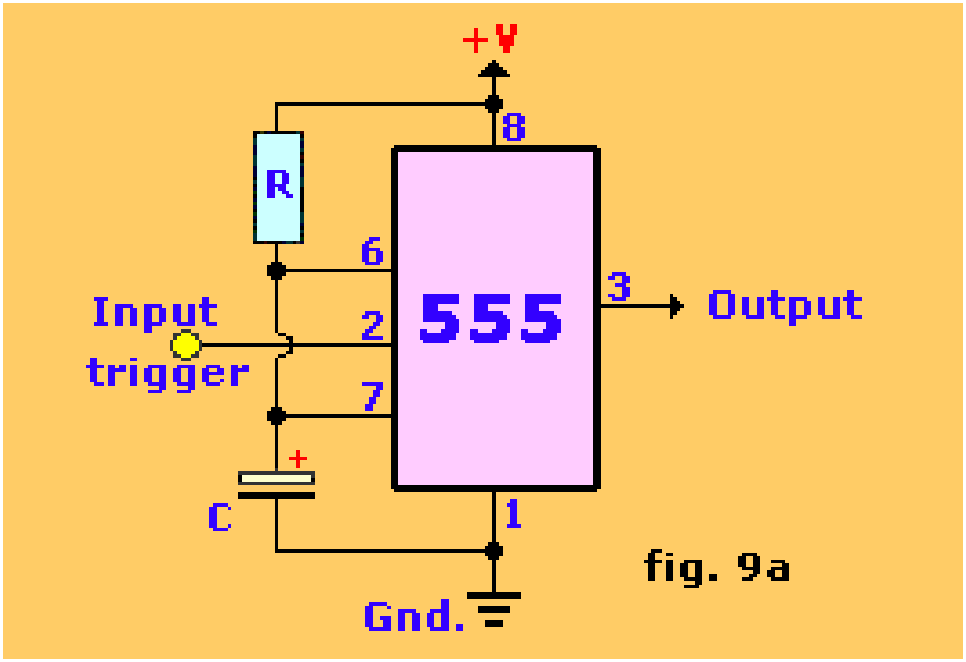


fig. 9a

VOLTAGE CONTROLLED OSCILLATOR

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage

The features of 566 VCO

1. Wide supply voltage range(10- 24V)
2. Very linear modulation characteristics
3. High temperature stability

PHASE LOCK LOOPED

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal

Applications of 565 PLL

1. Frequency multiplier
2. Frequency synthesizer
3. FM detector

UNIT-V

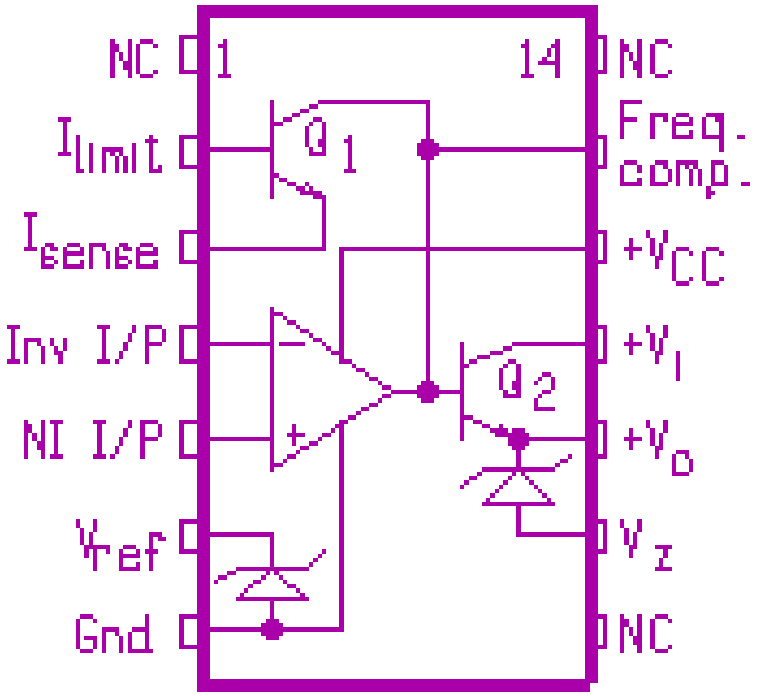
Data conversion devices

- Digital to Analog Conversion: DAC Specifications – DAC circuits
- Weighted Resistor DAC
- R-2R Ladder DAC
- Inverted R-2R Ladder DAC Monolithic DAC
- Analog to Digital conversion: ADC specifications
- ADC circuits-Ramp Type ADC
- Successive Approximation ADC
- Dual Slope ADC-Flash Type ADC
- Monolithic ADC.

IC VOLTAGE REGULATORS

- There are basically two kinds of IC voltage regulators:
  - Multipin type, e.g. LM723C
  - 3-pin type, e.g. 78/79XX
- Multipin regulators are less popular but they provide the greatest flexibility and produce the highest quality voltage regulation
- 3-pin types make regulator circuit design simple

MULTIPIN IC VOLTAGE REGULATOR



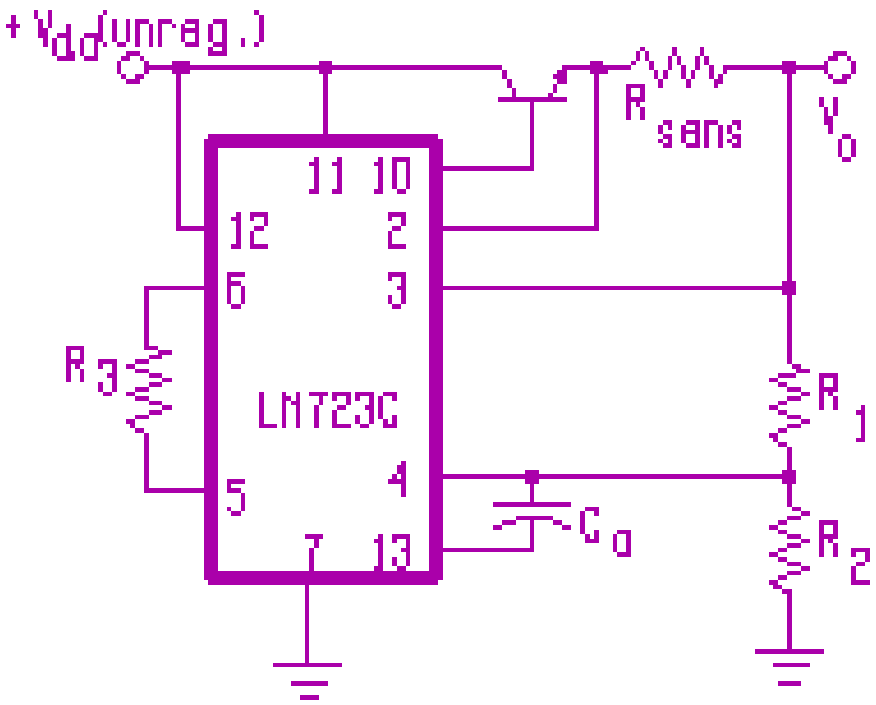
LM 723C Schematic

- The LM723 has an equivalent circuit that contains most of the parts of the op-amp voltage regulator discussed earlier.
- It has an internal voltage reference, error amplifier, pass transistor, and current limiter all in one IC package.

LM723 VOLTAGE REGULATOR

- Can be either 14-pin DIP or 10-pin TO-100 can
- May be used for either +ve or -ve, variable or fixed regulated voltage output
- Using the internal reference (7.15 V), it can operate as a high-voltage regulator with output from 7.15 V to about 37 V, or as a low-voltage regulator from 2 V to 7.15 V
- Max. output current with heat sink is 150 mA
- Dropout voltage is 3 V (i.e. $V_{CC} > V_{o(max)} + 3$)

LM723 IN HIGH-VOLTAGE CONFIGURATION



External pass transistor and current sensing added.

Design equations:

$$V_o = \frac{V_{ref}(R_1 + R_2)}{R_2}$$

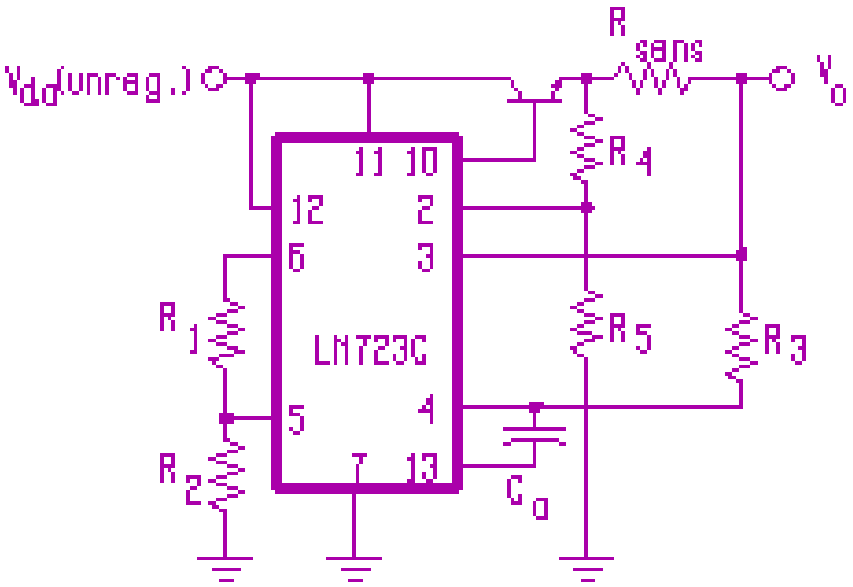
$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

$$R_{sens} = \frac{0.7}{I_{max}}$$

Choose $R_1 + R_2 = 10\ k\Omega$, and $C_c = 100$ pF.

To make V_o variable, replace R_1 with a pot.

LM723 IN LOW-VOLTAGE CONFIGURATION



With external pass transistor and foldback current limiting

$$V_o = \frac{R_2 V_{ref}}{R_1 + R_2}$$

$$I_{L(max)} = \frac{R_4 V_o + 0.7(R_4 + R_5)}{R_5 R_{sens}}$$

$$I_{short} = \frac{0.7(R_4 + R_5)}{R_5 R_{sens}}$$

$$R_{sens} = \frac{0.7 V_o}{I_{short}(V_o + 0.7) - 0.7 I_{L(max)}}$$

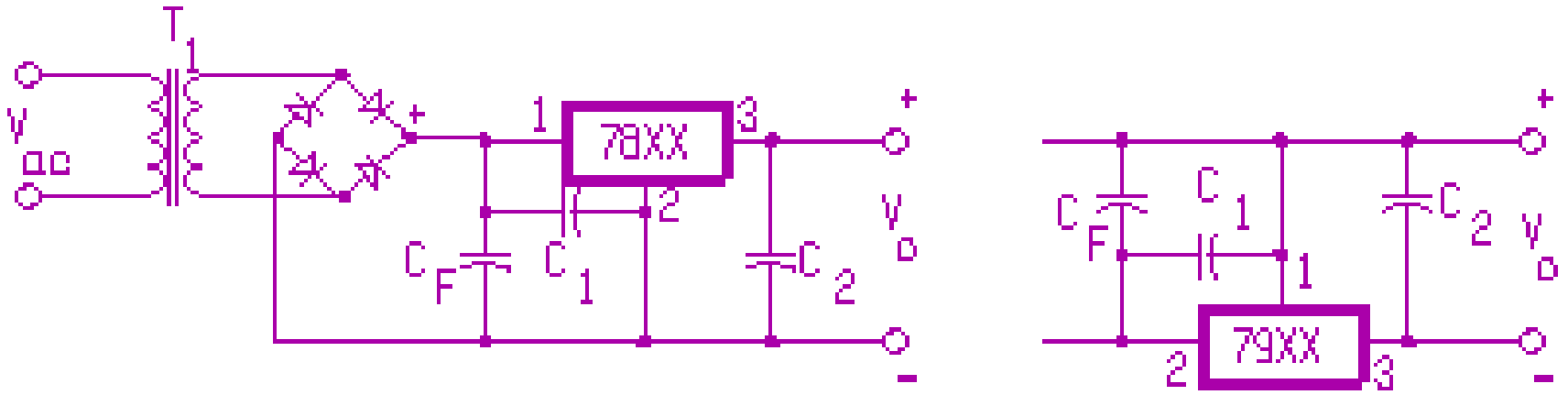
Under foldback condition:

$$V_o' = \frac{0.7 R_L (R_4 + R_5)}{R_5 R_{sens} - R_4 R_L}$$

THREE-TERMINAL FIXED VOLTAGE REGULATORS

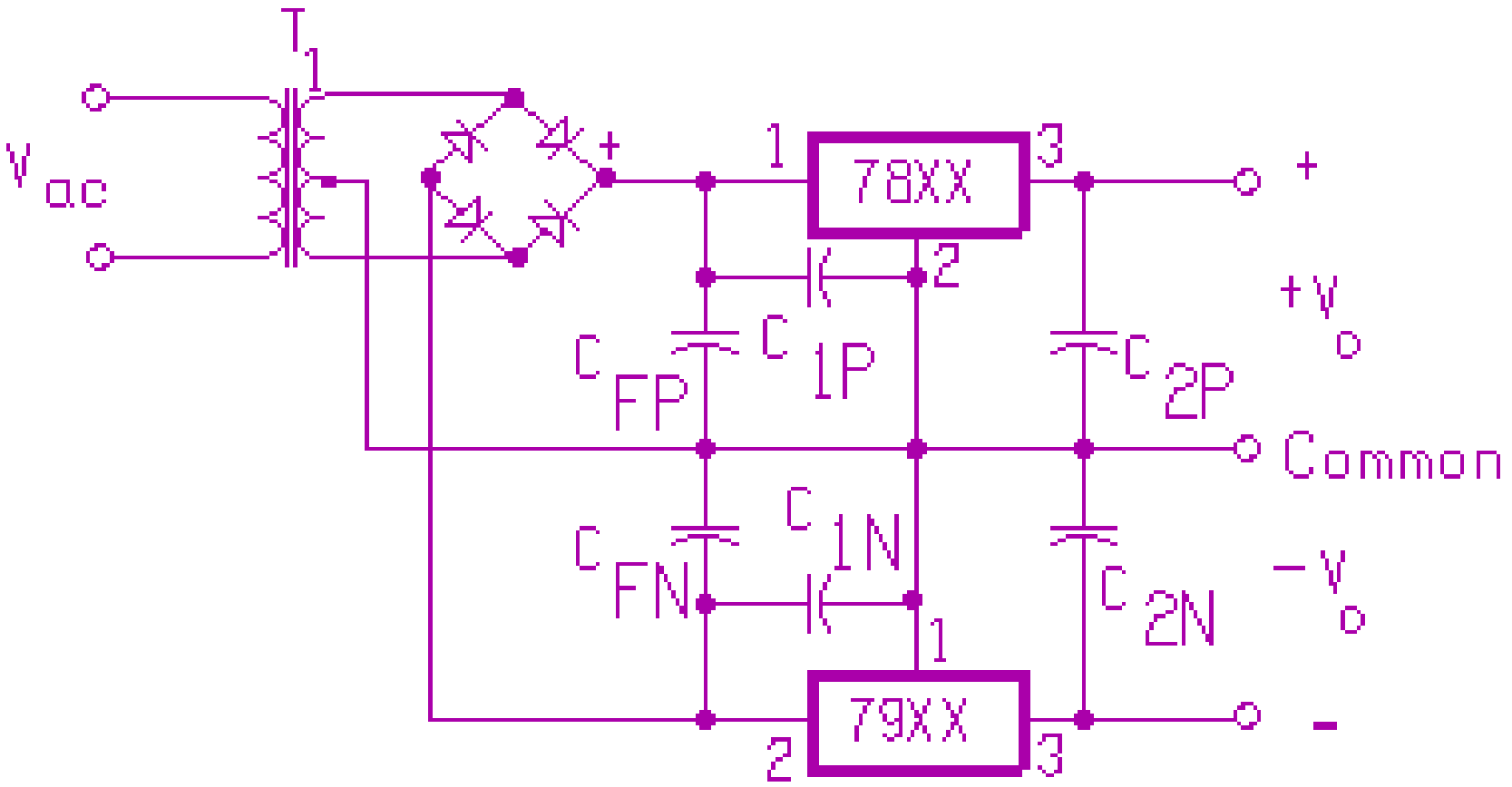
- Less flexible, but simple to use
- Come in standard TO-3 (20 W) or TO-220 (15 W) transistor packages
- 78/79XX series regulators are commonly available with 5, 6, 8, 12, 15, 18, or 24 V output
- Max. output current with heat sink is 1 A
- Built-in thermal shutdown protection
- 3-V dropout voltage; max. input of 37 V
- Regulators with lower dropout, higher in/output, and better regulation are available.

BASIC CIRCUITS WITH 78/79XX REGULATORS

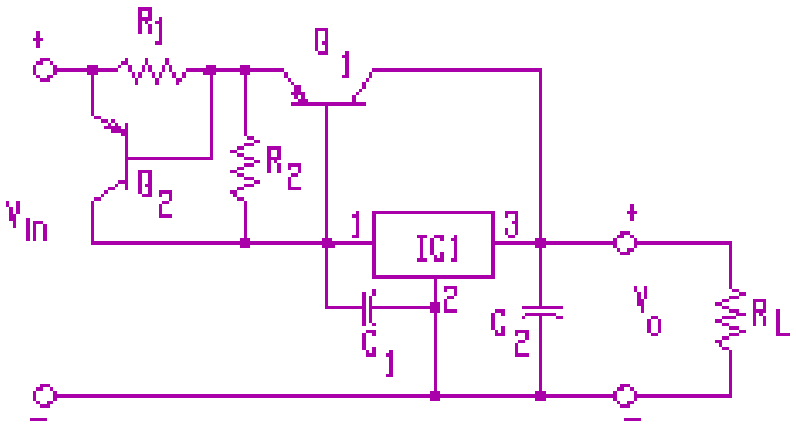


- Both the 78XX and 79XX regulators can be used to provide +ve or -ve output voltages
- C_1 and C_2 are generally optional. C_1 is used to cancel any inductance present, and C_2 improves the transient response. If used, they should preferably be either 1 μF tantalum type or 0.1 μF mica type capacitors.

DUAL-POLARITY OUTPUT WITH 78/79XX REGULATORS



78XX REGULATOR WITH PASS TRANSISTOR

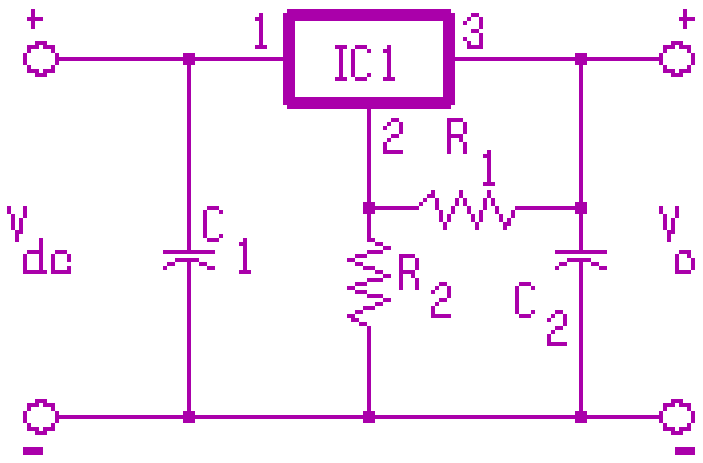


$$R_1 = \frac{0.7}{I_{max}}$$

$$R_2 = \frac{0.7}{I_{R2}}$$

- Q_1 starts to conduct when V_{R2} = 0.7 V.
- R2 is typically chosen so that max. I_{R2} is 0.1 A.
- Power dissipation of Q_1 is $P = (V_i - V_o)I_L$.
- Q_2 is for current limiting protection. It conducts when V_{R1} = 0.7 V.
- Q_2 must be able to pass max. 1 A; but note that max. V_{CE2} is only 1.4 V.

78XX FLOATING REGULATOR



- It is used to obtain an output > the V_{reg} value up to a max.of 37 V.
- R_1 is chosen so that $R_1 \leq 0.1\ V_{reg}/I_Q$, where I_Q is the c
t

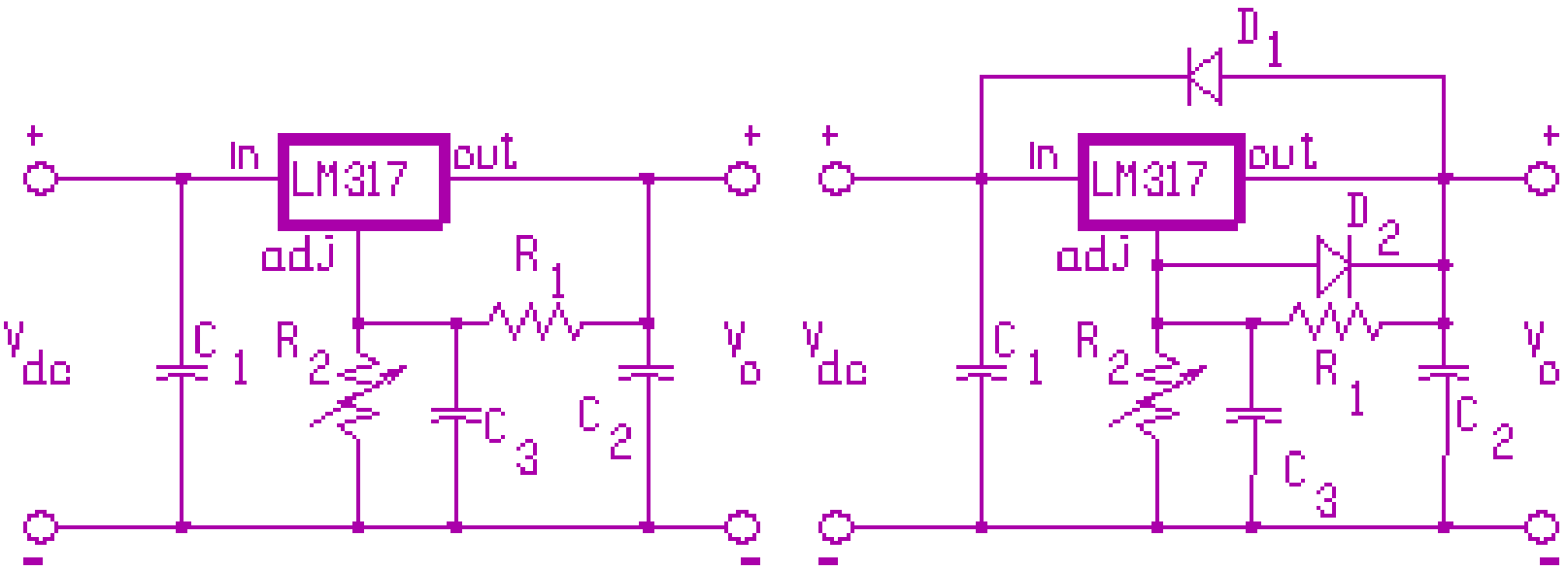
$$V_o = V_{reg} + \left(\frac{V_{reg}}{R_1} + I_Q\right) R_2$$

or $R_2 = \dfrac{R_1(V_o - V_{reg})}{V_{reg} + I_Q R_1}$ of

3-TERMINAL VARIABLE REGULATOR

- The floating regulator could be made into a variable regulator by replacing R_2 with a pot. However, there are several disadvantages:
  - Minimum output voltage is V_{reg} instead of 0 V.
  - I_Q is relatively large and varies from chip to chip.
  - Power dissipation in R_2 can in some cases be quite large resulting in bulky and expensive equipment.
- A variety of 3-terminal variable regulators are available, e.g. LM317 (for +ve output) or LM 337 (for -ve output).

BASIC LM317 VARIABLE REGULATOR CIRCUITS



(a)

Circuit with capacitors to improve performance

(b)

Circuit with protective diodes

NOTES ON BASIC LM317 CIRCUITS

- The function of C_1 and C_2 is similar to those used in the 78/79XX fixed regulators.
- C_3 is used to improve ripple rejection.
- Protective diodes in circuit (b) are required for high-current/high-voltage applications.

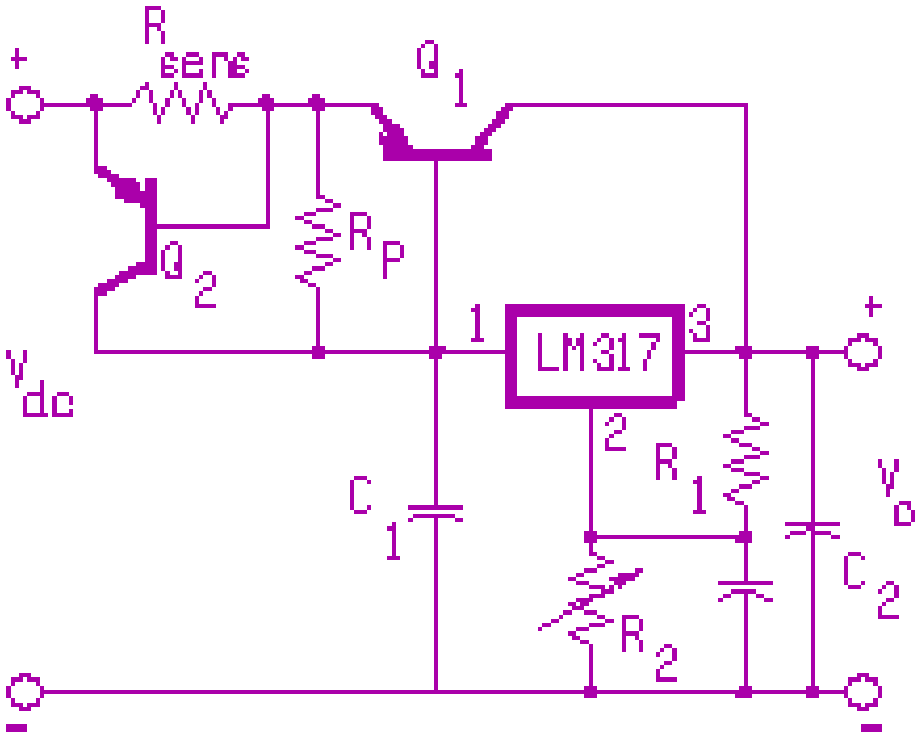
$$V_o = V_{ref} + \left(\frac{V_{ref}}{R_1} + I_{adj} \right) R_2$$

where V_{ref} = 1.25 V, and I_{adj} is the current flowing into the adj. terminal (typically 50 μA).

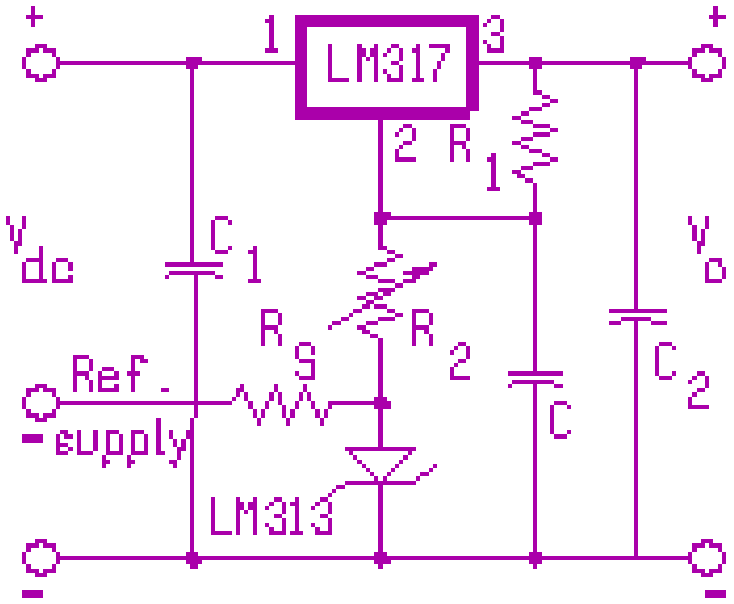
$$R_2 = \frac{R_1 (V_o - V_{ref})}{V_{ref} + I_{adj} R_1}$$

$R_1 = V_{ref} / I_{L(min)}$, where $I_{L(min)}$ is typically 10 mA.

LM317 REGULATOR CIRCUITS

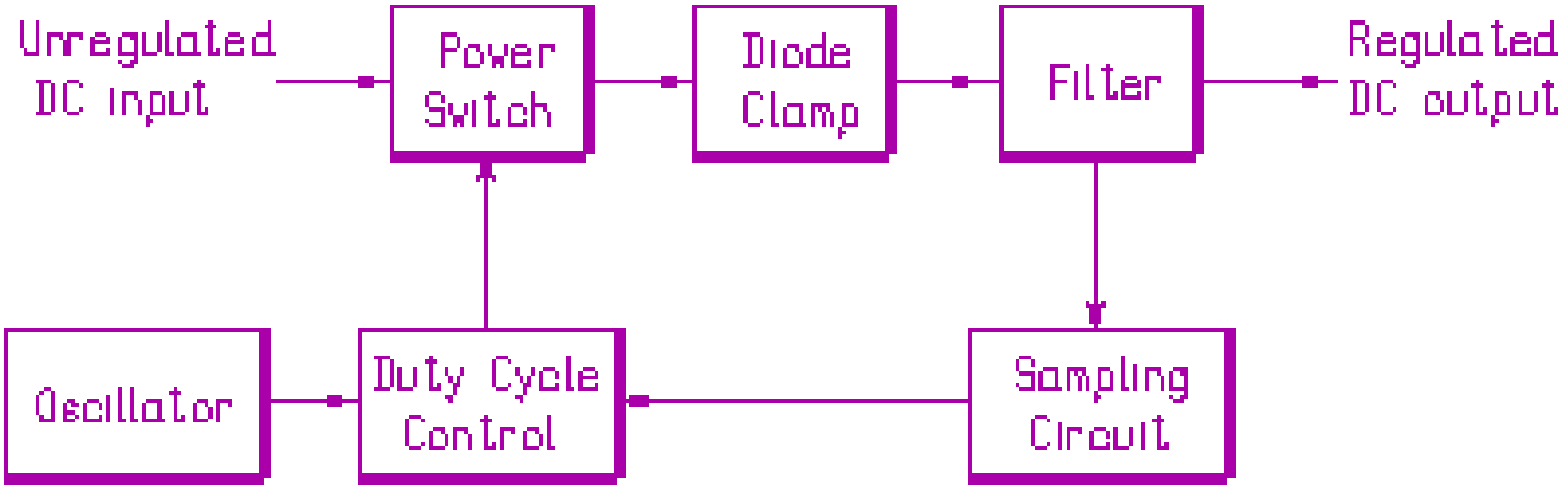


Circuit with pass transistor and current limiting



Circuit to give 0V min. output voltage

BLOCK DIAGRAM OF SWITCH-MODE REGULATOR



It converts an unregulated dc input to a regulated dc output. Switching regulators are often referred to as dc to dc converters.

COMPARING SWITCH-MODE TO LINEAR REGULATORS

Advantages:

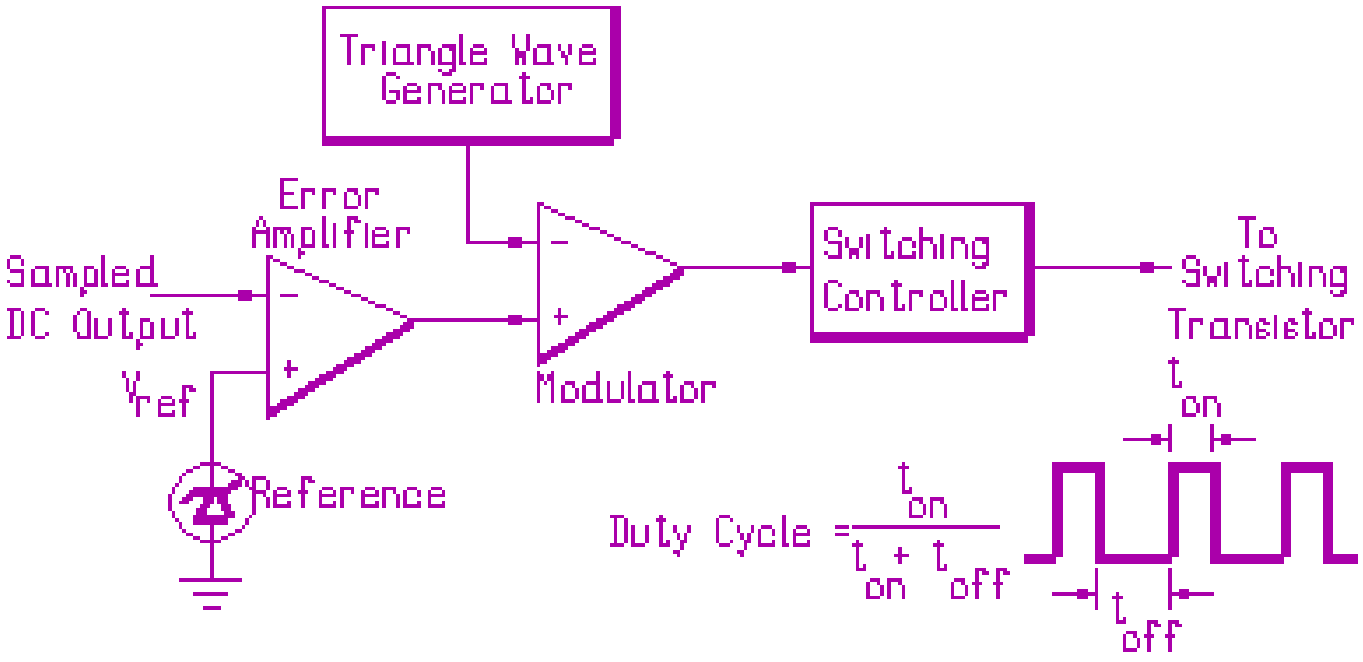
- 70-90% efficiency (about double that of linear ones)
- can make output voltage > input voltage, if desired
- can invert the input voltage
- considerable weight and size reductions, especially at high output power

Disadvantages:

- More complex circuitry
- Potential EMI problems unless good shielding, low-loss ferrite cores and chokes are used

GENERAL NOTES ON SWITCH-MODE REGULATOR

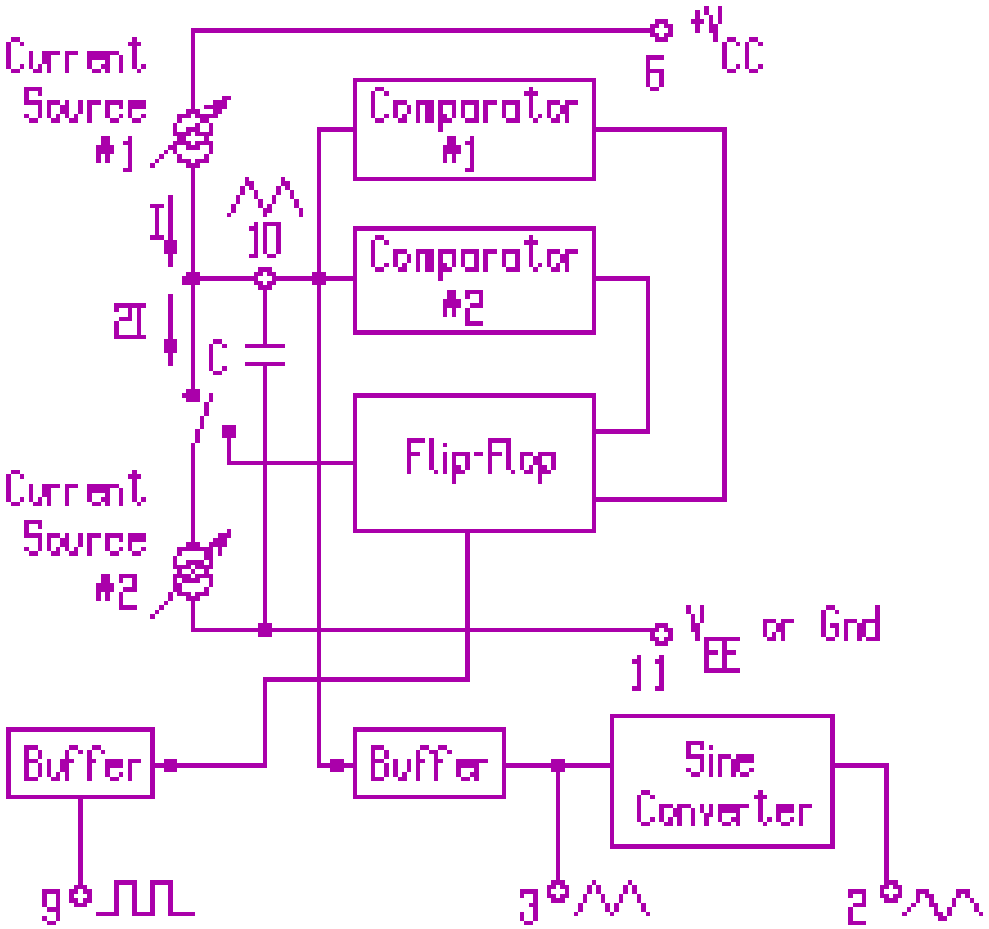
The duty cycle of the series transistor (power switch) determines the average dc output of the regulator. A circuit to control the duty cycle is the *pulse-width modulator* shown below:



GENERAL NOTES CONT'D . . .

- The *error amplifier* compares a sample of the regulator V_o to an internal V_{ref}. The difference or error voltage is amplified and applied to a *modulator* where it is compared to a triangle waveform. The result is an output pulse whose width is proportional to the error voltage.
- Darlington transistors and TMOS FETs with f_T of at least 4 MHz are often used. TMOS FETs are more efficient.
- A fast-recovery rectifier, or a Schottky barrier diode (sometimes referred to as a *catch diode*) is used to direct current into the inductor.
- For proper switch-mode operation, current must always be present in the inductor.

ICL8038 FUNCTION GENERATOR IC

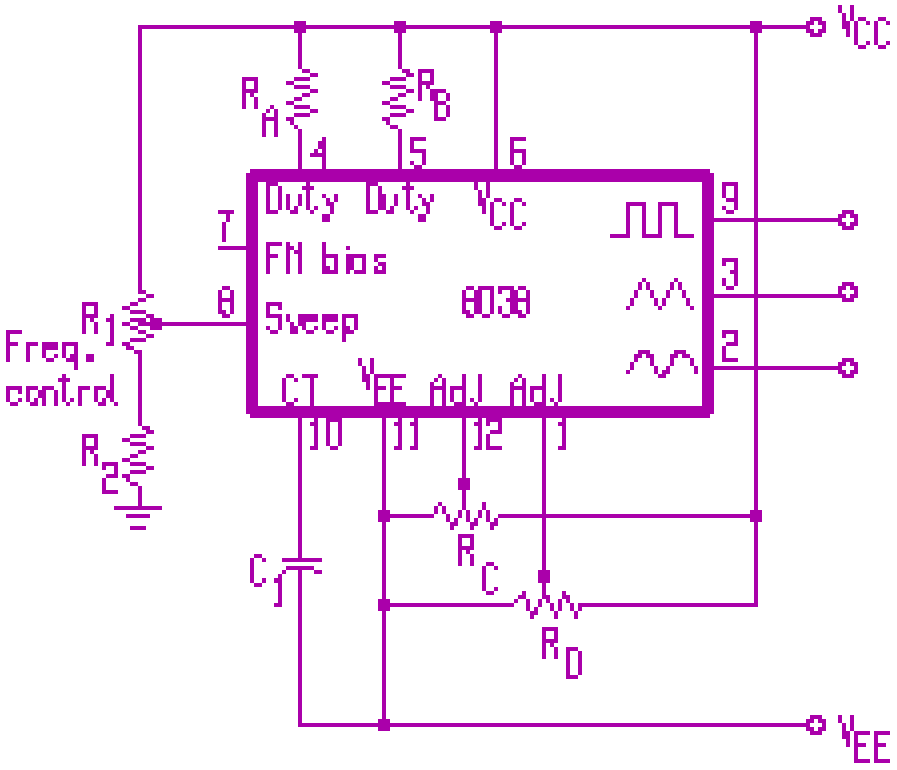


- Triangle wave at pin10 is obtained by linear charge and discharge of C by two current sources.
- Two comparators trigger the flip-flop which provides the square wave and switches the current sources.
- Triangle wave becomes sine wave via the sine converter .

ICL8038 FUNCTION GENERATOR IC

- To obtain a square wave output, a pull-up resistor (typically 10 to 15 kΩ) must be connected between pin 9 and V_{CC}.
- Triangle wave has a linearity of 0.1 % or better and an amplitude of approx. $0.3(V_{CC}-V_{EE})$.
- Sine wave can be adjusted to a distortion of < 1% with amplitude of $0.2(V_{CC}-V_{EE})$. The distortion may vary with f (from 0.001 Hz to 200 kHz).
- IC can operate from either single supply of 10 to 30 V or dual supply of ✂5 to ✂15 V.

ICL8038 FUNCTION GENERATOR CIRCUIT



$$+V_{CC} > V_{sweep} > \text{Ω}V_{total} + V_{EE} + 2$$

where $V_{total} = V_{CC} + |V_{EE}|$

$$f_o = \frac{3(V_{CC} - V_{sweep})}{2RC_1V_{total}}$$

where $R = R_A = R_B$

If pin 7 is tied to pin 8,

$$f_o = \frac{3}{5R_AC_1\left(1 + \frac{R_A}{2R_A - R_B}\right)}$$

For 50 % duty cycle,

$$f_o \approx \frac{0.3}{RC_1}$$

ISOLATION AMPLIFIER

- Provides a way to link a fixed ground to a floating ground.
- Isolates the DSP from the high voltage associated with the power amplifier.

ISOLATION AMPLIFIER

Purposes

- To break ground to permit incompatible circuits
- to be interfaced together while reducing noise
- To amplify signals while passing only low leakage current to prevent shock to people or damage to equipment
- To withstand high voltage to protect people, circuits, and equipment

METHODS

- Power Supply Isolation : battery, isolated power
- Signal Isolation : opto-isolation, capacitive

OPTOCOUPLER

- The optocouplers provide protection and high-speed switching

- An optocoupler, also known as an opto-isolator, is an integral part of the opto electronics arena. It has fast proven its utility as an electrical isolator or a high-speed switch, and can be used in a variety of applications.

- The basic design for optocouplers involves use of an LED that produces a light signal to be received by a photodiode to detect the signal. In this way, the output current or current allowed to pass can be varied by the intensity of light.

OPTOCOUPLER

- A very common application for the opto coupler is a FAX machine or MODEM, isolating the device from the telephone line to prevent the potentially destructive spike in voltage that would accompany a lightning strike. This protective tool has other uses in the opto electronic area. It can be used as a guard against EMI, removing ground loops and reducing noise.

- This makes the optocoupler ideal for use in switching power supply and motor control applications. Today as semiconductors are being designed to handle more and more power, isolation protection has become more important than ever before.

OPTOELECTRONIC INTEGRATED CIRCUITS

Applications

- Inter- and intra-chip optical interconnect and clock distribution
- Fiber transceivers
- Intelligent sensors
- Smart pixel array parallel processors

OPTOELECTRONIC INTEGRATED CIRCUITS

Approaches

- Conventional hybrid assembly: multi-chip modules
- Total monolithic process development
- Modular integration on ICs:
- epitaxy-on-electronics
- flip-chip bump bonding w. substrate removal
- self-assembly

LM380 POWER AMPLIFIER

General Description

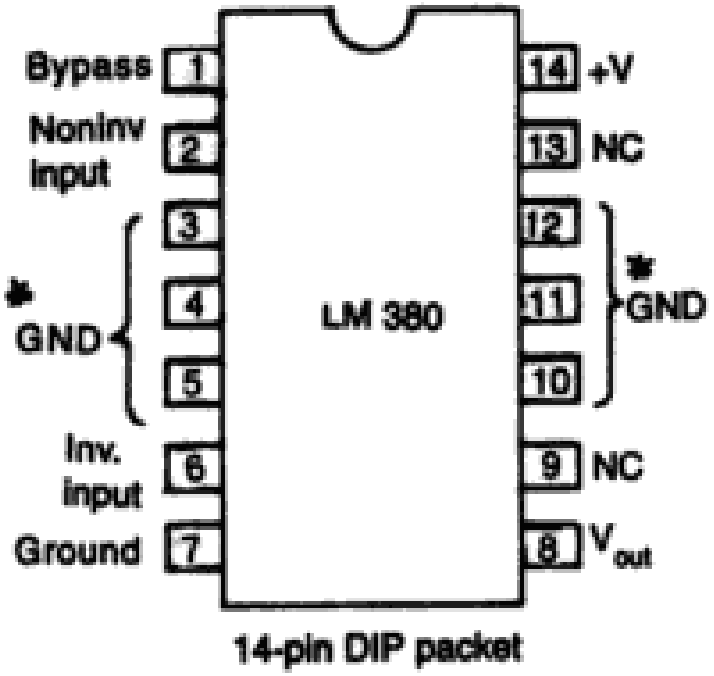
- The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage. The output is short circuit proof with internal thermal limiting.

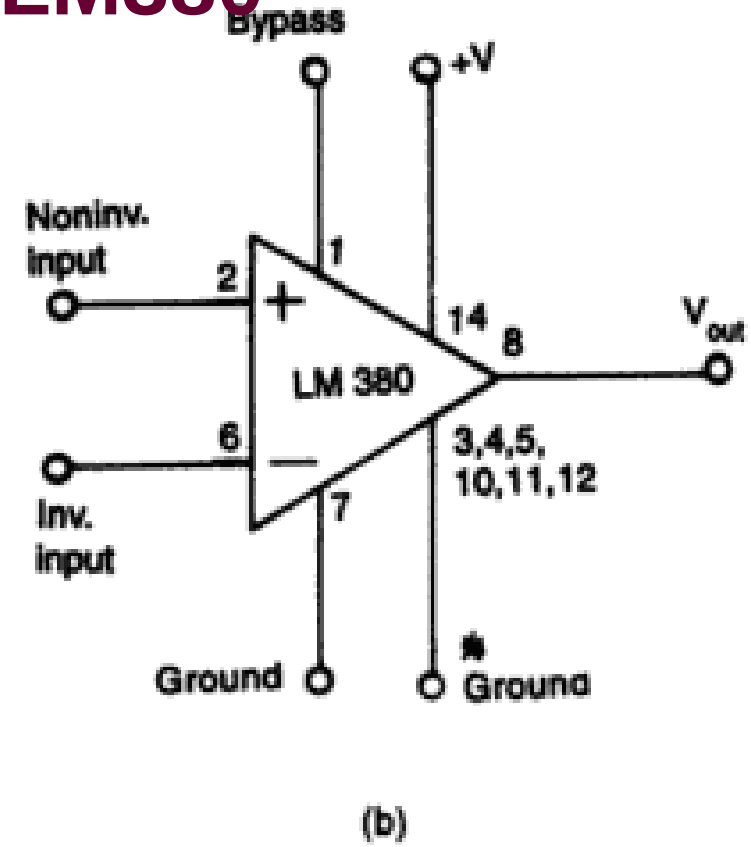
- The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

FEATURES

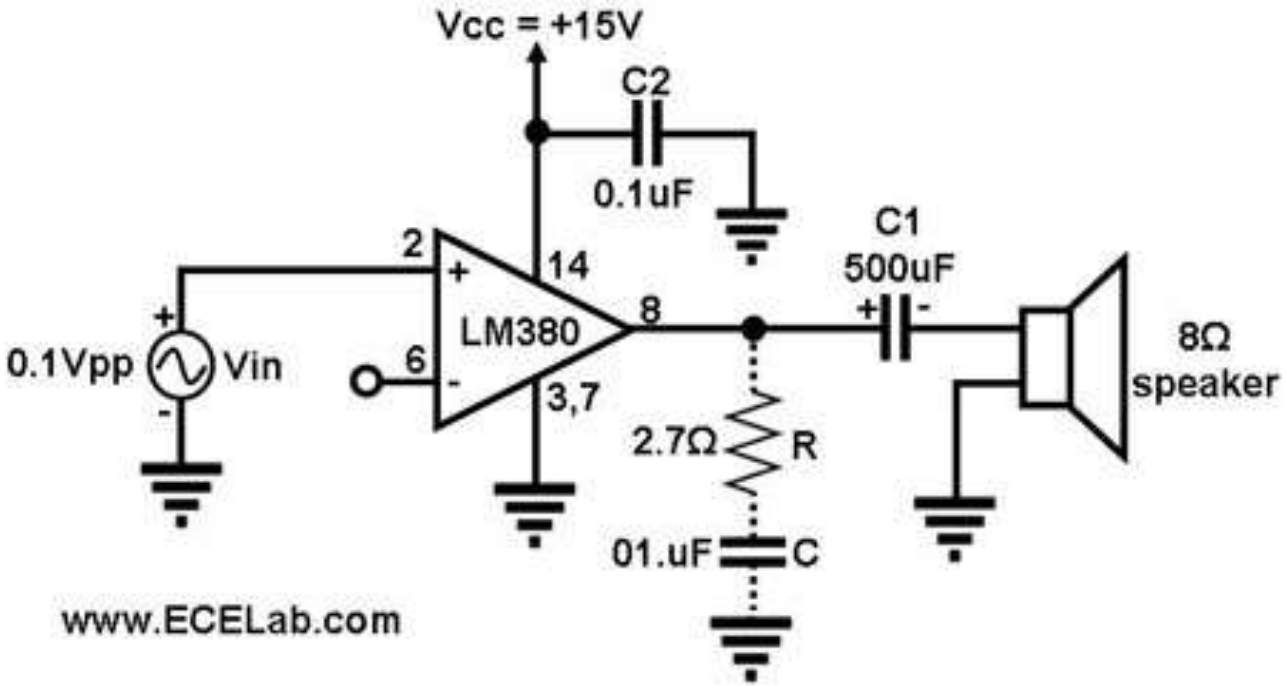
- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply
- voltage
- Standard dual-in-line package

PIN DIAGRAM AND BLOCK DIAGRAM OF LM380





CIRCUIT DIAGRAM FOR A SIMPLE LM380-BASED POWER AMPLIFIER



Questions
A differential amplifier
When a differential amplifier is operated single-ended,
In differential-mode
In the common-mode
The common-mode gain is
The differential gain is
If A_{DM} = 3500 and A_{CM} = 0.35, the CMRR is
With zero volts on both inputs, an OPamp ideally should have an output
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
A certain OP-amp has bias currents of 50 μA and 49.3 μA. The input offset current is
The output of a particular OP-amp increases 8 V in 12 μs. The slew rate is
For an OP-amp with negative feedback,the output is
The use of negative feedback
Negative feedback
A certain non-inverting amplifier has R_i of 1 kΩ and R f of 100 kΩ. The closed-loop voltage gain is
A certain non-inverting amplifier has R_i of 1 kΩ and R f of 100 kΩ. If feedback resistor is open, the voltage gain
A certain inverting amplifier has a closed loop voltage gain of 25. The OP-amp has an open-loop voltage gain of 100,000. If an OP-amp with an open-loop voltage gain of 200,000 is substituted in the arrangement, the closed-loop gain
A voltage follower
The OP-amp can amplify
The input offset current equals the

The tail current of a differential amplifier is
The node voltage at the top of the tail resistor is closest to.
The tail current in a differential amplifier equals
A common-mode signal is applied to
The common-mode voltage gain is
The input stage of an OP-amp is usually a
Current cannot flow to ground through
Which of the following electrical characteristics is not exhibited by an ideal op-amp?
An ideal op-amp requires infinite bandwidth because
Ideal op-amp has infinite voltage gain because
Find the output voltage of an ideal op-amp. If V_1 and V_2 are the two input voltages
How will be the output voltage obtained for an ideal op-amp?
Which is not the ideal characteristic of an op-amp?
Find the input voltage of an ideal op-amp. It's one of the inputs and output voltages are 2v and 12v. (Gain=3)
Which factor determine the output voltage of an op-amp?
The opamp can amplify
In a nonlinear op-amp circuit, the
The input signal for an instrumentation amplifier usually comes from
In a differential amplifier, the CMRR is limited mostly by the
An instrumentation amplifier has a high
The input offset electric current equals the
When the two input terminals of a differential amplifier are grounded

A common - mode signal is applied to
The common-mode voltage gain is
The input stage of an op amp is usually a
The common - mode rejection ratio is
A 741 C has
The voltage follower has a
An opamp has a voltage gain of 200,000. If the output voltage is 1 V, the input voltage is
The 741 C has a unity - gain frequency of
The typical input stage of an opamp has a
The input offset electric current is usually
With both bases grounded, the only offset that produces an error is the
The voltage gain of a loaded differential amp is
At the unity-gain frequency, the open-loop voltage gain is
The tail current in a differential amplifier equals
A common - mode signal is applied to
An instrumentation amplifier has a high
Of the values listed, the most realistic value for open-loop voltage gain of an OP-amp is
An ideal op-amp requires infinite bandwidth because
How many leads does the TO-5 metal can package of an operational amplifier have?

Op1	Op2	Op3
is a part of an OP-amp	has one input and one output	has two outputs
the output is grounded	one input is grounded and signal is applied to the other	both inputs are connected together
opposite polarity signals are applied to the inputs	the gain is one	the outputs are of different amplitudes
both inputs are grounded	the outputs are connected together	an identical signal appears on both inputs
very high	very low	always unity
very high	very low	dependent on input voltage
1225	10,000	80 dB
equal to the positive supply voltage	equal to the negative supply voltage	equal to zero
1	2000	80 dB
700 nA	99.3 µA	49.7 µA
90 V/ µs	0.67 V/ µs	1.5 V/ µs
increased	fed back to the inverting input	fed back to the noninverting input
reduces the voltage gain of an OP-amp	makes the OP-amp oscillate	makes linear operation possible
increases the input and output impedances	increases the input impedance and bandwidth	decreases the output impedance and bandwidth
100,000	1000	101
is not affected	increases	decreases
doubles	drops to 12.5	remains at 25
has a voltage gain of 1	in non-inverting	has no feedback resistor
a.c. signals only	d.c. signals only	both a.c. and d.c. signals
difference between two base currents	average of two base currents	collector current divided by current gain

half of either collector current	equal to either collector current	two times either collector current
collector supply voltage	zero	emitter supply voltage
difference between two emitter currents	sum of two emitter currents	collector current divided by current gain
the non-inverting in	the inverting input	both inputs
smaller than differential voltage gain	equal to differential voltage gain	greater than differential voltage gain
differential amplifier	class B push-pull amplifier	CE amplifier
a mechanical ground	an a.c. ground	a virtual ground
Infinite voltage gain	Infinite bandwidth	Infinite output resistance
Signals can be amplified without attenuation	Output common-mode noise voltage is zero	Output voltage occurs simultaneously with input voltage changes
To control the output voltage	To obtain finite output voltage	To receive zero noise output voltage
$V_O = V_1 - V_2$	$V_O = A \times (V_1 - V_2)$	$V_O = A \times (V_1 + V_2)$
Amplifies the difference between the two input voltages	Amplifies individual voltages input voltages	Amplifies products of two input voltage
Input Resistance –> 0	Output impedance –> 0	Bandwidth –> ∞
8v	4v	-4v
Both positive and negative saturation voltage	Positive saturation	Negative saturation
AC signals only	DC signals only.	both AC and DC signals
opamp never saturates	feedback loop is never opened	output shape is the same as the input shape.
an inverting amplifier.	resistor	differential amplifier.
CMRR of the opamp	gain - bandwidth product.	supply voltages
output impedance	power gain.	CMMR.
average of the two base currents	collector electric current divided by electric current gain.	difference between the two base-emitter voltages
the base currents are equal.	the collector currents are equal.	an output error voltage usually exists.

the non - inverting input.	the inverting input.	both inputs.
smaller than the voltage gain.	equal to the voltage gain.	greater than the voltage gain.
differential amp.	class B push-pull amplifier.	CE amplifier.
very low.	as high as possible.	equal to the voltage gain.
a voltage gain of 100,000.	an input impedance of 2 MΩ.	an output impedance of 75 Ω
closed - loop voltage gain of unity.	small open - loop voltage gain	closed - loop bandwidth of zero.
2 micro V.	5 micro V.	10 V.
10 Hz.	20 Hz.	1 MHz.
single - ended input and single-ended output	single - ended input and differential output.	differential input and single - ended output.
less than the input bias current.	equal to zero.	less than the input offset voltage.
input offset current.	input bias current.	input offset voltage.
large than the unloaded voltage gain.	equal to R_C / r_e.	smaller than the unloaded voltage gain.
1	$A_{V(mid)}$.	zero.
difference between two emitter currents	sum of two emitter currents	collector current divided by current gain
the non - inverting input.	the inverting input.	both inputs.
output impedance	power gain.	CMMR.
1	2000	80 dB
Signals can be amplified without attenuation	Output common-mode noise voltage is zero	Output voltage occurs simultaneously with input voltage changes
8, 10, or 12	6, 8, or 10	8 or 14

Op4	Op5	Op6
answers a and c		
the output is not inverted		
only one supply voltage is used		
the output signals are in-phase		
unpredictable		
about 100		
answers b and c		
equal to the CMRR		
100,000		
none of these		
none of these		
equal to the input		
answers a and c		
does not affect impedance or bandwidth		
100		
depends on R_i		
increases slightly		
has all of these		
neither d.c. nor a.c. signals		
none of these		

equal to the difference in base currents		
tail current times base resistance		
collector voltage divided by collector resistance		
top of the tail resistor		
none of the above		
swamped amplifier		
an ordinary ground		
Infinite slew rate.		
Output can drive infinite number of device		
None of the mentioned		
$V_O = V_1 \times V_2$		
None of the mentioned		
Open loop voltage gain –> ∞		
-2v		
Supply voltage		
neither AC not DC signals.		
opamp may saturate.		
Wheatstone bridge.		
tolerance of the resistors		
supply voltage.		
difference between the two base currents.		
the ac output voltage is zero.		

he top of the tail resistor		
none of the above.		
swamped amplifier.		
equal to the common-mode voltage gain.		
all of the above.		
large closed - loop output impedance.		
1 V.		
15 MHz.		
differential input and differential output		
unimportant when a base resistor is used.		
β.		
impossible to determine.		
very large		
collector voltage divided by collector resistance		
he top of the tail resistor		
supply voltage.		
100,000		
Output can drive infinite number of device		
8 or 16		

Answer
answers a and c
one input is grounded and signal is applied to the other
opposite polarity signals are applied to the inputs
an identical signal appears on both inputs
very low
very low
answers b and c
equal to zero
100,000
700 nA
0.67 V/ µs
fed back to the inverting input
makes the OP-amp oscillate
increases the input impedance and bandwidth
101
increases
remains at 25
has all of these
both a.c. and d.c. signals
difference between two base currents

two times either collector current
zero
sum of two emitter currents
both inputs
smaller than differential voltage gain
differential amplifier
a virtual ground
Infinite output resistance
Signals can be amplified without attenuation
To obtain finite output voltage
$V_O = A \times (V_1 - V_2)$
Amplifies the difference between the two input voltages
Open loop voltage gain –> ∞
-2v
Both positive and negative saturation voltage
both AC and DC signals
opamp may saturate.
Wheatstone bridge.
gain - bandwidth product.
CMMR.
collector electric current divided by electric current gain.
the base currents are equal.

both inputs.
greater than the voltage gain.
differential amp.
as high as possible.
all of the above.
closed - loop bandwidth of zero.
5 micro V.
1 MHz.
differential input and single - ended output.
less than the input bias current.
input offset voltage.
equal to R_C / r_e.
1
sum of two emitter currents
both inputs.
CMMR.
100,000
Signals can be amplified without attenuation
8, 10, or 12

Questions
A certain non - inverting amplifier has an R_i of 1.0 kΩ and an R_f of 100 kΩ. The closed loop gain is
The bandwidth of an ac amplifier having a lower critical frequency of 1 kHz and an upper critical frequency of 10 kHz is
The bandwidth of a d c amplifier having an upper critical frequency of 100 kHz is
At the unity gain frequency, the open – loop gain is
The cutoff frequency of an op - amp equals the unity - gain frequency divided by
The initial slope of a sine wave is directly proportional to
The 741C has a unity gain frequency of
When slew rate distortion of a sine wave occurs, the output
The 741C has
When negative feed back is used , the gain-band width product of an op - amp
A summing amplifier can have
An averaging amplifier has five inputs . The ratio R_f/R_i must be
In a scaling adder, the input resistors are
In an integrator , the feed back element is a
For step - in put , the out put of an integrator is a
In a differentiator , the feed back element is a
The output of the differentiator is proportional to
Current cannot flow to the ground through
In an averaging circuit, the input resistances are
When a large sine wave drives a Schmitt trigger, the output is a
A comparator with a trip point of zero is some times called a
To work properly, many IC comparators need an external
A Schmitt trigger uses
A Schmitt trigger
.An ideal operational amplifier has
Another name for a unity gain amplifier is:
The open-loop voltage gain (A_{ol}) of an op-amp is the
A series dissipative regulator is an example of a:
A noninverting closed-loop op-amp circuit generally has a gain factor:
. In order for an output to swing above and below a zero reference, the op-amp circuit requires:
Op-amps used as high- and low-pass filter circuits employ which configuration?
If ground is applied to the (+) terminal of an inverting op-amp, the (–) terminal will:
An astable multivibrator is also known as a:
With negative feedback, the returning signal:
. What starts a free-running multivibrator?

A portion of the output that provides circuit stabilization is considered to be:

If a noninverting amplifier has an R_{IN} of 1000 ohms and an R_{FB} of 2.5 kilohms, what is the R_{IN} voltage when 1.42 mV is applied to the correct input?
Input impedance [Z_{in} (I)] of an inverting amplifier is approximately equal to:
The closed-loop voltage gain of an inverting amplifier equals
All of the following are basic op-amp input modes of operation EXCEPT
A circuit whose output is proportional to the difference between the input signals is considered to be which type of amplifier?
With negative feedback, the returning signal
The voltage follower has a:
The ratio between differential gain and common-mode gain is called:
If the gain of a closed-loop inverting amplifier is 3.9, with an input resistor value of 1.6 kilohms, what value of feedback resistor is necessary?
In an open-loop op-amp circuit, whenever the inverting input (–) is negative relative to the noninverting input (+), the output will:
With a differential gain of 50,000 and a common-mode gain of 2, what is the common-mode rejection ratio?
If the input to a comparator is a sine wave, the output is a:
What three subcircuits does a phase locked loop (PLL) consist of?
The major difference between ground and virtual ground is that virtual ground is only a:
If an op-amp has one input grounded and the other input has a signal feed to it, then it is operating as what?
If the feedback/input resistor ratio of a feedback amplifier is 4.6 with 1.7 V applied to the noninverting input, what is the output voltage value?
The Schmitt trigger is a two-state device that is used for:
. When a capacitor is used in place of a resistor in an op-amp network, its placement determines:
. The common-mode voltage gain is
How many logic states does an S-R flip-flop have?
An output that is proportional to the addition of two or more inputs is from which type of amplifier?
In a PLL, to obtain lock, the signal frequency must:
An ideal amplifier should have:
In an analog multiplier, the reference Voltage V_{ref} is internally set to ____
In one quadrant multiplier, the polarity of the input voltage V_x is _____ and V_y is_____.

If $V_s = V_s \sin(2*pi*f_s*t)$ and $V_o = V_o \sin((2*pi*f_o*t) + \theta)$ are applied to a switch type phase detector, then the output consists of a DC term and the other term is _____
Division can be accomplished by placing the multiplier circuit in the _____ of the operational amplifier.
Analog Multiplier produces an output which is a

Op1	Op2	Op3
100,000	1000	101
1 kHz	9 kHz	10 kHz
100 kHz	unknown	infinity
1	Amid	zero
the cut off frequency	closed - loop voltage gain	unity
slew rate	frequency	voltage gain
10 Hz	20 kHz	1 MHz
is larger	appears triangular	is normal
an input impedance of 2 MΩ	an out put impedance of 75 Ω	all of the above
increases	decreases	stays the same
only one input	only two inputs	only three inputs
5	0.2	1
all of the same value	all of different values	each proportional to the weight of its input
resistor	capacitor	zener diode
pulse	triangular wave form	spike
resistor	capacitor	zener diode
the RC time constant	the rate at which the input is changing	the amplitude of the input
mechanical ground	an ac ground	a virtual ground
equal to the feedback resistor	less than the feedback resistor	greater than the feedback resistor
rectangular wave	triangular wave	rectified sine wave
threshold detector	zero - crossing detector	positive limit detector
pull - up resistor	compensating capacitor	by pass capacitor
positive feed back	negative feedback	compensating capacitors
is a zero - crossing detector has two trip points	has two trip points	produces triangular output waves
infinite output impedance	zero input impedance	infinite bandwidth
difference amplifier	comparator	single ended
external voltage gain the device is capable of	internal voltage gain the device is capable of	most controlled parameter
linear regulator	switching regulator	shunt regulator
less than one	greater than one	of zero
a resistive feedback network	zero offset	a wide bandwidth.
Noninverting	Comparator	open-loop
not need an input resistor	be virtual ground	have high reverse current
one-shot multivibrator	free-running multivibrator	bistable multivibrator
aids the input signal	is proportional to output current	opposes the input signal
a trigger	an input signal	an external circuit

negative feedback	distortion	open-loop

3.5 mV	Ground	1.42 mV
R_i	$R_f + R_i$	∞
the ratio of the input resistance to the feedback resistance	the open-loop voltage gain	the feedback resistance divided by the input resistance
inverting mode	common-mode	double-ended
common-mode	darlington	differential
is proportional to the output current	is proportional to the differential voltage gain	differential
closed-loop voltage gain of unity	small open-loop voltage gain	closed-loop bandwidth of zero
Amplitude	differential-mode rejection	common-mode rejection
6240 ohms	2.4 kilohms	410 ohms
swing negative	close the loop	be balanced
–87.9 dB	–43.9 dB	43.9 dB
ramp voltage	sine wave	rectangular wave
phase comparator, comparator, and VCO	phase comparator, bandpass filter, and VCO	phase comparator, bandpass filter, and demodulator
voltage reference	current reference	power reference
Common-mode	Single-ended	Double-ended
a) 7.82 V	Saturation	Cutoff
pulse shaping	peak detection	input noise rejection
open- or closed-loop gain	integration or differentiation	saturation or cutoff
smaller than differential voltage gain	equal to voltage gain	greater than differential voltage gain
2	3	4
Differentiator	Difference	Summing
come within the lock range	be less than the capture frequency	come within the capture range
high input current	zero set	high output impedance
15V	5V	20V
positive, negative.	positive, positive	negative, negative

f_o	$2* f_o$	$f_o/ 2$
feedback loop	inverting input terminal	output
product of two input signals divided by a reference voltage.	product of two input signals and reference voltage.	product of three input signals.

Op4	Op5	Op6
100		
11 kHz		
0 H z		
very large		
common - mode voltage gain		
capacitance		
15 MHz		
has no effect		
voltage gain of 100,000		
fluctuates		
any number of inputs		
2		
related by a factor of two		
voltage divider		
ramp		
voltage divider		
answers a and b		
an ordinary ground		
unequal		
series of ramps		
half - wave detector		
compensating resistor		
pull - up resistors		
is designed to trigger on noise voltage		
All of the above		
voltage follower		
same as A_{cl}		
dc-to-dc converter		
equal to one		
a negative and positive supply		
inverting		
not invert the signal		
monostable multivibrator.		
is proportional to differential voltage gain		
nothing		

positive feedback		

0.56 mV		
$R_f - R_i$		
the input resistance		
single-ended		
operational		
aids the input signal		
large closed-loop output impedance		
phase		
0.62 kilohms		
swing positive		
87.9 dB		
sawtooth wave		
phase comparator, low-pass filter, and VCO		
difference reference		
Noninverting mode		
9.52 V		
filtering		
addition or subtraction		
None of the above		
5		
analog subtractor		
be greater than the capture frequency		
moderate gain		
10V		
negative positive		

3* f_o		
non inverting terminal		
product of two input signals.		

Answer
101
9 kHz
100 kHz
1
closed - loop voltage gain
slew rate
1 **MHz**
appears triangular
voltage gain of 100,001
stays the same
any number of inputs
0.2
each proportional to the weight of its input
capacitor
ramp
capacitor
answers a and b
a virtual ground
greater than the feedback resistor
triangular wave
positive limit detector
by pass capacitor
compensating capacitors

has two trip points

infinite bandwidth
voltage follower
internal voltage gain the device is capable of
dc-to-dc converter
greater than one
a negative and positive supply
inverting
be virtual ground
free-running multivibrator
opposes the input signal
nothing

negative feedback

1.42 mV
R_i
the feedback resistance divided by the input resistance
inverting mode
differential
differential
closed-loop voltage gain of unity
common-mode rejection
6240 ohms
swing positive
87.9 dB
rectangular wave
phase comparator, low-pass filter, and VCO
voltage reference
Single-ended
9.52 V
pulse shaping
integration or differentiation
smaller than differential voltage gain
2
Summing
come within the capture range
zero set
10V
positive, positive

2* f_o
feedback loop
product of two input signals divided by a reference voltage.

Questions	Op1
The input stage of Phase Locked Loop is_____	Low Pass Filter
The Voltage Controlled Oscillator is also called as _____	relaxation oscillator
The function of phase detector is to compare the _____ of the incoming signal to that of the output V_0 of Voltage Controlled Oscillator.	phase and frequency
Phase detector is basically a _____.	summer
The output of phase detector is _____.	f_s+f_0
The signal V_c shifts the frequency in a direction to reduce the difference between f_s and f_0. Now the signal is in _____ range.	lock-in
The VCO continues to change the frequency till its output frequency is _____the input signal frequency.	less than
The range of frequencies over which the PLL can maintain the lock with the incoming signal is called _____ range.	tracking
The range of frequencies over which the PLL can acquire the lock with the incoming signal is called _____ range	tracking
The output frequency of Voltage Controlled Oscillator f_0 is _____	$(V_{cc}-v_c)/(R_T*C_T*V_{cc})$
Voltage Controlled Oscillator is otherwise called as _____.	voltage to frequency converter
In PLL, the high frequency component (f_s+f_0) is removed by_____	high pass filter
Which of the following are the stages of PLL? i) free running ii) capture iii) tracking iv) pull in	only i and ii
Which of the following are the problems associated with the switch type phase detector? i) since the output voltage Ve is directly proportional to Vs, the phase detector gain and loop gain becomes dependent on the input signal amplitude. ii) output is proportional to cosΦ which makes it non linear. iii) the circuit becomes unstable iv) full wave detector	i and ii
In switch type phase detector, at the locked state ($f_s = f_0$) the phase shift should be _____ in order to get zero error signal.	0^o
In balanced modulator type phase detector, the transistors act as _____.	switch
In balanced modulator type phase detector, the phase angle to voltage transfer co-efficient KΦ is _____	$(I_Q*R_L)/$ pi

In digital type phase detector, the phase angle to voltage transfer co-efficient KΦ is _____	V_{CC}/(2*pi)
In EX-OR type digital phase detector, the maximum dc output voltage occurs when the phase difference is _____ degrees.	0
The EX-OR type phase detector is used only when the input waves are _____.	square and sine
The output wave of Voltage Controlled Oscillator is _____.	square, triangular
The Voltage to Frequency conversion factor of VCO is _____.	f_0 / V_{CC}
The output from a Phase Locked Loop system is _____.	voltage or frequency
If a divide by N - network is inserted between VCO output and phase comparator input of PLL, then in the locked state f0 is _____.	f_s /N
When PLL is used as AM demodulator, the AM signal is shifted in phase by _____ before being fed to the multiplier.	0º
The other name for capture range is _____ range.	tracking
The other name for lock in range is _____ range.	tracking
The range of modulating input voltage applied to a VCO is _____.	0.5 V_{CC} to V_{CC}
Lock in range of a PLL is _____ the capture range.	greater than
Which of the following is the drawback of variable transconductance multiplier?	inaccurate
The time taken for a PLL to capture the incoming signal is called _____ time.	pull out
If the voltage at the modulation input of VCo is biased at 7/8 Vcc then the output frequency of VCO in PLL is given by f0 = _____.	0.25/ (R_T*C_T)
The maximum operated range of PLL 565 is_____.	0 to 500 kHz
The Lock in range of Phase Locked Loop is _____.	Δ f_L = 7.8 f_0/v
If the offset frequency f_1 is applied to the phase detector of frequency translator circuit, then at the locked state f0 is given by _____.	fs
_____ filter controls the capture range and lock in range of PLL.	high pass filter
The operating voltage range of IC 565 is _____.	+/- 6V to +/-12V
An external capacitor connected across IC 565 will act as _____.	passive device

If V_c shifts the VCO frequency from the free running frequency f_0 to a frequency f, then the new frequency shift from VCO in a PLL is _____.	$f_0 + k_v*Vc$
A _____ is an electronic system which generates any range of frequencies from a single fixed time base or oscillator.	frequency multiplier
Phase detector is basically a _____.	summer
In PLL, the output of the error amplifier is equal to the _____.	error voltage
Select correct statement of PLL.	capture range is smaller than lock in range
The following gate can be used as phase detector.	NAND
The output of divider circuit with input signals V_x as divisor and V_y as dividend using opamp ____.	$V_o= (V_{ref}*V_y)/V_x$
If $V_x=V_x*\sin wt$, $V_y= V_y*\sin(wt+\theta)$ are the inputs to the four quadrant Multiplier, then the output voltage is _____.	V_x*V_y
The Voltage to Frequency Converter of VCO is defined as ____	$\Delta V_c / \Delta f_0$
IC 566 functions as_____.	phase detector
The total time taken by PLL to establish the lock is called _____.	pull in time
If the frequency of the carrier wave is varied in accordance with the modulating signal, then the modulation refers to _____ modulation	frequency shift keying
The capture range of PLL is defined as _____.	$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C*(3.6*10\text{^}3))\}^{1/2}$
The lock in range of PLL is defined as _____.	$\Delta f_L = +/- (K_v*K_\Phi)$
Which of the following is the drawback of variable transconductance multiplier?	inaccurate
The basic blocks in Voltage Controlled Oscillator are _____	constant current source, buffer, astable multivibrator, inverter
The pulsewidth T of IC 555 as a monostable multivibrator is _____.	$RC* \ln(V_{cc}/(V_{cc} -V_{TH})$
A single 555 timer can provide time delay ranging from _____.	microseconds to minutes
The pulse width of monostable Multivibrator using 555 timer is _____.	0.693 *RC
IC 555 Timer is used in astable mode. The total time taken by the capacitor to charge and discharge is _____.	$T= 1.1*(2R_A+R_B)*C$
Which of the following are the applications of Monostable Multivibrator using 555 timer? i) missing pulse detector ii) pulse position modulator iii) pulse width modulator iv) frequency divider.	only ii

. For R_A =6.8k ohm, R_B = 3.3kohm and C=0.1microfarad, Calculate t_{HIGH} of astable multivibrator using 555 timer.	0.23ms
Which of the following are the applications of astable Multivibrator using 555 timer? i) missing pulse detector ii) pulse position modulator iii) pulse width modulator iv) FSK Generator	only ii
Match the following. i) pulse position modulator - A) Monostable Multivibrator ii) pulse width modulator - B) Class A iii) full cycle amplification - C) Class B iv) half cycle amplification - D) astable Multivibrator	i-D, ii-A, iii-B, iv-C
Which of the following is the application of astable multivibrator using 555 timer?	pulse position modulation
The duty cycle D of astable operation using 555 timer is defined as _____.	$R_B*(R_A+R_B)$
The efficiency of switching regulators compared to series voltage regulators is _____.	high
. Which of the following is one-shot application of IC 555 timer?	frequency divider
Which of the following are the operating modes of 555 timer? i) free running operation ii) one-shot operation. iii) bistable operation	only I
The value of output voltage of IC 555 timer in the off state is _____.	0V
When IC 555 timer is operated as one shot multivibrator, the output switches high due to _____.	negative going trigger pulse to the timer
The lower threshold voltage VLT and upper threshold voltage VUT for IC 555 timer is _____.	Vcc/3, 2Vcc/3
Thigh and Tlow for astable mode multivibrator of IC 555 are _____.	$t_{high} = 0.69(R_A+R_B)*C$, $t_{low} = 0.69(R_A+2R_B)*C$
When $R_A = R_B$ in IC 555 timer circuit, then the total time for output waveform T= $0.69(R_A + R_B)*C$. Duty cycle for the circuit is _____.	80%

If R_A =10k, C=0.1microfarad, calculate the timing interval for IC 555 monostable operation.	2 millisecond
The frequency of oscillation of astable multivibrator using IC 555 timer is _____.	$1.45 / ((R_A+2R_B)*C)$

Op2	Op3
Error Amplifier	Voltage Controlled Oscillator
free running multivibrator	monostable multivibrator
phase	frequency
subtractor	multiplier
f_s-f_0	f_s*f_0
capture	free running
exactly the same as	greater than
capture	free running
capture	free running
v_c /(R_T*C_T*V_{cc})	2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})
voltage to time converter	voltage to current converter
low pass filter	band pass filter
only ii and iv	i, ii and iii
i,ii and iii	ii,iii
180º	270º
amplifier	oscillator
V_0/(2*pi)	(4*I_Q*R_L)/pi

V_{CC}/(pi)	V_0/(2*pi)
90	180
square and cosine	square and triangular
square	triangular
$8*f_0 / V_{CC}$	$2*f_0 / V_{CC}$
only voltage	only frequency
$N*f_s$	f_s+N
180º	270º
lock in	free running
acquisition	free running
0.75 V_{CC} to V_{CC}	0 V_{CC} to V_{CC}
equal to	lesser than
costly	difficult to integrate in IC
capture	lock in
$(R_T*C_T)/4$	$4(R_T*C_T)$
0.001 to 500 kHz	100 to 400 kHz
$\Delta f_L = +/- (7.8 f_0/v)$	$\Delta f_L = +/- (8.7 f_0/v)$
fs * f_1	fs + f_1
low pass filter	band pass filter
+/- 10V to +/-12V	+/- 8V to +/-12V
low pass filter	charging device

$f_0 - k_v*Vc$	k_v*Vc
frequency synthesizer	frequency doubler
subtractor	multiplier
applied voltage	control voltage
capture range is greater than lock in range	capture range is equal to lock in range
AND	EX-OR
$V_o = - (V_{ref}*V_y)/V_x$	$V_o = (V_y)/V_x$
$\{(V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}/Vref$	$\{V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}$
Δf_0	ΔV_c
low pass filter	VCO
pull out time	rise time
frequency	amplitude
$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C)\}^{1/2}$	$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C*(3.6*10\text{^}3))\}$
$\Delta f_L = +/- (K_v*K_\Phi*A$	$\Delta f_L = +/- (K_v*K_\Phi)/(A*(pi/2))$
costly	difficult to integrate in IC
constant current source, astable multivibrator, triangular wave generator, inverter.	constant current source, buffer, Schmitt trigger, inverter
$RC* \ln(Vcc - V_{TH}/(Vcc)$	$RC* \ln(Vcc - V_{TH})$
microseconds to milliseconds	microseconds to seconds
1.1*RC	0.3*RC
$T= 0.69*(R_A+R*C)$	$T= 0.69*(R_A+2R_B)*C$
a) i, iii and iv	i and ii only

0.7ms	0.5ms
ii and iii only	ii and iv only
i-D, ii-A, iii-C, iv-B	i-A, ii-D, iii-B, iv-C
pulse width modulation	) pulse code modulation
c) $R_B / (R_A+2R_B)$	$R_B / (1+R_B)$
low	same
pulse position modulator	FSK generator
only i and ii	i,ii and iii
0.1V	1V
positive going trigger pulse to the timer	positive voltage
2Vcc/3, Vcc/3	Vcc, 2Vcc/3
$t_{high} = 0.69(R_A)*C$, $t_{low}=$ 0.69(R*C	$t_{high} = 0.69(R_A+R_B)*C$, $t_{low}= 0.69(R_B)*C$
50%	25%

1.1 millisecond	2.2 millisecond
$1.45((R_A+2R_B)*C)$	$((R_A+2R_B)*C)/ 1.45$

Op4	Op5
Phase Detector	
phase shift oscillator	
amplitude	
divider	
f_s+/ f_0	
unlocked	
twice that of	
pull in	
pull in	
$1/(R_T*C_T)$	
frequency to voltage converter	
band reject filter	
only iv	
only i	
90^o	
modulator	
$(I_Q*R_L)/2*pi$	

V_0/(pi)	
360	
square.	
sine	
$4*f_0 / V_{CC}$	
only phase.	
f_s –N	
90º	
acquisition	
capture	
0.25 V_{CC} to V_{CC}	
less than or equal to	
scale factor depends on temperature which affects the output	
pull in	
$(R_T*C_T)/0.25$	
10 to 400 kHz	
$\Delta f_L = 8.7 f_0/v$	
fs - f_1	
band reject filter	
+/- 12V	
discharging device	

Vc	
frequncy translator	
divider	
power supply voltage	
capture range is not equal to lock in range	
OR	
$V_o = V_{ref}/(V_x * V_y)$	
$(V_x * \sin * (wt+\theta)) * V_y$	
$\Delta f_0/\Delta V_c$	
PLL	
hold time	
phase	
$\Delta fc = +/- \{(\Delta f_L)/ (2*pi*C)\}$	
$\Delta f_L = +/- (K_v * K_\Phi * A * (pi/2))$	
scale factor depends on temperature which affects the output	
constant current source, buffer, Schmitt trigger	
$RC * \ln(V_{TH} - Vcc /(V_{TH})$	
microseconds to hours	
0.2*RC	
T= 1.1*RC	
only iv	

0.4ms	
i and ii only	
i-A, ii-D, iii-C, iv-B	
pulse amplitude modulation	
d) R_B / (1+R_B)	
halved	
FM demodulator	
only iii	
0.7V	
negative voltage	
Vcc, Vcc/3	
t_{high} = 0.69(R_B)*C, t_{low}= 0.69 (R_A+R_B)*C	
100%	

2.3 millisecond	
1.45/ $((R_A+R_B)*C)$	

Op6	Answer
	Phase Detector
	free running multivibrator
	phase and frequency
	multiplier
	f_s+/ f_0
	capture
	exactly the same as
	tracking
	capture
	$2*(V_{cc}-v_c)/(R_T*C_T*V_{cc})$
	voltage to frequency converter
	low pass filter
	i, ii and iii
	i and ii
	90º
	switch
	$(4*I_Q*R_L)/pi$

	V_{CC}/(pi)
	180
	square.
	square, triangular
	$8*f_0 / V_{CC}$
	voltage or frequency
	$N*f_s$
	90º
	acquisition
	tracking
	0.75 V_{CC} to V_{CC}
	greater than
	scale factor depends on temperature which affects the output
	capture
	$0.25/ (R_T*C_T)$
	0.001 to 500 kHz
	$\Delta f_L = +/- (7.8 f_0/v)$
	$fs + f_1$
	low pass filter
	+/- 6V to +/-12V
	low pass filter

	$f_0 + k_v*Vc$
	frequency synthesizer
	multiplier
	control voltage
	capture range is smaller than lock in range
	EX-OR
	$V_o = -(V_{ref}*V_y)/V_x$
	$\{(V_x*\sin wt)*(V_y*\sin*(wt+\theta))\}/Vref$
	$\Delta f_0/\Delta V_c$
	VCO
	pull in time
	frequency
	$\Delta fc = +/- \{(\Delta f_L)/(2*pi*C*(3.6*10\text{^}3))\}^{1/2}$
	$\Delta f_L = +/- (K_v*K_\Phi*A*(pi/2))$
	scale factor depends on temperature which affects the output
	constant current source, buffer, Schmitt trigger, inverter
	$RC*\ln(Vcc/(Vcc - V_{TH})$
	microseconds to hours
	1.1*RC
	$T = 0.69*(R_A+2R_B)*C$
	a) i, iii and iv

	0.7ms
	ii and iv only
	i-D, ii-A, iii-B, iv-C
	pulse position modulation
	R_B / (1+R_B)
	high
	frequency divider
	only i and ii
	0.1V
	negative going trigger pulse to the timer
	Vcc/3, 2Vcc/3
	$t_{high} = 0.69(R_A+R_B)*C$, $t_{low} = 0.69(R_B)*C$
	50%

	1.1 millisecond
	$1.45 / ((R_A+2R_B)*C)$

Questions
_____ is a highly stable device for generating accurate time delay or oscillation.
In the switched capacitor filter, the value of resistor is determined by _____.
For the given value of input voltage, if the time period is constant then the output voltage of switching regulator is _____.
A Regulated power supply provides a dc voltage independent of _____.) load current variations ii) temperature variations iii) load current and ac line voltage variations
_____ is defined as the change in the output voltage for a change in the load current.
The duty cycle of a switching regulator is
The output voltage of switching regulator is a function of _____.
The basic elements of switching regulators are _____.
To improve the efficiency of a switching regulator, which of the following device is used? .
The resonance frequency of the tuned circuit is _____.
The selectivity of tuned circuit is high when _____.
Video Amplifiers are called as wide band amplifiers because they have ____.
Small signal tuned amplifiers are operated in the mode of _____.
Tuned class-C amplifier are also called as _____.
In Class B tuned amplifier the efficiency increases linearly with the output amplitude V1 and it reaches its maximum when V1 is equal to _____.
The Class-B mode of operation means that the collector current flows in a transistor only for _____.
If the tuned amplifier bursts into oscillation instead of amplification then it is said to be _____.
The tuned amplifiers cannot be used at low frequency because _____.
The separation in Isolation amplifier is achieved by _____.
The large signal amplifiers are otherwise known as _____.
In which type of Power amplifier, the signal is amplified for full cycle?
Which of the following power amplifier has high efficiency?
Which of the following power amplifier is never used in audio amplifiers?
The output is obtained for more than 180° but less than 360° in _____.
Which of the following are the important sections of a voltage regulator IC?) reference voltage circuit ii) error amplifier iii) series pass transistor

The output voltage of linear regulator using op-amp is _____.
The name linear regulator is due to _____.
A voltage regulator is a circuit that provides _____.
Which of the following IC is a variable voltage regulator IC?
The fold back current limiting is employed in a _____.
Switching regulator has advantage over series regulator because of _____.
Which of the following is the limitation of a three terminal regulator?
Which of the following statement is incorrect?
The IC regulators use reference voltage source, error op-amp and pass transistor with _____. i) short-circuit current limiting ii) current foldback iii) thermal overload protection
A duty cycle of 50% (half the frequency) of timer will give _____.
The pass transistor used in regulators has switching frequency
In switching regulator, the series pass transistor is switched
In the voltage regulators, if the output is shorted or load current exceeds the set value, then the current through the series transistor _____.
Which of the following are the limitations of IC 723?
The constant output voltage and current from IC regulator is due to ____.

Op1	Op2	Op3
555 timer	VCO	Voltage to Time converter
$R = 1/(C*f_{clk})$	$R= Vin/I_{avg}$	$R= 1/(C*T_{clk})$
directly proportional to OFF time	directly proportional to ON time	inversely proportional to OFF time
only I	only i and ii	only iii
line regulation	load regulation	input regulation
t_{on} / f_s	$t_{off} * f_s$	$t_{on} / (t_{on} + t_{off})$
input voltage and frequency	ON and OFF time	On time and input voltage
switch, pulse generator, voltage source and filter	control element and voltage source	switch, pulse generator and control element
step-up transformer	series pass transistor	variable resistor
1/((2*pi*(sqrt(RC))	1/((2*pi*(sqrt(LC))	1/((2*pi*(sqrt(RL))
bandwidth is high	bandwidth is small	resonant frequency is high
high selectivity	small bandwidth	bandwidth from dc to high frequency
Class A	Class B	Class C
small signal tuned amplifiers	large signal tuned amplifiers	linear circuit amplifiers
Vcc	2*Vcc	Vcc/2
half the period of ac input cycle	one fourth of the period of ac input cycle	full period of ac input cycle
oscillator	open circuit	short circuit
the required gain is low	the size of L and C are large	the size of L and C are small
transistor	transformer	SCR
tuned amplifiers	voltage amplifiers	current amplifiers
Class B	Class A	Class C
Class B	Class A	Class C
Class B	Class A	Class C
Class B	Class A	Class C
only i and ii	i,ii and iii	only ii and iii

$V_0 = \{1+(R_2/R_1)\} * V_{ref}$	$V_0 = -\{1+(R_2/R_1)\} * V_{ref}$	$V_0 = -(R_2/R_1) * V_{ref}$
transistor in regulator conducts in cut-off region	transistor in regulator conducts in linear region	transistor conduction in cut-off and saturation region
stable dc voltage	stable dc voltage independent of load current	stable ac voltage
IC 723	LM 320	LM 340
low voltage current regulator circuits	high voltage current regulator circuits	low current voltage regulator circuits
improved efficiency	improved efficiency and high switching frequency	high switching frequency
no short-circuit protection	output voltage is fixed	no short-circuit protection and output voltage is fixed
switching regulators use switching speed of 20kHz and above	The output voltage of a switching regulator is controlled by altering the switching	both Bipolar transistors and FETs have very good switching characteristics
only I	only ii	i and iii
rectangular waveform	square waveform	sawtooth waveform
Below 20 kHz	20 kHz	Above 20 kHz
in saturation region	in active region	between active and saturation region
increases	folds back	remains same
no Short circuit protection	no in-built thermal protection	no Short circuit protection and no in-built thermal protection
constant current source	reference amplifier	constant current source and reference amplifier

Op4	Op5	Op6
Voltage to Frequency converter		
R= V_{sense}/I_{limit}		
inversely proportional to ON time		
only iv		
ripple rejection		
$t_{off}/ (t_{on} + t_{off})$		
input voltage and duty cycle		
control element and switch		
variable inductor.		
(2*pi*(sqrt(RC))		
resonant frequency is low		
bandwidth from zero to infinity		
Class AB		
stagger tuned amplifiers		
infinity		
dc input		
unstable		
the required bandwidth is high		
inverter		
power amplifiers		
Class AB		
Class AB		
Class AB		
Class AB		
nly i and iii		

$V_0 = (R_2/R_1) * V_{ref}$		
transistor conduction in saturation region		
stable ac voltage with no load current variations		
IC7805		
high current voltage regulator circuits		
less number of components needed		
more number of components needed		
switching regulator is that their power consumption is very low		
only iii		
ramp waveform		
10 kHz		
between cutoff and saturation		
gets doubled		
output voltage is fixed		
constant voltage source		

Answer
555 timer
$R = 1/(C*f_{clk})$
directly proportional to ON time
only iv
load regulation
$t_{on} / (t_{on} + t_{off})$
input voltage and duty cycle
switch, pulse generator, voltage source and filter
series pass transistor
1/((2*pi*(sqrt(LC))
bandwidth is small
bandwidth from dc to high frequency
Class A
large signal tuned amplifiers
Vcc/2
half the period of ac input cycle
unstable
the size of L and C are large
transformer
power amplifiers
Class A
Class C
Class C
Class AB
i,ii and iii

$V_0 = \{1+(R_2/R_1)\} * V_{ref}$
transistor in regulator conducts in linear region
stable dc voltage independent of load current
IC 723
high current voltage regulator circuits
improved efficiency and high switching frequency
no short-circuit protection and output voltage is fixed
The output voltage of a switching regulator is controlled by altering the switching frequency
i and iii
square waveform
Above 20 kHz
between cutoff and saturation
folds back
no Short circuit protection and no in-built thermal protection
constant current source and reference amplifier

Questions
JFET is used as an analog switch. If V_{GS} is less than or equal to V_{GS} (OFF), JFET operates in _____ region and it acts as _____ switch.
Which of the following are the drawbacks in weighted resistor DAC? i) wide range of resistors are required. ii) for better resolution the binary word length has to be increased. The fabrication of large resistance in IC is impractical. iii) voltage across the resistor due to bias current will affect the accuracy.
What is the drawback of R-2R ladder type DAC?
The time required for the conversion of analog signal into a digital equivalent is called _____ time.
Which of the following is the fastest ADC?
Which of the following are the advantages of R-2R ladder DAC? i) easier to build accurately as only resistors of two values are required. ii) number of bits can be expanded by adding more sections of R-2R values. iii) conversion time is less
Which of the following are the drawbacks of flash type ADC? i) slowest ADC ii) number of comparator almost doubles for each added bit iii) most expensive iv) for larger value of bits, more complex is the priority encoder
Which of the following is a direct type ADC?
JFET is used as an analog switch. If V_{GS} = 0v,JFET operates in _____ region and it acts as _____ switch.
10. The other name for flash type comparator is _____comparator ADC.
Which of the following is integrating type ADC?
The conversion time for flash type converter is in the order of _____.
The number of comparators required for a 3-bit flash type ADC is _____.
Which of the following ADC uses trial and error method to find the digital output?
In successive approximation ADC, with the arrival of START command, the SAR register sets _____.
ADC and DAC are otherwise called as _____.
Digital to Analog conversion can be done by _____.
The only two values of resistor required for DAC is _____.

The main disadvantage of binary weighted resistor method is _____
The R-2R ladder DAC has a drawback of _____.
ADC can be classified as _____.
The resolution of DAC for 8-bit length is _____. i) 8-bit resolution ii) resolution of 0.392 of full scale iii) resolution of 1 part in 255
The property of DAC in which analog output increases with digital input is called _____.
The linearity error of DAC should be _____.
The accuracy of Data converters can be specified in _____.
Which of the following components are required by DAC? i) resistors ii) op-amp iii) electronic switches
ADC 0800/0801/0802 is _____.
The amount by which the actual output of a DAC differs from the ideal straight line characteristics is _____
Which of the following ADC is low speed ADC?
JFET is used as a shunt switch. When V_{GS}=0, JFET acts as _____ switch and the output V0= _____.
For D/A converter, analog output voltage for MSB is _____.
The Sample and Hold circuit is not needed for _____ ADC.
The main drawback of dual slope ADC is _____
The advantage of dual slope ADC is _____.
A V/F Converter circuit is used in _____.
_____ of ADC gives error when an analog signal changes rapidly.
For D/A converter, analog output voltage for LSB is _____.
The conversion time of 10-bit successive approximation A/D converter is ____, if the input clock is 5MHz.
The smallest possible change in the analog output voltage is referred to as _____.

The time required for the holding capacitor C to charge upto a level close to the input voltage during sampling is _____
_____ indicates how close the analog output voltage is to its theoretical value.
The non- zero level of analog output when all the digital inputs are zero is called _____.
To obtain close approximation of input waveform, the sampling frequency should be atleast _____ that of the input frequency.
What would be the output voltage produced by a D/A Converter, if output range is 0 to 10V and binary number is 102 (2 bit DAC)?
The input stage of any data acquisition system will be _____.
The total number of clock pulses required for 8-bit successive approximation ADC is _____.
What is the expression for analog voltage Va of dual slope ADC? (N=digital count, V_R= reference voltage)
The maximum deviation between actual converter output and ideal converter output is _____
The maximum deviation between actual converter output and ideal converter output after gain and offset errors have been removed is _____
The main drawback of single slope ADC is _____.
_____ ADC is suitable for accurate measurement of slowly varying signals such as thermocouples.
An analog voltage can be converted into digital form by producing pulses whose frequency is proportional to analog voltage _____.
The converter that converts an analog input signal into a linear function of time or frequency and then to a digital code is _____
Which of the following electronic switches are used in DAC? i) SPDT ii) totem pole MOSFET switches iii) CMOS inverter switch
What is the main difference between n-JFET and n-MOSFET when V_{GS}=0?

In ADC, the control line used to indicate the start and end of conversion is _____
Match the following. i) R-2R ladder type - A) fastest ADC ii) successive approximation - B) current flow through the resistor is not constant iii) inverted R-2R type - C) slowest ADC iv) flash type - D) current flow through the resistor is constant
In dual slope ADC, the unknown voltage and the reference voltages are converted into an equivalent _____using an integrator.
DAC 0800/0801/0802 is _____.
Inverted R-2R ladder DAC works on the principle of _____.

Op1	Op2
cut-off, closed	cut-off, open
i only	i, ii and iii
current is not constant in all branches	The fabrication of large resistance in IC is impractical.
aperture	acquisition
flash	successive approximation
only I	only i and ii
only I	only iv
successive approximation	single slope
cut-off, closed	cut-off, open
successive approximation	single slope
successive approximation	single slope
nanosecond	millisecond
3	6
successive approximation	single slope
LSB = 1 and all other bits to 0	MSB = 0 and all other bits to 1
amplifiers	data converters
weighted resistor method	successive approximation method
weighted resistor method	binary weighted method

word length of binary word is small	temperature variations
direct type, comparator type	indirect type, comparator type
only i	only i and ii
linearity	stability
+/- (1/2) LSB	+/- (1/2) MSB
LSB level	MSB level
only i and ii	i,ii and iii
1 bit ADC	2 bit ADC
offset error	linearity error
successive approximation	parallel comparator
open, zero	open, Vin
$V_0= (2^{N-1}) V_R / 2^N-1$	$V_0= (2^N) V_R / 2^N-1$
direct type	counter type
high cost	a) comparator and ADC are needed
long conversion time	excellent noise rejection
charge balancing ADC	dual slope ADC
direct type	counter type
$V_0= (2^{N-1}) V_R / 2^N-1$	$V_0= (2^N) V_R / 2^N-1$
1 microsec	2 microsec
accuracy	resolution

aperture time	acquisition time
accuracy	resolution
offset error	linearity error
same as	twice
3.75V	4V
DAC	Sample and Hold circuit
4	2
Va = $V_R (N+1)/ 2^n$	Va = $V_R (2^n)/ N$
monotonicity	relative accuracy
monotonicity	relative accuracy
resolution is less	comparator and ADC are needed
successive approximation	parallel comparator
ADC	VCO
counter type ADC	direct type ADC
only i	only ii and iii
n-JFET is ON and n-MOSFET is OFF	n-JFET is OFF and n-MOSFET is ON

only EOC	only SOC
i-B , ii-C, iii-D, iv-A	i-B , ii-A, iii-D, iv-C
time period	frequency
1 bit DAC	2 bit DAC
summing currents	summing voltages

Op3	Op4	Op5
ohmic, closed	ohmic, open	
i,ii only	iii only	
) voltage across the resistor due to bias current will affect the accuracy.	conversion time is less.	
conversion	settling	
dual slope	single slope	
only iii	only i and iii	
only i,ii and iii	only ii and iv	
dual slope	delta sigma	
ohmic, closed	ohmic. Open	
dual slope	parallel	
parallel comparator	flash comparator	
microsecond	second	
8	4	
dual slope	parallel	
LSB = 1 and all other bits to 1	MSB = 1 and all other bits to 0	
rectifiers	clampers	
single slope method	dual slope method	
R-2R ladder method	multiplying type	

less resolutions	wide range of resistor values	
integrating type, comparator type	direct type, integrating type	
only i,ii and iii	only iii	
monotonocity	accuracy	
+/- LSB	+/- MSB	
Voltage increments	percentage of full scale voltage	
only ii and iii	only ii	
4 bit ADC	8 bit ADC	
gain error	accuracy error	
dual slope	charge balancing	
closed, Vin	closed, zero	
$V_0 = (2^{N-1}) V_R / 2^N$	$V_0 = (2^{N-1}) V_R$	
integrating type	tracking type	
b) long conversion time	poor noise rejection	
fastest in operation	slow varying in nature	
parallel comparator ADC	successive approximation ADC	
tracking type	integrating type	
$V_0 = (2^{N-1}) V_R / 2^N$	$V_0 = (2^{N-1}) V_R$	
3 microsec	4 microsec	
linearity	gain	

pull in time	hold time	
linearity	gain	
gain error	accuracy error	
less than	half	
5V	7V	
ADC	Voltage to Time Converter	
16	8	
$Va = V_R (N)/ 2^n$	$Va = V_R (2^n)/ N+1$	
resolution	absolute accuracy	
resolution	absolute accuracy	
long conversion time	poor noise rejection	
dual slope	charge balancing	
V to F converter	V to T converter	
comparator type ADC	integrating type ADC	
i,ii and iii	only i and ii	
n-JFET is ON and n-MOSFET is ON	n-JFET is OFF and n-MOSFET is OFF	

either SOC or EOC	both SOC and EOC	
i-D , ii-A, iii-B, iv-C	i-D , ii-C, iii-B, iv-A	
current	digital	
8 bit DAC	4 bit DAC	
same currents in all ladders	difference currents	

Op6	Answer
	cut-off, open
	i, ii and iii
	current is not constant in all branches
	conversion
	flash
	only i and ii
	only i,ii and iii
	successive approximation
	ohmic, closed
	parallel
	single slope
	nanosecond
	8
	successive approximation
	MSB = 1 and all other bits to 0
	data converters
	weighted resistor method
	R-2R ladder method

	wide range of resistor values
	0
	direct type, integrating type
	only i,ii and iii
	monotonocity
	+/- (1/2) LSB
	percentage of full scale voltage
	only ii and iii
	8 bit ADC
	linearity error
	successive approximation
	closed, Vin
	$V_0 = (2^{N-1}) V_R / 2^N - 1$
	integrating type
	b) long conversion time
	excellent noise rejection
	charge balancing ADC
	integrating type
	$V_0 = (2^N) V_R / 2^N - 1$
	2 microsec
	resolution

	acquisition time
	accuracy
	offset error
	twice
	5V
	Sample and Hold circuit
	8
	Va = V_R (N)/ 2^n
	absolute accuracy
	relative accuracy
	resolution is less
	dual slope
	V to F converter
	integrating type ADC
	i,ii and iii
	n-JFET is ON and n-MOSFET is OFF

	both SOC and EOC
	i-B , ii-C, iii-D, iv-A
	time period
	8 bit DAC
	summing currents