15BEEC6E13 DIGITAL LOGIC DESIGN USING CPLD'S AND HDL 3 0 0 3 100

OBJECTIVES

- To describe the features of system-level design options
- To describe basic structures and features of cell -based ASICs, gate array ASICs , programmable logic devices (PLDs), field-programmable gate arrays (FPGAs), Complex PLD (CPLDs)
- To understand how to model combinational circuits and sequential circuits using PLDs, Complex PLDs
- To understand how to model combinational circuits and sequential circuits using VHDL

INTENDED OUTCOMES:

- Gain knowledge about the features of system-level design options
- Gain knowledge about the basic structures and features of cell-based ASICs, gate array ASICs, programmable logic devices (PLDs), field- programmable gate arrays (FPGAs), Complex PLD (CPLDs)
- Gain knowledge about how to model combinational circuits and sequential circuits using PLDs, Complex PLDs
- Gain knowledge about how to model combinational circuits and sequential circuits using VHDL

UNIT I ADVANCED T OPICS IN BOOLEAN ALGEBRA

Shannon's Expansion theorem and its application ,Consensus theorem, Reed Muller Expansion technique, Multiplexer logic as function generators, Implementation of Multiple output logic functions, Static and Dynamic hazards, Design of static hazard-free and dynamic hazard-free logic circuits.

UNIT II SEQUENTIAL CIRCUIT DESIGN

Mealy and Moore machines, clocked synchronous sequential circuit design procedure-state diagrams-state table-state reduction-state assignment, Incompletely Specified Sequential Machines.

UNIT III DESIGN WITH PROGRAMMABLE LOGIC DEVICES

Basic concepts, PROM as PLD, Programmable Array Logic (PAL),Programmable Logic Array (P LA), Design of combinational and sequential circuits using PLD's, Complex PLD (CPLD), Introduction to Field Programmable Gate Arrays (FPGA), Xilinx FPGAs-Xilinx 3000 series and 4000 series FPGA.

UNIT IV INTRODUCTION TO VHDL

VHDL Description of combination circuits, VHDL Modules- entity and architecture description, Sequential statements and VHDL processes, VHDL Data types and Operators, Concurrent and Sequential Assignment Statements(All types), Different types of Modeling in VHDL – Behavioral, dataflow and structural modeling, Variables, Signals and Constants in VHDL, Package in VHDL.

UNIT V DIGITAL DESIGN WITH VHDL

Combinational Circuit Design using Structural, behavioral and data flow modeling (Circuits like Arithmetic circuits, decoders, encoders, multiplexers, demultiplexers, code converters, 4-bit binary adders, BCD adder, comparator, ALU etc.,), Design of Sequential Elements, Registers, Counters and Synchronous Sequential Circuits using VHDL.

TEXT BOOKS:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
01	Charles. H. Roth, Jr	Digital Systems Design using VHDL	CENGAGE Learning, Third Indian Reprint	2012
02	Zwolinski	Digital System Design With VHDL	Pearson Education India	2004

REFERENCE

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ian Grout	Digital Systems Design with FPGAs and CP LDs	Newness	2011
2.	Brian Holdsworth and Clive Woods	Digital Logic Design	Elsevier	2008

Staff In-Charge **HOD/ECE**

http://www2.elo.utfsm.cl/~lsb/elo211/aplicaciones/katz/chapter3/chapter03.doc4.html hazard