ELECTRONIC CIRCUITS 3H-3C

Course Objectives

- To learn various biasing arrangements for BJT and FET
- To know about various high frequency models for BJT
- To learn various feedback configurations
- To study Op-amp configurations with its applications
- Design simple circuits using OPAMPs
- Gain knowledge on Data converters

Course Outcomes

At the end of this course students will demonstrate the ability to

- Understand the characteristics of transistors.
- Design and analyze high frequency models
- Design sinusoidal and non-sinusoidal oscillators
- Understand the functioning of OP-AMP and design OP-AMP based circuits.
- Design ADC and DAC

UNIT I BIASING CIRCUITS AND SMALL SIGNAL MODELS

Voltage amplifier, current amplifier, trans-conductance amplifier and trans-resistance amplifier. Biasing schemes for BJT and FET amplifiers, bias stability, various configurations (such as CE/CS, CB/CG, CC/CD) and their features, small signal analysis, low frequency transistor models, estimation of voltage gain, input resistance, output resistance etc., design procedure for particular specifications, low frequency analysis of multistage amplifiers.

UNIT II HIGH FREQUENCY MODELS

High frequency transistor models, frequency response of single stage and multistage amplifiers, cascode amplifier. Various classes of operation (Class A, B, AB, C etc.), their power efficiency and linearity issues.

UNIT III FEEDBACK AND OSCILLATOR CIRCUITS

Feedback topologies: Voltage series, current series, voltage shunt, current shunt, effect of feedback on gain, bandwidth etc., calculation with practical circuits, concept of stability, gain margin and phase margin. Review of the basic concept, Barkhausen criterion, RC oscillators(phase shift, Wien bridge etc.), LC oscillators (Hartley, Colpitt, Clapp etc.), non-sinusoidal oscillators. Current mirror: Basic topology and its variants, V-I characteristics, output resistance and minimum sustainable voltage (VON), maximum usable load.

UNIT IV OP-AMP AND ITS APPLICATIONS

Differential amplifier: Basic structure and principle of operation, calculation of differential gain, common mode gain, CMRR and ICMR. OPAMP design: design of differential amplifier for a given specification, design of gain stages and output stages, compensation. review of inverting and non-inverting amplifiers, integrator and differentiator, summing amplifier, precision rectifier, Schmitt trigger and its applications. Active filters: Low pass, high pass, band pass and band stop, design guidelines.

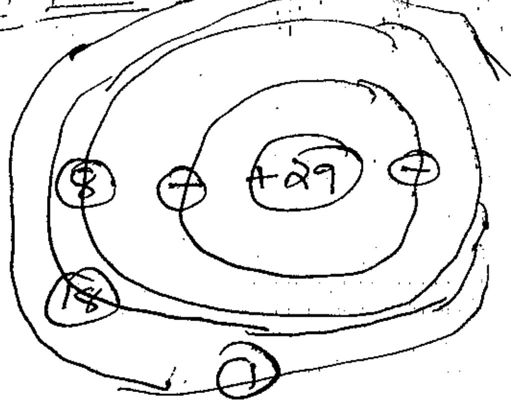
UNIT V DATA CONVERTORS

Digital-to-analog converters (DAC): Weighted resistor, R-2R ladder, resistor string etc. Analog-todigital converters (ADC): Single slope, dual slope, successive approximation, flash etc. Switched capacitor circuits: Basic concept, practical configurations, application in amplifier, integrator, ADC etc.

Suggested Readings

1. J.V. Wait, L.P. Huelsman and GA Korn, Introduction to Operational Amplifier theory and applications, McGraw Hill, 1992.
2. J. Millman and A. Grabel, Microelectronics, 2nd edition, McGraw Hill, 1988.
3. P. Horowitz and W. Hill, The Art of Electronics, 2nd edition, Cambridge University Press,1989.
4. A.S. Sedra and K.C. Smith, Microelectronic Circuits, Saunder's College11 Publishing, Edition IV
5. Paul R. Gray and Robert G.Meyer, Analysis and Design of Analog Integrated Circuits, John
   Wiley, 3rd Edition

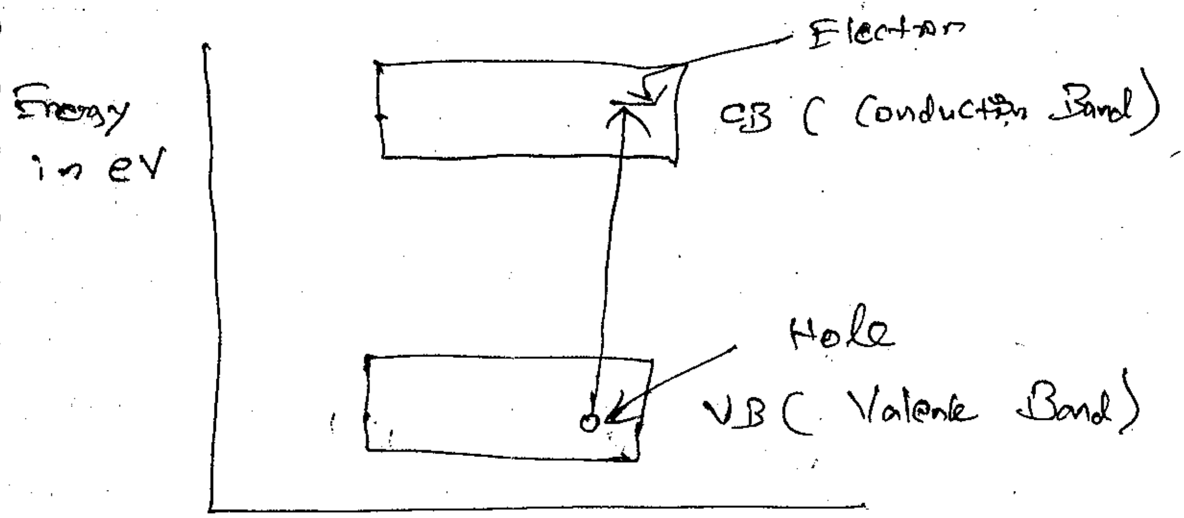
Copper atom



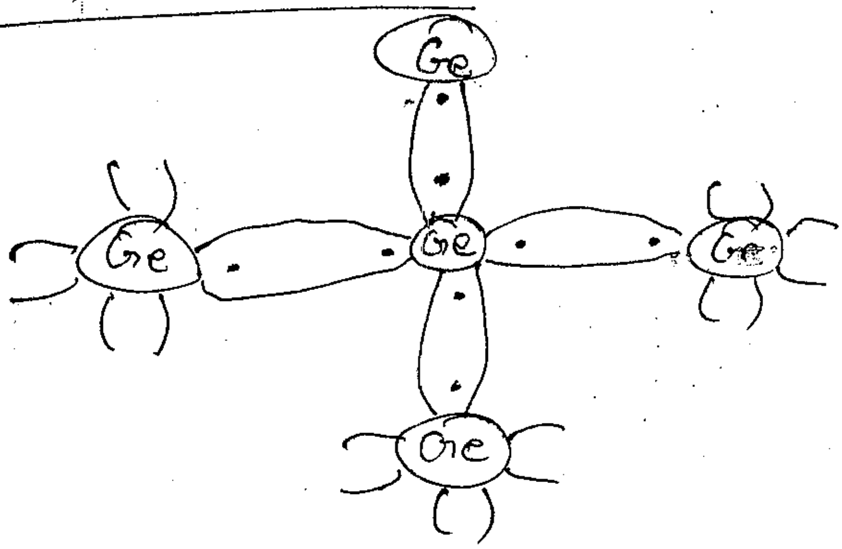
SEMICONDUCTOR

1. Intrinsic Semiconductor (Pure)
2. Extrinsic " (Impure).

Creation of electron-hole Pair in a Semiconductor

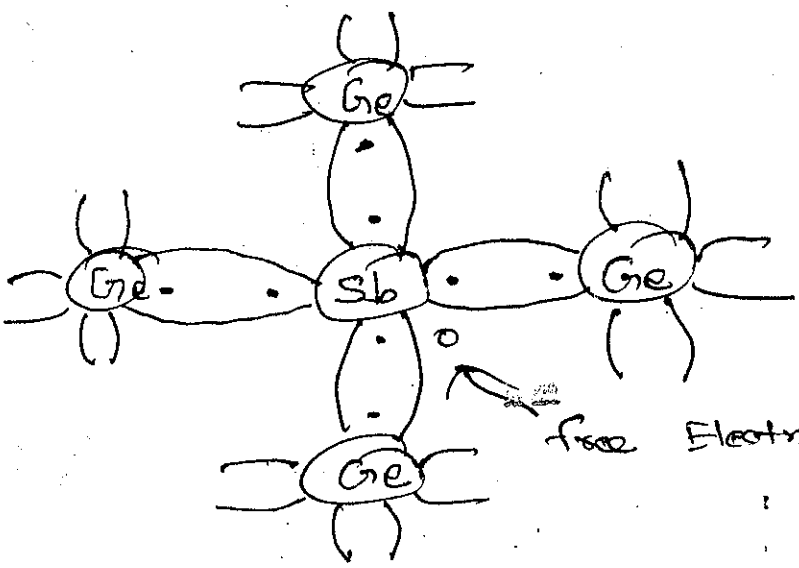


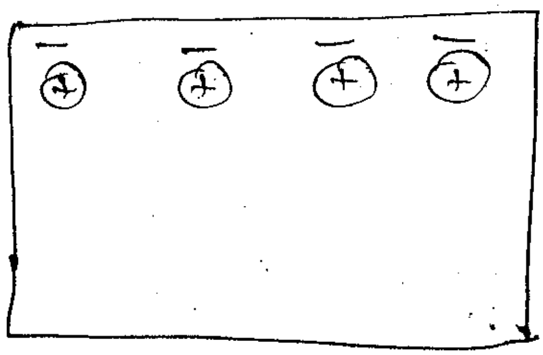
Intrinsic ~~n-type~~ Semiconductor (Pure Semiconductor)



N-type Semiconductor

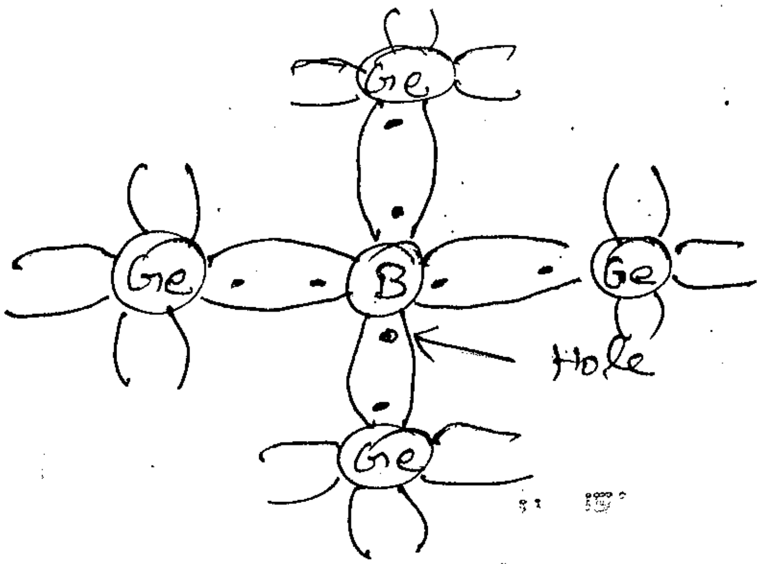
A small amount of pentavalent impurities such as arsenic, antimony (or) phosphorous is added to pure semiconductor, to get N-type semiconductor.





P-type Semiconductor

A small amount of trivalent impurities such as aluminium (or) boron is added to the pure semiconductor to get P-type semiconductor.



FORWARD BIAS

PN JUNCTION

A manufacturer can produce a single crystal with P-type material on one side and n-type on the other side as shown below.

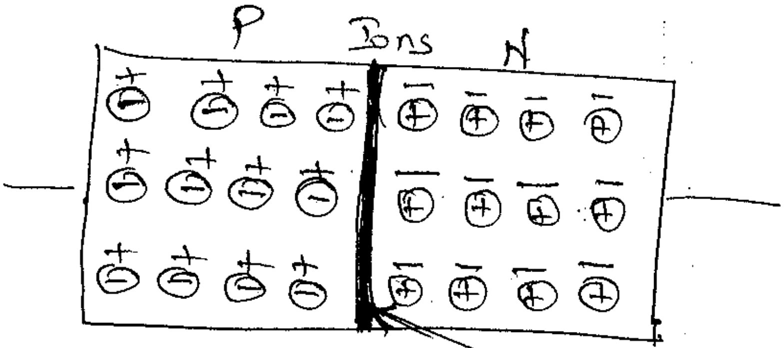
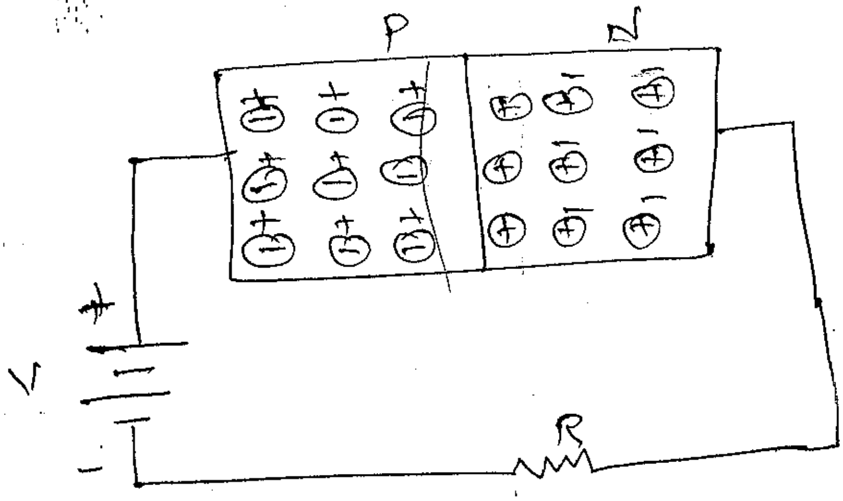
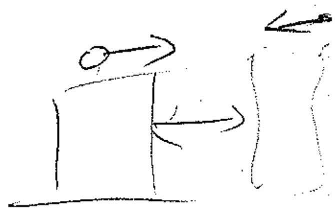


Fig. PN Junction → Depletion Layer

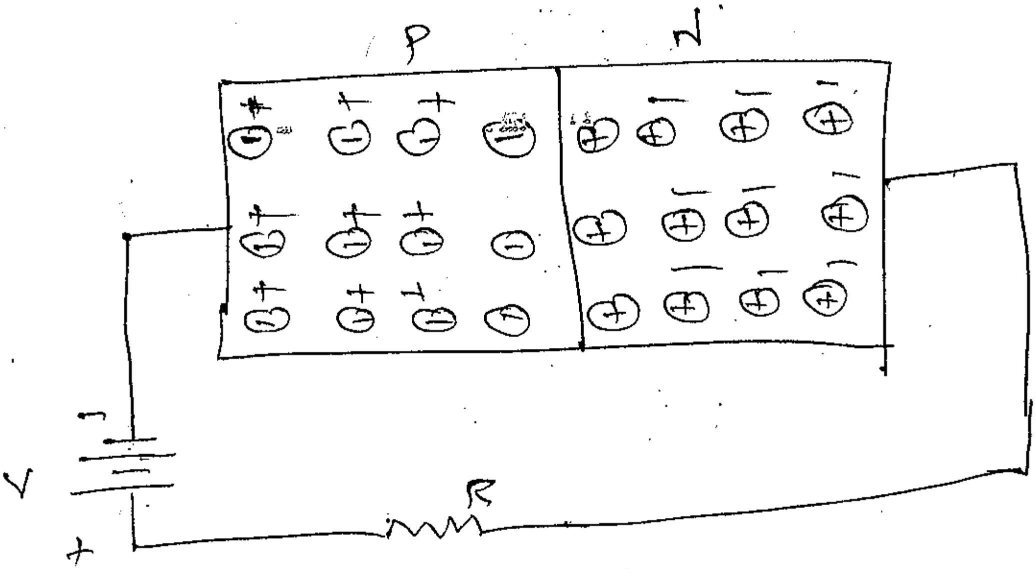
FORWARD BIAS

The negative source terminal is connected to the n-type material, and the positive terminal is connected to the p-type material. This connection produces what is called "Forward Bias".



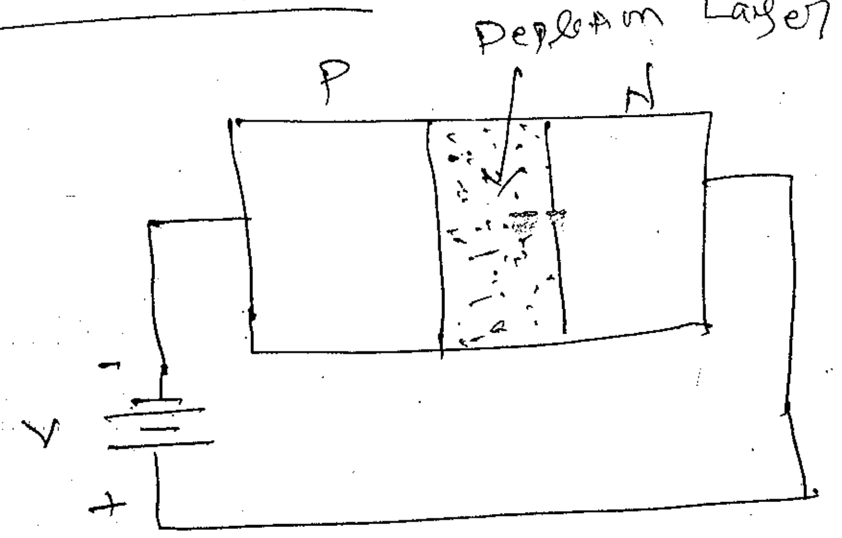


REVERSE BIAS



The negative battery terminal is connected to the p side, and the positive battery terminal to the n side. This connection produces what is called "Reverse Bias".

Depletion Layer



Saturation Current

The reverse current caused by the thermally produced minority carriers is called the "Saturation current."

Breakdown

The breakdown voltage of the most common type is greater than 50V.

DIODE

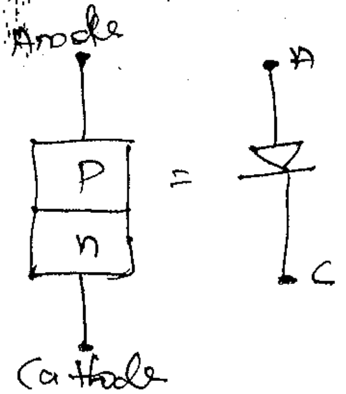
Basics

An ordinary resistor is a linear device because the graph of its current versus voltage is a straight line. A diode is a nonlinear device because the graph of its current versus voltage is not a straight line. The reason is barrier potential.

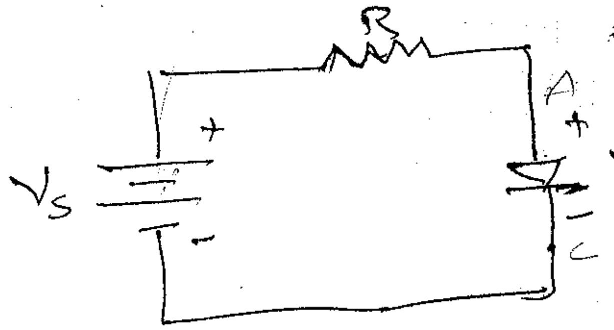
* when the diode Voltage < barrier potential, the diode current is Small.

* when the diode Voltage ≥ barrier potential the diode current increases rapidly.

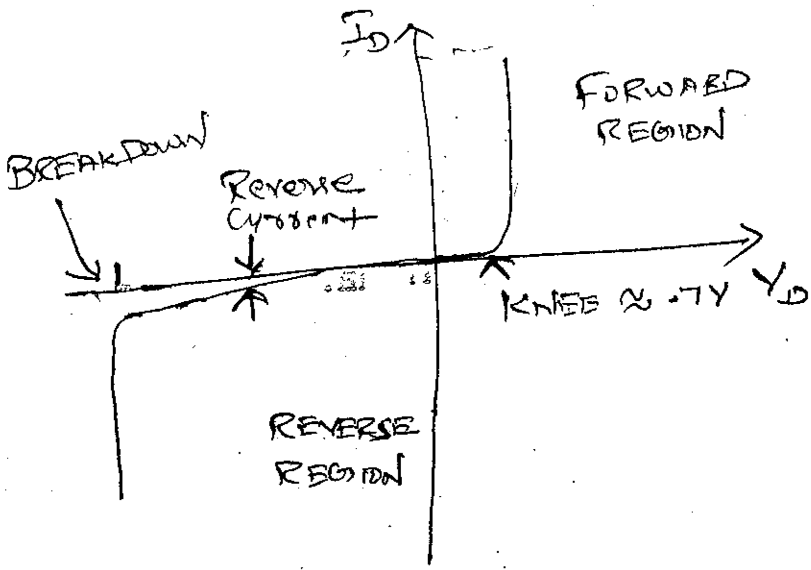
Symbol (Schematic)



Circuit



Diode Curve (IV)



KNEE Voltage

In the forward region, the voltage at which the current starts to increase rapidly is called the Knee voltage of diode.

For, germanium, its ≈ 0.3V & silicon ≈ 0.7V

Bulk Resistance

The sum of the ohmic resistances is called the bulk resistance. $R_B = R_P + R_N$

ohmic resistance is nothing but sum of P and n region resistance.

Maximum DC Forward current (I_{max})

The maximum forward current is one of the maximum ratings given on a data sheet. This current is ~~be~~ listed as I_{max}, $I_{F(max)}$, I_O.

Power Dissipation (P_D)

Power Dissipation,

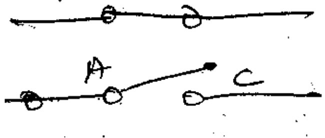
$$P_D = V_D I_D$$

The power rating is the maximum power the diode can safely dissipate without shortening its life or degrading its properties.

$$P_{max} = V_{max} I_{max}.$$

Ideal Diode

An ideal acts like a switch that closes when forward biased (conducts) and opens when reverse biased (Resists).



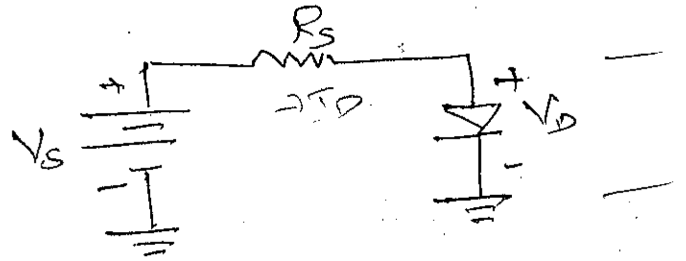
(Forward Bias)

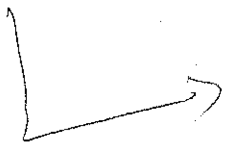
(Reverse ")

Load Lines

A tool used to find the exact value of diode current and voltage.

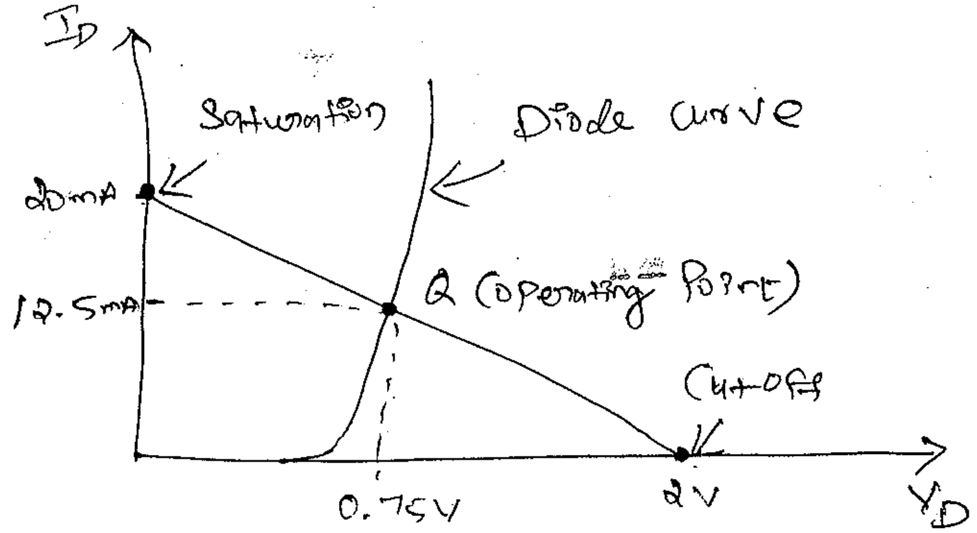
Load line eqn. $I_D = \dfrac{V_S - V_D}{R_S}$





Q Point

Below figure shows the load line and a diode curve. The point of intersection, known as the Q point, represents a simultaneous solution between the diode curve and the load line.



when, $V_D = 0$, diode reaches "Saturation Region"

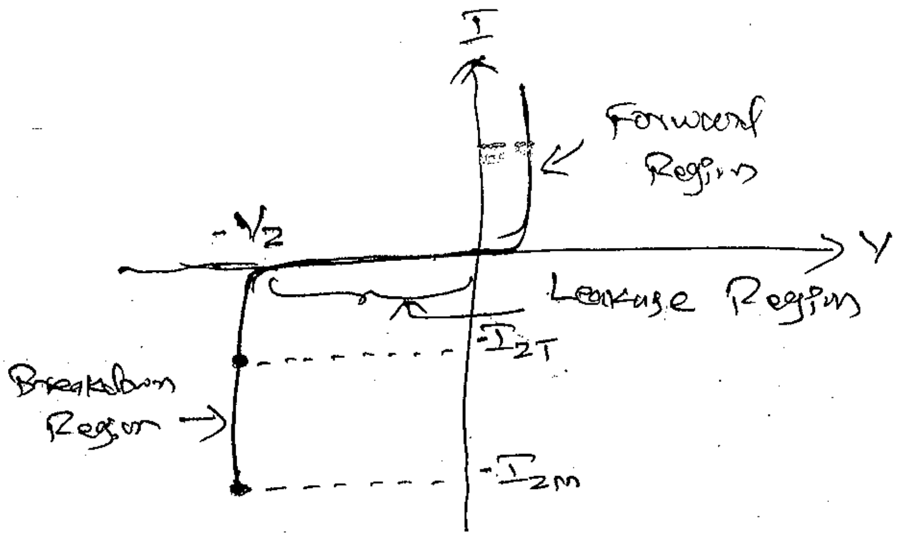
$I_D = 0$ " " " Cut off "

SPECIAL PURPOSE DIODES

Small signal and rectifier diodes are never intentionally operated in the breakdown region because this may damage them. A zener diode is a different. It's silicon diode that the manufacturer has optimized for operation in the breakdown region. The zener diode is the backbone of voltage regulators circuits that hold the load voltage almost constant despite large changes in line voltage and load resistance.

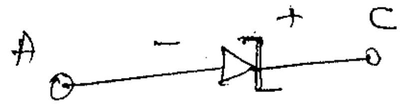
I-V Graph

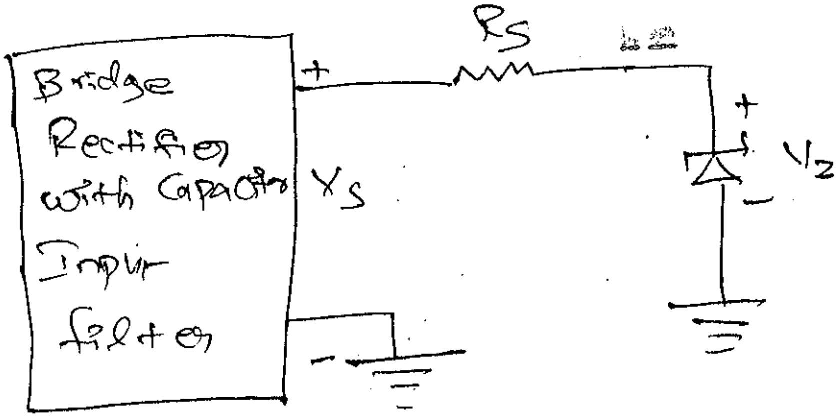
* Breakdown voltage from 2 to over 1000 V.



- I_{ZT} → Reverse Zener Test Current
- I_{ZM} → " " maximum " .

Symbol

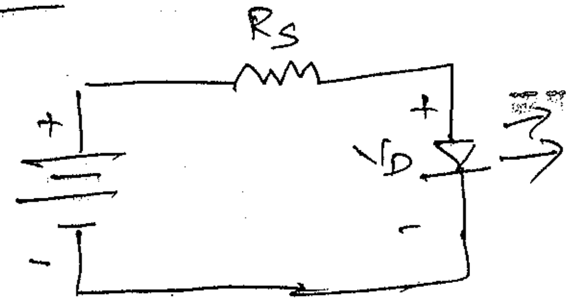




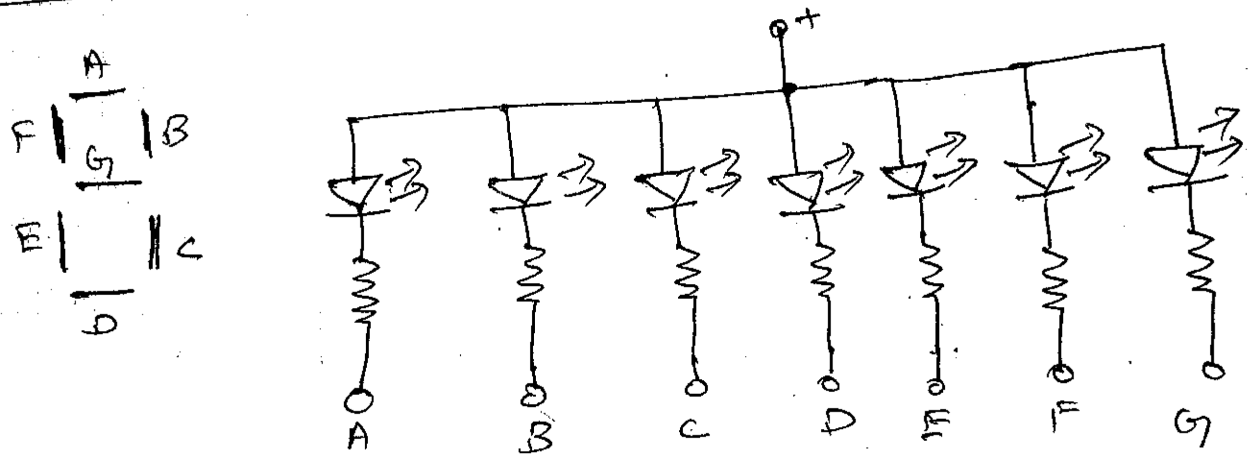
OPTOELECTRONIC DEVICES

Optoelectronics is the technology that combines optics and electronics. ~~this field~~ Examples: LED, photodiodes, opto couplers and laser diodes.

LED

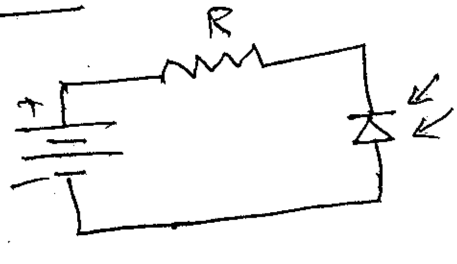


Seven - Segment Display

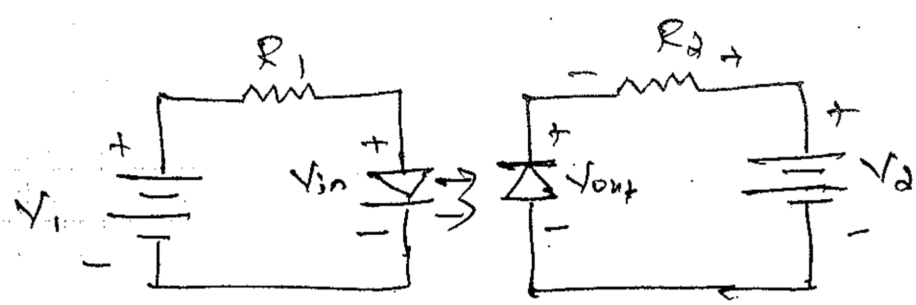


(Common Anode)

Photo diode

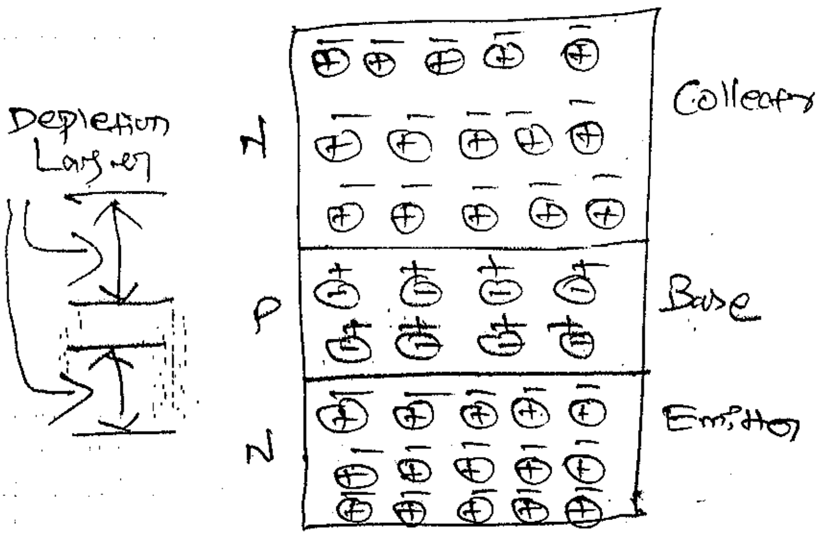


Opto Coupler



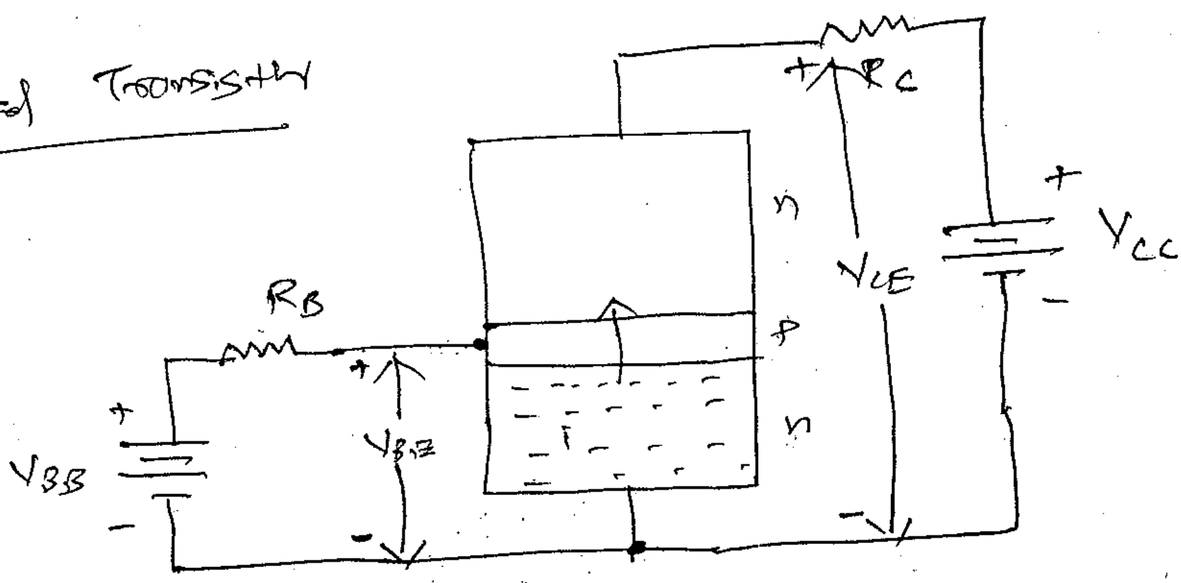
BIPOLAR JUNCTION TRANSISTOR

Unbiased Transistor



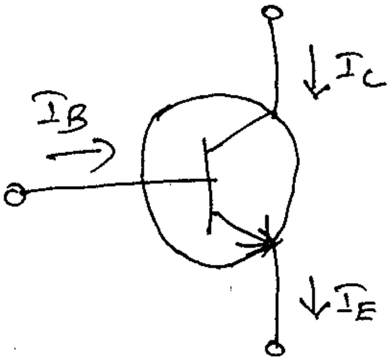
* Emitter heavily doped
* Base lightly ,,
* Collector intermediate between emitter & base.

Biased Transistor

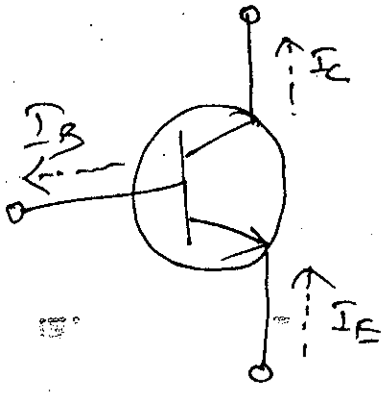


Transistor Currents

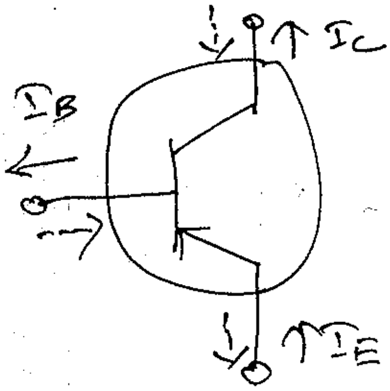
Below figure show the Schematic symbol for an npn transistor.



(a) Conventional Flow



(b) Electron Flow



(c) PNP Transistor.

$$I_E = I_C + I_B \longrightarrow (1)$$

Since the base current is much smaller than the collector current: $I_C \approx I_E$ $(I_B << I_C)$.

Alpha

The dc alpha (α_{dc}) is defined as the dc collector current divided by the dc emitter current:

$$\alpha_{dc} = \frac{I_C}{I_E} \longrightarrow (2)$$

* The dc alpha is slightly less than 1. In a low-power transistor the dc alpha is > .99 in a high-power transistor, the dc alpha is > 0.95

Beta

The dc beta (β_{dc}) of a transistor is defined as the ratio of dc collector current to the dc base current:

$$\beta_{dc} = \frac{I_C}{I_B} \longrightarrow (3)$$

The dc beta is known as 'current gain' because a small base current controls a much larger collector current.

* For low-power transistors (under 1W), β_{dc} is 100 to 300.
* For high-power transistors (over 1W), β_{dc} is 20 to 100.

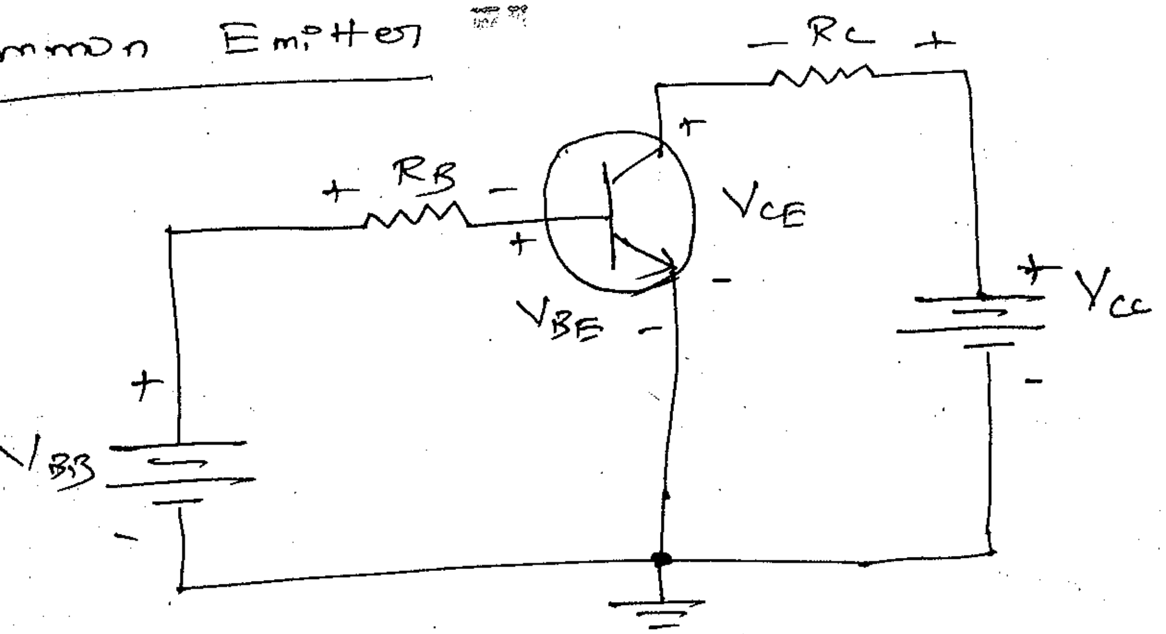
From eqn (3), $I_C = \beta_{dc} I_B$

$$I_B = \frac{I_C}{\beta_{dc}}$$

CE Connection

There are three useful ways to connect a transistor:
(i) CE (Common emitter)
(ii) CC (Common collector)
(iii) CB (Common Base).

Common Emitter



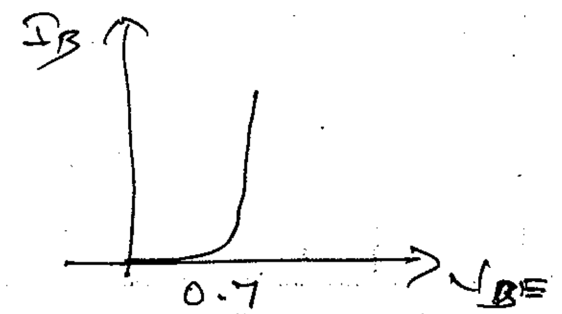
Double subscripts — V_{BB} & V_{CE}

Single " — $V_{CE} = V_C - V_E = V_C$

$V_{CB} = V_C - V_B$

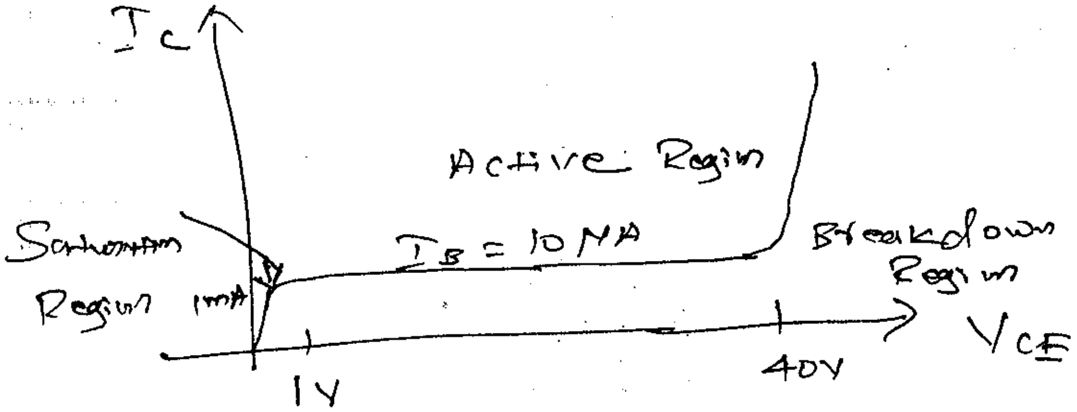
$V_{BE} = V_B - V_E = V_B$

The Base Curve



$$I_B = \frac{V_{BB} - V_{BB}}{R_B}$$

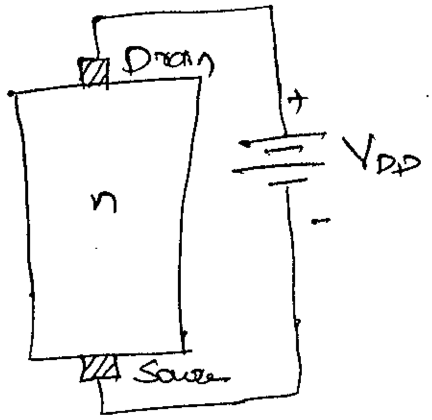
Collector Curve

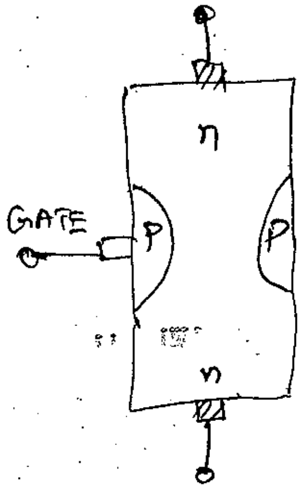


$$\beta_{dc} = \frac{I_c}{I_B} = \frac{1mA}{1\mu A} = 100.$$

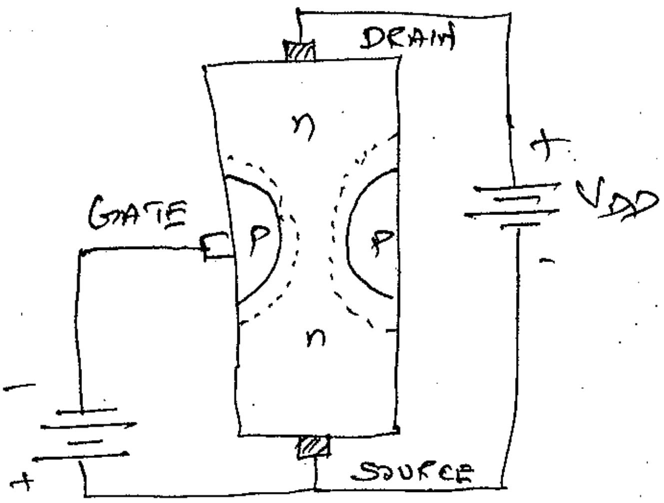
(gain)

JFET (Junction Field Effect Transistor)





The above figure shows a piece of n-type semiconductor. The lower end is called the source and the upper end is called the drain. A manufacturer diffuses two areas of P-type semiconductors into the n-type semiconductor, as shown in below figure. The P regions are connected internally to get a single external 'gate' lead.



This figure shows the normal biasing voltages for a JFET. The drain supply voltage is positive and the gate supply voltage is negative. The term field effect is related to the depletion layers around each P region.

* With JFET, we always reverse-bias the gate-source diode. Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.

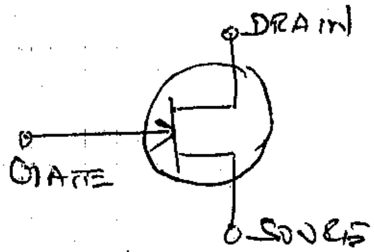
Gate Voltage Controls Drain Current

In the above figure, electrons flowing from the Source to drain must pass through the narrow chan between the depletion layers. when the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.

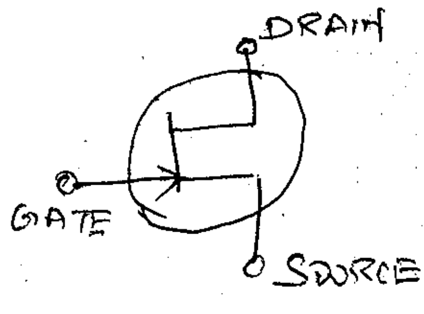
The JFET is a voltage-controlled device because an input voltage controls an output current.

* when $V_{GS} = 0$, maximum drain current flows through the JFET. (ON)
* when V_{GS} is negative enough (reverse bias), the depletion layers touch and the drain current is cut-off. (OFF)

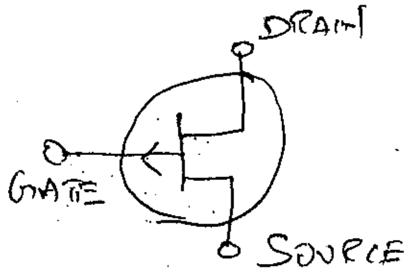
Schematic Symbol



N-channel JFET

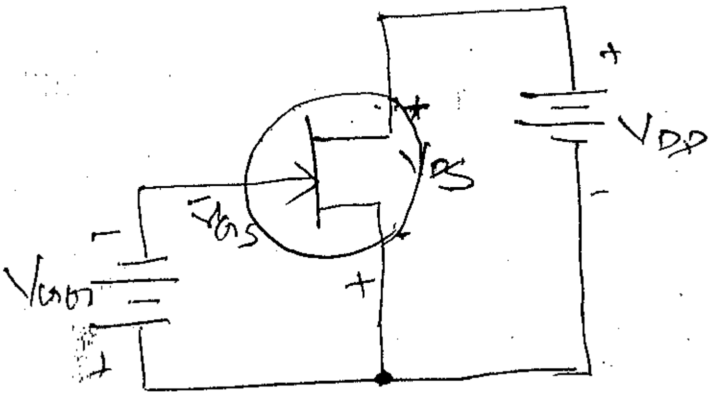


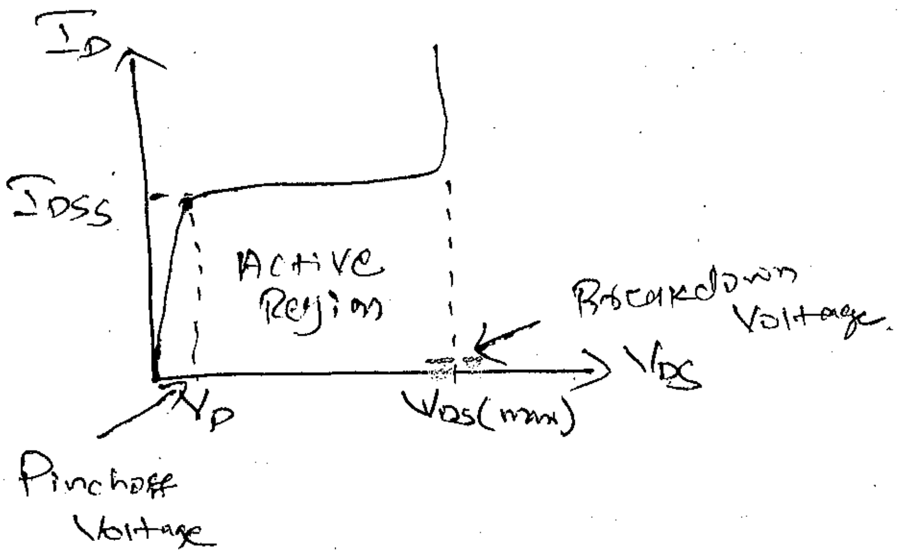
Offset-gate symbol



P-channel JFET

Drain Curves

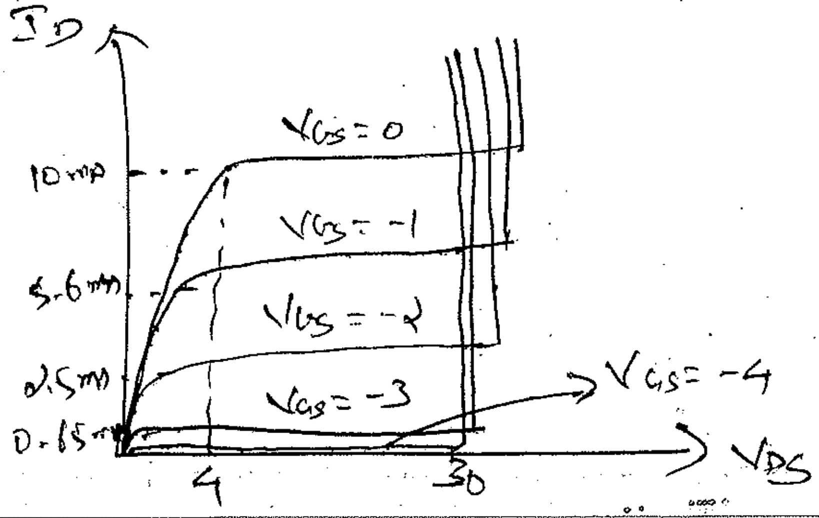




when $V_{GS}=0$, maximum drain current

$\therefore$ V_{GS} = enough negative, no drain current.

Gate Cutoff Voltage



TRANSISTOR BIASING

UNIT-I

The quiescent operating point of a Transistor amplifier should be established in the active region of ~~this~~ its characteristics since the transistor parameters such as β, I_{CO} and V_{BE} are function of temperature the operating point shifts with changes in temperature.

Need for Biasing:

In order to produce distortion-free output in amplifier circuit, the supply voltage and resistances in the circuit must be suitably chosen. these voltages and resistances establish a set of d.c voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region these voltages and currents are called quiescent values which determine the operating point (or) Q point for the transistor.

The process of giving proper supply voltages and resistances for obtaining the desired Q point is called biasing. The circuits used for getting the desired and proper operating point are known as biasing circuits.

the collector current for Common-emitter amplifier is expressed by,

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1+\beta) I_{CO} \longrightarrow (1)$$

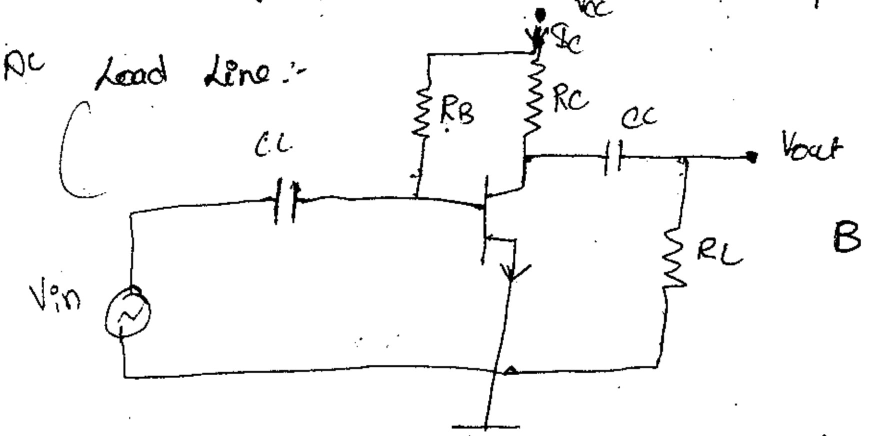
Here the three variables h_{FE} (β), I_B and I_{CO} are found to increase with temperature.

For every $10^\circ C$ rise, I_{CO} doubles itself.

When I_{CO} increases, I_C increases significantly

causes power dissipation to increase and hence to make I_{CO} increase. This will cause becomes cumulative which will lead to thermal runaway that will destroy the ...
This leads to, the quiescent operating point to shift, into saturation region. To establish the operating point in the active region, compensation techniques are needed.

DC Load Line :-

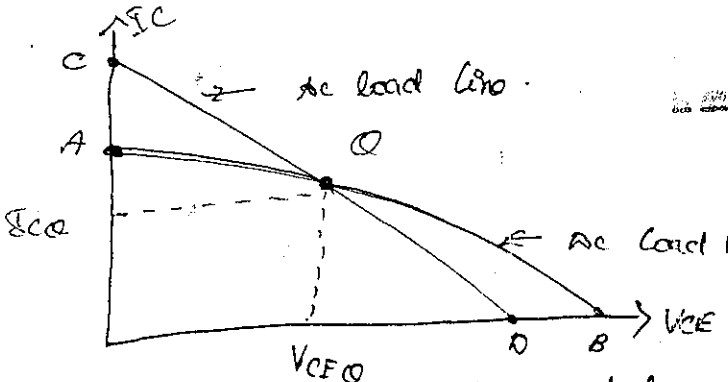


Biasing Circuit

Referring to the above biasing circuit in the fig the values of Vcc and Rc are fixed and Ic and VcE are dependent on RB

Applying Kirchhoff's Voltage Law to collector circuit in fig. we get.

$$V_{CC} = I_C R_C + V_{CE} \longrightarrow (1)$$



Characteristic and load line

The straight line represented by "AB" in active fig is called dc load line. the co-ordinates are obtained.

Point A $(V_{CE} = 0)$, $V_{CC} = I_C R_L \Rightarrow I_C = V_{CC}/R_C$

Point B $(I_C = 0)$, $V_{CC} = V_{CE} \rightarrow (3)$.

As shown in the above fig the Q point is fixed at the midpoint of dc load line "AB"

Q1:

i) D.c load line:

we have $V_{CC} = V_{CE} + I_C R_C$.

For maximum, $V_E = V_{CC} = 24V$ (since $I_C = 0$).

For maximum, $I_C = \frac{V_{CC}}{R_C} = \frac{24}{8 \times 10^3} = 3\,mA$ (since $V_{CE} = 0$).

Therefore, the d.c load line — draw with point B (24V on VCE axis and point A (3mA) on IC axis.)

ii) For fixing the optimum operating point Q, mark middle of d.c load line AB.

Here, $V_{CEQ} = \frac{V_{CC}}{2} = 12V$ and $I_{CQ} = 1.5\,mA$.

iii) a.c load line:

The A.c load, $R_{a.c} = R_C \parallel R_L = \frac{8 \times 24}{8 + 24} = 6k\Omega$

maximum, $V_{CE} = V_{CEQ} + I_{CQ} R_{a.c}$

$= 12 + 1.5 \times 10^{-3} \times 6 \times 10^3 = 21V$.

This locates the point D on VCE axis.

maximum collector current $= I_{CQ} + \frac{V_{CEQ}}{R_{a.c}}$

$= 1.5 \times 10^{-3} + \frac{12}{6 \times 10^3} = 3.5\,mA$

This locates the point 'C' on IC axis.

Hence the d.c and a.c load lines are,

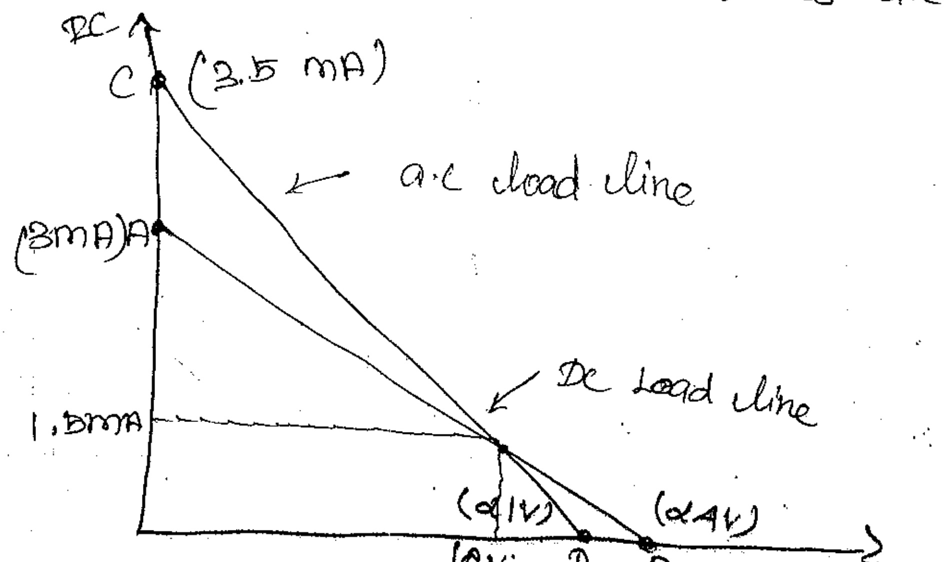


Fig 1.2

In practice, the ... to any
or, all of following 3 main factors:

* Reverse saturation current, I_{CO}, which doubles for every 10°C increase in temp.

* Base-emitter voltage, V_{BE}, which decreases by 2.5 mV per °C.

* Transistor current gain, β (or) h_{FE} which ↑ with temp.

Ac load line:

After drawing the d.c load line, the operating point Q is properly located at the center of dc load line this operating point is chosen under zero input signal condition of the circuit. the effective d.c load resistance, $R_{a.c}$ is $R_C \| R_L$ so the slope of a.c load line CQD will be $(-1/R_{a.c})$

To draw an a.c load ~~line~~ line, two end points namely maximum V_{CE} and maximum I_C when the input signal is applied are required.

$$\text{Maximum } V_{CE} = V_{CEQ} + I_{CQ} R_{a.c} \quad \text{which locates } D$$

$$\text{,, } I_C = I_{CQ} + \frac{V_{CEQ}}{R_{a.c}} \quad \text{which locates } C$$

By joining points C and D, the a.c load line CD is constructed.

From fig 1.2, it's clear that the intersection of d.c and a.c load lines is the operating Q point.

Problem 1:

In the transistor amplifier shown in fig 1.1, $R_C = 8k\Omega$, $R_L = 24k\Omega$ and $V_{CC} = 24V$. draw the d.c load line and determine the optimum operating point. Also draw the a.c load line

Stability Factor (S) (3)

The extent to which the collector current I_C is stabilised with varying I_{CO} is measured by a stability factor S. It's defined by the rate of change of collector current I_C with respect to collector-base leakage current I_{CO}, keeping both ~~to collector-base~~ the current I_B and the current gain β

$$S = \frac{\partial I_C}{\partial I_{C_0}} \approx \frac{dI_C}{dI_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}, \quad \beta \text{ and } I_B \text{ constant} \quad \text{—(1)}$$

The collecter current for CE amplifier is given by,

$$I_C = \beta I_B + (\beta+1) I_{CO} \rightarrow (2)$$

differentiating the above eqn with respect to I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta+1) \frac{dI_{CO}}{dI_C} \Rightarrow \left(1 - \beta\frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\left(1 - \beta\frac{dI_B}{dI_C}\right) = \frac{dI_{CO}}{dI_C} \Rightarrow S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)} \quad \text{—(3)}$$

It's clear that this factor S should be as small as possible to have better thermal stability.

Stability Factor S' and S''

The stability factor S' is defined as the rate ~~of~~ of change of I_C with V_{BE}, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}, \quad \Big| \; I_{CO} \text{ and } \beta \text{ constant}$$

The stability factor S' is defined as the of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{dI_C}{d\beta} \approx \frac{\Delta I_C}{\Delta \beta}, \quad \Big| \; I_{CO} \text{ and } V_{BE} \text{ constant}$$

(i) Fixed Bias (or) Base resistor method:-

A common emitter amplifier using fixed bias circuit is shown in fig 1.4 the d.c analysis of the circuit yields the following equation.

$VCC = IBRB + VBE$ — ①

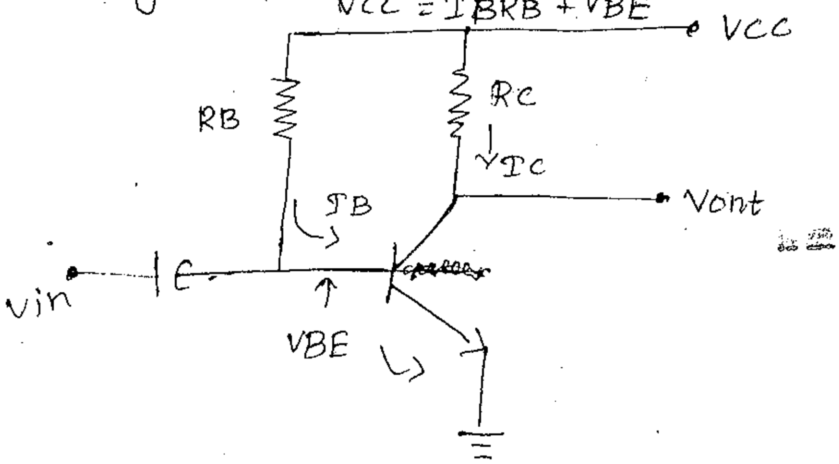


Fig 1.4 Fixed Bias circuit

$$IB = \frac{VCC - VBE}{RB} \quad — ②$$

since this eqn is Independent of current I_C, $\frac{dI_B}{dI_C} = 0$ and the stability factor is reduced to,

$$S = \frac{1+\beta}{1-\beta\left(\frac{dIB}{dIC}\right)} = 1+\beta \quad — ③$$

since β is large quantity, this is a very poor bias stable circuit.

Advantages:

1. simplicity
2. small number of components required
3. If VCC >>> VBE, the base current (IB) becomes independent of VBE

Problem 2:

In the fixed bias compensation method (fig 1.4), a silicon transistor with β=100 is used, VCC=6V, RC=3 kΩ RB=530 kΩ. draw the d.c Load line and determine the operating point. what is the stability factor?

Sol :- (4)

(i) DC Load line:

$V_{CE} = V_{CC} = I_C R_C$

when, $I_C = 0 \Rightarrow V_{CE} = V_{CC} = 6V$

" $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{6}{3\times10^3} = 2mA.$

(ii) operating point Q:

For 'si' transistor, $V_{BE} = 0.7V$

$V_{CC} = I_B R_B + V_{BE}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{6-0.7}{530\times10^3} = 10mA.$

$I_C = \beta I_B = 100\times10\times10^{-6} = 1mA$

$V_{CE} = V_{CC} - I_C R_C = 6 - (+1\times10^{-3}\times3\times10^3) = 3V$

Therefore operating point is $V_{CEQ} = 3V$ & $I_{CBQ} = 1mA.$

(iii) stability factor:

$S = 1 + \beta = 1 + 100 = 101.$

Stability factor for fixed bias circuit

since eqn ② is independent of current, I_C, $\frac{dI_B}{dI_C} = 0$ and

the stability factor

becomes $\boxed{S = 1+\beta}$

stability factor S':

$S' = \frac{\Delta I_C}{\Delta V_{BE}} \Big| I_{CO}, \beta$ constant

$I_C = \beta I_B + (\beta+1) I_{CO}.$

$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (\beta+1) I_{CO}$ $\left[\because I_B = \frac{V_{CC} - V_{BE}}{R_B}\right.$

$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CO}$

$\frac{\Delta I_C}{\Delta V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = \frac{-\beta}{R_B}$ $\boxed{S' = \frac{-\beta}{R_B}}$

Stability factors

$$S'' = \frac{\Delta I_C}{\Delta \beta} \Big/ V_{BE},\ I_{CO}\ \text{Constant}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (\beta+1) I_{CO}$$

$$\frac{\Delta I_C}{\Delta \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CO} = I_B + I_{CO}$$

Since,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta I_B + I_{CO} + \beta I_{CO}$$

$$I_C = \beta(I_B + I_{CO}) + I_{CO}$$

$$\frac{I_C}{\beta} = I_B + I_{CO} + I_{CO} \approx I_B + I_{CO}$$

Hence $\boxed{\frac{\Delta I_C}{\Delta \beta} = \frac{I_C}{\beta}} = S''$

Collector to Base Bias (or) Biasing with feed back resistor

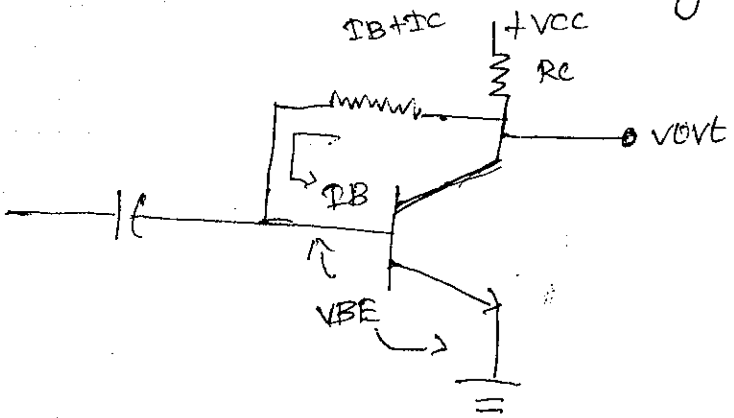


Fig 1.5 Collector-to-Base Bias

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

$$\frac{dI_B}{dI_C} = -\frac{R_C}{R_C + R_B}$$

$$S = \frac{1+B}{1+B\left(\frac{dI_B}{dI_C}\right)}$$

$$S = \frac{1+B}{1+B\left(\frac{R_C}{R_C+R_B}\right)}$$

S can be made small and the stability can be improved by making RB small (or) RC large.

(iii) Voltage Divider Bias / self Bias circuit:-

voltage divider bias circuit (as shown in fig 1.6) is providing biasing by three resistors R1, R2 and RE. R1 & R2 act as a potential divider giving a fixed voltage to point B which is base. If collector current increases due to change in temperature (or) change in B, the emitter current IE also increases and the voltage drop across RE increases, reducing the voltage difference between base and emitter (VBE). Due to reduction in VBE, base current IB & hence collector current Ic also reduces.

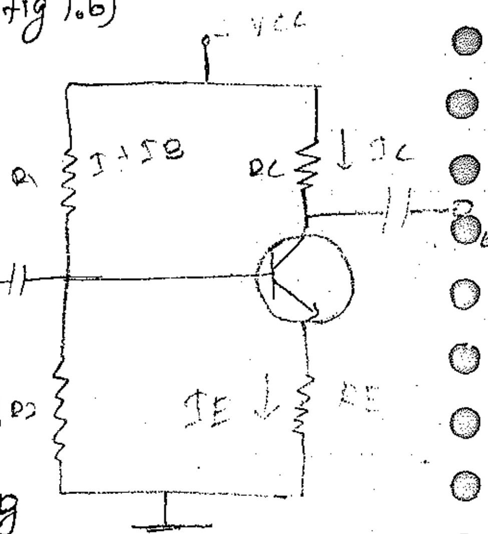
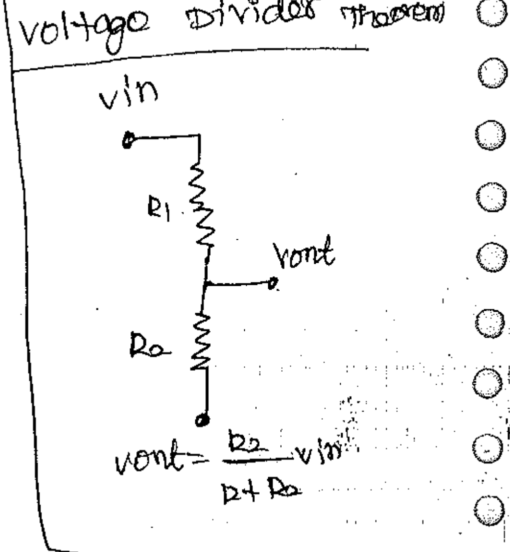


Fig 1.6 voltage Divider Bias (VDB)



Base circuit

$$V_B = \frac{R_2(I)}{R_1(I+I_B)+R_2(I)} \times V_{CC}$$

$$= \frac{R_2}{R_1+R_2} \times V_{CC} \quad (\because I >> I_B)$$

collector circuit:-

voltage across RE (VE),

$$V_E = I_E R_E = V_B - V_{BE}$$

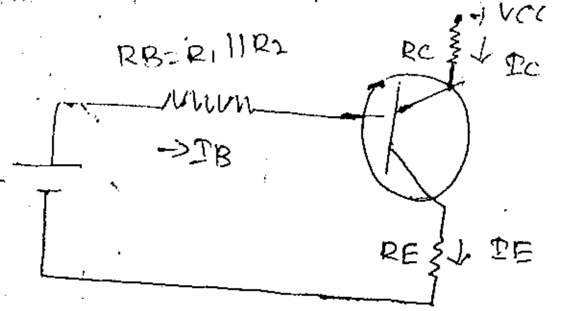
$$I_E = \frac{V_B - V_{BE}}{R_E} \longrightarrow (1)$$

Applying KVL to collecting ckt,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \longrightarrow (2)$$

simplified ckt of it:



$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = R_B$$

$$V_T = I_B R_B + V_{BE} + I_E R_E = I_B(R_B + R_E) + V_{BE} + I_C R_E$$

stability factor 's':-

$$S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

from the above eqn, VT

$$I_B = \frac{V_T - V_{BE} - I_C R_E}{R_B + R_E} = \frac{V_T}{R_B+R_E} - \frac{V_{BE}}{R_B+R_E} - \frac{I_C R_B}{R_B+R_E}$$

Diff. w.r.to I_C,

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B+R_E}$$

now,

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}} \quad \text{—④}$$

if $R_E >> R_B$, then $S = \frac{1+\beta}{1+\beta} = 1$

Advantages:-

stability factor 's' for self bias is less as compared to other biasing circuits so this circuit is more stable so hence it's most commonly used.

stability Factor's:-

The stability factors is defind as the rate of change of I_C with VBE, keeping I_{CO} and β constant.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

From eqn (3),

$$VT = I_B R_B + V_{BE} + I_E R_E = I_B [R_B + R_E] + I_C R_E + V_{BE} \quad \text{--(5)}$$

since $I_E = I_B + I_C$

w.k.T, $I_B = \dfrac{I_C - (1+\beta) I_{CO}}{\beta}$ → (6a)

substituting eqn in (5),

$$VT = \frac{I_C}{\beta}(R_B + R_E) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1+\beta)(R_B + R_E) \rightarrow (6b)$$

Diff the above eqn w.r.t V_{BE},

$$0 = \frac{dI_C}{dV_{BE}}\left(\frac{R_B + R_E}{\beta}\right) + 1 + \frac{dI_C}{dV_{BE}} R_E + 0$$

$$-1 = \frac{dI_C}{dV_{BE}}\left[R_E + \frac{R_B + R_E}{\beta}\right] = \frac{dI_C}{dV_{BE}}\left[\frac{R_B + R_E(1+\beta)}{\beta}\right]$$

$$\boxed{\therefore S' = \frac{dI_C}{dV_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E}} \quad \text{--(7)}$$

stability factor S''

from eqn (6b),

$$VT = \frac{I_C}{\beta}(R_B + R_B) + V_{BE} + I_C R_E + \frac{I_{CO}}{\beta}(1+\beta)(R_B + R_E)$$

$$= I_C\left(\frac{R_B + R_E}{\beta} + R_E\right) + V_{BE} + \frac{I_{CO}}{\beta}(1+\beta)(R_B + R_E)$$

$$= I_C\left(\frac{R_B + R_E(1+\beta)}{\beta}\right) + V_{BE} + \frac{I_{CO}}{\beta}(1+\beta)(R_B + R_E)$$

$$I_C = \frac{VT\beta - V_{BE}\beta - I_{CO}(1+\beta)(R_B + R_E)}{R_B + (1+\beta) R_E}$$

Let rearrange the above eqn

$$I_C = \frac{\beta(VT - V_{BE})}{R_B + (1+\beta) R_E} - \frac{I_{CO}\,\beta\dfrac{(1+\beta)}{\beta}(R_B + R_E)}{R_B + (1+\beta) R_E}$$

since $\beta \gg 1$, the numerator of 2nd term reduces to

$$(R_B + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} \approx (R_B + R_E) I_{CO}$$

$$\frac{\ldots}{RB\,(1+B)RE} \qquad \frac{\ldots}{RB+(1+B)\,RE}$$

$$\therefore I_C = \frac{B\,[V_T - V_{BE} - (RB+RE)\,I_{CO}]}{RB\,(1+B)RE}$$

Let, $V' = (RB+RE)\,I_{CO}$,

$$\therefore I_C = \frac{B\,[V_T - V_{BE} + V']}{RB + (1+B)RE}$$

Diff w.r.t. B,

$$S'' = \frac{dI_C}{dB} = \frac{I_C}{B\left[1+B\left(\frac{RE}{RE+RB}\right)\right]} = \frac{SI_C}{B(1+B)}$$

BIAS COMPENSATION:-

Diode, thermistors and sensistors can be used to compensate for variations in current.

1. Diode compensation:-

Fig 1.7 shows a transistor amplifier with a diode 'D' connected across the base-emitter junction for compensation of change in collector-saturation current I_{CO}. The base current $I_B = I - I_D$. As long as temperature is constant, diode 'D' operates as a resister. As temp increases, I_{CO} of transister increases. Hence, to compensate for this, the base current I_B should be decreased. The increase in temperature will also cause the leakage current I_D through D to increase and there by decreasing the base current I_B. This is the required action to keep I_C constant.

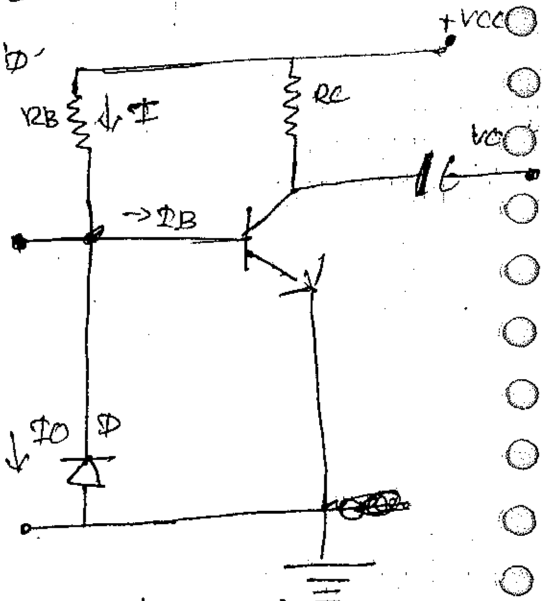
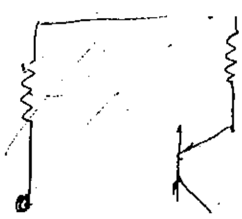


Fig 1.7 Diode compensation

2. Thermister compensation

The thermister, RT, having a negative temperature coefficient is connected in parallel with RE. The resistance of thermister decreases exponentially with increase of temperature. An increase in temperature will decrease the base voltage VBE, reducing I_B and I_C. Bias stabilisation is also provided by RE and CE.



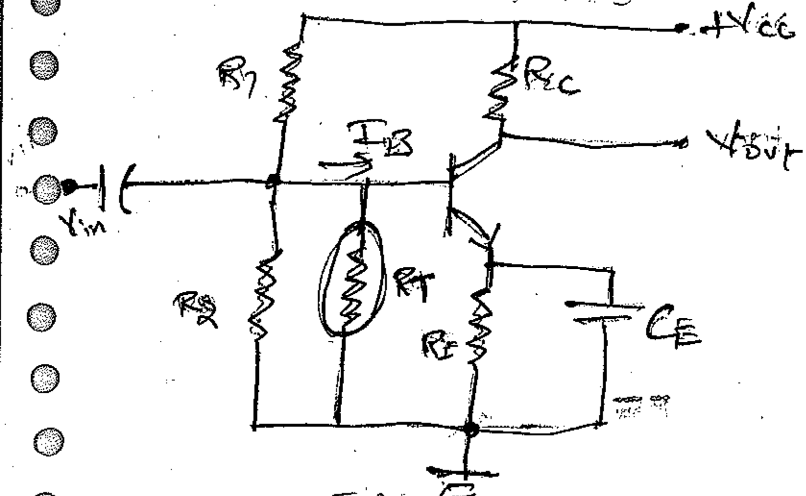


Fig 1.8

3. Sensistor compensation:-

A sensistor, RS, having a positive temperature coefficient is connected across R1 (or RE). RS increases with temperature. As temperature increases, the equivalent resistance of parallel combination ~~sensistor compensation~~ of R1 and RS also increases and hence the base voltage VBE decreases, reducing IB and IC. This reduced IC compensates for the increased IC caused by increase in ICO, VBE and β due to temperature rise.

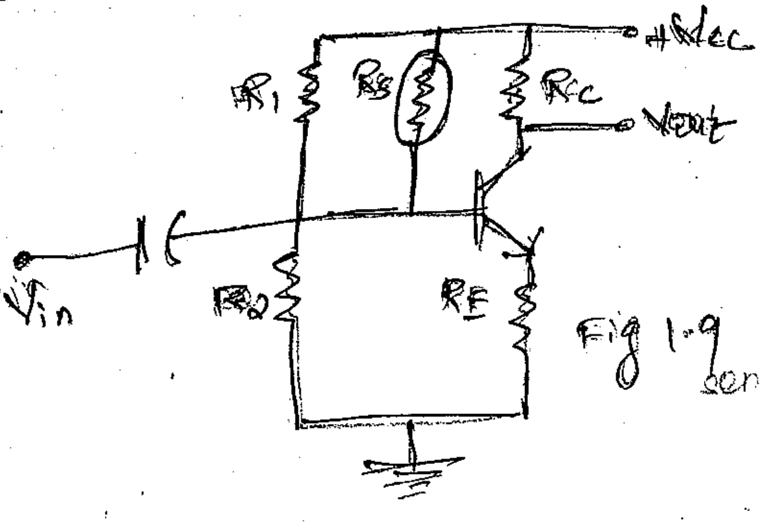


Fig 1.9 sensistor compensation

UNIT-II MIDBAND ANALYSIS OF SMALL SIGNAL AMPLIFIERS

Two-Port Devices and Network Parameters

* A transistor can be treated as a two-port network. The terminal behaviour of any two port network can be specified by the terminal voltages V_1 and V_2 at Port 1 and Port 2 respectively, and currents i_1 and i_2, entering Ports 1 and 2 respectively as shown in fig 2.1

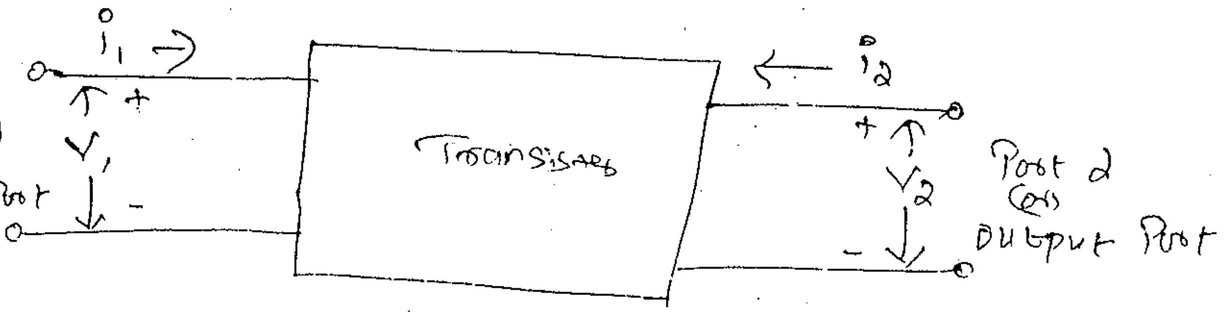


Fig 2.1 Two-Port network.

Of these four variables V_1, V_2, i_1 and i_2, two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This lead to various two-Port parameters:

(i) Z-Parameters (or) Impedance parameters
(ii) Y- " (or) Admittance "
(iii) H- " (or) Hybrid "

Z- Parameters (or) Impedance Parameters

Here i_1 and i_2 are taken as independent Variables.

$$V_1 = Z_{11} i_1 + Z_{12} i_2 \longrightarrow (1)$$

$$V_2 = Z_{21} i_1 + Z_{22} i_2 \longrightarrow (2)$$

where,

$Z_{11} = \left[\frac{V_1}{i_1}\right]$ with $i_2 = 0$; $Z_{22} = \left[\frac{V_2}{i_2}\right]$ with $i_1 = 0$

Input impedance with output port open circuited = output impedance with input port open circuited.

$Z_{12} = \left[\frac{V_1}{i_2}\right]$ with $i_1 = 0$; $Z_{21} = \left[\frac{V_2}{i_1}\right]$ with $i_2 = 0$

reverse transfer impedance with Port 1 open circuited

Forward transfer impedance with Port 2 open circuited.

Y- Parameters (or) Admittance Parameters

Here V_1 and V_2 are taken as independent Variables.

$$i_1 = Y_{11} V_1 + Y_{12} V_2 \longrightarrow (3)$$

$$i_2 = Y_{21} V_1 + Y_{22} V_2 \longrightarrow (4)$$

where,

$Y_{11} = \left[\frac{i_1}{V_1}\right]$ with $V_2 = 0$; $Y_{22} = \left[\frac{i_2}{V_2}\right]$ with $V_1 = 0$

Input admittance with output port short circuited

output admittance with Input Port short circuited

$Y_{12} = \left[\frac{i_1}{V_2}\right]$ with $V_1 = 0$

$Y_{21} = \left[\frac{i_2}{V_1}\right]$ with $V_2 = 0$

Reverse transfer admittance

Forward transfer

Hybrid Parameters (or) h- Parameters

Here the input current i_1 and the output voltage V_0 are taken as independent variables.

$$V_1 = h_{11} i_1 + h_{12} V_2 \rightarrow (5)$$

$$i_2 = h_{21} i_1 + h_{22} V_2 \rightarrow (6)$$

The four hybrid parameters,

$h_{11} = \left[\frac{V_1}{i_1}\right]$ with $V_2 = 0$; $h_{22} = \left[\frac{i_2}{V_2}\right]$ with $i_1 = 0$

Input impedance with output port short circuited ; Output admittance with Input port open circuited.

$h_{12} = \left[\frac{V_1}{V_2}\right]$ with $i_1 = 0$; $h_{21} = \left[\frac{i_2}{i_1}\right]$ with $V_2 = 0$

Reverse voltage transfer ratio with input port open circuited ; Forward current gain with output port short circuited.

It can be alternatively subscribed and noted,

$i = 11 =$ input ; $o = 22 =$ output

$f = 21 =$ forward transfer ; $r = 12 =$ Reverse transfer.

Notations

$h_{ie} = h_{11e} =$ short circuit input impedance

$h_{oe} = h_{22e} =$ open " output admittance

$h_{re} = h_{12e} =$ " " Reverse voltage transfer ratio

$h_{fe} = h_{21e} =$ short " forward current gain.

Hybrid Model For Two-Port Network

Eqn (5) & (6) Can be written as,

$$V_1 = h_i i_1 + h_r V_2 \rightarrow (7)$$

$$i_2 = h_f i_1 + h_o V_2 \rightarrow (8)$$

The proposed model shown in Fig 2.2 should satisfy the above two equations.

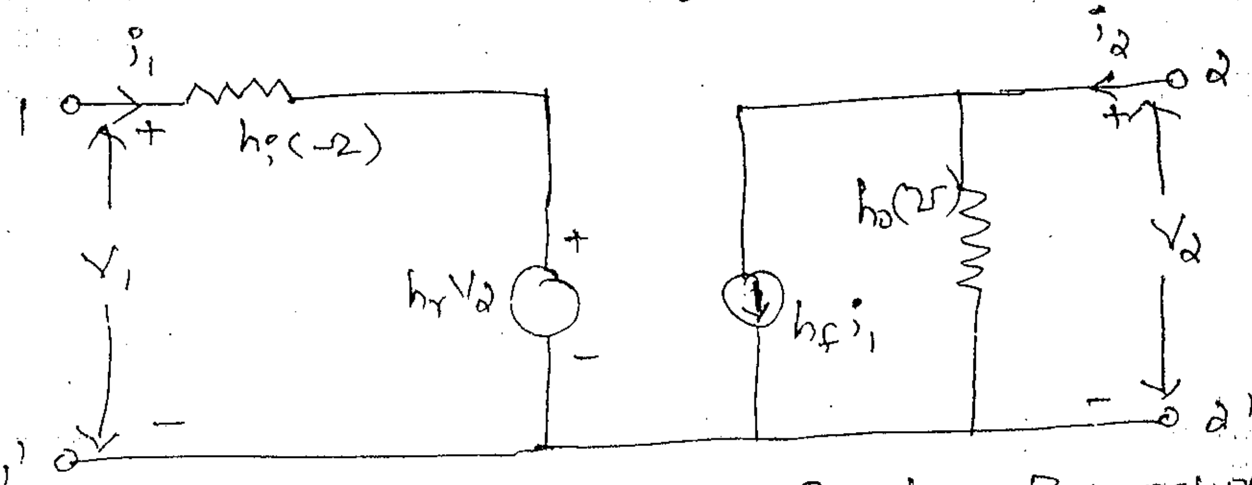


Fig 2.2 Hybrid model for two-Port network.

It is noted that the input circuit have a dependent voltage generators and the output circuit contains a dependent current generator.

Transistor Hybrid model

In order to derive a hybrid model for CE transistor (shown in fig 2.3) consider i_B and V_C as independent variables. Hence eqns (7) & (8) can be written as,

$$V_b = h_{ie} i_b + h_{re} V_c \rightarrow (9)$$

$$i_c = h_{fe} i_b + h_{oe} V_c \rightarrow (10)$$

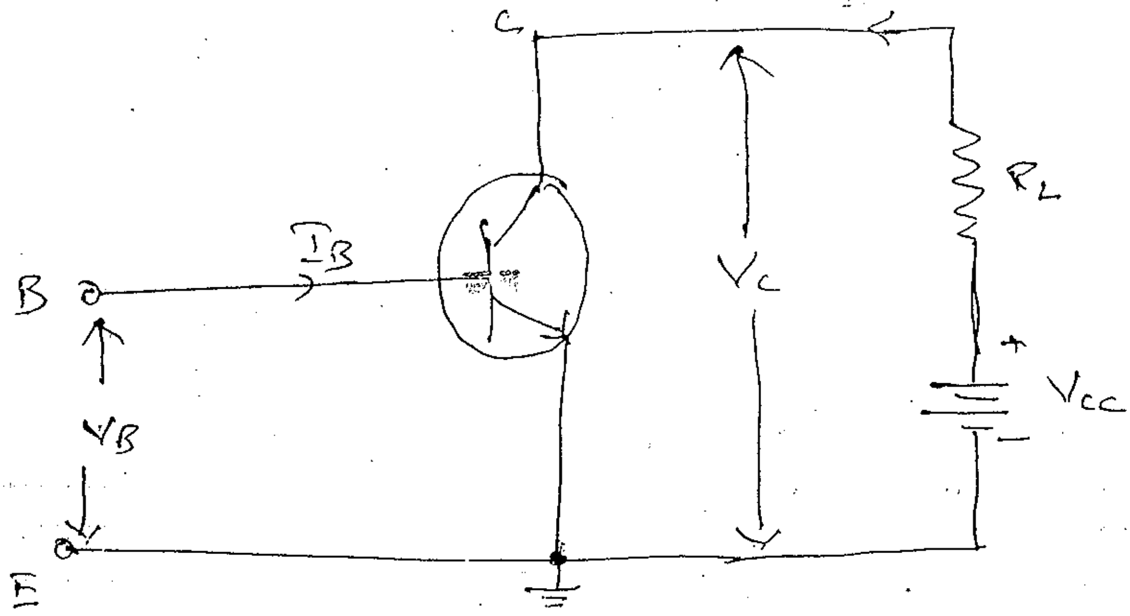
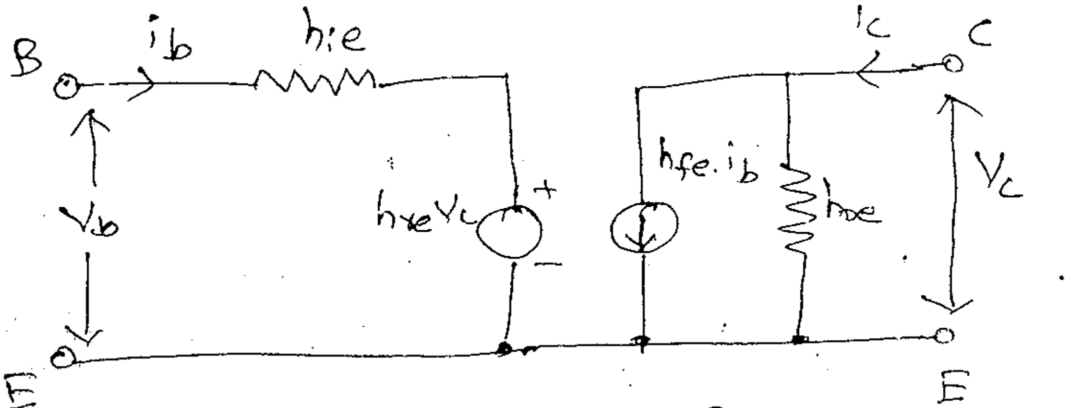


Fig 2.3 CE transistor circuit



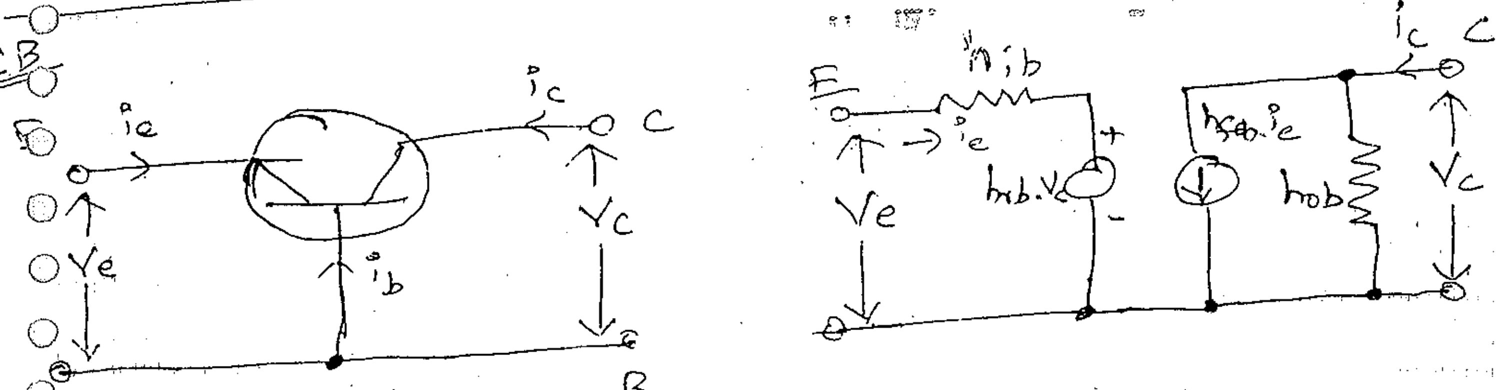
$V_b = h_{ie} i_b + h_{re} V_c$

$i_c = h_{fe} \cdot i_b + h_{oe} \cdot V_c$

Fig 2.4 Hybrid model for CE

Hybrid model for CC and CB Configurations

CB



B

Fig 2.5 Hybrid model for CB

$$\boxed{\begin{aligned} V_e &= h_{ib} \cdot i_e + h_{rb} V_c \\ i_c &= h_{fb} \cdot i_e + h_{ob} \cdot V_c \end{aligned}}$$

CC

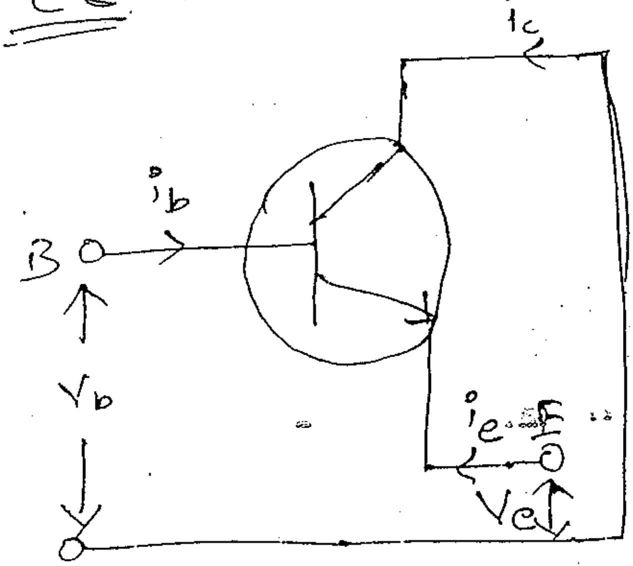
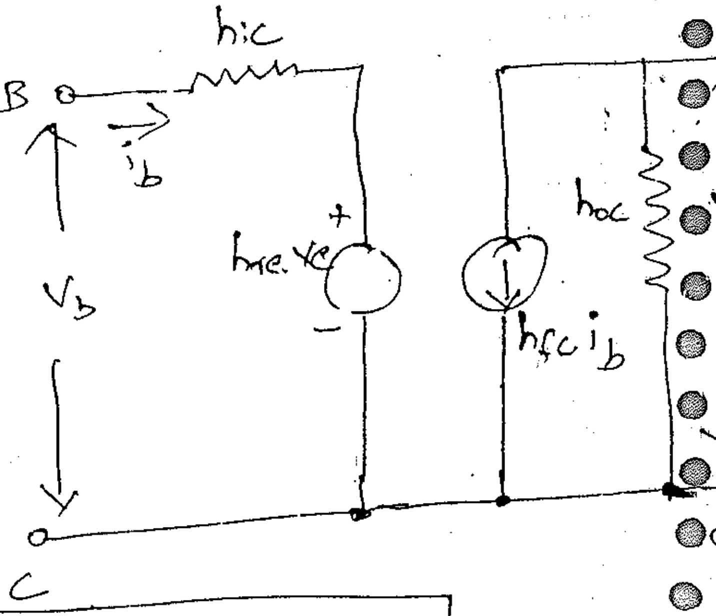


Fig 2.6



$$\boxed{\begin{aligned} V_b &= h_{ic}\,.\,i_b + h_{re}\,.\,V_e \\ i_e &= h_{fc}\,.\,i_b + h_{oc}\,.\,V_e \end{aligned}}$$

ANALYSIS OF TRANSISTOR AMPLIFIER CIRCUIT USING h- PARAMETERS

A transistor amplifier can be constructed by connecting an external load and signal source as shown in Fig 2.7

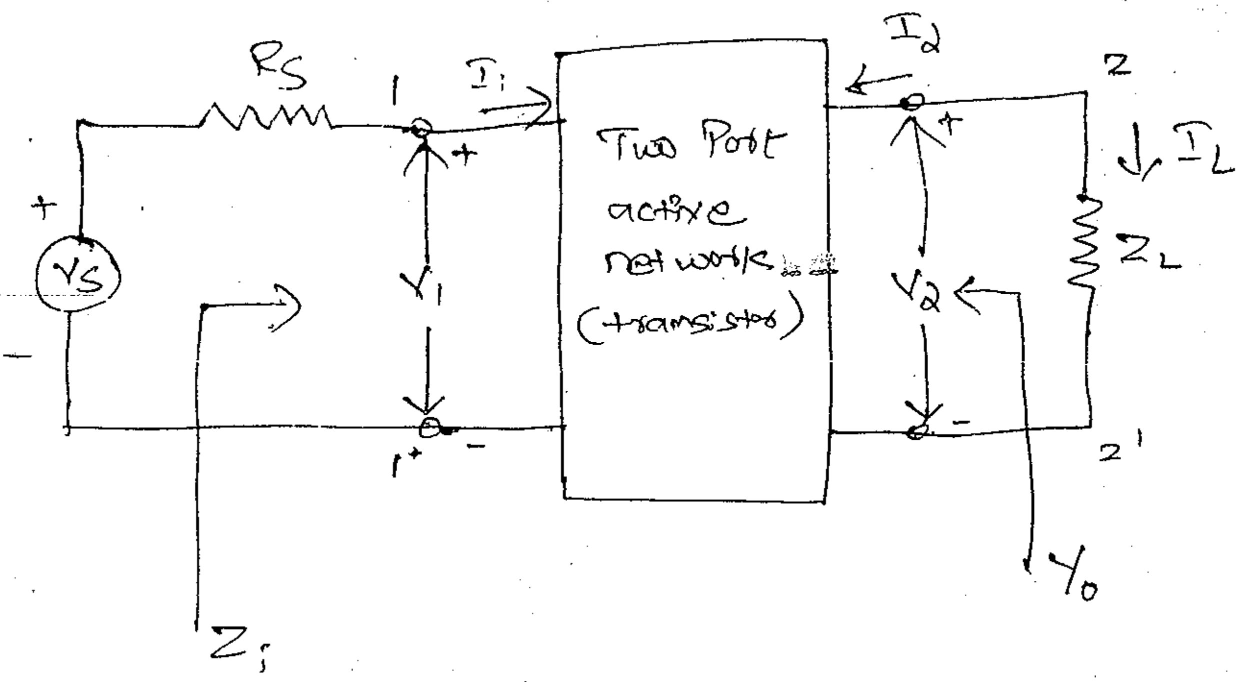


Fig 2.7 Basic amplifier circuit

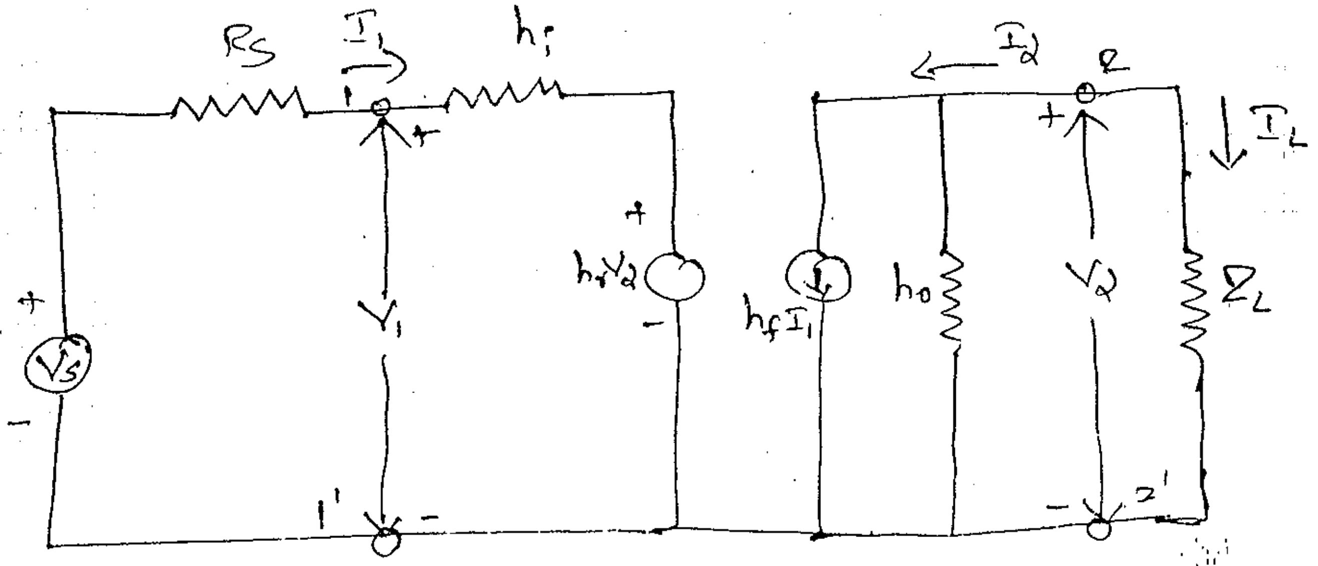


Fig 2.8 Hybrid model (Basic amplifier circuit)

(i) Current Gain (or) Current Amplification, A_i

For a transistor amplifier the current gain A_I is defined as the ratio of output current to input current (ie),

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1} \longrightarrow (1)$$

From fig 2.8, $I_2 = h_f I_1 + h_o V_2 \longrightarrow (2)$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$,

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$$I_2 + I_2 Z_L h_o = h_f I_1 \Rightarrow I_2(1 + Z_L h_o) = h_f I_1$$

$$\boxed{A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}} \longrightarrow (3)$$

(ii) Input Impedance, Z_i

In Fig 2.8, R_s is the signal source resistance. The impedance seen when looking into the amplifier terminals (1, 1') is the amplifier input impedance Z_i

(i) $Z_i = \dfrac{V_1}{I_1} \longrightarrow (4)$

From the fig 2.8, $V_1 = h_i I_1 + h_r V_2$

Hence, $Z_i = \dfrac{h_i I_1 + h_r V_2}{I_1} = h_i + \dfrac{h_r V_2}{I_1} \longrightarrow (5)$

Substituting, $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$Z_i = h_i + h_r \frac{A_I I_1 Z_L}{I_1} = h_i + h_r A_I Z_L$$

Substituting for A_I,

$$Z_i = h_i - \frac{h_f}{1 + h_o Z_L} h_r Z_L = h_i - \frac{h_f h_r}{Z_L\left(\frac{1}{Z_L} + h_o\right)} Z_L$$

Taking the load admittance, $Y_L = \dfrac{1}{Z_L}$

$$\boxed{Z_i = h_i - \frac{h_f h_r}{Y_L + h_o}} \longrightarrow (6)$$

(iii) Voltage Gain (or) Voltage Amplification factor, A_V

The ratio of output voltage V_2 to input voltage V_1 gives the voltage gain of the transistor, (i.e)

$A_V = \dfrac{V_2}{V_1} \longrightarrow (7)$

Substituting, $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$\boxed{A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}} \longrightarrow (8)$$

(iv) Output Admittance, Y_o

By definition, Y_o is obtained by setting V_s to zero, R_L to infinity and by driving the output terminals from a generator V_2. If the current drawn from V_2 is I_2, then

$$Y_o = \left.\frac{I_2}{V_2}\right|_{V_s=0 \;\&\; R_L=\infty}$$

From the Fig 2.8, $I_2 = h_f I_1 + h_o V_2$

Dividing by V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \rightarrow (9)$

With $V_s = 0$, by KVL in input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0 \Rightarrow I_1(R_s + h_i) + h_r V_2 = 0$$

Hence, $\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \rightarrow (10)$

Substituting eqn (10) in (9),

$$\frac{I_2}{V_2} = h_f\left(\frac{-h_r}{R_s+h_i}\right) + h_o$$

$$\boxed{Y_o = h_o - \frac{h_f h_r}{R_s + h_i}} \rightarrow (11)$$

(v) Voltage Amplification (A_{vs}) taking into account the Resistance (R_s) of the source

This overall voltage gain A_{vs} is given by,

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1}\frac{V_1}{V_s} = A_v \frac{V_1}{V_s} \rightarrow (12)$$

The thevenin's equivalent circuit for the figure is shown in fig 2.9.

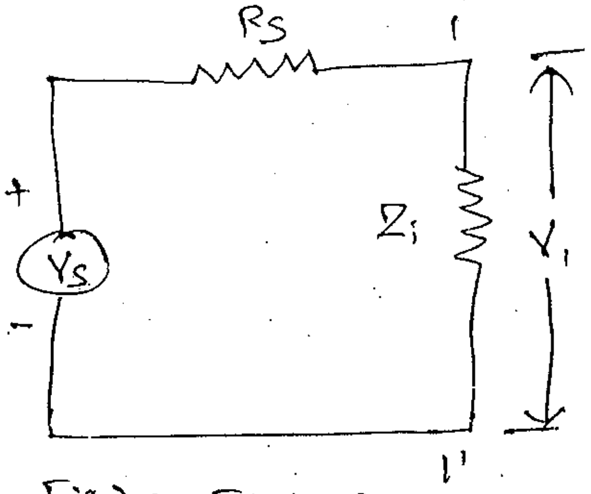


Fig 2.9 Equivalent Input Circuit

$$V_1 = \frac{V_s Z_i}{Z_i + R_s} \Rightarrow \frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s}$$

Then,

$$A_{VS} = \frac{A_V Z_i}{Z_i + R_s} \rightarrow (13)$$

Substituting, $A_V = \frac{A_I Z_L}{Z_i} \Rightarrow \boxed{A_{VS} = \frac{A_I Z_L}{Z_i + R_s}} \rightarrow (14)$

(vi) Current Amplification (A_{IS}) taking into Account the Source Resistance (R_s)

The modified input circuit using Norton's equivalent circuit for the source for the calculation of A_{IS} is shown in fig 2.10.

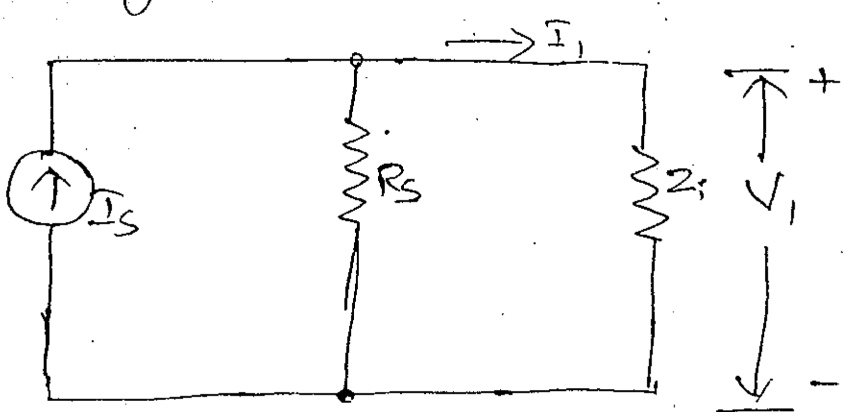


Fig 2.10 modified Input equivalent circuit.

Overall current gain, $A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S} = A_I \cdot \frac{I_1}{I_S}$ (11) → (15)

From fig 2.10, $I_1 = I_S \frac{R_S}{R_S + Z_i}$ → (16)

$$\frac{I_1}{I_S} = \frac{R_S}{R_S + Z_i}$$

and hence, $\boxed{A_{IS} = A_I \frac{R_S}{R_S + Z_i}}$

From eqn (14), $A_{VS} = \frac{A_I Z_L}{Z_i + R_S} \cdot \frac{R_S}{R_S} \Rightarrow \boxed{A_{VS} = \frac{A_{IS} \cdot Z_L}{R_S}}$ → (17)

(vii) Operating Power Gain, A_P

From fig 2.8, average power delivered to the load is $P_2 = |V_2||I_L| \cos\theta$, where θ is the phase angle b/w V_2 and I_L. Assume that $Z_L = R_L$, the power delivered to the load is $P_2 = V_2 I_L = -V_2 I_2$.

The operating power gain, $A_P = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V A_I$

$$= A_I A_I \frac{R_L}{R_i} \Rightarrow \boxed{A_P = A_I^2 \left(\frac{R_L}{R_i}\right)}$$

SINGLE STAGE AMPLIFIERS

Single stage amplifiers have only one amplifying device say, BJT in CE, CC (or) CB configuration (or) FET in CS, CD (or) CG configuration.

(i) Common Emitter Amplifier

Fig 2.11 Shows the circuit of Single Stage CE amplifier using NPN Transistor.

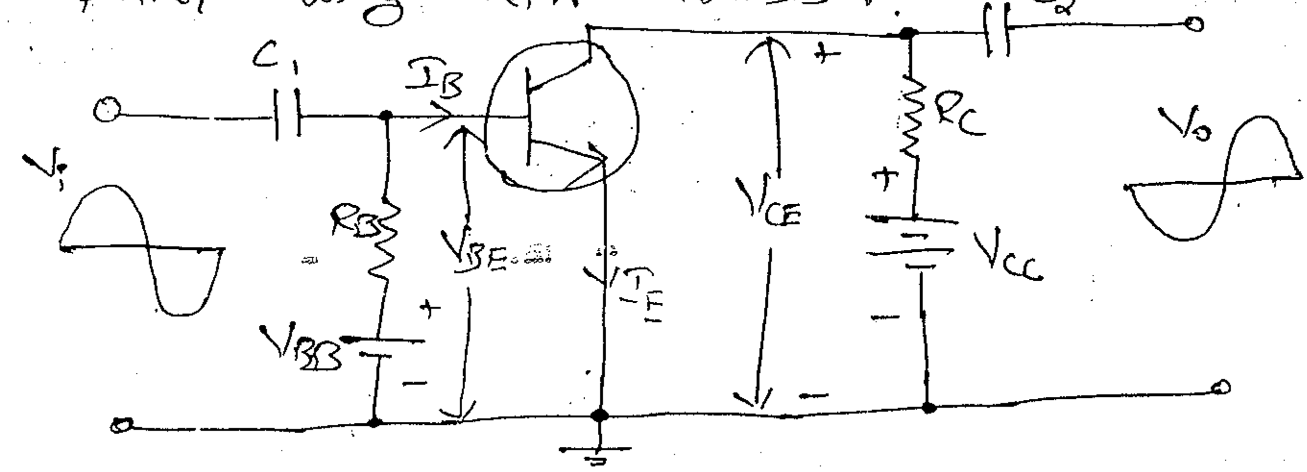
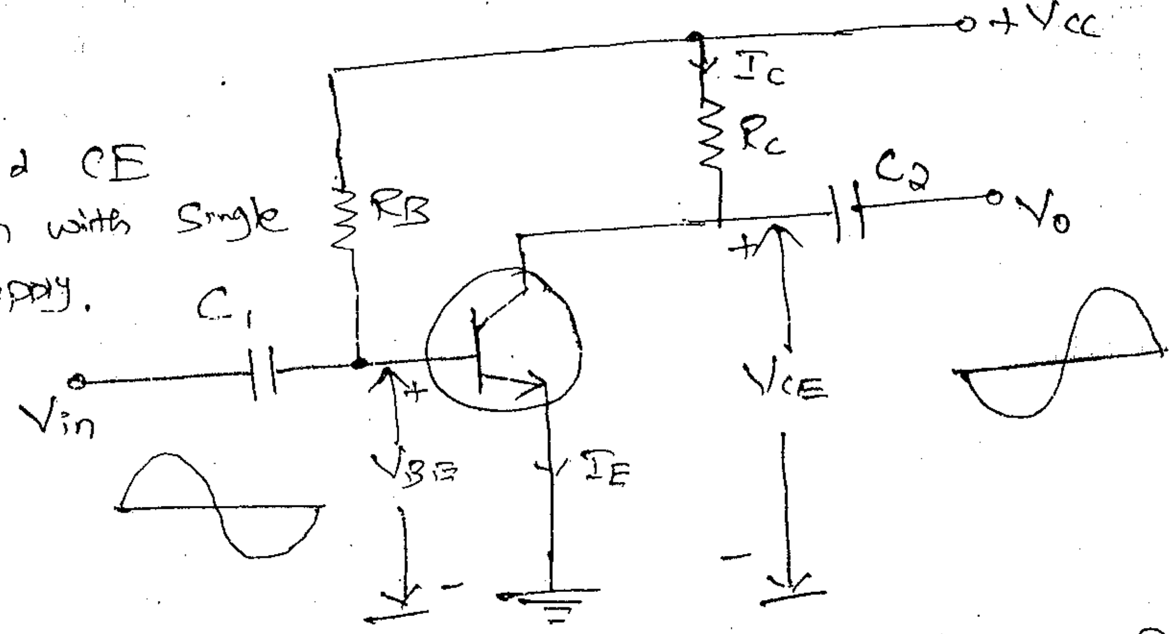


Fig 2.11 Common Emitter Amplifier

Fig 2.12 CE amplifier with Single Power supply.



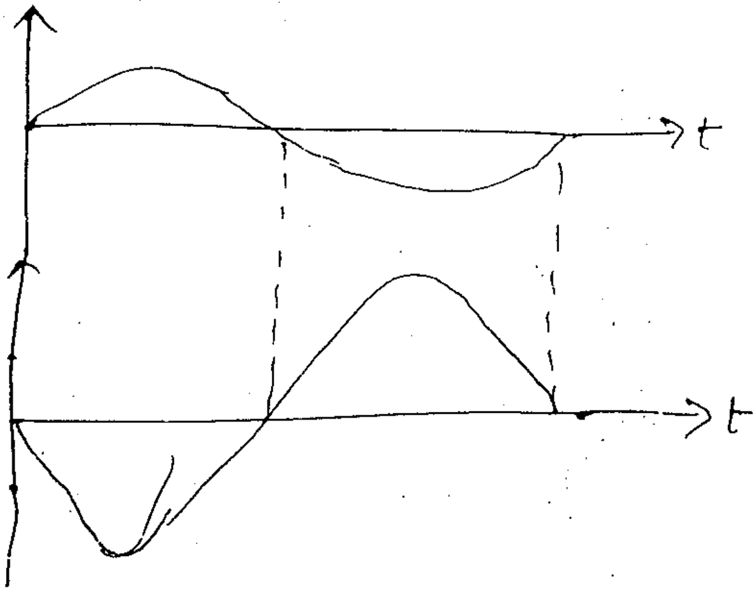
The emitter-base junction is forward biased by Power supply 'V_{BB}' and Collector-base junction is reverse biased by power supply 'V_{CC},' so that the transistor remains in active region.

Referring to fig 2.12, when no a.c signal i/p is given, (i) under d.c. conditions, $I_B = \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B}$ → (1)

$I_C = \beta I_B$ → (2)

When a sinusoidal a.c signal is applied at the input terminals of the circuit, during the positive half cycle the forward bias of V_{BE} is increased, resulting in an increase in I_B. The collector current I_C is increased by β time the increase in I_B.

Fig 2.13 input & output



Thus in a CE amplifier a positive going signal is converted into a negative going o/p signal, (i.e) a 180° phase shift is introduced b/w the o/p & i/p.

Further the o/p signal is an amplified version of o/p signal.

(ii) Common Collector (CC) amplifier

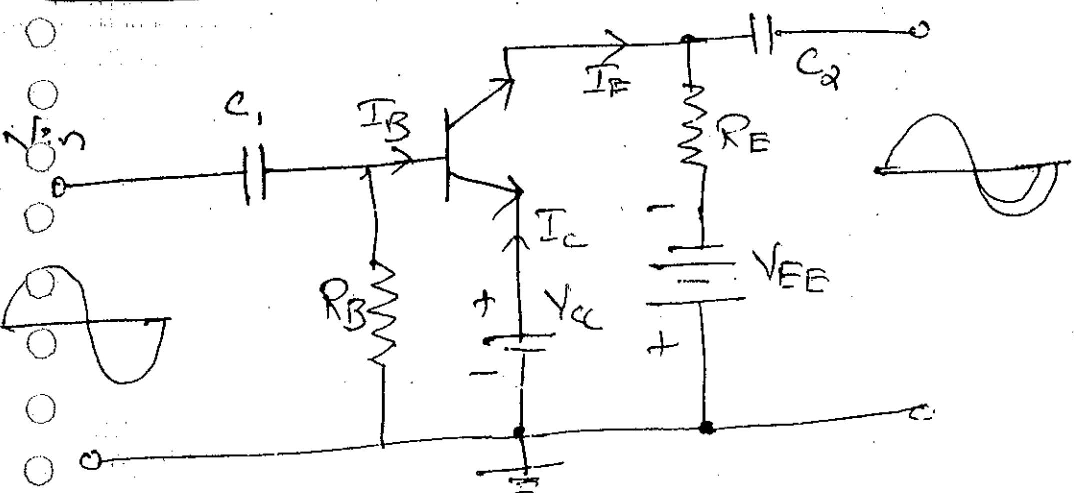


Fig 2.14

o/p Voltage, $V_o = I_E R_E = \beta I_B R_E$

When a sinusoidal a.c signal is applied at input, during the positive half cycle of signal applied, base Current I_B. Hence, emitter Current $I_E = I_C + I_B$ increases and voltage drop across R_E.

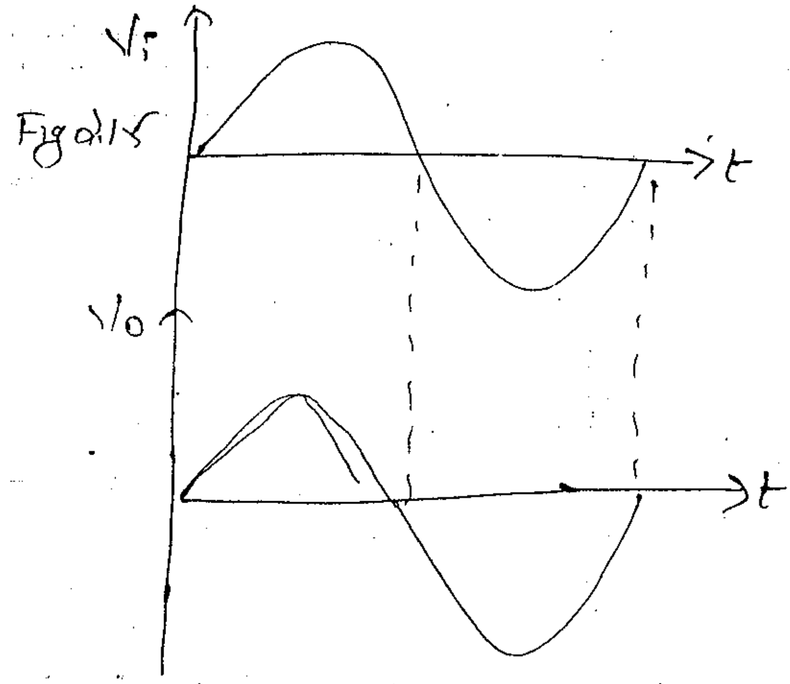


Fig 2.15

Thus, a positive going input signal results in a positive going output signal. As the o/p signal taken at the emitter terminal almost follows the i/p signal, the CC amplifier is called as "Emitter follower".

(iii) Common Base (CB) Amplifier

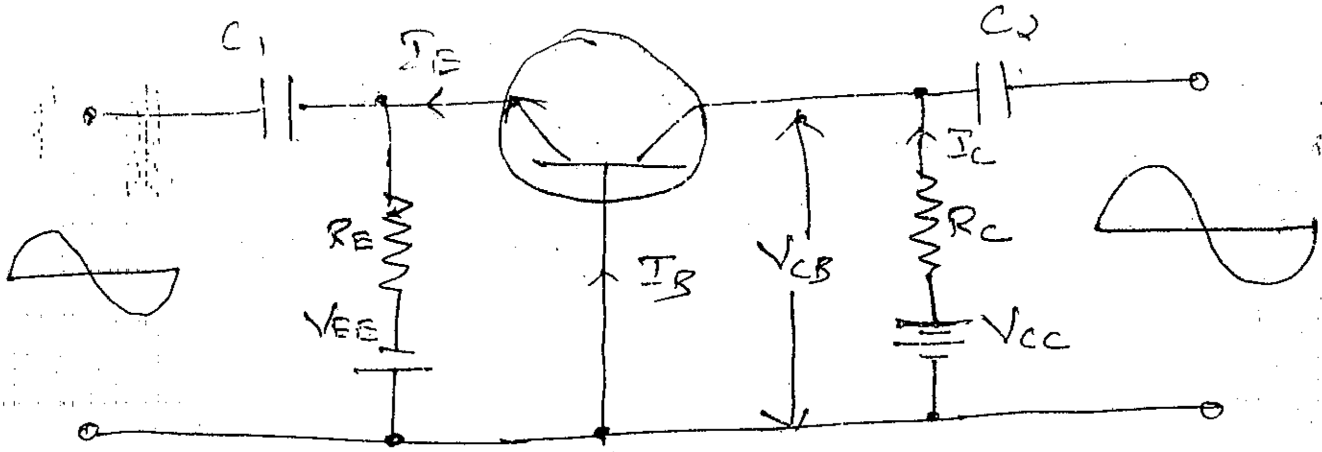
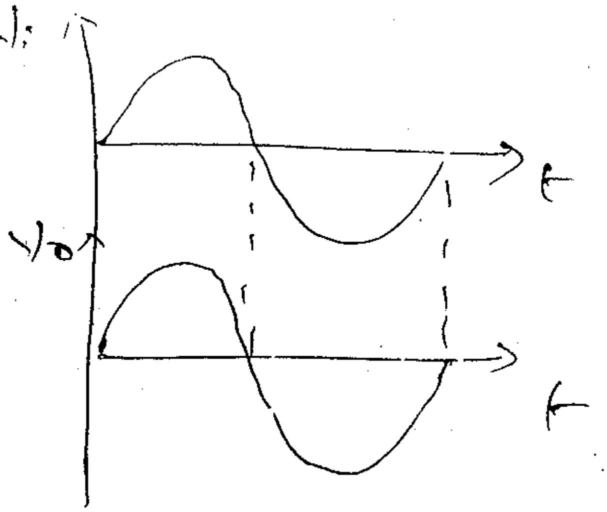


Fig 2.16

The o/p voltage, V_{CB} is $V_o = V_{CC} - I_C R_C$.

When a sinusoidal a.c signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in I_B. As a result $I_E (\approx \beta I_B)$ and hence I_C also decreases.

Thus, a positive half cycle appears at the o/p ...



SMALL SIGNAL ANALYSIS OF SINGLE STAGE (BJT)

(Method of drawing small signal equivalent circuit)

CE Amplifier with Fixed Bias:

The circuit of fig 2.17 shows a CE amplifier in fixed bias configuration. The ac equivalent circuit of amplifier can be drawn by the steps mentioned as follows:

(i) Remove the d.c. effects of Power Supply (V_{cc}) by grounding them.

(ii) Replace the capacitors (C_1 and C_2) by short circuits.

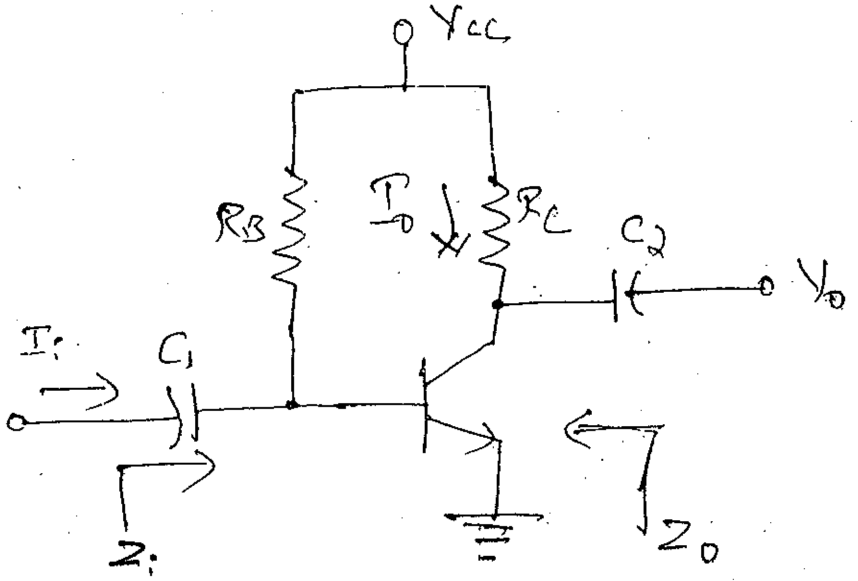


Fig 2.17 CE fixed bias configuration.

Thus the circuit of fig 2.17 reduce to fig

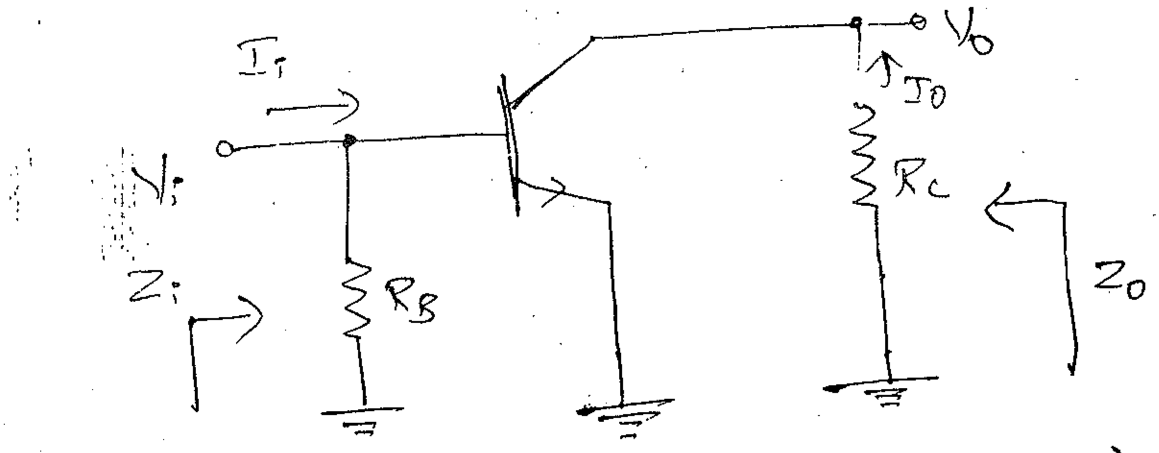


Fig 2.18 AC equivalent circuit of CE.

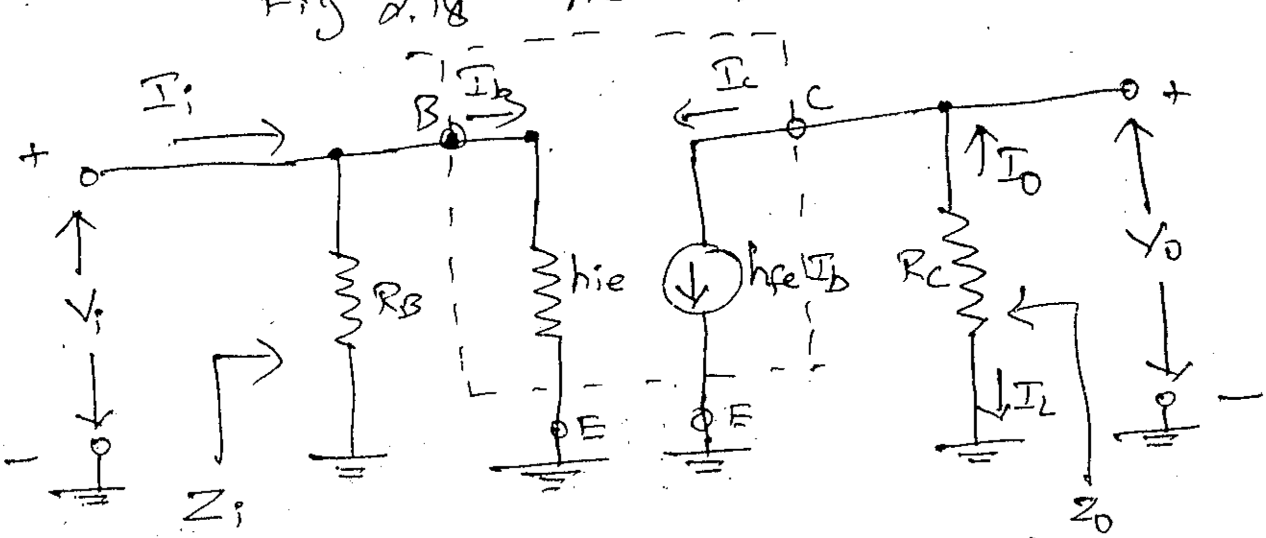


Fig 2.19 AC equivalent circuit of CE using hybrid model.

Substituting the approximate hybrid model for the transistors in Fig 2.18, the circuit reduces to Fig 2.19. From the circuit of Fig 2.19, the equations for input impedance, output impedance, voltage gain and current gain can be derived.

Input Impedance

$$Z_i = R_B \parallel h_{ie} = \frac{R_B h_{ie}}{R_B + h_{ie}}$$

if $R_B >> h_{ie}$

$$Z_i = \frac{R_B h_{ie}}{R_B} \approx h_{ie} \quad \boxed{Z_i \approx h_{ie}} \rightarrow 1$$

Output Impedance

It's the impedance determined with $V_i = 0$. with $V_i = 0$, $I_b = 0$ and $h_{fe} I_b = 0$ indicating an open circuit equivalent for the current source.

Hence $\boxed{Z_0 = R_1 (= R_C)}$ → (2)

Voltage Gain

Voltage gain, $A_V = \frac{V_O}{V_i}$; $V_O = -I_O R_C$

Substituting $I_O = h_{fe} I_b \Rightarrow V_O = -h_{fe} I_b R_C$

Assume, $R_B \gg h_{ie} \Rightarrow I_i \approx I_b$ and $V_i = I_b h_{ie}$

$$\therefore A_V = \frac{-h_{fe} I_b R_C}{I_b h_{ie}} \Rightarrow \boxed{A_V = \frac{-h_{fe} R_C}{h_{ie}}}$$

The -ve sign indicates a 180° phase shift between i/n and o/p signals. → (3)

Current Gain

$$A_I = \frac{I_L}{I_i} = \frac{-I_O}{I_i} \approx \frac{-h_{fe} I_b}{I_b} \Rightarrow \boxed{A_I = -h_{fe}}$$ → (4)

CB Amplifier

Fig 2.20 shows the circuit of CB amplifier.

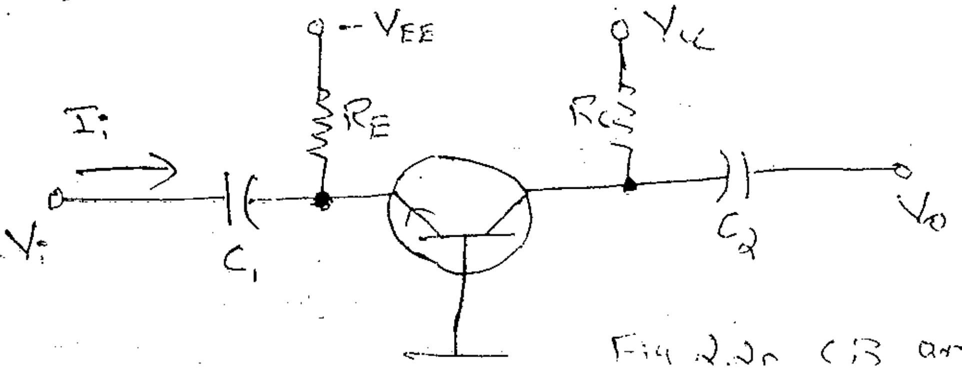


Fig 2.20 CB amplifier

By applying the steps, the AC circuit reduces to as shown in fig 2.21.

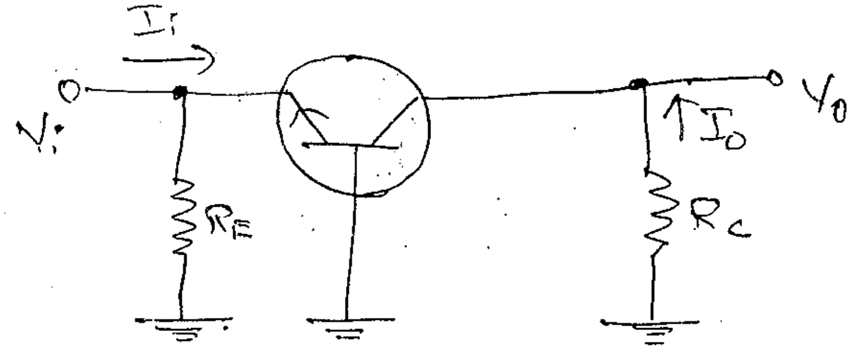


Fig 2.21 AC equivalent circuit of CB amplifier

Substituting the approximate hybrid model,

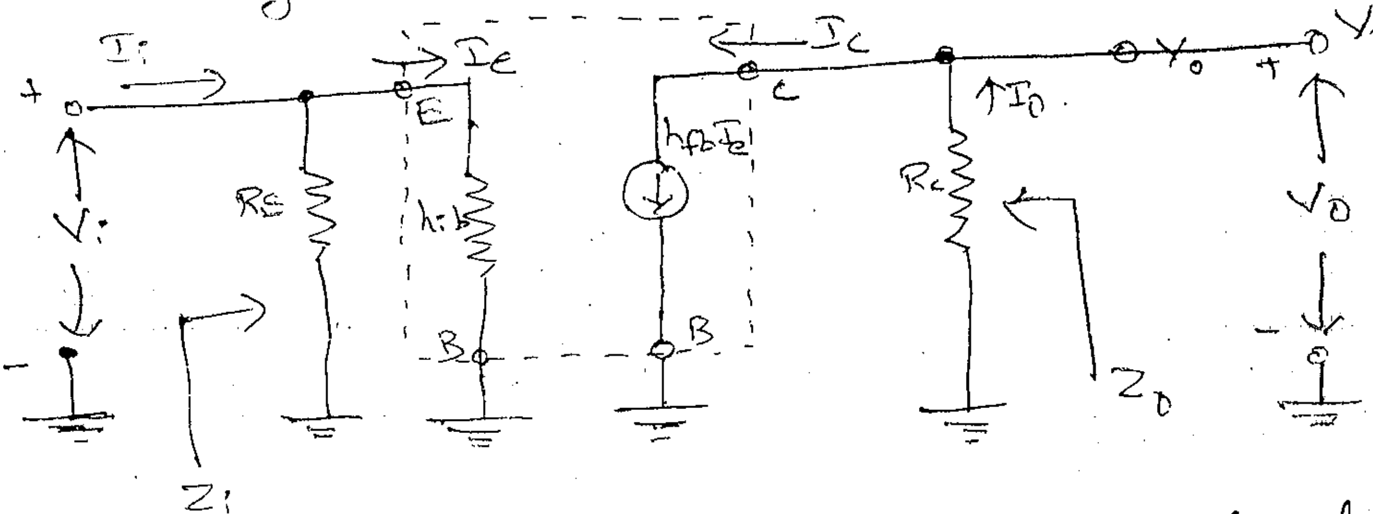


Fig 2.22 AC equivalent circuit using hybrid model

Input Impedance

$$\boxed{Z_i = R_E \parallel h_{ib}} \rightarrow (1)$$

Output Impedance

$$\boxed{Z_0 = R_C} \rightarrow (2)$$

Voltage Gain

$A_v = \frac{V_0}{V_i}$; $V_0 = -I_0 R_C = -h_{fb} I_e R_C$

Assume, $R_E >> h_{ib} \Rightarrow I_e \approx I_i$ and $V_i = I_e h_{ib}$

$$A_v = \frac{-h_{fb} I_e R_C}{I_e h_{ib}} = \frac{-h_{fb} R_C}{h_{ib}} \quad \boxed{A_v = \frac{-h_{fb} R_C}{h_{ib}}}$$

Current Gain

$$A_I = \frac{-I_0}{I_i} \approx \frac{-\cancel{h_{fb}} R_C}{\cancel{h_{ib}}} \quad \frac{-h_{fb} I_{e}}{I_e}$$

$$\boxed{A_I = -h_{fb}}$$

(iii) CC Amplifier (or) Emitter Follower

Fig 2.23 shows the CC amplifier circuit using a single power supply.

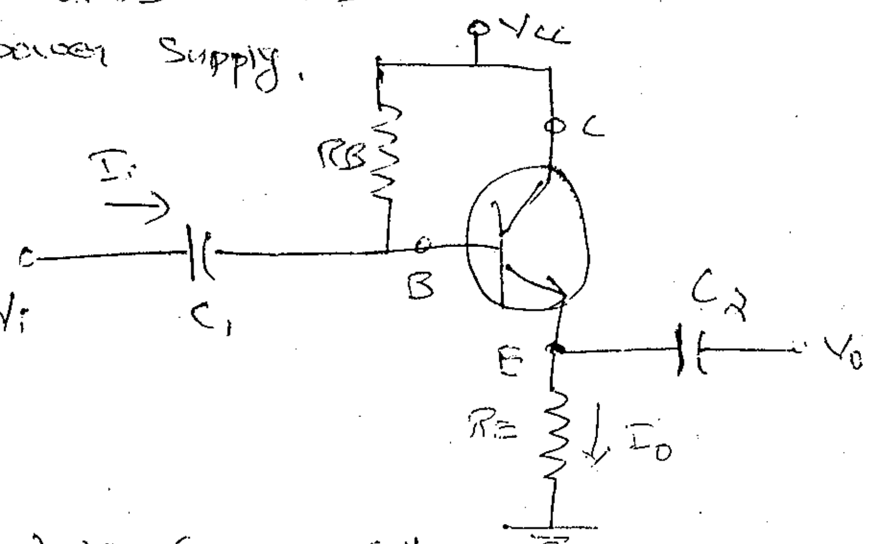


Fig 2.23 Common Collector Amplifier

Input Impedance, $Z_i = R_B || Z_b$, where $Z_b = h_{ie} + h_{fe} R_E$

$\approx h_{fe} R_E$

Output " , $Z_o = R_E || \frac{h_{ie}}{1 + h_{fe}}$

Voltage Gain, $A_v = \frac{R_E}{R_E + \left[\frac{h_{ie}}{1 + h_{fe}}\right]}$

Current Gain, $A_i = \frac{(h_{fe}) R_B}{R_B + Z_b}$

DARLINGTON CONNECTION

A very popular connection of two bipolar junction transistors for operation as one "Super beta" transistor is the Darlington connection shown in fig. 2.24. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of current gains of the individual transistors.

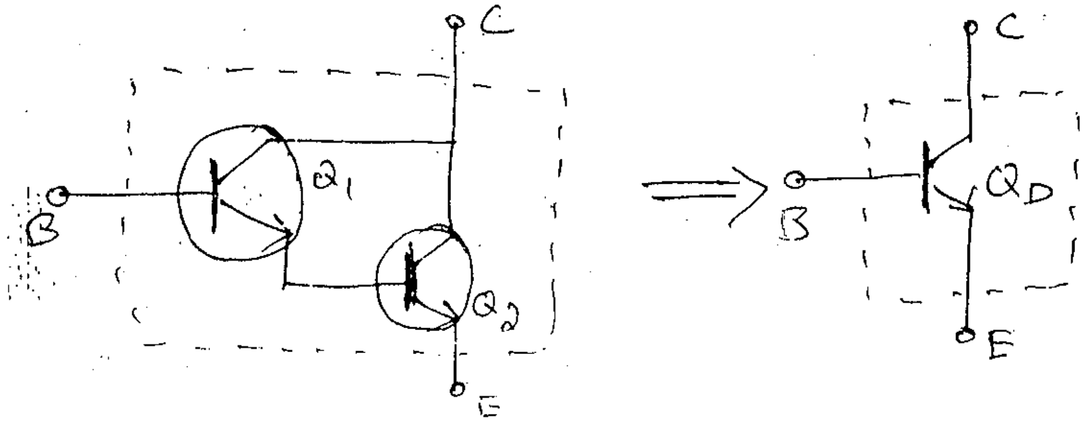


Fig 2.24 Darlington Combination.

If the connection is made using two separate transistors having current gains of β_1 & β_2, the Darlington connection provides a current gain of,

$$\boxed{\beta_D = \beta_1 \beta_2} \longrightarrow (1)$$

If the two transistors are matched, $\beta_1 = \beta_2 = \beta$,

the current gain of $\boxed{\beta_D = \beta^2} \longrightarrow (2)$

"A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand"

D: bias of Darlington Circuit

A basic Darlington circuits is shown in Fig 2.25.

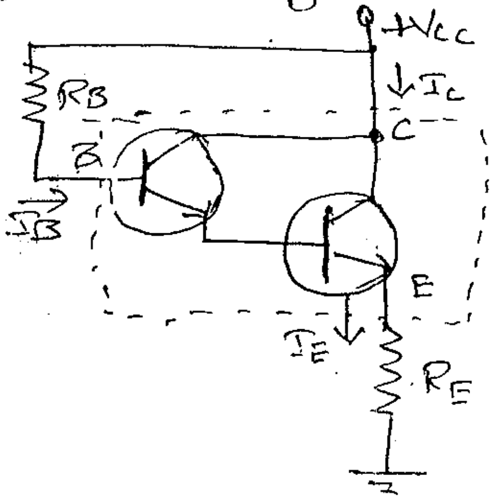


Fig 2.25 Basic Darlington bias circuit.

The base current, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}$ $\longrightarrow$ (3)

The emitter current, $I_E \approx (\beta_D + 1) I_B \approx \beta_D I_B$ $\rightarrow$ (4)

The dc voltages are, $V_E = I_E R_E$ $\longrightarrow$ (5)

$V_B = V_E + V_{BE}$ $\longrightarrow$ (6)

* In emitter follower, $\beta_D = \dfrac{I_E}{I_B}$.

AC Equivalent Circuit

A Darlington emitter-follower circuit is shown in Fig 2.26.

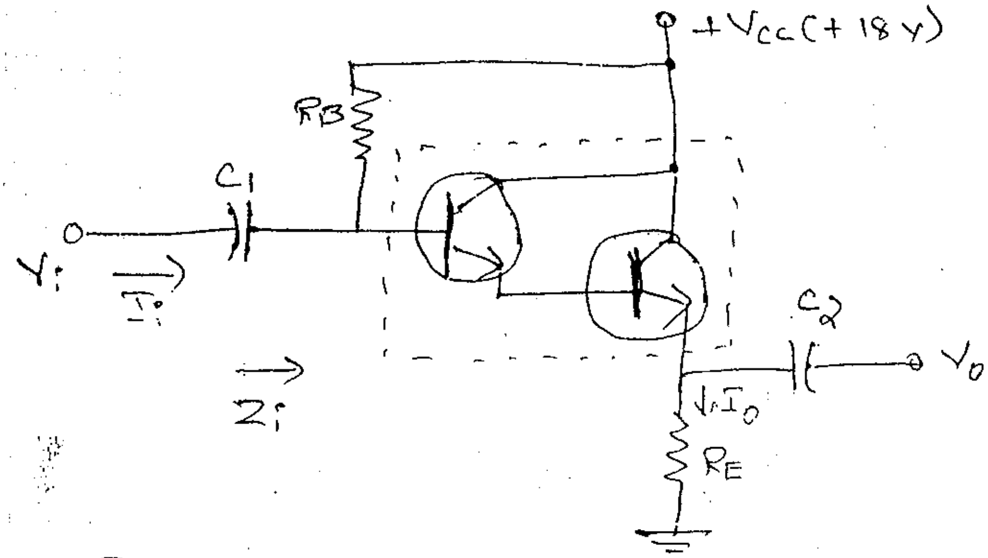


Fig 2.26 Darlington emitter-follower circuit.

Input Impedance [Z_i]

The Input impedance Can be determined using the equivalent network fig 2.27.

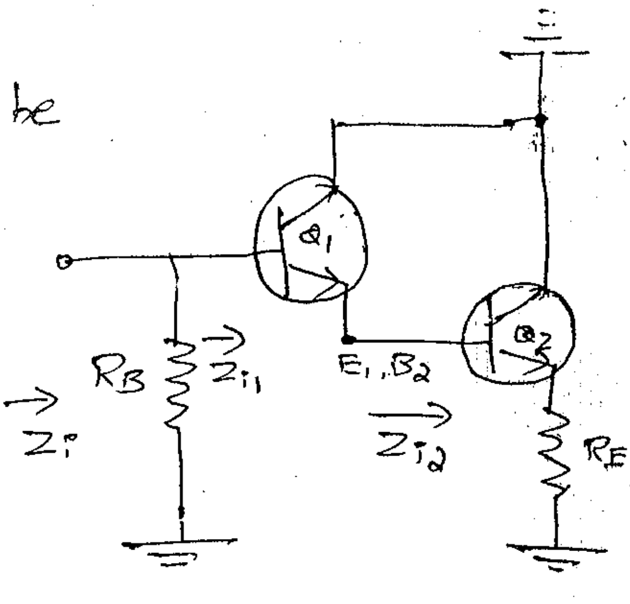


Fig 2.27

As defined in Fig 2.27,

$$Z_{i_2} = \beta_2(r_{e_2} + R_E)$$

$$Z_{i_1} = \beta_1(r_{e_1} + Z_{i_2})$$

& $$Z_{i_1} = \beta_1(r_{e_1} + \beta_2(r_{e_2}+R_E))$$

assume, $R_E \gg r_{e_2}$ and $Z_{i_1} = \beta_1(r_{e_1} + \beta_2 R_E)$

Since $\beta_2 R_E \gg r_{e_1}$ $\Rightarrow$ $Z_{i_1} \simeq \beta_1\beta_2 R_E$ $= \cancel{R_B}$

$\boxed{Z_i = R_B \| Z_{i_1}}$ $\rightarrow$ (7) $\boxed{Z_i = R_B \| \beta_1\beta_2 R_E}$

For $\beta_1 = \beta_2 = \beta$, $\boxed{Z_i = R_B \| \beta^2 R_E}$ $\rightarrow$ (8) (or) $\boxed{Z_i = R_B \| \beta_D R_E}$

Current Gain [A_i]

The current gain can be determined from the equivalent network of Fig 2.28.

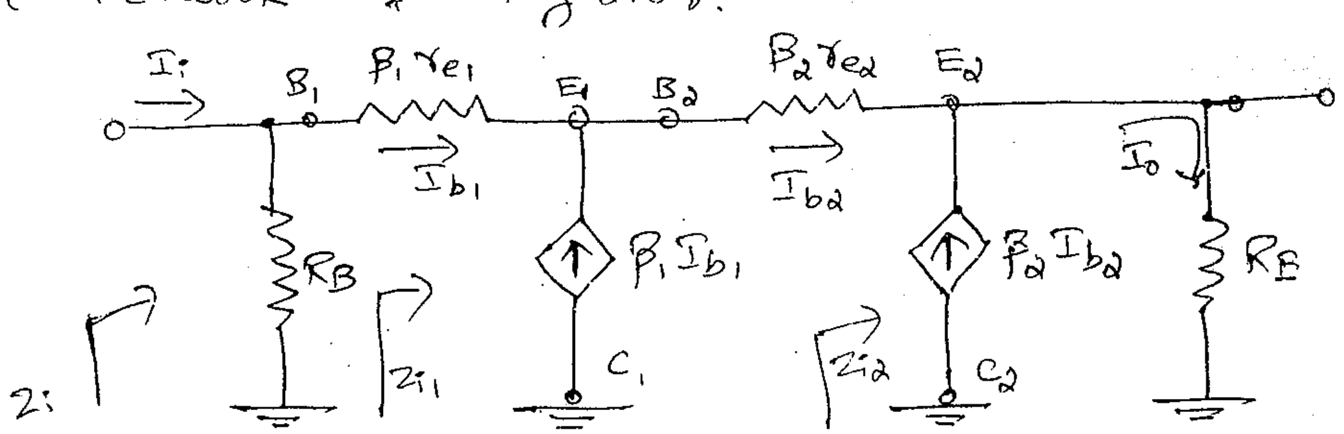


Fig 2.28 Determining A_i

Solving for the o/p current, $I_o = I_{b2} + \beta_2 I_{b2}$ (23)

$= (\beta_2+1) I_{b2}$

with, $I_{b2} = \beta_1 I_{b1} + I_{b1} = (\beta_1+1) I_{b1}$

then, $I_o = (\beta_2+1)(\beta_1+1) I_{b1}$

Using the current-divider rule on the i/p circuit:

$$I_{b1} = \frac{R_B}{R_B + Z_{i1}} I_i = \frac{R_B}{R_B + \beta_1\beta_2 R_E} \cdot I_i$$

and $I_o = (\beta_2+1)(\beta_1+1)\left(\frac{R_B}{R_B+\beta_1\beta_2 R_E}\right) I_i$

So that,
$$A_i = \frac{I_o}{I_i} = \frac{(\beta_1+1)(\beta_2+1) R_B}{R_B + \beta_1\beta_2 R_E}$$

Using $\beta_1, \beta_2 >> 1$

$$A_i = \frac{I_o}{I_i} \simeq \frac{\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_E} \simeq \boxed{\frac{\beta_D R_B}{R_B + \beta_D R_E}} \rightarrow (9)$$

Voltage Gain $[A_v]$

The voltage gain can be determined using Fig 2.28.

$V_o = I_o R_E$; $V_i = I_i(R_B \| Z_{i1})$.

$$R_B \| Z_{i1} = R_B \| \beta_D R_E = \frac{\beta_D R_B R_E}{R_B + \beta_D R_E}$$

$$A_v = \frac{V_o}{V_i} = \frac{I_o R_E}{I_i (R_B \| Z_i)} = (A_i)\left(\frac{R_E}{R_B \| Z_i}\right)$$

$$= \left[\frac{\beta_D R_B}{R_B + \beta_D R_E}\right]\left[\frac{R_E}{(R_B Z_{i1}/R_B+Z_{i1})}\right]$$

$$= \left(\frac{\cancel{\beta_D} R_B}{R_B + \beta_D R_E}\right)\left(\frac{\cancel{R_E}(R_B + \beta_D R_E)}{\cancel{R_B} \cdot \beta_D \cdot \cancel{R_E}}\right)$$

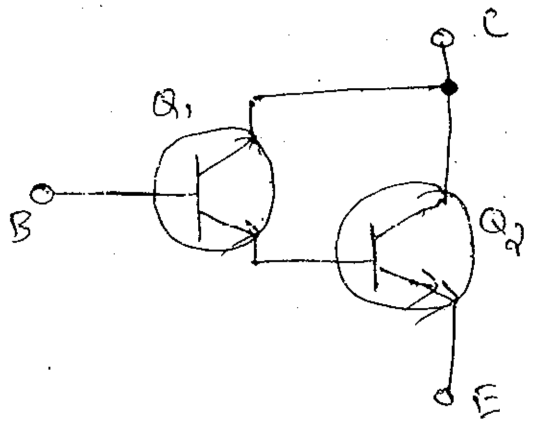
which is an expected result for emitter-follower configuration.

Output Impedance

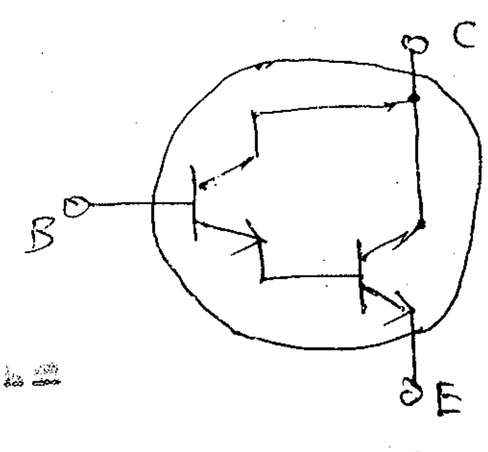
The output impedance will be determined by setting V_i to '0' and R_B is "shorted-out".

$$\boxed{Z_0 = \frac{r_{e_1}}{\beta_2} + r_{e_2}} \rightarrow (11)$$

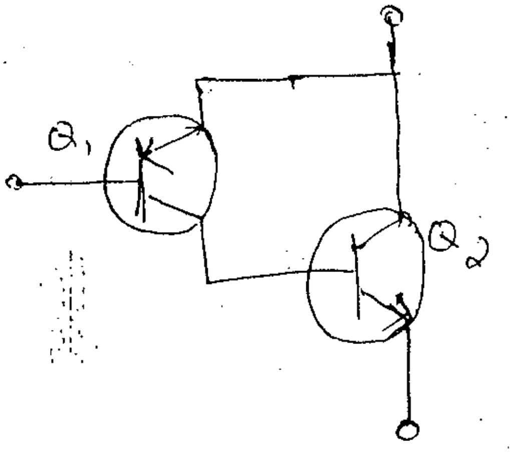
Darlington Connection using similar and complementary Transistors



(a) Darlington Pair (Similar)



(b) Darlington Transistor (Similar)



(c) Complementary Darlington.

MULTISTAGE AMPLIFIERS

If the voltage (or) power gain obtained from a single stage small signal amplifier is not sufficient for a practical application, one have to use more than one stage of amplification to achieve necessary voltage and power gain. Such an amplifier is called as "multistage amplifier". In multistage amplifier, the o/p of one stage is fed as the i/n to next as shown in Fig 2.29.

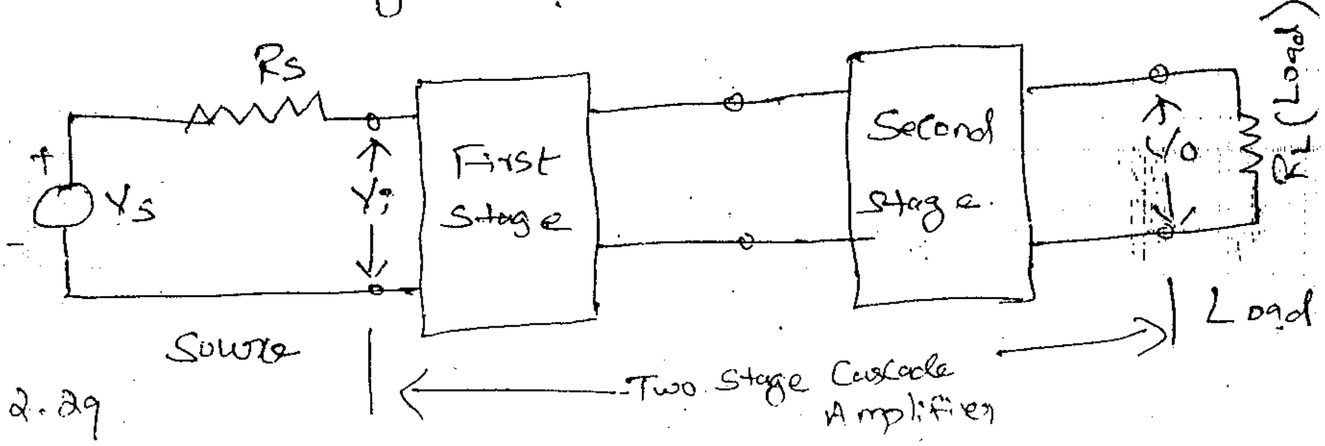


Fig 2.29

Different Coupling schemes used in Amplifiers

When amplifiers are cascaded, it's necessary to use a coupling network between the o/p of one amplifier and the i/n of the following amplifier. This type of coupling is called inter stage coupling. Basically, these coupling networks serve the following two purposes.

(i) It transfers the a.c. o/p of one stage to i/p of next stage.

(ii) It isolates the d.c. conditions of one stage to next.

Types:

1. Resistance - Capacitance (RC) Coupling
2. Transformer Coupling.
3. Direct "

1. RC Coupled Amplifier

Below Fig 2.30 shows the two stage RC Coupled common emitter amplifier.

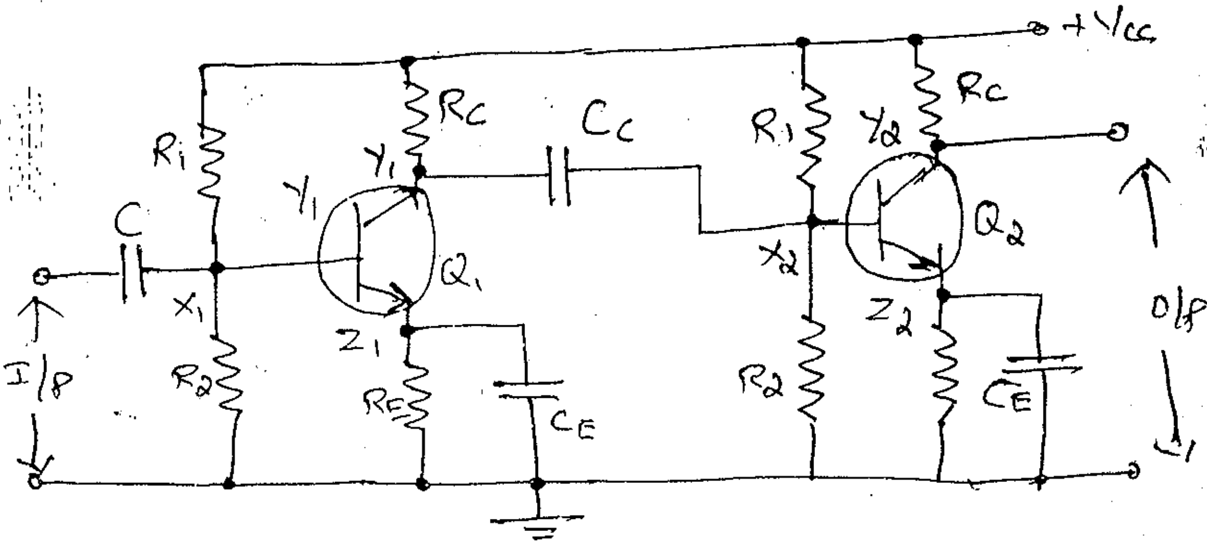


Fig 2.30 A two Stage RC coupled amplifier

It's phase is reversed and the amplified o/p appears across its Collector load Rc. The o/p of first stage across Rc is given to the base of second stage transistor Q_2 through the coupling capacitor Cc. This signal at the base of Q_2 is further amplified and its phase is again reversed. Hence the o/p signal is the twice amplified replica of i/n signal. The o/p signal is in phase with the i/n signal, because it has been reversed

Advantages:

1. It requires cheap components like resistors and capacitors and not expensive or bulky components. Hence it's small, light and inexpensive.

2. It gives uniform voltage amplification over a wide fr range from a few Hz to a few MHz because resistor values are independent of fr changes. It can be used in speech, music, etc.

3. It has minimum possible nonlinear distortion, since it does not use any coil or transformer.

Disadvantages:

1. Due to large drop across collector load resistors, the collectors work at relatively small voltages unless higher supply voltage is used to overcome this voltage drop.

2. It is noisy in humid weather.

3. The impedance matching is poor. (several hundred ohms)

Applications

Since audio fidelity is excellent, it is extensively used as a voltage amplifier.

2. Transformer Coupled Amplifier

Fig 2.31 shows the circuit diagram of multistage transformer coupled amplifier

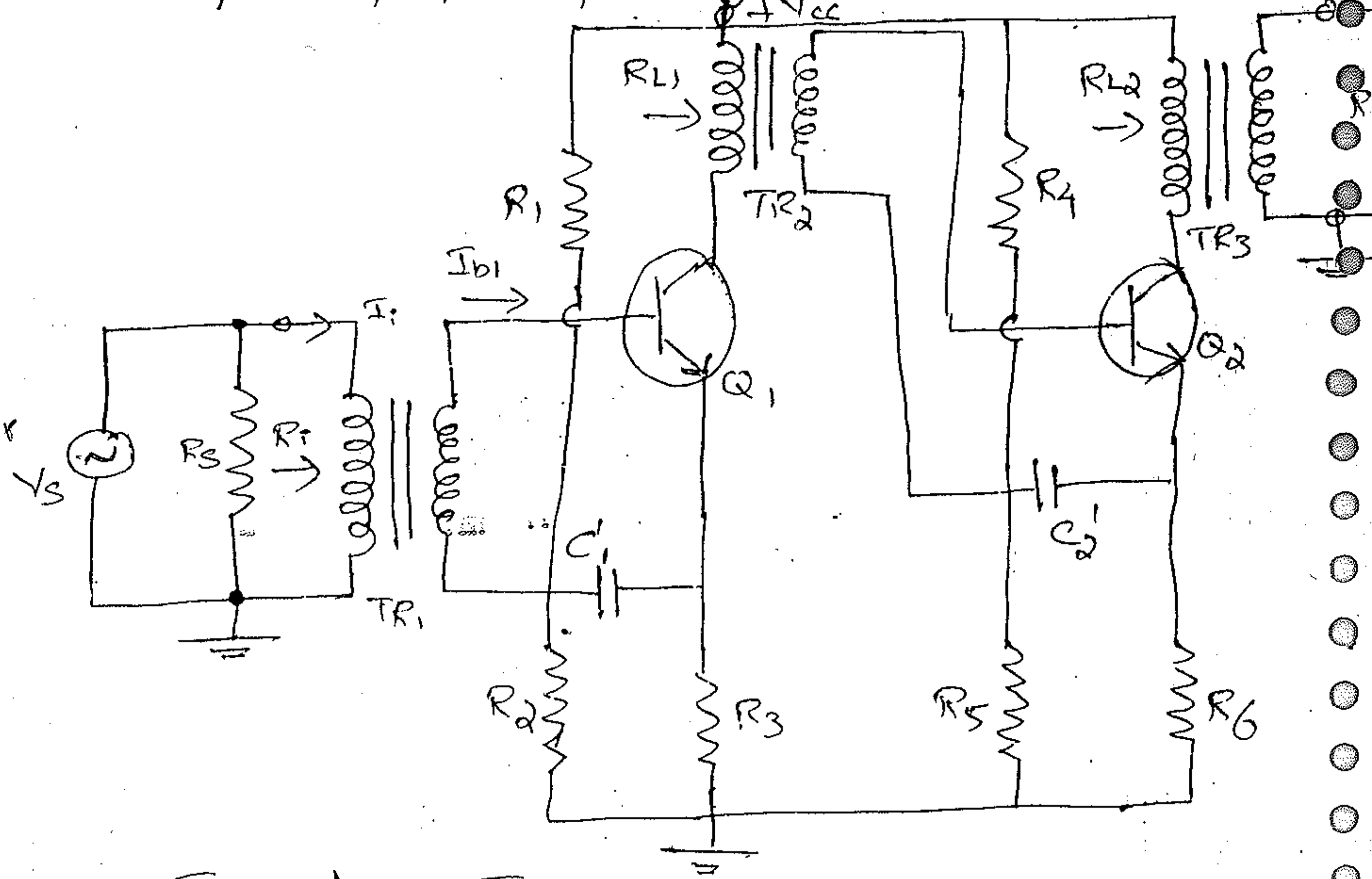


Fig 2.31 Transformer Coupled Amplifier.

~~Fig 2.31 Sho~~ A current source I_s with shunt resistance R_s drives the amplifier through the input transformer TR_1. The load resistor R_L is connected to the o/p circuit of the second amplifier stage through transformer TR_3. The transformer coupled amplifier may be used in the following three ways:

(i) As i/n stage usually driven by a microphone

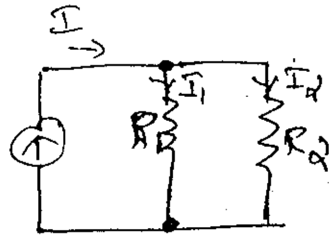
(ii) As o/p " feeding the load impedance

(iii) As intermediate stage.

The coupling of one stage to another may be made more effective by the use of transform...

impedance of the next. this impedance matching results in increased power gain. Further, this method of coupling isolates the load impedance circuit of the amplifier from d.c. bias stabilisation network of the next stage. For good results, it's necessary to shield the transformer against noise, hum and unwanted signal pickups.

Current Divider Rule



To find I_1,

$$I_1 = \frac{1/R_1}{1/R_1 + 1/R_2} \cdot I$$

$$= \frac{R_1 R_2}{(R_1+R_2) \cdot R_1} \cdot I$$

$$\boxed{I_1 = \frac{R_2}{R_1+R_2} \cdot I}$$

To find I_2,

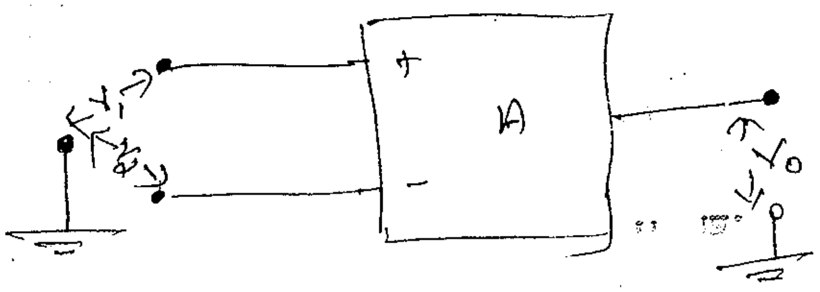
$$I_2 = \frac{1/R_2}{1/R_1 + 1/R_2} \cdot I$$

$$= \frac{R_1 R_2}{(R_1+R_2) \cdot R_2} \cdot I$$

$$\boxed{I_2 = \frac{R_1}{R_1+R_2} \cdot I}$$

[illegible]

DIFFERENTIAL AMPLIFIERS



The function of differential amplifier is to amplify the difference between two signals. The o/p signal in a differential amplifier is proportional to difference between two i/p signals,

$$V_o = A_d (V_1 - V_2) \rightarrow (i)$$

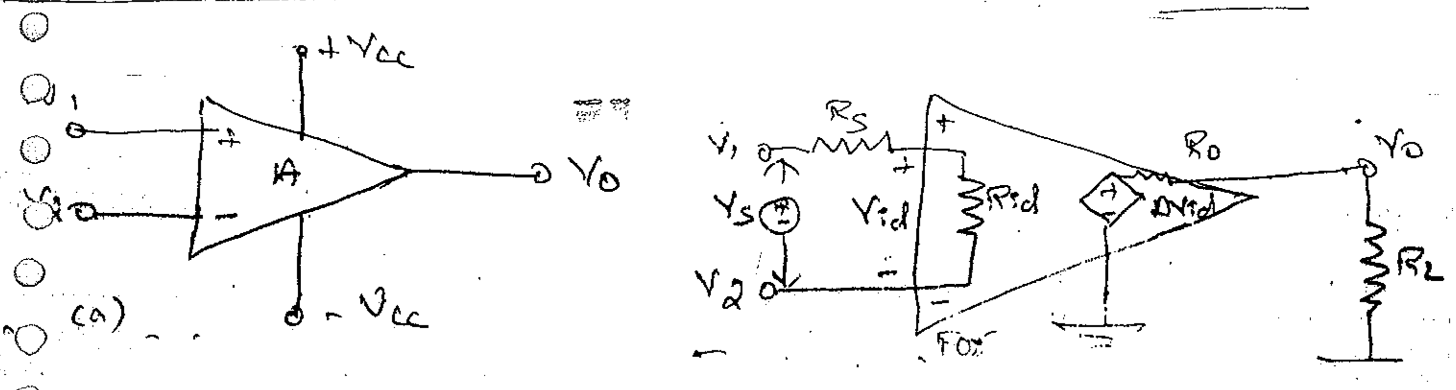
If $V_1 = V_2 \Rightarrow V_o$ is zero.

$V_1 \neq V_2 \Rightarrow V_o$ is non-zero.

The difference mode i/p voltage is defined as $V_d = (V_1 - V_2)$ & common mode i/p voltage is

$$V_{cm} = \left(\frac{V_1 + V_2}{2}\right)$$

Differential Amplifier using Operational Amplifier



The basic differential amplifier is shown in Fig 2.33. The amplifier has two i/p signals V_1 and V_2 and single output V_o. For the purpose of signal analysis they can be represented by it's input resistance R_i, output resistance R_o and controlled voltage source as shown in Fig 2.33(b).

The signal voltage developed at o/p of amplifier is in phase with voltage applied to positive i/p terminal and 180° out of phase to negative i/p terminal. The V_1 and V_2 terminals are therefore referred to as non-inverting input and inverting input respectively.

$$V_o \propto (V_1 - V_2) \quad (\text{ie}) \quad V_o = A(V_1 - V_2)$$

From fig 2.33(b), the Thevenin resistance,

$$R_{th} = \frac{R_L}{R_o + R_L} \quad ; \quad V_o = A V_{id} \frac{R_L}{R_o + R_L} \rightarrow (2)$$

An ideal differential amplifier produces an o/p that depends on voltage difference (V_{id}) b/w two i/p terminals and independent of source and load resistance,

$$\therefore \frac{R_L}{R_o + R_L} = 1$$

From eqn (2), $V_o = A V_{id} \Rightarrow A_v = \frac{V_o}{V_{id}} = A_d$

where, A_d is differential voltage gain.

$$\therefore V_o = A_v (V_1 - V_2)$$

A practical amplifier depends on average level called Common mode signal, $V_c = \frac{V_1 + V_2}{2}$

Considering the above, the o/p, $V_o = A_c V_c$.

where A_c is common mode gain.

Hence the total o/p of any differential amplifier,

$$\boxed{V_o = A_d V_{id} + A_c V_c} \rightarrow (3)$$

Common mode Rejection Ratio (CMRR)

One of the main requirements of the differential amplifier is to cancel (or) reject the noise signal that appears as a common input signal to both the input terminals of the differential amplifiers. Hence a figure of merit called Common Mode Rejection Ratio (CMRR) is introduced to define the ability of differential amplifier to reject a common mode signal.

$$CMRR = 20 \log_{10} \left| \frac{A_d}{A_c} \right|$$

In ideal cases, since $A_c = 0$, $CMRR = \infty$ and in practical cases, since $A_d >> A_c$ CMRR is high.

$$V_o = A_d V_{id} + A_c V_c$$

$$= A_d V_{id} \left[1 + \frac{A_c V_c}{A_d V_{id}} \right] = A_d V_{id} \left[1 + \frac{1}{(A_d / A_c)} \frac{V_c}{V_{id}} \right]$$

$$= A_d V_{id} \left[1 + \frac{1}{CMRR} \frac{V_c}{V_{id}} \right]$$

As CMRR approaches ∞, the o/p Voltage becomes,

$V_o = A_d V_{id}$.

Differential Amplifiers using BJT

The differential amplifiers using BJT are broadly classified into two types:

(i) Differential BJT amplifier with resistive loading

(ii) " " " " active "

AC analysis of an emitter - Coupled pair

The differential gain Ad, Common mode gain Ac, input and output resistances R_i and R_o can be obtained using the h-Parameter model.

Differential mode gain (A_d):

For the analysis, let the two input signals have a magnitude of $V_s/2$ and differ from each other by 180° as shown in below fig 2.36(b). The a.c equivalent ckt of fig 2.36(b) is shown in Fig 2.37, and a similar structure for Q_2 also.

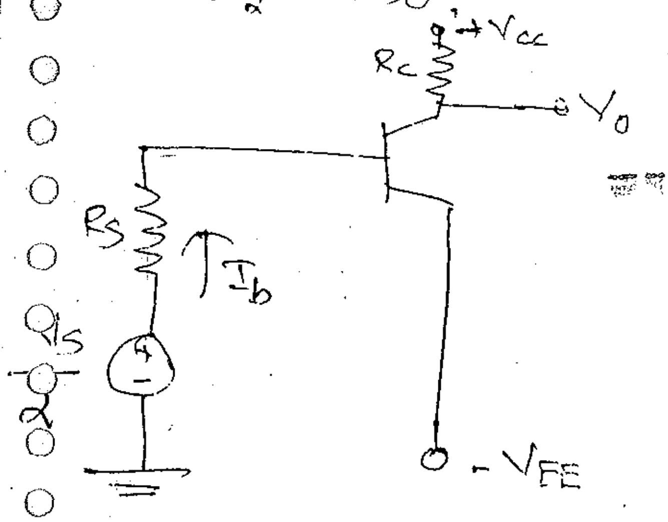


Fig 2.36(b) Ad Analysis

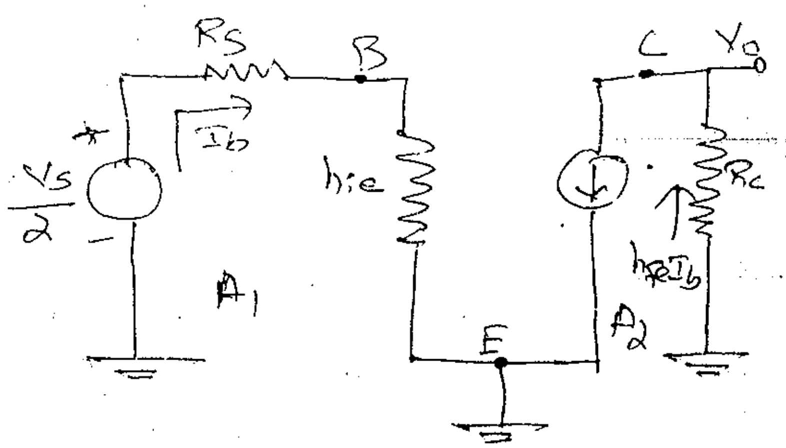


Fig 2.37 h-model

Applying KVL to loop A_1 (from fig 2.37), the input loop,

$$I_b(R_s+h_{ie}) = \frac{V_s}{2} \Rightarrow I_b = \frac{V_s}{2(R_s+h_{ie})}$$

Applying KVL to loop A_2, the o/p Voltage is

$$V_o = -h_{fe} I_b R_C = -h_{fe} R_C \frac{V_s}{2(R_s+h_{ie})}$$

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_C}{2(R_s + h_{ie})}$$

It's noted that minus sign indicates 180° phase difference between i/p and o/p.

$$V_{id} = V_1 - V_2 = \frac{V_s}{2} - \left(-\frac{V_s}{2}\right) = V_s.$$

$$\therefore \quad A_d = \frac{V_O}{V_{id}} = \frac{V_o}{V_s} = \frac{+h_{fe} R_C}{2(R_s + h_{ie})}$$

Ad for a balanced case can be derived by considering the balanced o/p across the two collectors of Q_1 and Q_2, which are assumed to be perfectly matched. Ad for such a condition,

$$A_d = \frac{2 h_{fe} R_C}{2(R_s + h_{ie})} = \frac{h_{fe} R_C}{(R_s + h_{ie})}$$

Common mode gain (Ac)

$$A_c = \frac{-R_c h_{fe}}{R_s + h_{ie} + 2R_E(1 + h_{fe})}$$

Common mode Rejection Ratio (CMRR)

$$CMRR = 20\log_{10}\left|\frac{A_d}{A_c}\right| = 20\log_{10}\left|\frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{R_s + h_{fe}}\right|$$

for balanced case

$$= 20\log_{10}\left|\frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{2(R_s + h_{ie})}\right|$$

Input Impedance (R_i) and Output Impedance (R_o)

$$R_i = \frac{V_s}{I_b} = R_s + h_{ie}$$ (~~one~~ single transistor unbalanced case)

For two transistors (balanced case), $R_i = 2(R_s + h_{ie})$

Output Impedance, $\boxed{R_o = R_c}$

BODE PLOT ANALYSIS

The cut-off frequencies of single stage BJT amplifiers are influenced by the R-C combination formed by the network capacitors C_C, C_E etc., and the resistive parameters that are present in the network.

A methodology for determining the lower cut-off frequency (f_1) will be presented and the circuit is shown in Fig 3.3

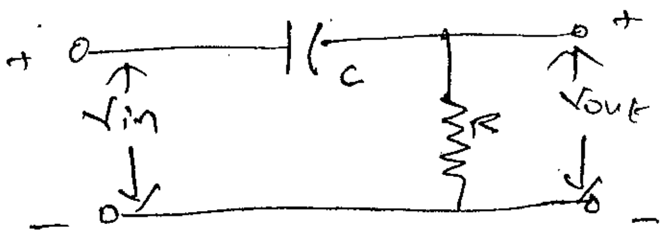


Fig 3.3

Fig. Equivalent circuit for lower cut-off frequency analysis.

At high frequencies, $X_C = \frac{1}{2\pi fC} \simeq 0\,\Omega$ (short)

At Low ", $X_C = \frac{1}{2\pi fC} \simeq \infty\,\Omega$ (open)

The above fig can be approximated as,

A typical frequency response between the above two extremes is as shown.

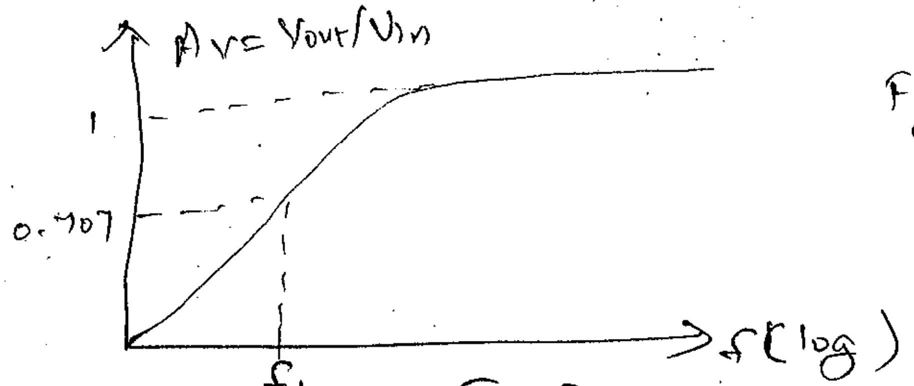


Fig. Av VS frequency

Fig 3.4

Applying VDR to above fig.

$$V_{out} = \frac{R V_{in}}{R - jX_c} \rightarrow (1)$$

where, magnitude of V_{out} is given by,

$$|V_{out}| = \frac{R V_{in}}{\sqrt{R^2 + X_c^2}} \rightarrow (2)$$

(i) when $X_c = R$

$$|V_{out}| = \frac{R V_{in}}{\sqrt{R^2 + R^2}} \Rightarrow |V_{out}| = \frac{1}{\sqrt{2}} V_{in} \rightarrow (3)$$

WKT, ~~From~~, $|A_v|_{mid} = \left| \frac{V_{out}}{V_{in}} \right|$

$$|A_v| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}} \frac{V_{in}}{V_{in}} = \frac{1}{\sqrt{2}} = 0.707$$ at $X_c = R$.

$\rightarrow (4)$

so
Now, as per assumption,

$$X_c = R \Rightarrow \frac{1}{2\pi f_1 C} = R \Rightarrow f_1 = \frac{1}{2\pi RC} \rightarrow (5)$$

From eqn (1) $A_v = \frac{V_{out}}{V_{in}} = \frac{R}{R - jX_c} \rightarrow (6)$

$$= \frac{R}{R - jX_c} = \frac{\cancel{R}}{\cancel{R}(1 - j(X_c/R))} = \frac{1}{1 - j(X_c/R)}$$

$$= \frac{1}{1 - j\left(\frac{1}{2\pi f C R}\right)} \rightarrow (7)$$

Substituting eqn (5) into (7),

$$A_v = \frac{1}{1-j(f_1/f)} \rightarrow (8)$$

when $f = f_1$

$$|A_v| = \frac{1}{\sqrt{1+(1)^2}} = \frac{1}{\sqrt{2}} = 0.707, \ (-3dB). \rightarrow (9)$$

In general,
'A_v' can be written in magnitude and phase form.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1+(f_1/f)^2}} \underline{\angle \tan^{-1}(f_1/f)} \rightarrow (10)$$

In logarithmic form (dBs),

$$|A_v|_{dB} = 20\log_{10}\frac{1}{\sqrt{1+(f_1/f)^2}} = -10\log_{10}\left[1+\left(\frac{f_1}{f}\right)^2\right] \rightarrow (11)$$

If ~~$f_1 \gg f$~~, $(f_1/f)^2 \gg 1$

$$|A_v|_{dB} = -10\log_{10}\left(\frac{f_1}{f}\right)^2 = -20\log_{10}\left(\frac{f_1}{f}\right) \rightarrow (12)$$

If $f \ll f_1$,

when, $f = f_1$; $\frac{f_1}{f} = 1 \Rightarrow |A_v|_{dB} = -20\log_{10} 1 = 0dB$

when, $f = \frac{1}{2}f_1$; $\frac{f_1}{f} = 2 \Rightarrow |A_v|_{dB} = -20\log_{10} 2 = -6dB$

$f = \frac{1}{4}f_1$; $\frac{f_1}{f} = 4 \Rightarrow |A_v|_{dB} = -20\log_{10} 4 = -12dB$

A plot of these values is shown in Fig

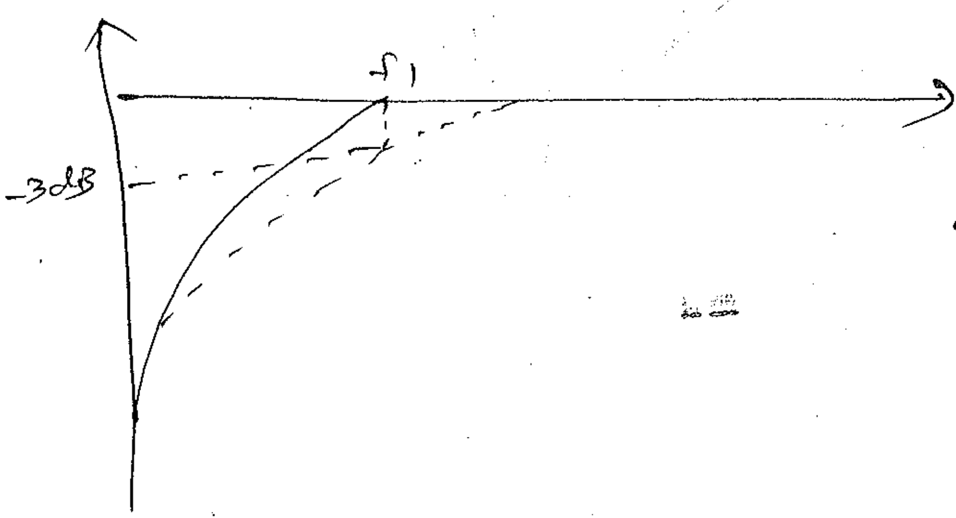


Fig 3.5

LOW-FREQUENCY RESPONSE - BJT AMPLIFIER

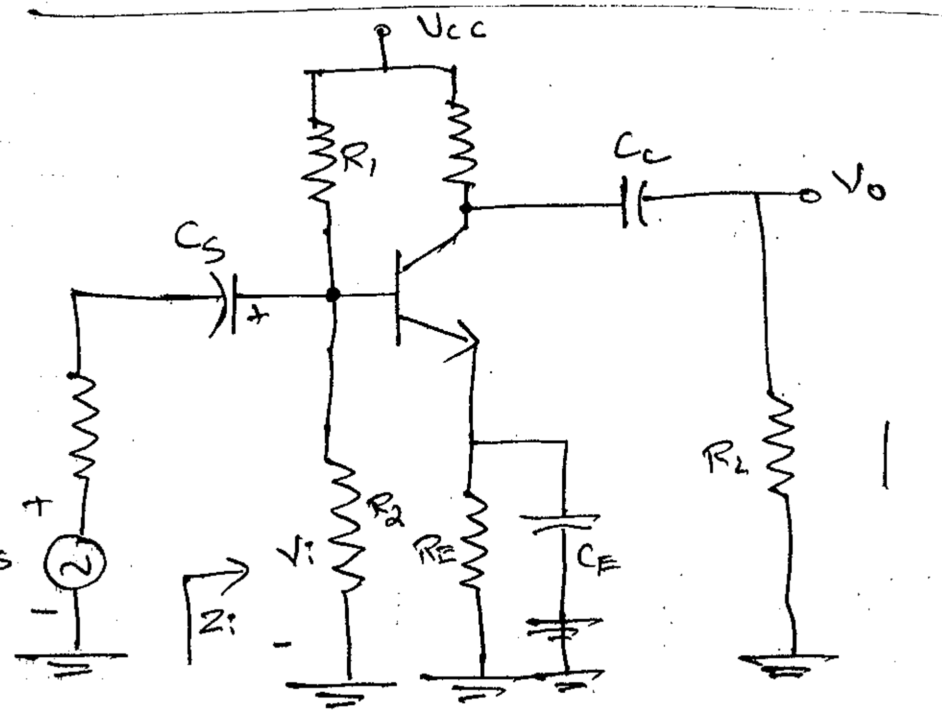


Fig. 3.6

For the network of Fig 3.6 the capacitors C_s, C_c, and C_E will determine the low-frequency response.

C_S (Source Capacitor)

C_s is normally connected between the applied source and the active device, the general form of RC configuration is established by network of Fig 3.7

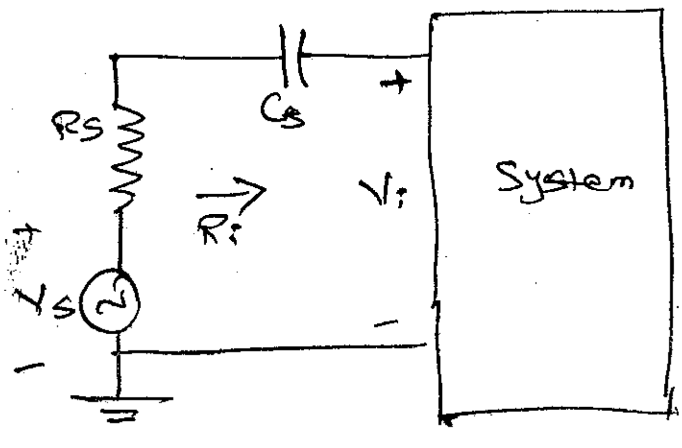


Fig. 3.7.

Applying the voltage-divider rule:

$$V_i = \frac{R_i V_s}{R_s + R_i - jX_{C_s}} \longrightarrow (1)$$

Rewriting eqn (1),

$$\frac{V_i}{V_s} = \frac{R_i}{R_s + R_i - jX_{C_s}} = \frac{1}{1 + \frac{R_s}{R_i} - j\frac{X_{C_s}}{R_i}}$$

$$= \frac{1}{\left(1 + \frac{R_s}{R_i}\right)\left[1 - j\frac{X_{C_s}}{R_i}\left(\frac{1}{1 + \frac{R_s}{R_i}}\right)\right]} = \frac{1}{\left(1 + \frac{R_s}{R_i}\right)\left(1 - j\frac{X_{C_s}}{R_i + R_s}\right)}$$

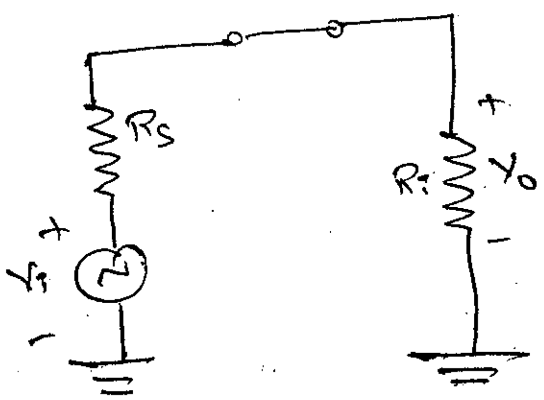
The factor,

$$\frac{X_{C_s}}{R_i + R_s} = \left(\frac{1}{2\pi f C_s}\right)\left(\frac{1}{R_i + R_s}\right) = \frac{1}{2\pi f (R_i + R_s) C_s}$$

WKT, $f_i = \frac{1}{2\pi (R_i + R_s) C_s}$ $\Rightarrow$ we have $\frac{V_i}{V_s} = \frac{1}{\left(1 + \frac{R_s}{R_i}\right)\left(1 - j\frac{f_i}{f}\right)}$

$$A_v = \frac{V_i}{V_s} = \left[\frac{R_i}{R_i + R_s}\right]\left[\frac{1}{1 - j(f_i/f)}\right]$$

For the midband f_r, the network will appear as



$$\boxed{A_{v\,mid} = \frac{V_o}{V_i} = \frac{R_i}{R_i + R_s}} \longrightarrow (2)$$

and $\frac{A_v}{A_{v\,mid}} = \frac{1}{1 - j(f_i/f)}$

The cutoff frequency is defined by f_i,

$$\boxed{f_{L_s} = \frac{1}{2\pi (R_s + R_i) C_s}} \longrightarrow (3)$$

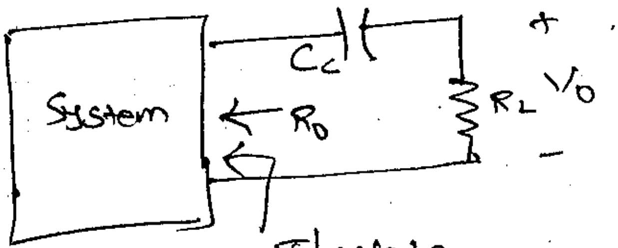
C_c (Coupling Capacitor)

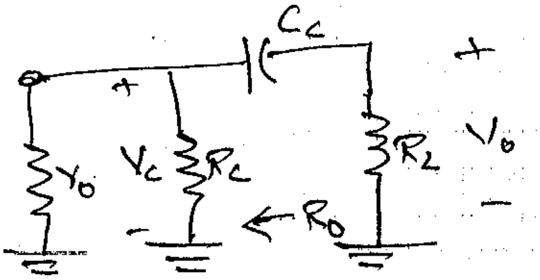
The coupling capacitor is normally connected between the output of active device and the applied load. The total series resistance is now $R_o + R_L$, and the cut off frequency due to C_c,

$$\boxed{f_{Lc} = \frac{1}{2\pi (R_o + R_L) C_c}} \longrightarrow (4)$$

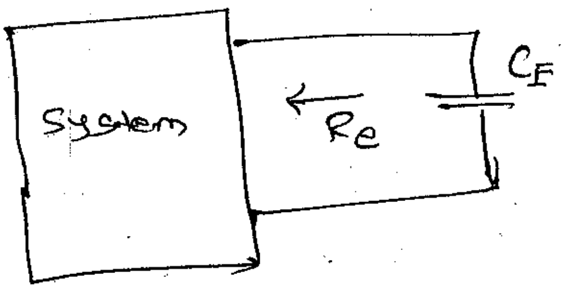
Ignoring the effects of C_s and C_E, we have that the o/p voltage V_o will be 70.7% of its midband value at f_{Lc}.

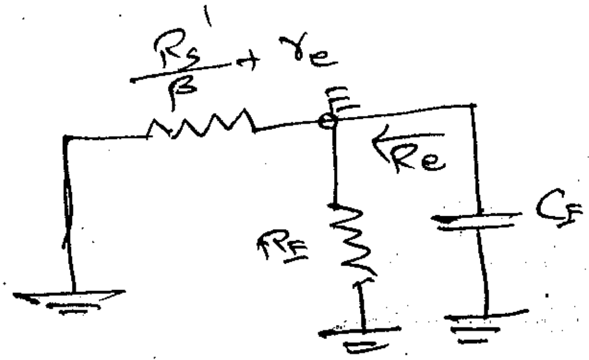
$$\boxed{R_o = R_c \,||\, r_o} \longrightarrow (5)$$





C_E (Emitter bypass capacitor)





The cut off fr due to C_E can be determined, using

$$\boxed{f_{LE} = \frac{1}{2\pi R_e C_E}} \longrightarrow (6)$$

$$\boxed{R_e = R_E \,||\, \left(\frac{R_s'}{\beta} + r_e\right)} \longrightarrow (7)$$

where,

$R_s' = R_s \,||\, R_1 \,||\, R_2$

LOW-FREQUENCY RESPONSE - FET AMPLIFIER

The analysis of FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier, the frequency response of FET is depends upon the three capacitors, C_G, C_C, C_S as shown in the figure Fig 3.7

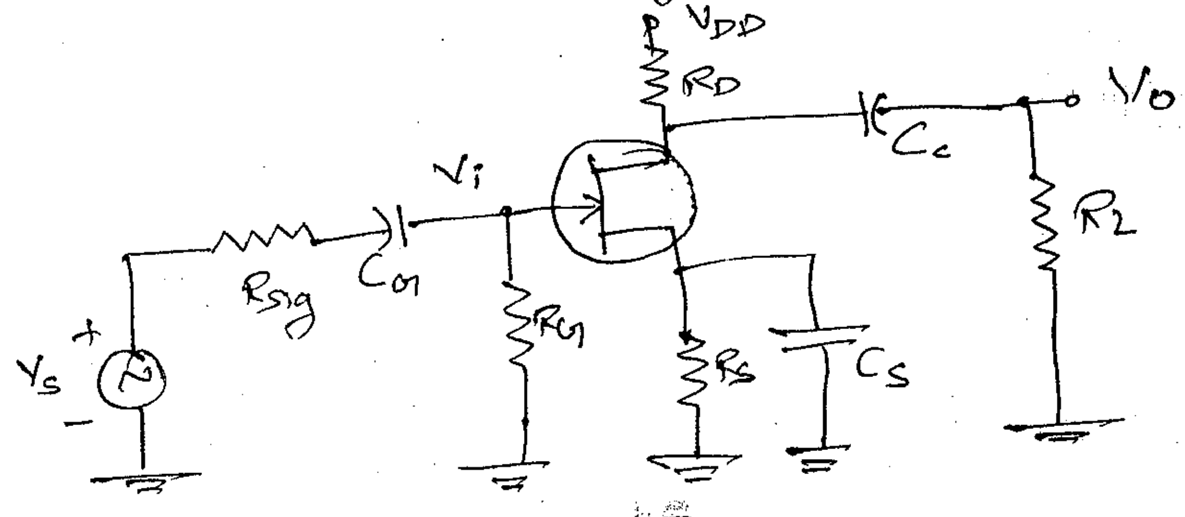


Fig 3.7 JFET Amplifier.

C_G (Gate Capacitor)

The coupling capacitor between the source and the active device, the ac equivalent networks is shown in Fig 3.8.

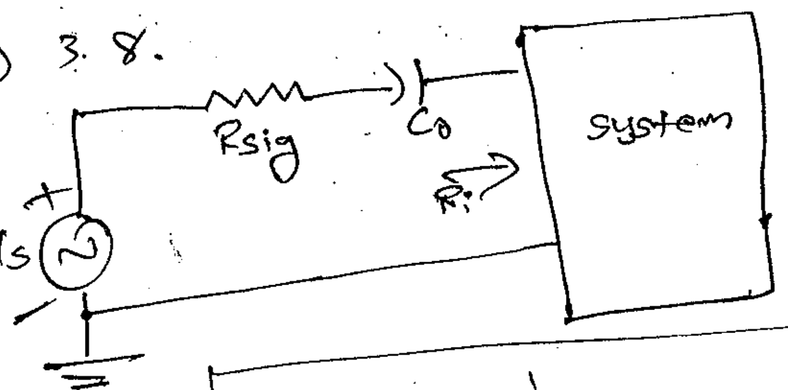


Fig 3.8

$$\boxed{f_{LG} = \frac{1}{2\pi (R_{sig} + R_i) C_G}} \rightarrow (1)$$

The eqn (1) is similar to low frequency response of BJT

$$\boxed{R_i = R_G} \rightarrow (2)$$

Typically, $R_G \gg R_{sig}$, and the lower cut off frequency is determined primarily by R_G and C_G.

C_c (Coupling Capacitor)

For the coupling capacitor between the active device and the load ~~the~~ as shown in Fig 3.9. The resulting cut off frequency is,

$$\boxed{f_{Lc} = \frac{1}{2\pi(R_o + R_L)C_c}} \rightarrow (2)$$

$$\boxed{R_o = R_D \| r_d} \rightarrow (3)$$

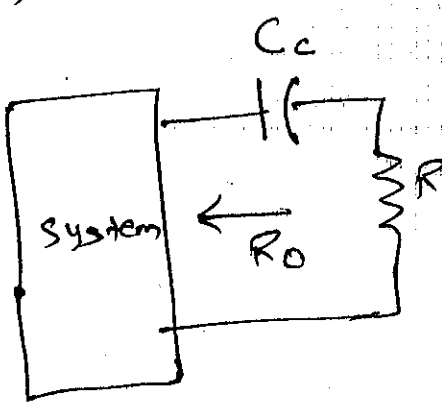


Fig 3.9.

C_s (Source Capacitor)

The cut off frequency, $\boxed{f_{Ls} = \frac{1}{2\pi R_{eq} C_s}} \rightarrow (4)$

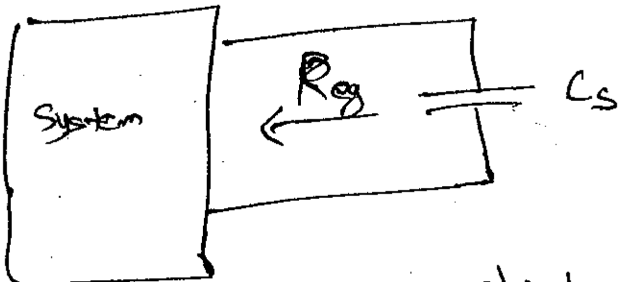


Fig 3.10

$$R_{eq} = \frac{R_s}{1 + R_s(1 + g_m r_d)/(r_d + R_D \| R_L)}$$

which for $r_d = \infty\ \Omega$ becomes,

$$\boxed{R_{eq} = R_s \| \frac{1}{g_m}} \rightarrow (5)$$

HIGH - FREQUENCY RESPONSE - BJT AMPLIFIER

At the high-frequency end, there are two factors that define the $-3dB$ cut off point;

(i) the network capacitance (parasitic and introduced)

(ii) the frequency dependence of $h_{fe}(\beta)$.

(i) Network parameters

The most significant difference is in the following general form of A_v:

$$A_v = \frac{1}{1+j(f/f_2)} \longrightarrow (1)$$

this results in a magnitude plot as shown in Fig 3.12.

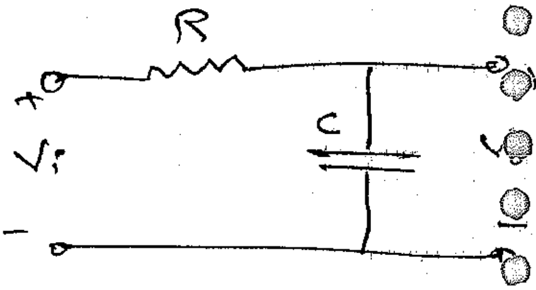


Fig 3.11 R-C combination defines high cut off frequency.

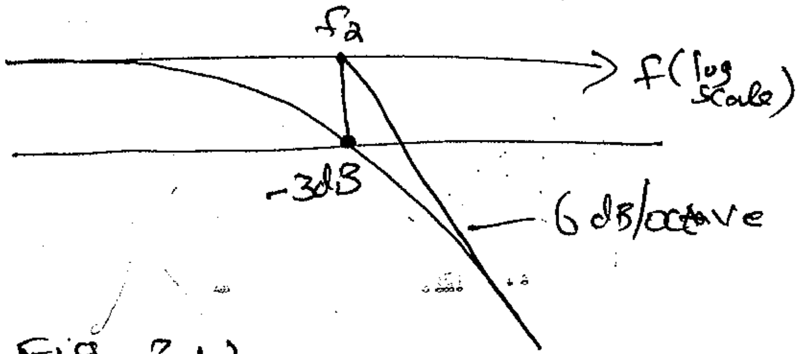


Fig 3.12

Parasitic capacitances — C_{be}, C_{bc}, C_{ce}

Wiring " — C_{wi}, C_{wo}

External " — C_s, C_C, C_E

In general, $C_{be} \gg C_{ce}$.

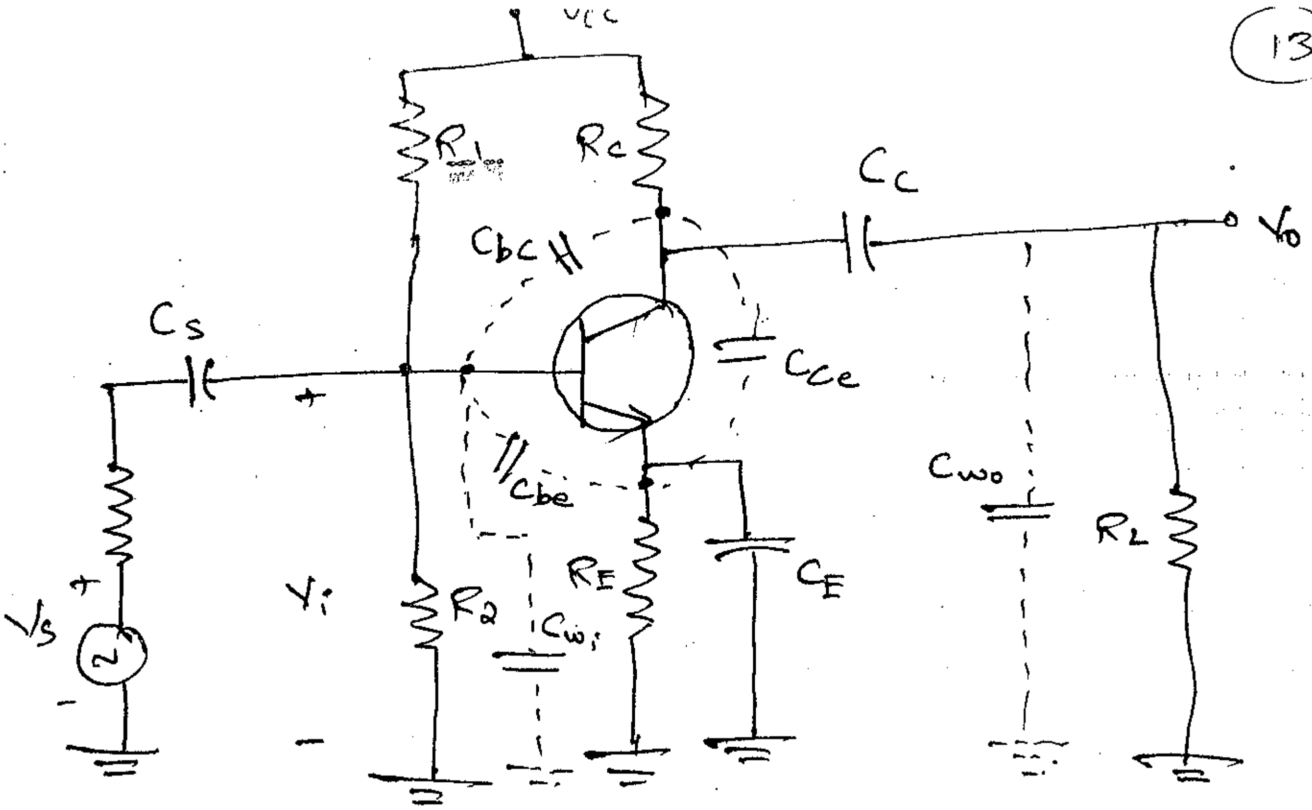


Fig 3.13 High fr Response – BJT Amplifier

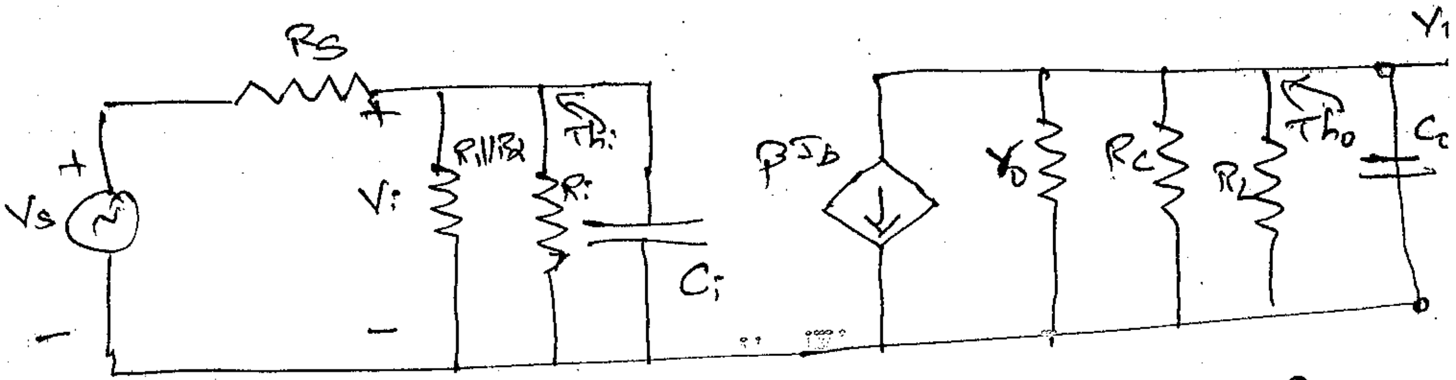


Fig 3.14 High fr ac equivalent model.

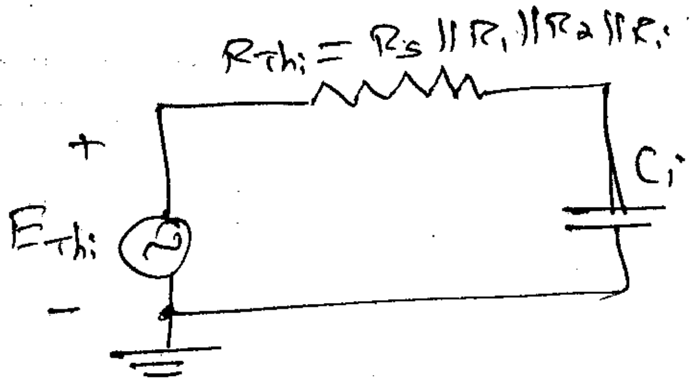
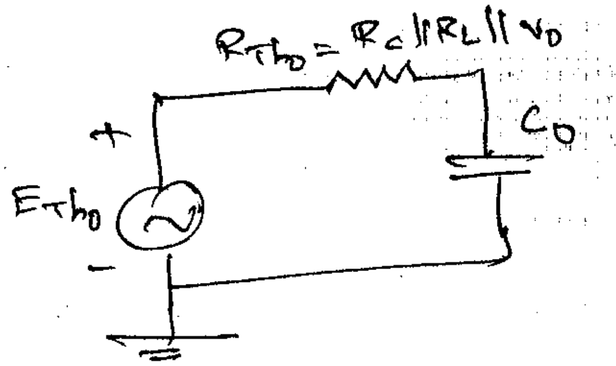


Fig 3.15 (a) Thevenin Eqv Input Side



(b) Thevenin Eqv Output Side

$\boxed{R_{Th_i} = R_S \parallel R_1 \parallel R_2 \parallel R_i} \longrightarrow (2) \quad f_{H_i} = \frac{1}{2\pi R_{Th_i}}$

$C_i = C_{wi} + C_{be} + C_{M_i} = C_{wi} + C_{be} + (1 - A_v) C_{bc}$

$\longrightarrow (3)$

For the O/P network,

$$f_{H_o} = \frac{1}{2\pi R_{Th_o} C_o} \longrightarrow (4)$$

$R_{Th_o} = R_C \parallel R_L \parallel r_o$ and $C_o = C_{wo} + C_{ce} + C_{M_o}$

$= C_{wo} + C_{ce} + (1 - 1/A_v) C$

$1 >> 1/A_v \Rightarrow C_o \approx C_{wo} + C_{ce} + C_{bc}$.

HIGH FREQUENCY RESPONSE - FET AMPLIFIER

The analysis of high-frequency response of FET amplifier will proceed in a very similar manner of BJT amplifier.

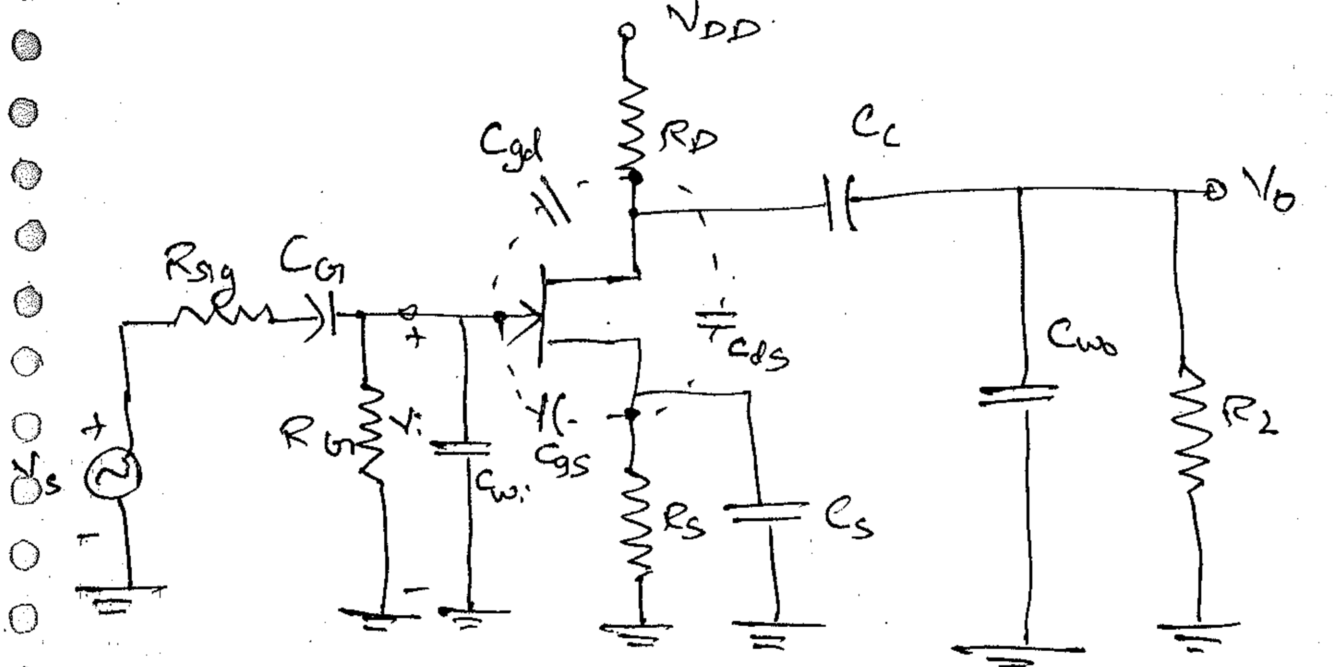


Fig 3.16 High frequency Response - FET Amplifier

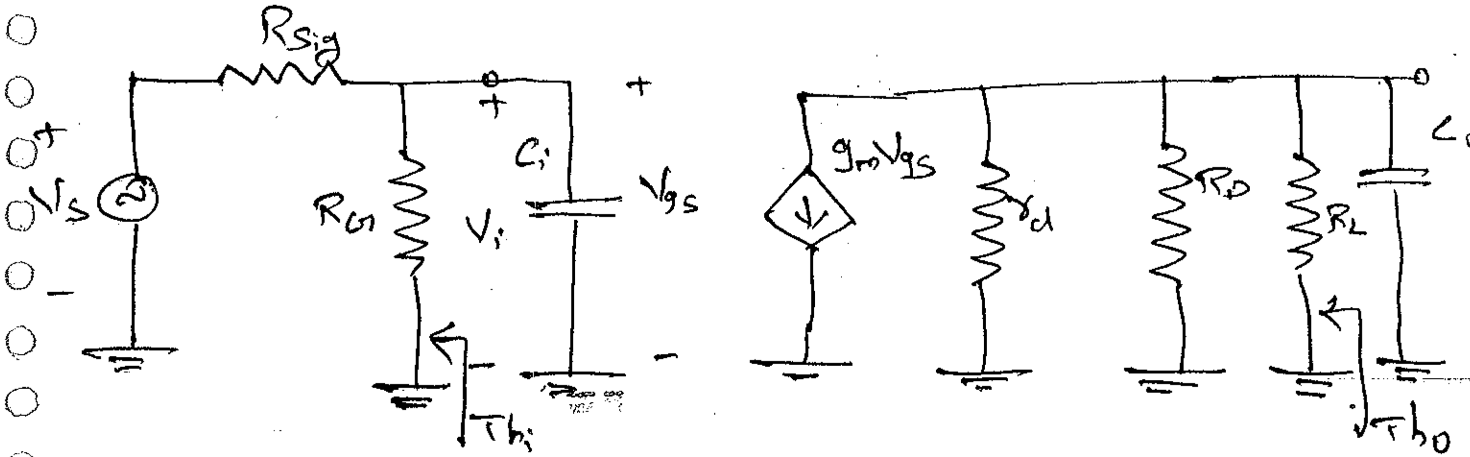


Fig 3.17 AC equivalent circuit.

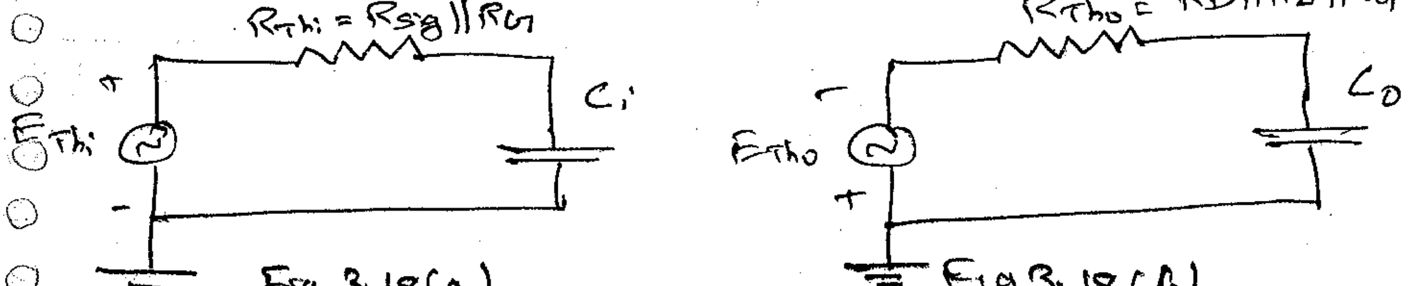


Fig 3.18(a) Fig 3.18(b)

$$\boxed{f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}} \rightarrow (1) \quad \text{and}$$

$R_{Thi} = R_{sig} \parallel R_G$ and $C_i = C_{wi} + C_{gs} + C_{Mi}$

where, $C_{Mi} = (1 - A_v)\, C_{gd}$.

For the output circuit,

$$\boxed{f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}} \rightarrow (2) \quad \text{and}$$

$R_{Tho} = R_D \parallel R_L \parallel r_d$ and $C_o = C_{wo} + C_{ds} + C_{Mo}$

where, $C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$.

UNIT-IV LARGE SIGNAL AMPLIFIERS

[POWER AMPLIFIERS]

Large Signal (or) Power amplifiers, Primarily provide Sufficient Power to an output Load to drive a Speaker (or) other power device, typically a few watts to tens of watts. The main feature of a large-Signal amplifier are the Circuits power efficiency, the maximum amount of power that the circuit is Capable of handling, and the impedance matching to the output device, whereas a Small Signal amplifier provides Voltage amplification primarily to increase the Voltage of input signal.

One method used to Categorize amplifiers is by class. Basically, amplifier classes represent the amount the output Signal Varies over one cycle of operation for a full cycle of input signal.

Class A:

The output Signal Varies for a full 360° of the cycle. Fig 4.1a Shows that this requires the Q-Point to be biased at a level So that at least half the signal Swing of the output may Vary up and down without going to a high enough Voltage to be limited by the supply Voltage level (or) too low to approach the lower Supply level, (or) 0V.

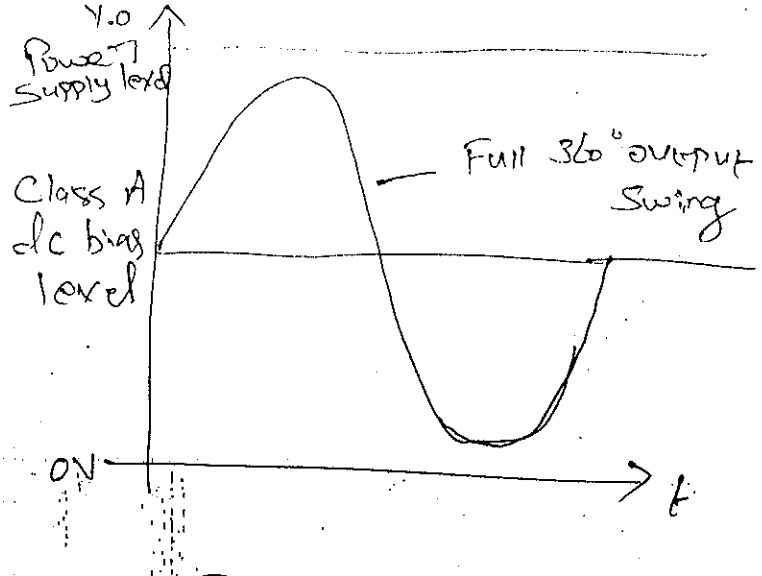


Fig 4.1a class A

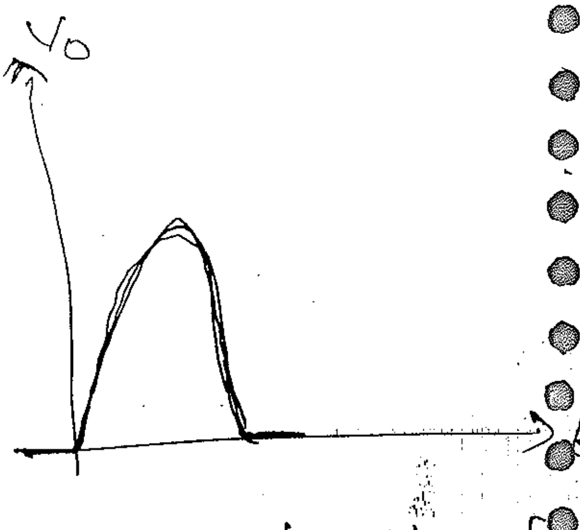


Fig 4.1 b class B

Class B

A class B circuit provides an output signal varying over one-half the input signal cycle, on for 180° of signal as shown in Fig 4.1b. The dc bias level for class B is at 0V. Two class B operations one to provide output on positive output half cycle and another to provide ~~an~~ on the negative output half-cycle. The combined half-cycles then provide an output for a full 360° of operation is known as Push Pull operation.

Class AB

An amplifier may be biased at a dc level above the zero-base current level of class B and above one half the supply voltage level of class A. So class AB, the output signal swing occurs between 180° and 360°

Class C

The output of class C amplifier is biased for operation at less than 180° of cycle and will operate only with a tuned circuit

SERIES-FED CLASS A AMPLIFIER (Class A - RC Coupled Amplifier)

The Simple fixed-bias Circuit is shown in Fig 4.2. The only difference between this circuit and the small-signal version is the signals handled by the large-signal circuit are in the range of few to ten of volts and the transistor used is a Power transistor in the range of few to ten of watts.

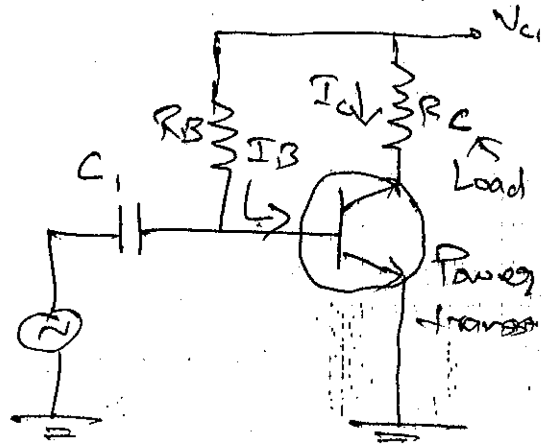


Fig 4.2 Series-fed class A large-signal amplifier.

DC Bias operation

Base-Bias Current,

$$I_B = \frac{V_{CC} - 0.7V}{R_B} \rightarrow (1)$$

Collector Current, $I_C = \beta I_B \rightarrow (2)$

Collector-emitter Voltage,

$$V_{CE} = V_{CC} - I_C R_C \rightarrow (3)$$

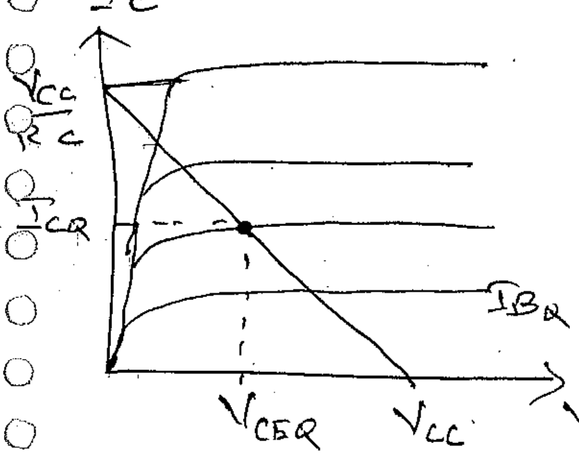


Fig 4.3 DC Load line

Point, A @ $I_C = 0 \Rightarrow V_{CC} = V_{CE}$

Point, B @ $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C}$

AC operation

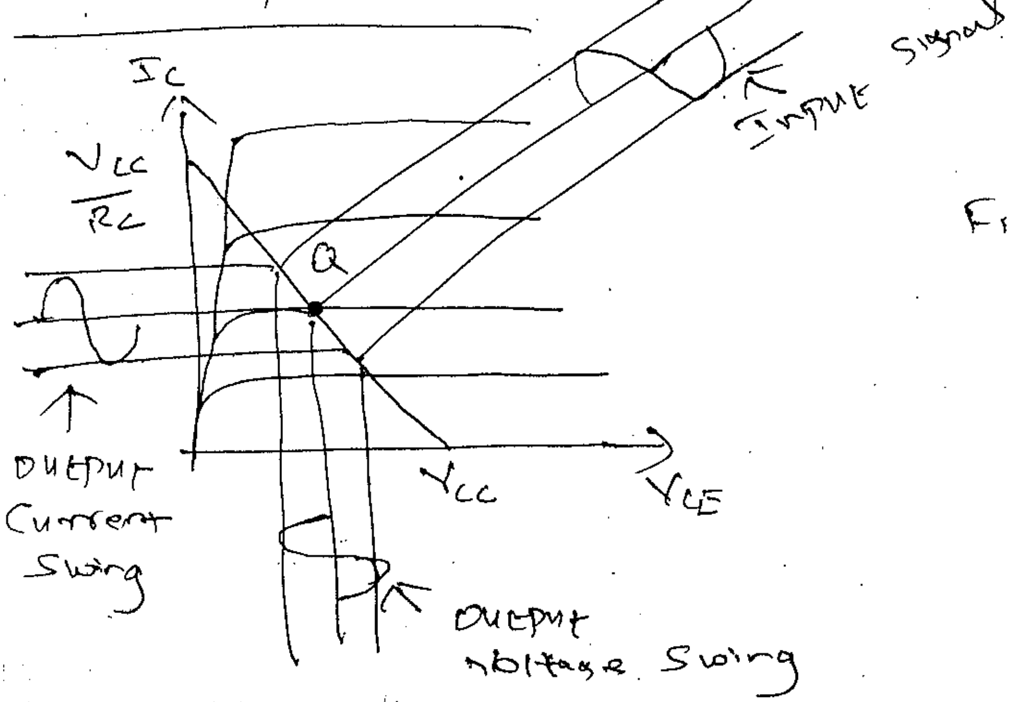
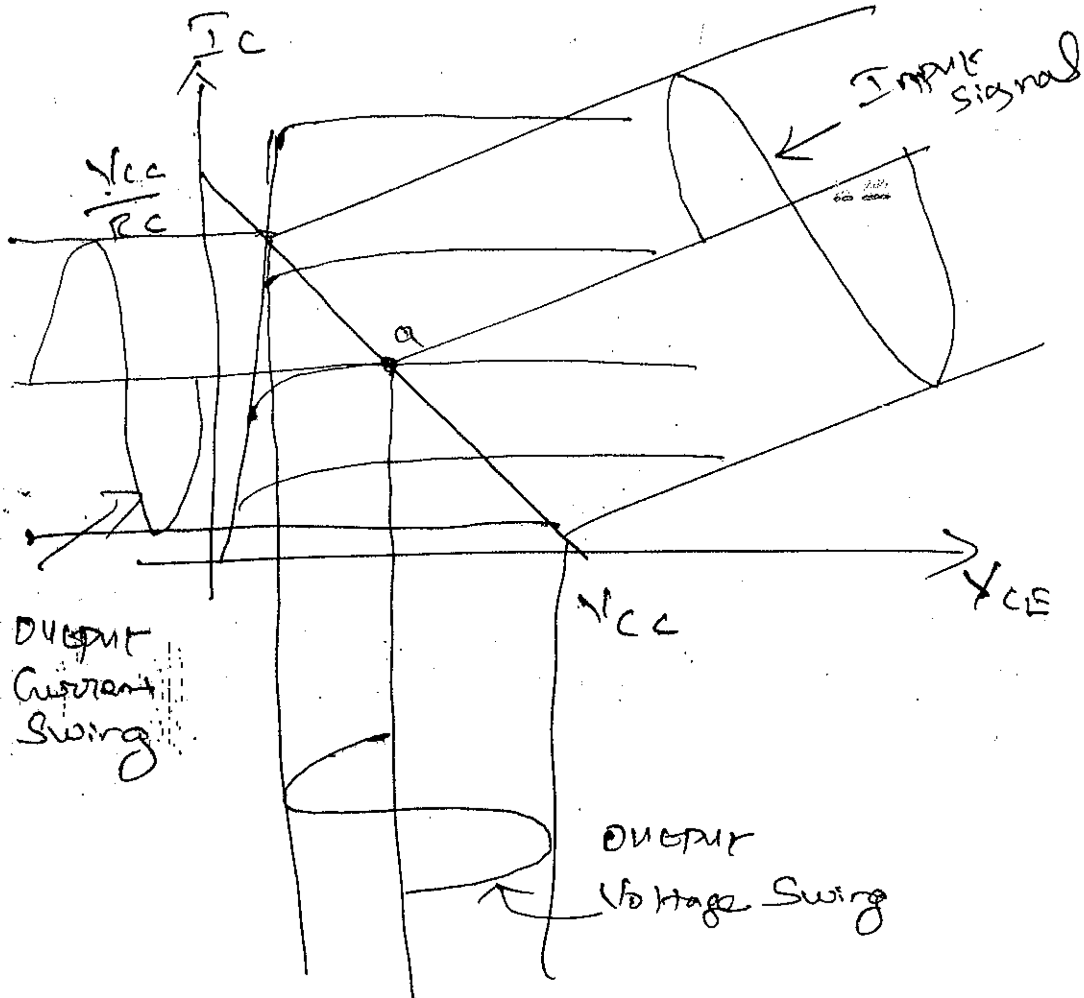


Fig 4.4 Amplifier input and output Signal Variation.



Power considerations

The power drawn from the supply is

$$P_i(dc) = V_{CC} I_{CQ} \longrightarrow (4)$$

Output Power

The output voltage and current varying around the bias point provide ac power to load.

Using Rms signals,

$$P_o(ac) = V_{CE}(rms)\, I_C(rms) \rightarrow (5)$$

$$P_o(ac) = I_C^2(rms)\, R_C \rightarrow (6)$$

$$P_o(ac) = \frac{V_C^2(rms)}{R_C} \rightarrow (7)$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered from the dc source.

$$\%\,\eta = \frac{P_o(ac)}{P_i(dc)} \times 100\,\% \rightarrow (8)$$

Maximum Efficiency

The maximum efficiency can be determined using the maximum voltage and current swings.

For the voltage swing, maximum $V_{CE}(P-P) = V_{CC}$

For the current ", maximum $I_C(P-P) = \frac{V_{CC}}{R_C}$

The output power, maximum, $P_o(ac) = \frac{V_{CE} \times I_C}{8}$

$$= \frac{V_{CC}(V_{CC}/R_C)}{8}$$

$$P_o(ac) = \frac{V_{CC}^2}{8 R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value,

$$\text{maximum } P_i(dc) = V_{CC} \times I_C = V_{CC} \cdot \frac{V_{CC}/R_C}{2}$$

$$= \frac{V_{CC}^2}{2R_C}$$

The maximum efficiency:

$$\text{maximum } \% \eta = \frac{\text{maximum } P_o(ac)}{\text{maximum } P_i(dc)} \times 100\%$$

$$= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\%.$$

$$\boxed{\text{maximum, } \eta = 25\%.}$$

TRANSFORMER COUPLED CLASS-A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig.

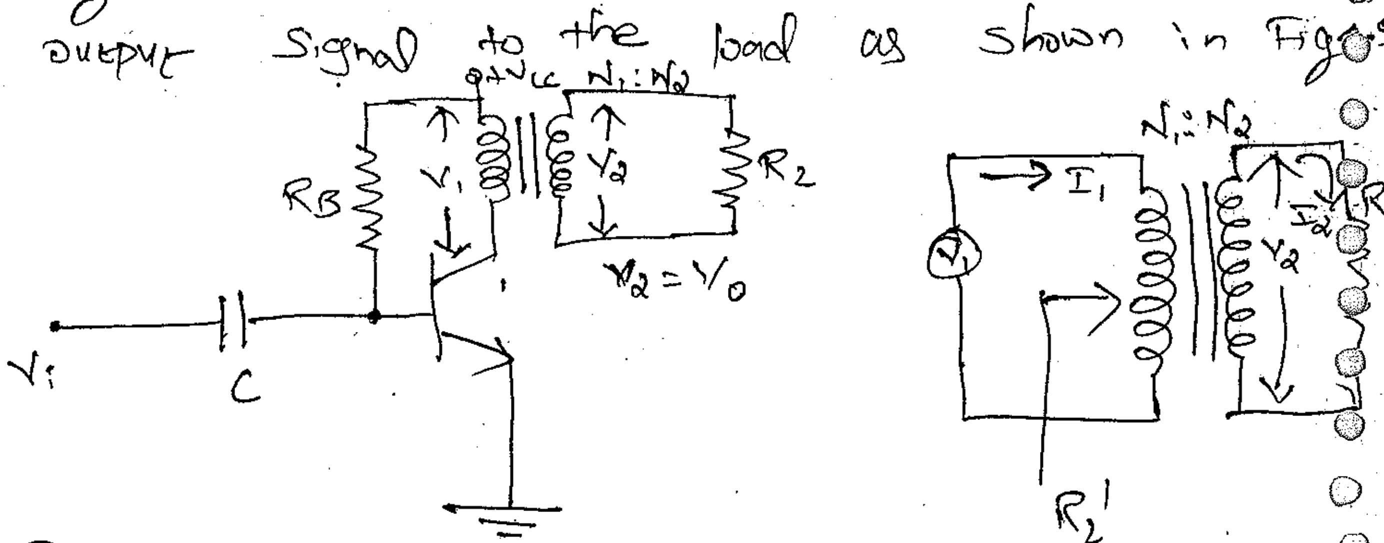


Fig 4.5 Transformer-Coupled audio power amplifier.

Voltage Transformation – Current transformation – Impedance transformation

The Voltage transformation, $\frac{V_2}{V_1} = \frac{N_2}{N_1} \longrightarrow (1)$

The current " , $\frac{I_2}{I_1} = \frac{N_1}{N_2} \longrightarrow (2)$

Impedance " , $\frac{R_L}{R_L'} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1}$

$$= \frac{V_2}{I_2}\frac{I_1}{V_1}$$

$$= \frac{V_2}{V_1}\cdot\frac{I_1}{I_2}$$

$$= \frac{N_2}{N_1}\cdot\frac{N_2}{N_1} = \left(\frac{N_2}{N_1}\right)^2$$

Let $a = \frac{N_1}{N_2} \Rightarrow \frac{R_L'}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2 \rightarrow (3)$

We can express the load resistance,

$$\frac{R_L}{R_L'} = \left(\frac{N_2}{N_1}\right)^2 = \left(\frac{1}{a}\right)^2 \Rightarrow \boxed{R_L' = a^2 R_L} \rightarrow (4)$$

As shown in eqn (4), the reflected impedance is related directly to the square of the turns ratio.

Operations of Amplifier stage

The dc load line is drawn straight vertically from the voltage point, $V_{CEQ} = V_{CC}$.

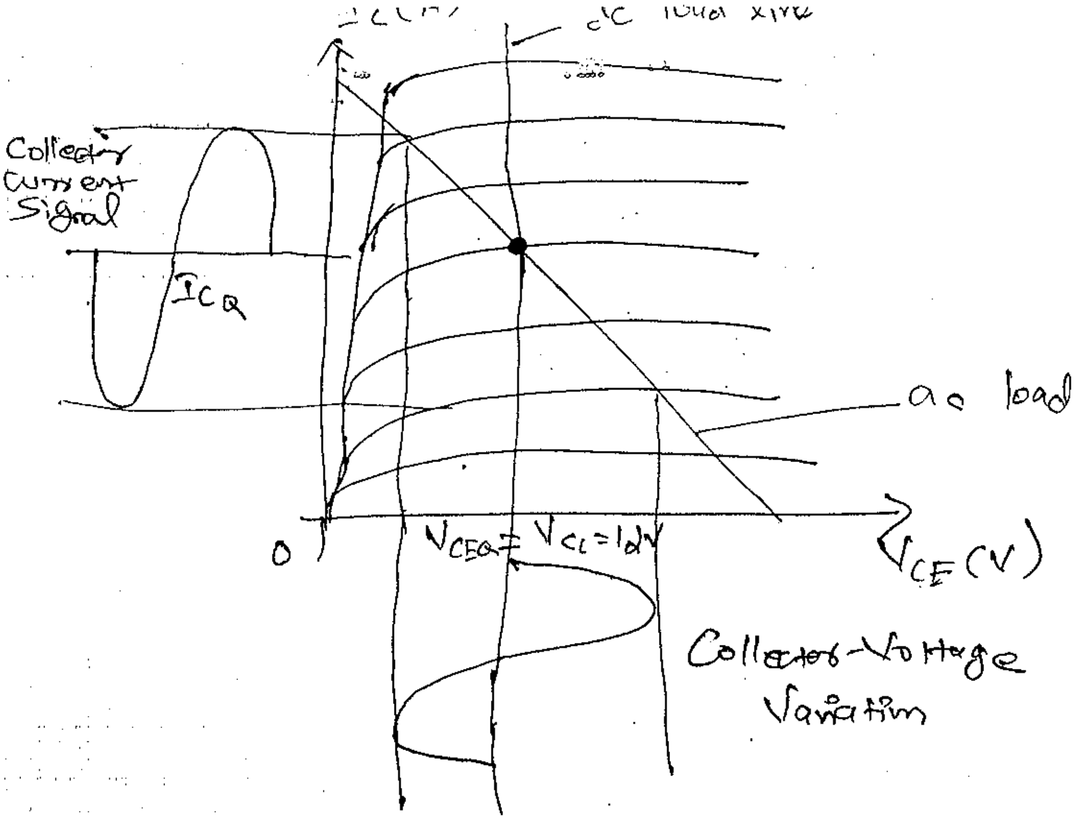


Fig 4.6 Load Line

* The operating Point (Q) in the characteristic curve of Fig 4.6 is the Point of intersection of dc load line and the base current.

* The ac load line is drawn so that it passes through the operating Point and has a slope equal to $-1/R_L'$.

Signal Swing and Output Ac Power

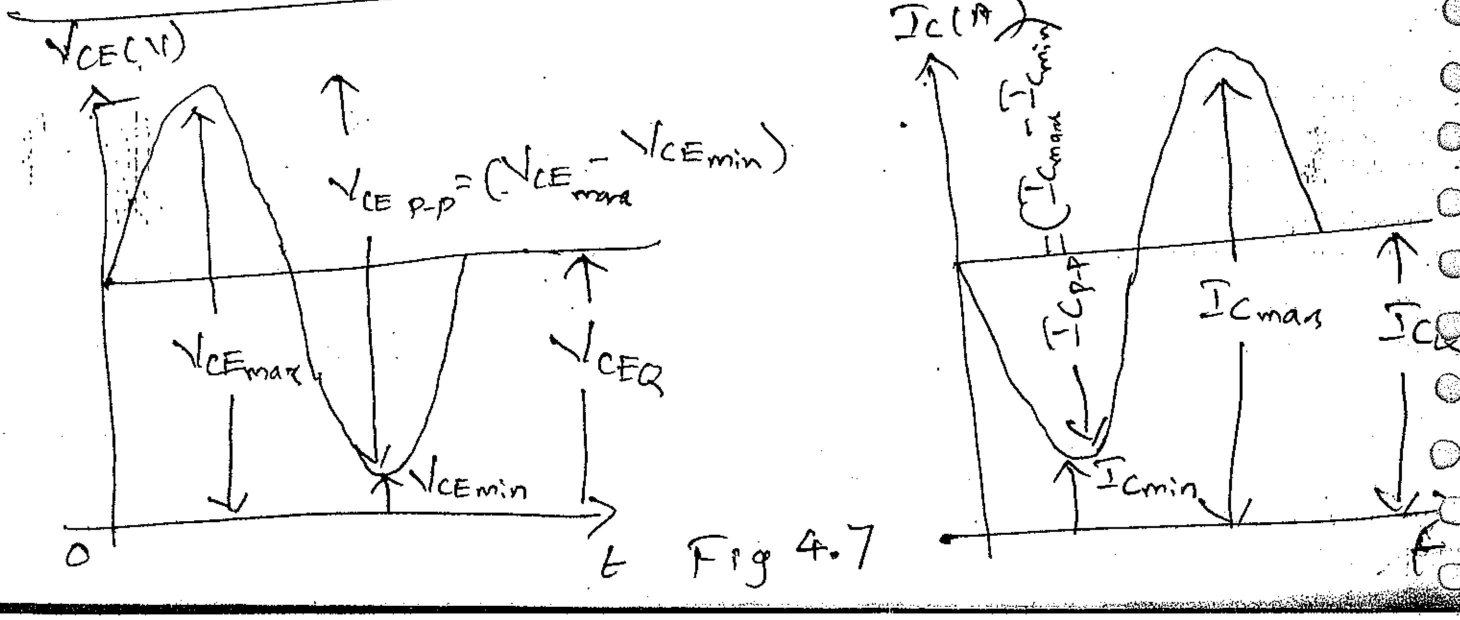


Fig 4.7

The Values of Peak-to-Peak Swings are,

$$V_{CE(p-p)} = V_{CE max} - V_{CE min}$$

$$I_{C(p-p)} = I_{C max} - I_{C min}$$

The ac Power developed across the transformer Primary,

$$P_o(ac) = \frac{(V_{CE max} - V_{CE min})(I_{C max} - I_{C min})}{8}$$

From eqn ①, the Voltage delivered to the load, → ⑤

$$V_L = V_2 = \frac{N_2}{N_1} V_1$$

Output Power

The power across the load, $P_L = \frac{V_L^2(rms)}{R_L}$

The load current, $I_L = I_2 = \frac{N_1}{N_2} I_C$

$$P_L = I_L^2(rms) R_L.$$

~~V_{CE}~~

Maximum Efficiency

The input Power obtained from the supply,

$$P_i(dc) = V_{CC} I_{CQ} \longrightarrow ⑤$$

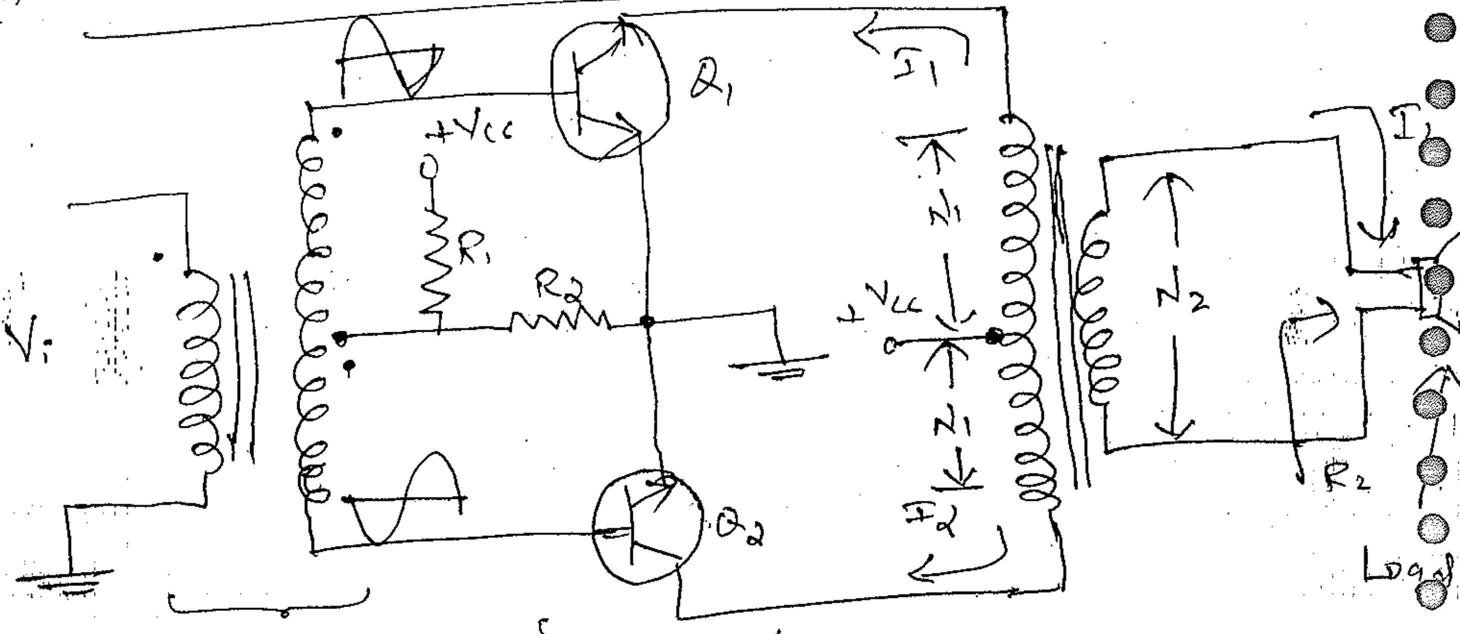
$$P_Q = P_i(dc) - P_o(ac)$$

where, P_Q is the power dissipated as heat.

$$\% \eta = 50 \left(\frac{V_{CE max} - V_{CE min}}{V_{CE max} + V_{CE min}} \right)^2 \%$$

CLASS B Amplifier Circuits

(i) Transformer - Coupled push-pull circuits



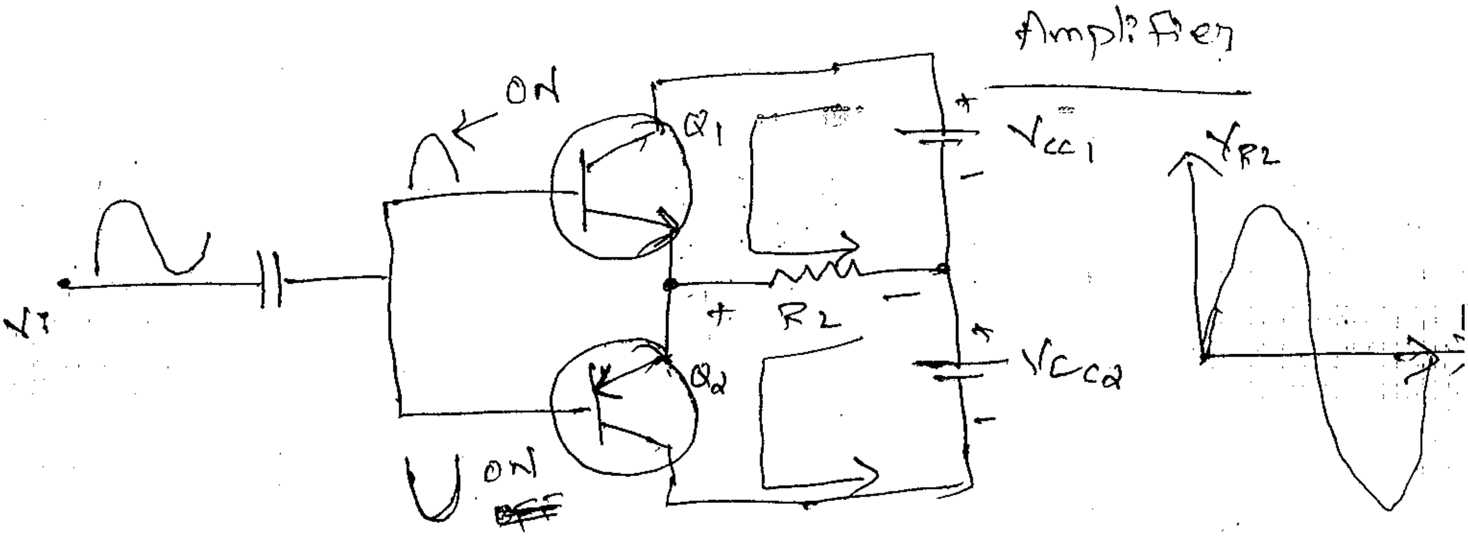
Phase splitting input transformer

Push-Pull Circuit Connection

* During the first half-cycle of operation, transistor Q_1 is driven into conduction and the current I_1 through the transformer results in first half cycle of signal to load. The transistor Q_2 is driven off.

* During the second half-cycle of the signal Q_2 conducts, results in second half cycle of signal to load. The transistor Q_1 is driven off. The overall signal developed across the load then varies over the full cycle.

Complementary - symmetry Push-Pull Power Amplifier

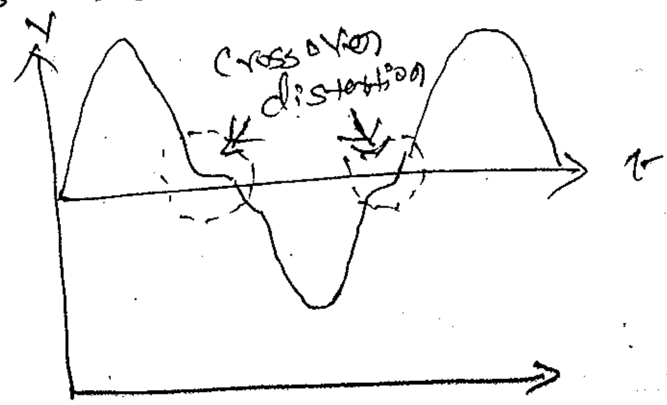


* At Positive half cycle, $Q_1 \to$ ON ; $Q_2 \to$ OFF
  " negative " " , $Q_1 \to$ OFF ; $Q_2 \to$ ON

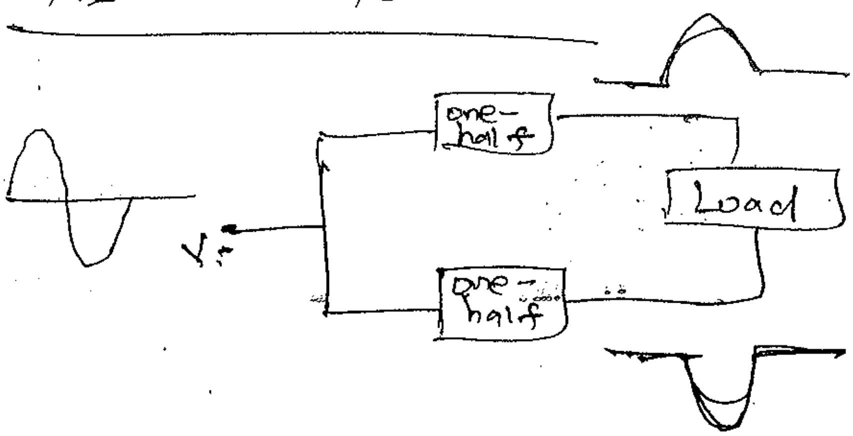
* Using Complementary transistors, It's possible to obtain a full cycle output across a load using half-cycles of operation from each transistor.

Crossover distortion

It's refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal.



Push-Pull operation



In class B, the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal it's necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal and this operation is known as push-pull operation.

Input Power (DC)

$$P_i(dc) = V_{cc} I_{dc} \longrightarrow (1)$$

$$= V_{cc}\left(\frac{2}{\pi} I(p)\right)$$

where, $I_{dc} = \frac{2}{\pi} I(p)$,

$I(p) \rightarrow$ Peak value of O/P current

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Output (AC) Power

The output power, $P_o(ac) = \dfrac{V_L^2(rms)}{R_L}$

$$= \frac{V_L^2(P-P)}{8R_L} = \frac{V_L^2(P)}{2R_L}$$

Efficiency

$$\% \eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{V_L^2(P)/2R_L}{V_{cc}\left[\frac{2}{\pi} I(P)\right]} \times 100\%$$

$$= \frac{\pi}{4} \frac{V_L(P)}{V_{cc}} \times 100\%$$

$\Rightarrow$ when $V_L(P) = V_{cc}$, $\left(\because \dfrac{I(P)}{R_L} = V_L(P) \right)$

$$\% \eta = \frac{\pi}{4} \times 100\% = \frac{3.14}{4} \times 100\% = 78.5\%$$

Power Dissipated by output Transistors

The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

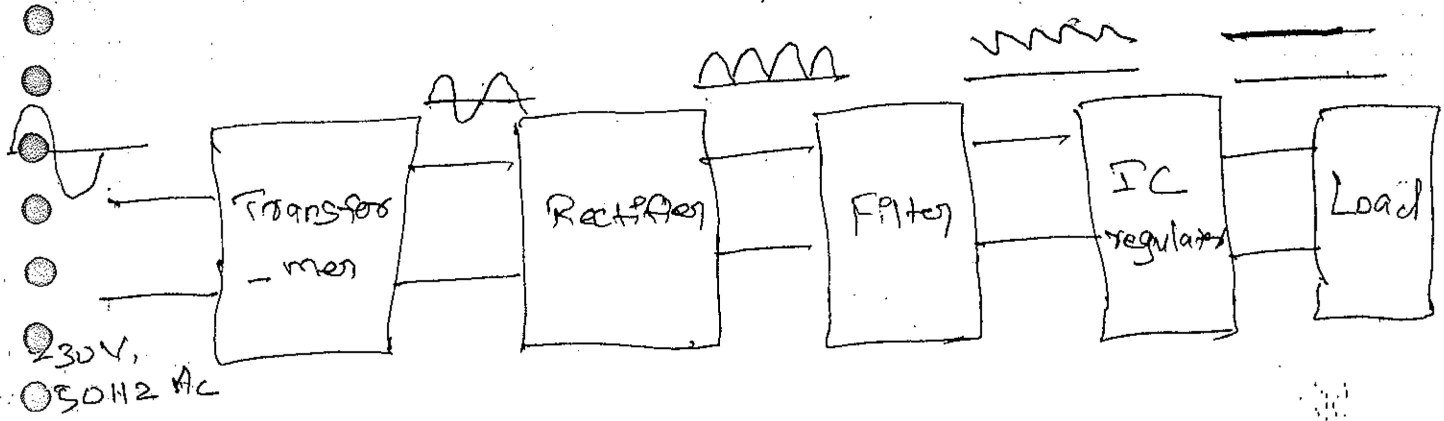
$$P_{2Q} = P_i(dc) - P_o(ac)$$

The dissipated power handled by each transistor is then,

$$P_Q = \frac{P_{2Q}}{2}$$

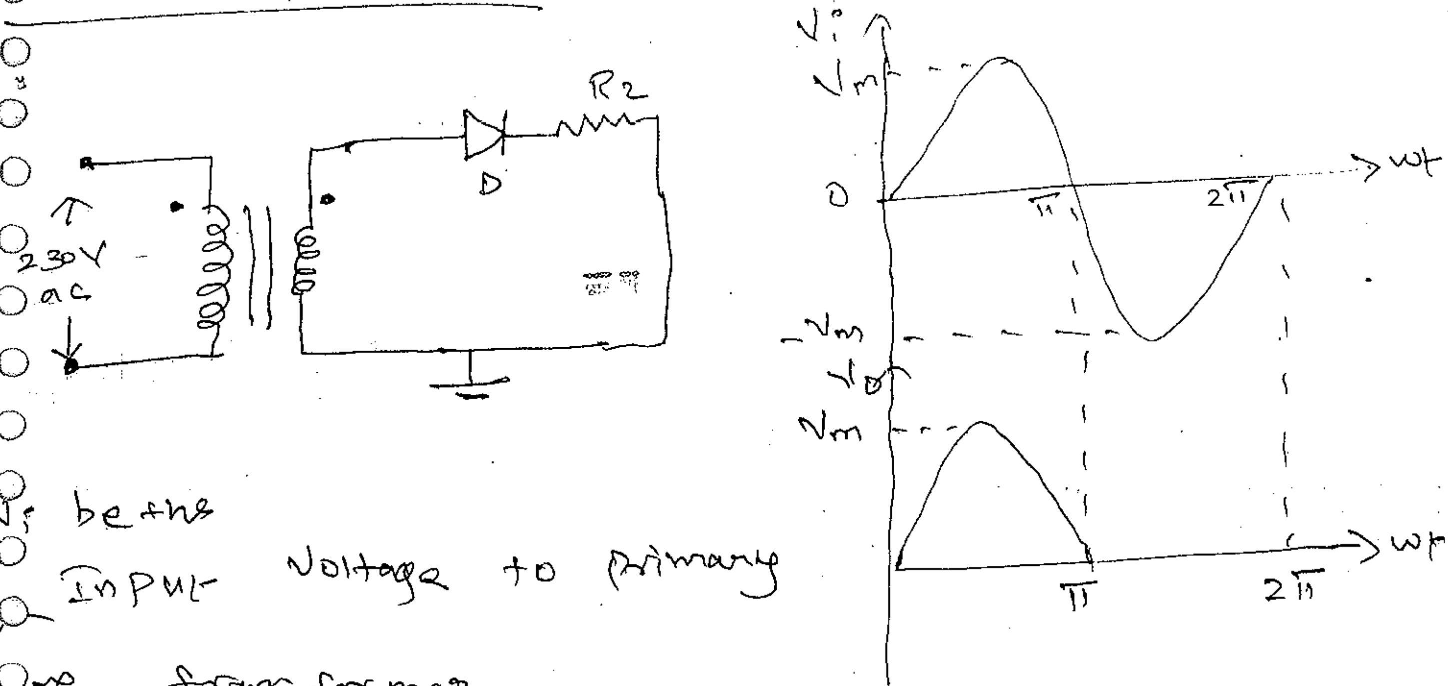
UNIT – V RECTIFIERS & POWER SUPPLIES

Block diagram of Power Supply



(i) Rectifiers

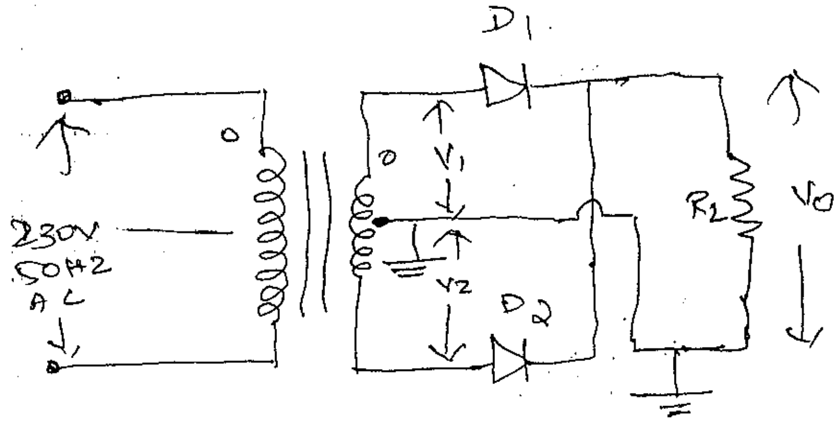
Half-wave rectifier

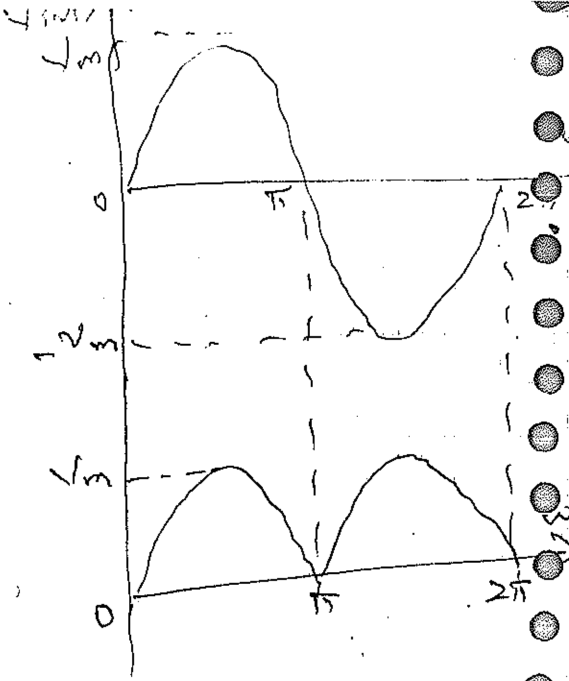


V_i be the input voltage to primary of transformer,

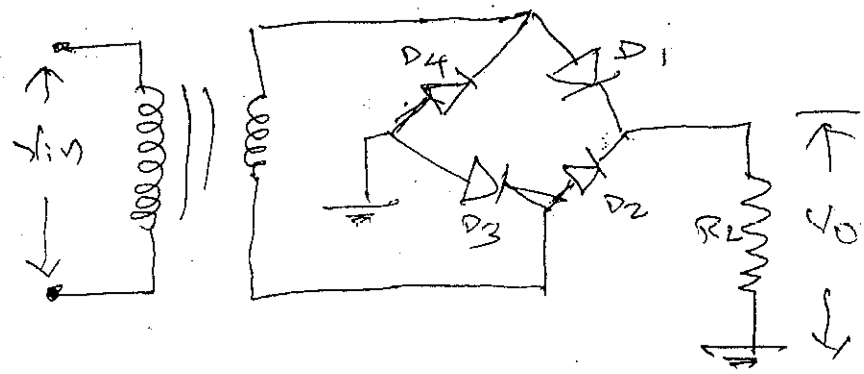
$V_i = V_m \sin\omega t$; $V_m >> V_r$

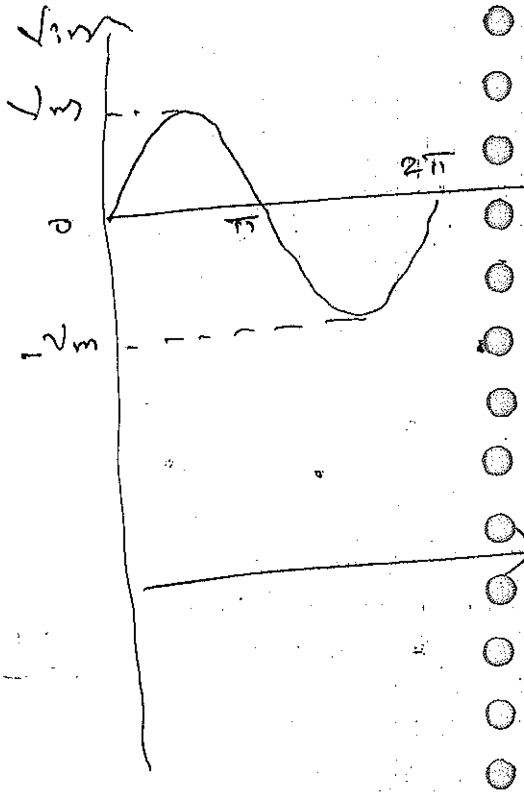
Full-wave rectifier





Bridge rectifier





Zener diode Shunt Regulator

A Zener diode, under reverse bias breakdown condition, can be used to regulate the voltage across a load, irrespective of the supply voltage (or) load current variations. A simple Zener voltage regulator circuit is shown in Fig.

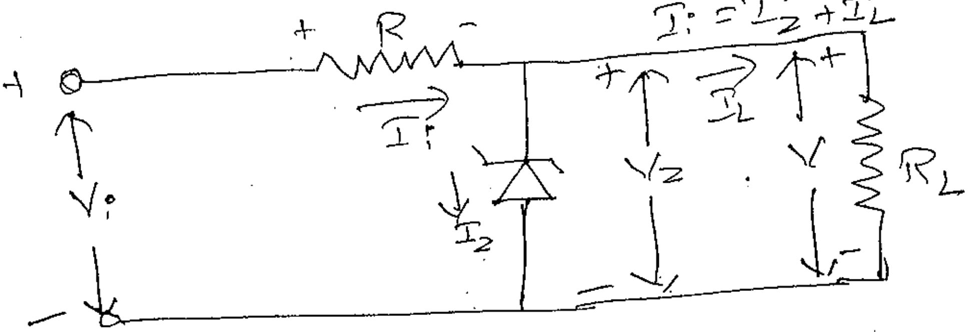


Fig. Zener Voltage Regulator.

The Zener diode has a characteristic that under reverse bias condition, the voltage across it practically remains constant, even if the current through it changes by a large extent.

The Zener diodes can be used as 'stand-alone' voltage regulator circuits and also as reference voltage sources.

Electronic Voltage Regulators (IC Voltage Regulators)

Although voltage regulators can be designed using op-amps, it's quicker and easier to use IC voltage regulators. Some important types of linear IC voltage regulators:

1. Fixed positive/negative output voltage regulators
2. Adjustable output voltage regulators.

Voltage Regulations

A Voltage regulator is an electronic circuit that provides a stable d.c voltage independent of the load current, temperature and ac line voltage variation. The output d.c. voltage V_o depends on the input unregulated d.c. voltage V_{in}, Load current I_L and temperature T. Here the change in output voltage of power supply can be expressed as:

$$\Delta V_o = \frac{\partial V_o}{\partial V_{in}} \Delta V_{in} + \frac{\partial V_o}{\partial I_L} \Delta I_L + \frac{\partial V_o}{\partial T} \Delta T.$$

Line Regulation

Line regulation is defined as the change in output voltage for a change in line supply voltage keeping the load current and temperature constant.

$$\text{Line regulation} = \frac{\text{Change in output voltage}}{\text{Change in input voltage}} = \frac{\Delta V_o}{\Delta V_{in}}$$

Load Regulation

Load regulation is expressed as,

$$= \frac{(V_{no\ load} - V_{full\ load})}{V_{no\ load}}$$

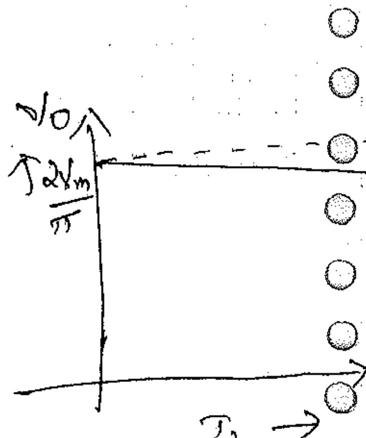


Fig. Load regulation characteristics

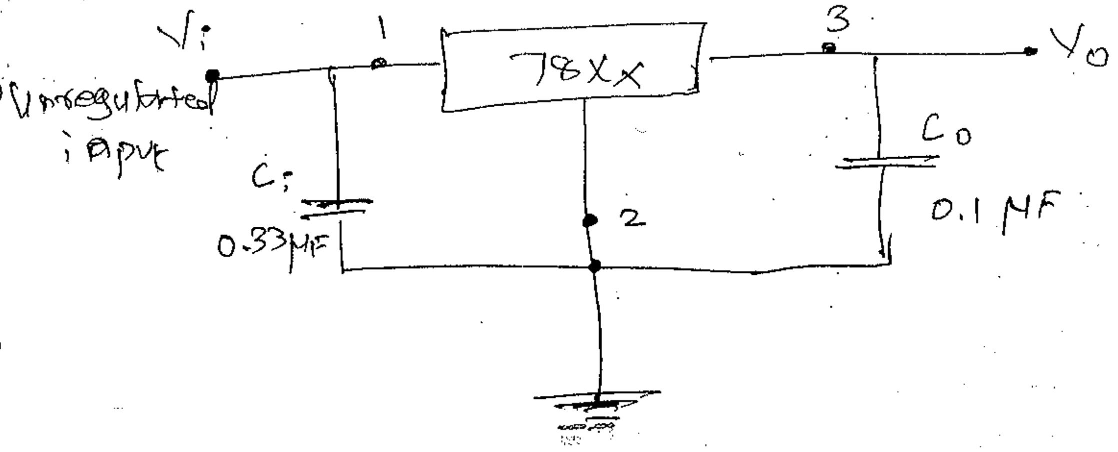
$V_{no\ load} \rightarrow$ Output voltage at zero load current

$V_{full\ load} \rightarrow$ " " " rated "

Fixed Voltage Regulators

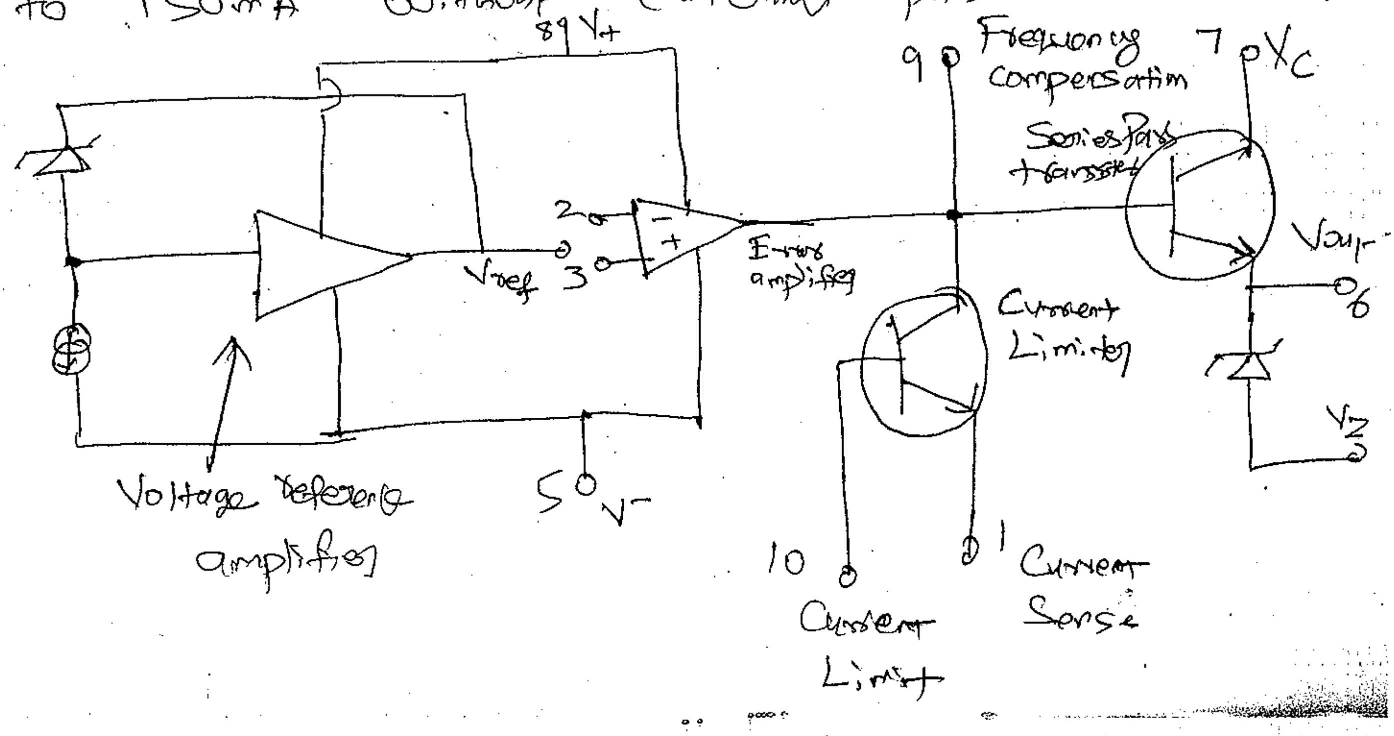
78xx series are three terminal, positive fixed voltage regulators. 79xx series are negative fixed voltage regulators.

E.g 7805 (5V Regulator); 7905 (−5V regulator)
7812 (12V ,,); 7912 (−12V ,,)



Adjustable Voltage Regulators

LM723C is the general purpose adjustable voltage regulator. The output voltage is adjustable from 2 to 37V. It will supply output currents up to 150mA without external pass transistor.



SWITCHED MODE POWER SUPPLY (SMPS)