**2017 -2020 BATCH**

**KARPAGAM ACADEMY OF HIGHER EDUCATION**
**(Deemed to be University)**
**(Established Under Section 3 of UGC Act 1956)**
**Coimbatore – 641 021.**
**(For the candidates admitted from 2017 onwards)**
**DEPARTMENT OF PHYSICS**

**SUBJECT: PHYSICS OF DEVICES AND COMMUNICATION**

**SEMESTER : IV**

**SUBJECT CODE: 17PHU302**

**Objective:** This paper is intended to give an idea about the physics of different electronic devices and physics of communication electronics.

**UNIT-I**

**Devices:** Characteristic and small signal equivalent circuits of UJT and JFET. Metal semiconductor Junction. Metal oxide semiconductor (MOS) device. Ideal MOS and Flat Band voltage. SiO2-Si based MOS. MOSFET– their frequency limits. Enhancement and Depletion Mode MOSFETS, CMOS. Charge coupled devices. Tunnel diode.

**UNIT -II**

**Power supply and Filters:** Block Diagram of a Power Supply, Qualitative idea of C and L Filters. IC Regulators, Line and load regulation, Short circuit protection. Active and Passive Filters, Low Pass, High Pass, Band Pass and band Reject Filters.

Multivibrators: Astable and Monostable Multivibrators using transistors.

**UNIT- III**

**Phase Locked Loop(PLL):** Basic Principles, Phase detector(XOR & edge triggered), Voltage Controlled Oscillator (Basics, varactor). Loop Filter– Function, Loop Filter Circuits, transient response, lock and capture. Basic idea of PLL IC (565 or 4046).

**Processing of Devices:** Basic process flow for IC fabrication, Electronic grade silicon. Crystal plane and orientation. Defects in the lattice. Oxide layer. Oxidation Technique for Si.

Metallization technique. Positive and Negative Masks. Optical lithography. Electron lithography. Feature size control and wet anisotropic etching. Lift off Technique. Diffusion and implantation.

**UNIT- IV**

**Digital Data Communication Standards:** Serial Communications: RS232, Handshaking, Implementation of RS232 on PC. Universal Serial Bus (USB): USB standards, Types and elements of USB transfers. Devices (Basic idea of UART). Parallel Communications: General Purpose Interface Bus (GPIB), GPIB signals and lines, Handshaking and interface management, Implementation of a GPIB on a PC. Basic idea of sending data through a COM port.

**UNIT-V**

**Introduction to CRO:** Block Diagram of CRO. Applications of Oscilloscope: (1) Study of Waveform, (2) Measurement of Voltage, Current, Frequency and Phase Difference.

**Power Supply:** Half-wave Rectifiers. Centre-tapped and Bridge Full-wave Rectifiers Calculation of Ripple Factor and Rectification Efficiency, Basic idea about capacitor filter, Zener Diode and Voltage Regulation Timer IC: IC 555 Pin diagram and its application as Astable and Monostable Multivibrator.

**TEXT BOOKS**

1. Electronic devices and integrated circuits, A.K. Singh, 2011, PHI Learning Pvt. Ltd.
2. Physics of Semiconductor Devices, By Massimo Rudan, 2015, Springer New York Heidelberg Dordrecht London, ISBN- 978-1-4939-1150-9, Semiconductor Devices: Physics and Technology by S. M. Sze, John Wiley & Sons Singapore Pte. Limited, 2012, ISBN - 9780470873670.

**REFERENCE BOOKS:**

1. Linear Integrated Circuits & Applications By U.A.Bakshi, A.P.Godse, Technical Publications Pune, 2010, ISBN- 9788184317619.
2. Electronic Devices and Circuits by G. S. N. Raju, I.K. International Publishing House Pvt. Limited, 2010, ISBN- 9788189866020.Semiconductor Physics and Devices, D.A.

Neamen, 2011, 4th Edition, McGraw Hill, Principles of Electronic Communication Systems by Louis Frenzel, McGraw-Hill Education, 2015, ISBN – 9780073373850.

3. Introduction to Instrumentation and Measurements, Third Edition, By Robert B. Northrop, CRC press, Taylor and Francis group, ISBN – 978-1-4822-1482-6

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**DEPARTMENT OF PHYSICS**

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**SEMESTER : IV**

**SUBJECT CODE: 17PHU302** **CLASS : II B.Sc. PHYSICS**

# LECTURE PLAN

# DEPARTMENT OF PHYSICS

| S No | Lecture duration | Topics | Support Materials |
|---|---|---|---|
| | | **UNIT -I** | |
| 1 | 1hr | Devices: Characteristic and small signal equivalent circuits of UJT and JFET | T1:250-251 |
| 2 | 1hr | Metal semiconductor Junction. | T1:212-215 |
| 3 | 1hr | Metal oxide semiconductor (MOS) device, Ideal MOS. | T1:169, 168 |
| 4 | 1hr | Flat Band voltage, $SiO_2$-Si based MOS | T1: 170,173 |
| 5 | 1hr | MOSFET– their frequency limits. | T1: 179-184 |
| 6 | 1hr | MOSFET Enhancement & Depletion Mode MOSFETS | T1:186-190 |
| 7 | 1hr | CMOS. Charge coupled devices. | T1:190-192 |
| 8 | 1hr | Tunnel diode | T1:170,185 |
| 9. | 1hr | Revision | |
| | | Total number of hours planned | 09 hrs |

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|---|---|---|---|
| | **UNIT -II** | | |
| | | | |
| 1 | 1hr | Power supply and Filters, Block Diagram of a Power Supply | T1:446-447 |
| 2 | 1hr | Qualitative idea of C and L Filters | T1:446-449 |
| 3 | 1hr | IC Regulators, Line and load regulation, | T1:480-483 |
| 4 | 1hr | Short circuit protection | T1:484-488 |
| 5 | 1hr | Active and Passive Filters, Low Pass, Band, High Pass Filters | T1:489-495 |
| 6 | 1hr | Pass and band Reject Filters | T2:249-256 |
| 7 | 1hr | Multivibrators: Astable using transistors | T2:256-266 |
| 8 | 1hr | Monostable Multivibrators using transistors. | T2:266-276 |
| 9 | 1hr | Revison | |
| | Total number of hours planned | | 09hrs |
| | **UNIT -III** | | |
| | | | |
| 1 | 1hr | Phase Locked Loop(PLL): Basic Principles, | T2:413-420 |
| 2 | 1hr | Phase detector(XOR & edge triggered), | T2 415 -425 |
| 3 | 1hr | Voltage Controlled Oscillator (Basics, varactor). | T2:420-424 |
| 4 | 1hr | Loop Filter– Function, Loop Filter Circuits, | T2:425430 |
| 5 | 1hr | Transient response, lock and capture. Basic idea of PLL IC (565 or 4046). | T2:124-129 |
| 6 | 1hr | Processing of Devices: Basic process flow for IC fabrication, Electronic grade silicon | T2:412-428 |
| 7 | 1hr | Crystal plane and orientation. Defects in the lattice.Oxide layer. Oxidation Technique for Si. | T1:628-630 |
| 8 | 1hr | Metallization technique. Positive and Negative Masks. Optical lithography | T1:634-636 |
| 9 | 1hr | Electron lithography. Feature size control and wet anisotropic etching. | T1:637-638 |

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|---|---|---|---|
| 10 | 1hr | Lift off Technique. Diffusion and implantation | T1:631-638 |
| 11 | 1hr | Revision | |
| | | Total number of hours planned | 11hrs |
| | | **UNIT -IV** | |
| 1 | 1hr | Digital Communication :Serial Communications: RS232, | T2:184-186 |
| 2 | 1hr | Handshaking, Implementation of RS232, Universal Bus | T2:181-183 |
| 3 | 1hr | Types and elements of USB transfers. | T2:185 -187 |
| 4 | 1hr | Devices (Basic idea of UART).Parallel | T2:200-203 |
| 5 | 1hr | Communications: General Purpose Interface Bus (GPIB), | T2 : 210 -214 |
| 6 | 1hr | GPIB signals and lines | T2:187-190 |
| 7 | 1hr | Handshaking and interface management, | T2:190-200 |
| 8 | 1hr | Implementation of a GPIB on a PC, Basic idea of sending data through a COM port | T2 : 202 -208 |
| 9 | 1hr | Revision | |
| | | Total number of hours planned | 09 hrs |
| **UNIT - V** | | | |
| 1 | 1hr | Introduction to CRO: Block Diagram of CRO | T2:573-574 |
| 2 | 1hr | Applications of Oscilloscope: (1) Study of Waveform, (2) Measurement of Voltage, Current, Frequency and Phase Difference, Rectifiers: Centre-tapped | T2:574-594 |
| 3 | 1hr | Bridge Full-wave Rectifiers | T2:469-473 |
| 4 | 1hr | Calculation of Ripple Factor and Rectification Efficiency | T2:479-481 |
| 5 | 1hr | Basic idea about capacitor filter, | T2:490-496 |
| 6 | 1hr | Zener Diode and Voltage Regulation Timer, IC 555 Pin diagram and its applications Astable Multi-vibrator and Monostable Multi-vibrator | T2:490-498 |

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|---|---|---|---|
| 7 | 1hr | Revision | |
| 8 | 1hr | Old question paper discussion | |
| 9 | 1 hr | Old question paper discussion | |
| 10 | 1hr | Old question paper discussion | |
| | | Total number of hours planned | 10 hrs |

**SUGGESTED READINGS:**

T1: Electronic devices and integrated circuits, A.K. Singh, 2011, PHI Learning Pvt. Ltd.

T2: Physics of Semiconductor Devices, By Massimo Rudan, 2015, Springer New York Heidelberg Dordrecht London, ISBN- 978-1-4939-1150-9, Semiconductor Devices: Physics and Technology by S. M. Sze, John Wiley & Sons Singapore Pte. Limited, 2012,

**WEB SITES:**

1) www.circuitstoday.com/dc-power-supplies
2) www.hit.bme.hu/~papay/edu/GPIB/tutor.htm
3) circuitdigest.com/tutorials

**JOURNALS:**

1) **R.KRISHNA "Free-running Monostable Multi-vibrator" Journal of Electronics and control, volume- 17,issue no5, 15 Feb 1964.**

## UNIT-I

### SYLLABUS

Devices:Characteristic and small signal equivalent circuits of UJT and JFET. Metal semiconductor Junction. Metal oxide semiconductor (MOS) device Ideal MOS and Flat Band voltage. SiO2-Si based MOS. MOSFET– their frequency limits. Enhancement and Depletion Mode MOSFETS, CMOS. Charge coupled devices. Tunnel diode.

### JUNCTION FIELD EFFECT TRANSISTOR

The Field Effect Transistor is a three terminal unipolar semiconductor device that has very similar characteristics to those of their Bipolar Transistor counterparts ie, high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT) cousins.

Field effect transistors can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

The field effect transistor is a three terminal device that is constructed with no PN-junctions within the main current carrying path between the Drain and the Source terminals, which correspond in function to the Collector and the Emitter respectively of the bipolar transistor. The current path between these two terminals is called the “channel” which may be made of either a P-type or an N-type semiconductor material.The control of current flowing in this channel is achieved by varying the voltage applied to the Gate. As their name implies, Bipolar Transistors are “Bipolar” devices because they operate with both types of charge carriers, Holes and Electrons. The Field Effect Transistor on the other hand is a “Unipolar” device that depends only on the conduction of electrons (N-channel) or holes (P-channel).

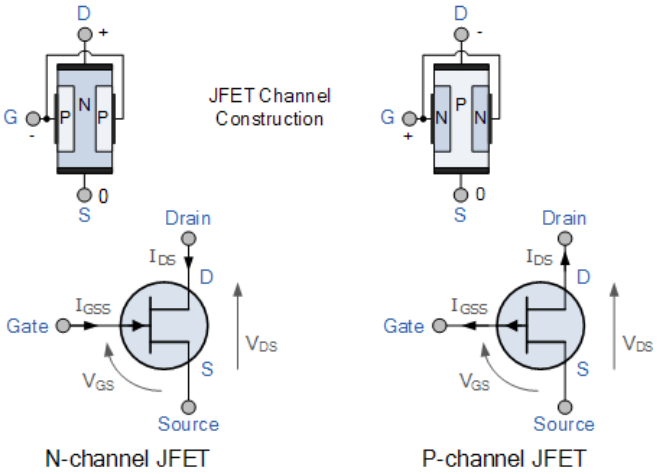
The Field Effect Transistor has one major advantage over its standard bipolar transistor cousins, in that their input impedance, ( Rin ) is very high, (thousands of Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

There are two main types of field effect transistor, the Junction Field Effect Transistor and the Insulated-gate Field Effect Transistor or IGFET), which is more commonly known as the standard Metal Oxide Semiconductor Field Effect Transistor .

. The Junction Field Effect Transistor (JUGFET or JFET) has no PN-junctions but instead has a narrow piece of high resistivity semiconductor material forming a "Channel" of either N-type or P-type silicon for the majority carriers to flow through with two ohmic electrical connections at either end commonly called the Drain and the Source respectively. There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons.

Likewise, the P-channel JFET's channel is doped with acceptor impurities meaning that the flow of current through the channel is positive (hence the term P-channel) in the form of holes. N-channel JFET's have a greater channel conductivity (lower resistance) than their equivalent P-channel types, since electrons have a higher mobility through a conductor compared to holes. This makes the N-channel JFET's a

The symbols and basic construction for both configurations of JFETs are shown below.

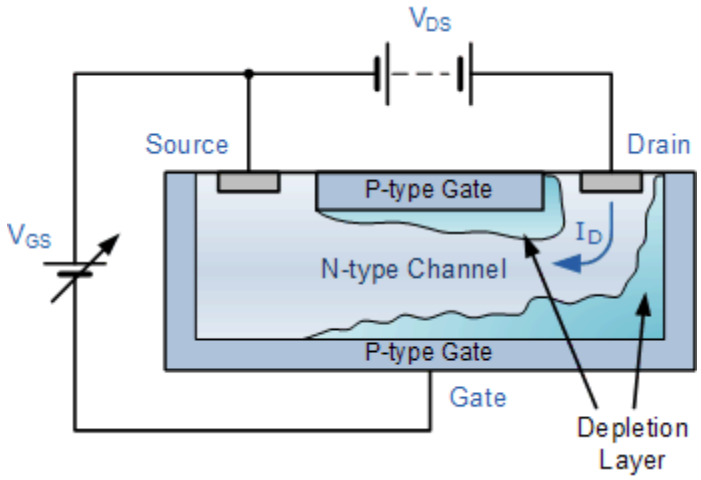



The semiconductor "channel" of the Junction Field Effect Transistor is a resistive path through which a voltage $V_{DS}$ causes a current $I_D$ to flow and as such the junction field effect transistor can conduct current equally well in either direction. As the channel is resistive in nature, a voltage gradient is thus formed down the length of the channel with this voltage becoming less positive as we go from the Drain terminal to the Source terminal.The result is that the PN-junction therefore has a high reverse bias at the Drain terminal and a lower reverse bias at the Source terminal. This bias causes a "depletion layer" to be formed within the channel and whose width increases with the bias.

The magnitude of the current flowing through the channel between the Drain and the Source terminals is controlled by a voltage applied to the Gate terminal, which is a reverse-biased. In an N-channel JFET this Gate voltage is negative while for a P-channel JFET the Gate voltage is positive. The main

difference between the JFET and a BJT device is that when the JFET junction is reverse-biased the Gate current is practically zero, whereas the Base current of the BJT is always some value greater than zero.

Biasing of an N-channel JFET




The cross sectional diagram above shows an N-type semiconductor channel with a P-type region called the Gate diffused into the N-type channel forming a reverse biased PN-junction and it is this junction which forms the depletion region around the Gate area when no external voltages are applied. JFETs are therefore known as depletion mode devices.This depletion region produces a potential gradient which is of varying thickness around the PN-junction and restrict the current flow through the channel by reducing its effective width and thus increasing the overall resistance of the channel itself.Then we can see that the most-depleted portion of the depletion region is in between the Gate and the Drain, while the least-depleted area is between the Gate and the Source. Then the JFET's channel conducts with zero bias voltage applied (ie, the depletion region has near zero width).

With no external Gate voltage ( $V_G = 0$ ), and a small voltage ( $V_{DS}$ ) applied between the Drain and the Source, maximum saturation current ( $I_{DSS}$ ) will flow through the channel from the Drain to the Source restricted only by the small depletion region around the junctions.If a small negative voltage ( $-V_{GS}$ ) is now applied to the Gate the size of the depletion region begins to increase reducing the overall effective area of the channel and thus reducing the current flowing through it, a sort of "squeezing" effect takes place. So by applying a reverse bias voltage increases the width of the depletion region which in turn reduces the conduction of the channel.

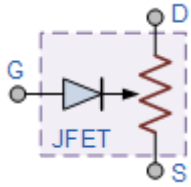
Since the PN-junction is reverse biased, little current will flow into the gate connection. As the Gate voltage ( $-V_{GS}$ ) is made more negative, the width of the channel decreases until no more current flows

between the Drain and the Source and the FET is said to be "pinched-off" (similar to the cut-off region for a BJT). The voltage at which the channel closes is called the "pinch-off voltage", ( $V_P$ ).

**JFET Channel Pinched-off**

In this pinch-off region the Gate voltage, $V_{GS}$ controls the channel current and $V_{DS}$ has little or no effect.

**JFET-Model**

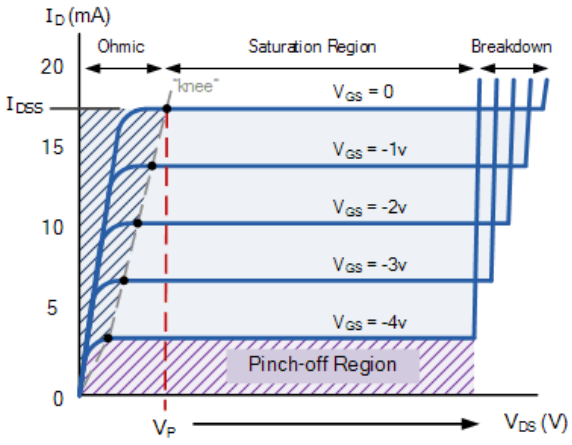


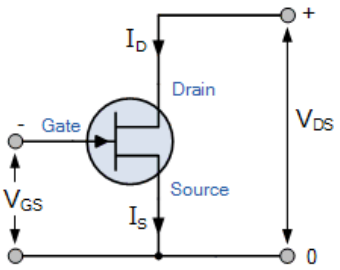

The result is that the FET acts more like a voltage controlled resistor which has zero resistance when $V_{GS}$ = 0 and maximum "ON" resistance ( $R_{DS}$ ) when the Gate voltage is very negative. Under normal operating conditions, the JFET gate is always negatively biased relative to the source.It is essential that the Gate voltage is never positive since if it is all the channel current will flow to the Gate and not to the Source, the result is damage to the JFET. Then to close the channel:

- No Gate voltage ( $V_{GS}$ ) and $V_{DS}$ is increased from zero.
- No $V_{DS}$ and Gate control is decreased negatively from zero.
- $V_{DS}$ and $V_{GS}$ varying.

The P-channel Junction Field Effect Transistor operates the same as the N-channel above, with the following exceptions: 1). Channel current is positive due to holes, 2). The polarity of the biasing voltage needs to be reversed.

The output characteristics of an N-channel JFET with the gate short-circuited to the source is given as




The voltage $V_{GS}$ applied to the Gate controls the current flowing between the Drain and the Source terminals. $V_{GS}$ refers to the voltage applied between the Gate and the Source while $V_{DS}$ refers to the voltage applied between the Drain and the Source.

Because a Junction Field Effect Transistor is a voltage controlled device,"NO current flows into the gate!" then the Source current ( $I_S$ ) flowing out of the device equals the Drain current flowing into it and therefore ($I_D = I_S$ ).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

- Ohmic Region – When $V_{GS}$ = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
- Cut-off Region – This is also known as the pinch-off region were the Gate voltage, $V_{GS}$ is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, ( $V_{GS}$ ) while the Drain-Source voltage, ( $V_{DS}$ ) has little or no effect.
- Breakdown Region – The voltage between the Drain and the Source, ( $V_{DS}$ ) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current $I_D$ decreases with an increasing positive Gate-Source voltage, $V_{GS}$.The Drain current is zero when $V_{GS} = V_P$. For normal operation, $V_{GS}$ is biased to be somewhere between $V_P$ and 0. Then we can calculate the Drain current, $I_D$ for any given bias point in the saturation or active region as follows:

Drain current in the active region.

$$I_D = I_{DSS}[1-V_{GS}/Vp]^2$$

Note that the value of the Drain current will be between zero (pinch-off) and $I_{DSS}$ (maximum current). By knowing the Drain current $I_D$ and the Drain-Source voltage $V_{DS}$ the resistance of the channel ( $I_D$ ) is given as:

Drain-Source channel resistance.

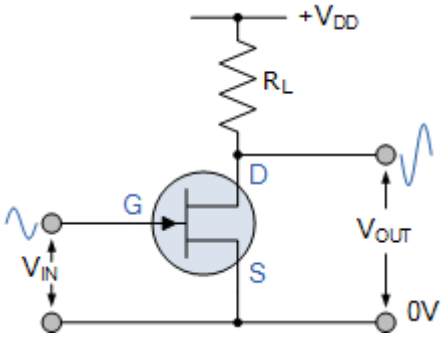
$$R_{DS} = \Delta V_{DS} / \Delta I_D = 1/g_m$$

Where: $g_m$ is the "transconductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage.

Modes of FET's

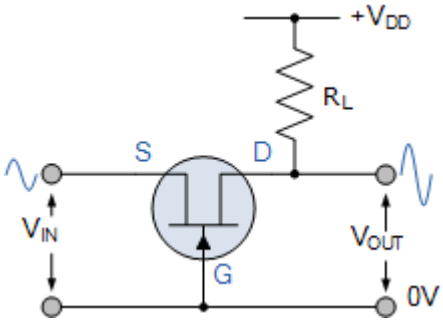
Like the bipolar junction transistor, the field effect transistor being a three terminal device is capable of three distinct modes of operation and can therefore be connected within a circuit in one of the following configurations.

Common Source (CS) Configuration



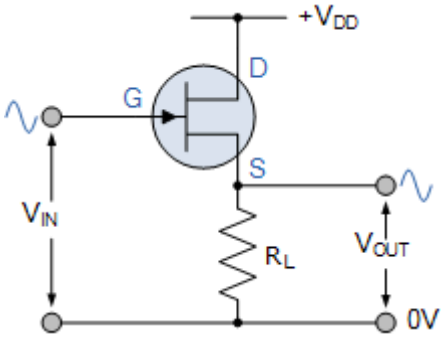

In the Common Source configuration the input is applied to the Gate and its output is taken from the Drain as shown. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification and as such Common Source amplifiers are widely used.The common source mode of FET connection is generally used audio frequency amplifiers and in high input impedance pre-amps and stages. Being an amplifying circuit, the output signal is 180° "out-of-phase" with the input.

Common Gate (CG) Configuration




In the Common Gate configuration the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance.This type of FET configuration can be used in high frequency circuits or in impedance matching circuits were a low input impedance needs to be matched to a high output impedance. The output is "in-phase" with the input.

Common Drain (CD) Configuration

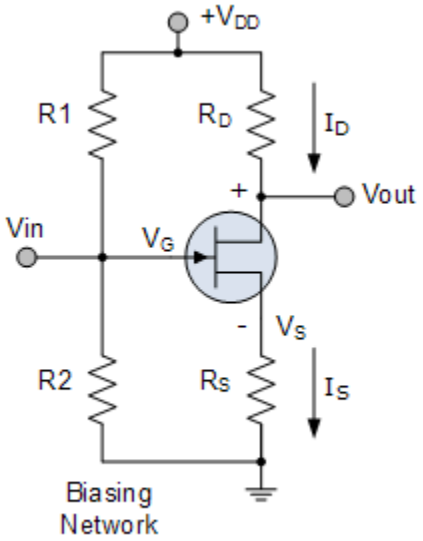



In the Common Drain configuration the input is applied to the Gate and its output is taken from the Source. The common drain or "source follower" configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is "in-phase", $0^o$ with the input signal.This type of configuration is referred to as "Common Drain" because there is no signal available at the drain connection, the voltage present, $+V_{DD}$ just provides a bias. The output is in-phase with the input.

**The JFET Amplifier**

Like the bipolar junction transistor, JFET's can be used to make single stage class A amplifier circuits with the JFET common source amplifier and characteristics being very similar to the BJT common emitter circuit. The main advantage JFET amplifiers have over BJT amplifiers is their high input impedance which is controlled by the Gate biasing resistive network formed by R1 and R2 as shown.

Biasing of JFET Amplifier



This common source (CS) amplifier circuit is biased in class "A" mode by the voltage divider network formed by resistors R1 and R2. The voltage across the Source resistor $R_S$ is generally set to be about one quarter of $V_{DD}$, ( $V_{DD}$ /4 ) but can be any reasonable value. The required Gate voltage can then be calculated from this $R_S$ value. Since the Gate current is zero, ( $I_G = 0$ ) we can set the required DC quiescent voltage by the proper selection of resistors R1 and R2.

The control of the Drain current by a negative Gate potential makes the junction Field Effect Transistor useful as a switch and it is essential that the Gate voltage is never positive for an N-channel JFET as the channel current will flow to the Gate and not the Drain resulting in damage to the JFET. The principals of operation for a P-channel JFET are the same as for the N-channel JFET, except that the polarity of the voltages need to be reversed.

**MOSFET**

The MOSFET – Metal Oxide FET

The IGFET or MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.This ultra thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the MOSFET extremely high way up in the Mega-ohms ( MΩ ) region thereby making it almost infinite.

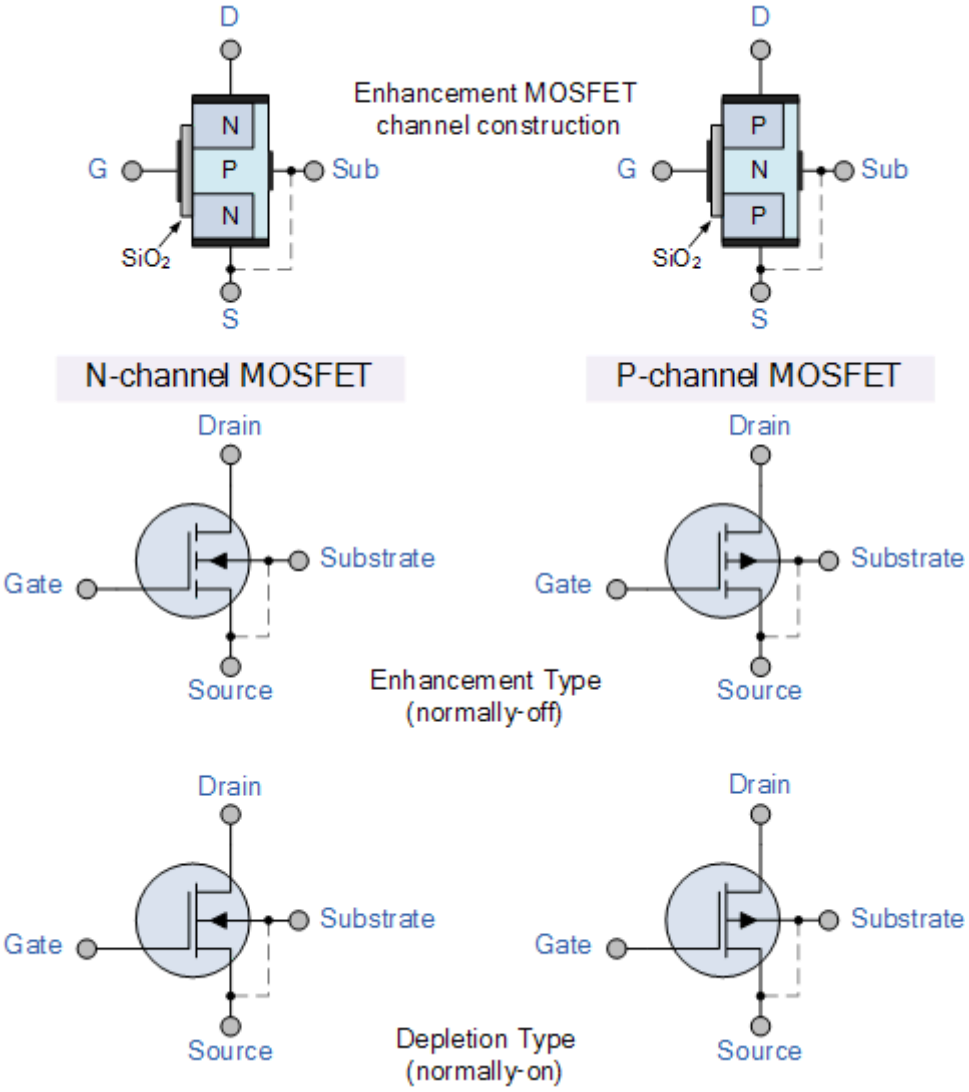
As the Gate terminal is isolated from the main current carrying channel"NO current flows into the gate" and just like the JFET, the MOSFET also acts like a voltage controlled resistor were the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the MOSFET becoming easily damaged unless carefully handled or protected.

MOSFETs are also three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

- Depletion Type – the transistor requires the Gate-Source voltage, ( $V_{GS}$ ) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.

- Enhancement Type – the transistor requires a Gate-Source voltage, ( $V_{GS}$ ) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

The symbols and basic construction for both configurations of MOSFETs are shown below.

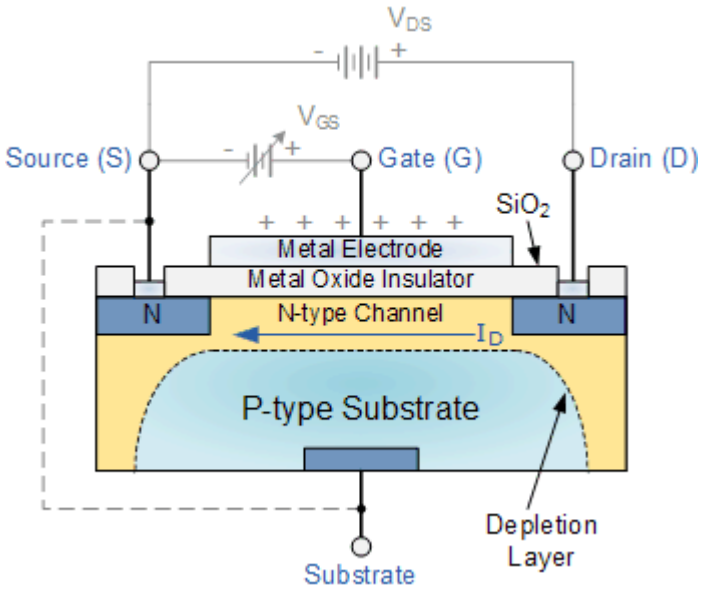



The four MOSFET symbols above show an additional terminal called the Substrate and is not normally used as either an input or an output connection but instead it is used for grounding the substrate. It connects to the main semi conductive channel through a diode junction to the body or metal tab of the MOSFET. Usually in discrete type MOSFETs, this substrate lead is connected internally to the source terminal. When this is the case, as in enhancement types it is omitted from the symbol for clarification.

The line between the drain and source connections represents the semi conductive channel. If this is a solid unbroken line then this represents a "Depletion" (normally-ON) type MOSFET as drain current can flow with zero gate potential. If the channel line is shown dotted or broken it is an "Enhancement"

(normally-OFF) type MOSFET as zero drain current flows with zero gate potential. The direction of the arrow indicates whether the conductive channel is a p-type or an n-type semiconductor device.

**Basic MOSFET Structure and Symbol**




The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semi conductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes. It is possible to bias the gate of a MOSFET in either polarity, positive (+ve) or negative (-ve).

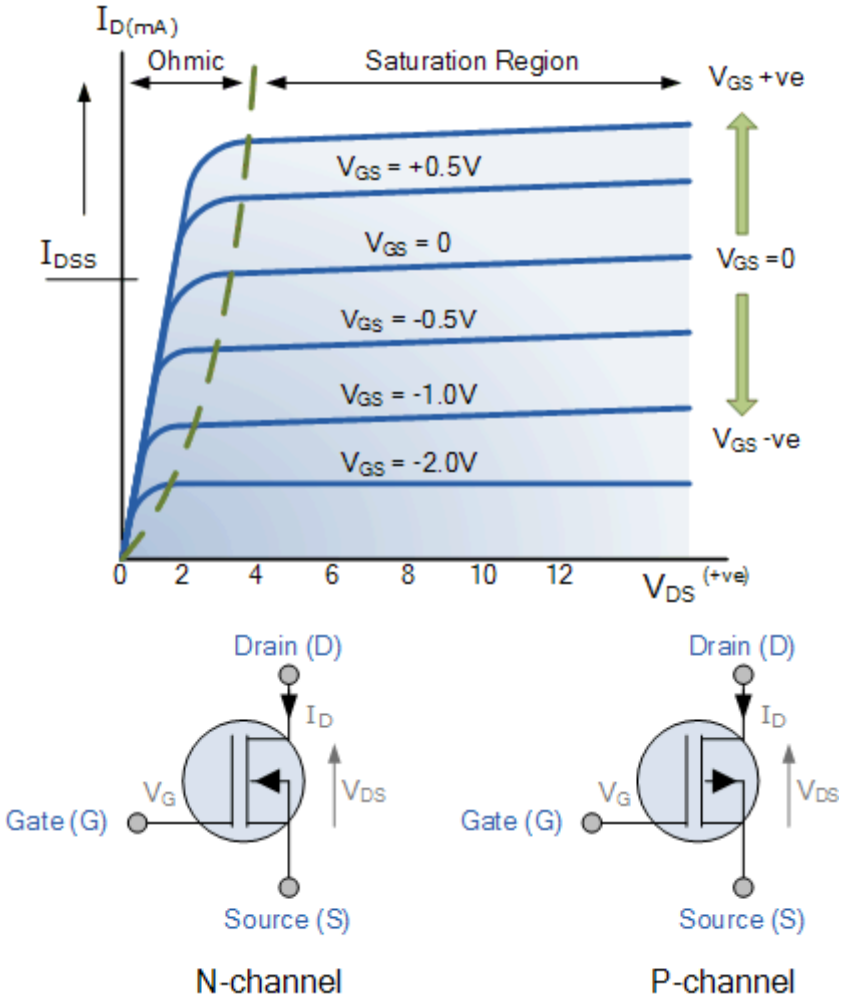
This makes the MOSFET device especially valuable as electronic switches or to make logic gates because with no bias they are normally non-conducting and this high gate input resistance means that very little or no control current is needed as MOSFETs are voltage controlled devices. Both the p-channel and the n-channel MOSFETs are available in two basic forms, the Enhancement type and the Depletion type.

**Depletion-mode MOSFET**

The Depletion-mode MOSFET, which is less common than the enhancement mode types is normally switched "ON" (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$ making it a "normally-closed" device. The circuit symbol shown above for a depletion MOS transistor uses a solid channel line to signify a normally closed conductive channel.

For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete (hence its name) the conductive channel of its free electrons switching the transistor "OFF". Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, $+V_{GS}$ will deplete the channel of its free holes turning it "OFF".In other words, for an n-channel depletion mode MOSFET: $+V_{GS}$ means more electrons and more current. While a $-V_{GS}$ means less electrons and less current. The opposite is also true for the p-channel types. Then the depletion mode MOSFET is equivalent to a "normally-closed" switch.

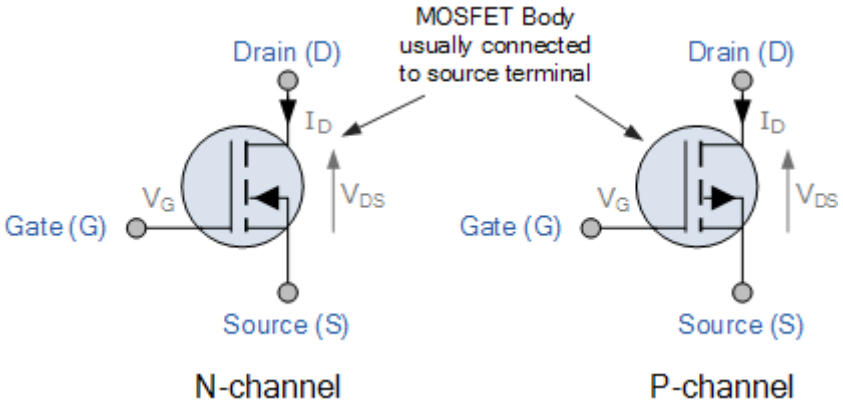
**Depletion-mode N-Channel MOSFET and circuit Symbols**




The depletion-mode MOSFET is constructed in a similar way to their JFET transistor counterparts were the drain-source channel is inherently conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the Drain andSource with zero Gate bias.

**Enhancement-mode MOSFET**

The more common Enhancement-mode MOSFET or e - MOSFET, is the reverse of the depletion-mode type. Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally "OFF" (non-conducting) when the gate bias voltage, $V_{GS}$ is equal to zero. The circuit symbol shown above for an enhancement MOS transistor uses a broken channel line to signify a normally open non-conducting channel.

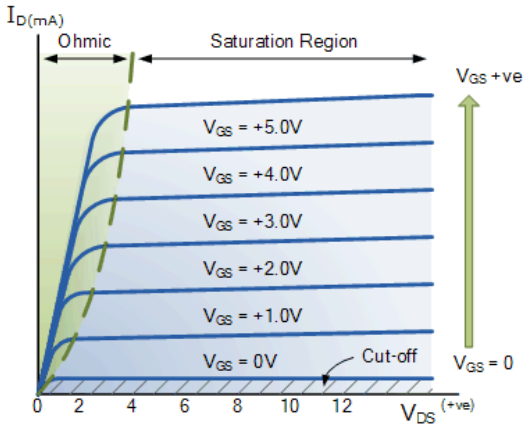



For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( $V_{GS}$ ) is applied to the gate terminal greater than the threshold voltage ( $V_{TH}$ ) level in which conductance takes place making it a transconductance device.

The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, $I_D$ through the channel. In other words, for an n-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "ON", while a zero or $-V_{GS}$ turns the transistor "OFF". Then, the enhancement-mode MOSFET is equivalent to a "normally-open" switch.

The reverse is true for the p-channel enhancement MOS transistor. When $V_{GS} = 0$ the device is "OFF" and the channel is open. The application of a negative (-ve) gate voltage to the p-type e - MOSFET enhances the channels conductivity turning it "ON". Then for an p-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "OFF", while $-V_{GS}$ turns the transistor "ON".

**Out-put Characteristics**



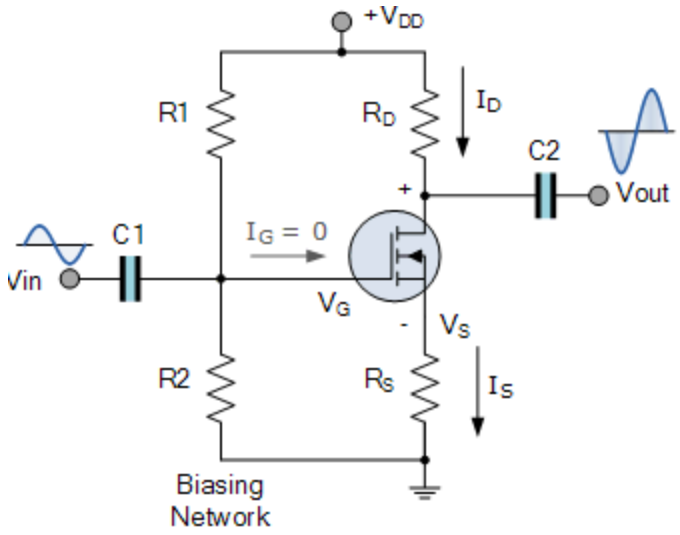

Enhancement-mode MOSFETs make excellent electronics switches due to their low "ON" resistance and extremely high "OFF" resistance as well as their infinitely high input resistance due to their isolated gate. Enhancement-mode MOSFETs are used in integrated circuits to produce CMOS type Logic Gates and power switching circuits in the form of as PMOS (P-channel) and NMOS (N-channel) gates. CMOS actually stands for Complementary MOS meaning that the logic device has both PMOS and NMOS within its design.

**The MOSFET Amplifier**

MOSFETs can be used to make single stage class "A" amplifier circuits with the enhancement mode n-channel MOSFET. The depletion mode MOSFET amplifiers are very similar to the JFET amplifiers, except that the MOSFET has a much higher input impedance.

This high input impedance is controlled by the gate biasing resistive network formed by R1 and R2. Also, the output signal for the enhancement mode common source MOSFET amplifier is inverted because when $V_G$ is low the transistor is switched "OFF" and $V_D$ (Vout) is high. When $V_G$ is high the transistor is switched "ON" and $V_D$ (Vout) is low.

Enhancement-mode N-Channel MOSFET Amplifier




The DC biasing of this common source (CS) MOSFET amplifier circuit is identical to the JFET amplifier. The MOSFET circuit is biased in class A mode by the voltage divider network formed by resistors R1 andR2. The AC input resistance is given as $R_{IN} = R_G = 1M\Omega$.

**UNIJUNCTION TRANSISTOR** OR UJT

The Unijunction Transistor or UJT for short, is another solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triacs for AC power control type applications.

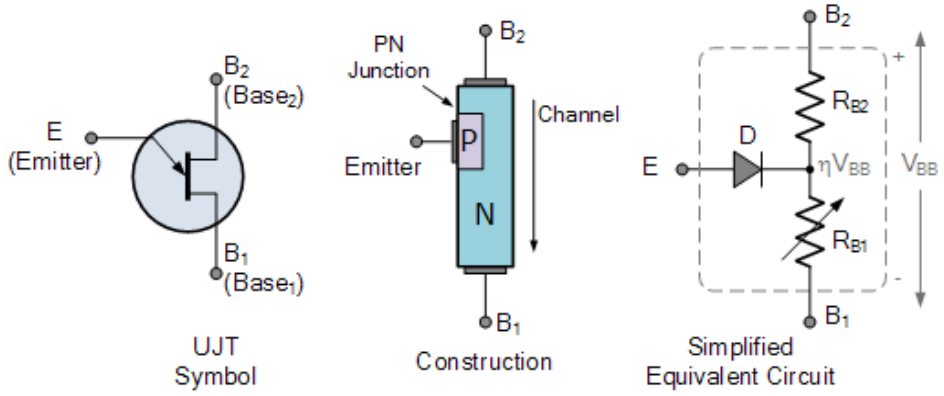
Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.

Although the Unijunction Transistor has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can not be used to amplify a signal but instead is used as a ON-OFF switching transistor. UJT's have unidirectional conductivity and negative impedance characteristics acting more like a variable voltage divider during breakdown.

Like N-channel FET's, the UJT consists of a single solid piece of N-type semiconductor material forming the main current carrying channel with its two outer connections marked as Base 2 ( $B_2$ ) and Base 1 ( $B_1$ ). The third connection, marked as the Emitter ( E ) is located along the channel. The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base.The Emitter rectifying p-n junction of the unijunction transistor is formed by fusing the P-type material into the N-type silicon channel. The Emitter junction is positioned along the channel so that it is closer to terminal $B_2$ than $B_1$. An arrow is

used in the UJT symbol which points towards the base indicating that the Emitter terminal is positive and the silicon bar is negative material.

**Unijunction Transistor Symbol and Construction**




From the simplified equivalent circuit it is clear that the N-type channel consists of two resistors $R_{B2}$ and $R_{B1}$ in series with an equivalent diode, D representing the p-n junction connected to their center point. This Emitter p-n junction is fixed in position along the ohmic channel .Resistance $R_{B1}$ is given between the Emitter, E and terminal $B_1$, while resistance $R_{B2}$ is given between the Emitter, E and terminal $B_2$. As the physical position of the p-n junction is closer to terminal $B_2$ than $B_1$ the resistive value of $R_{B2}$ will be less than $R_{B1}$.

The total resistance of the silicon bar will be dependent upon the semiconductors actual doping level as well as the physical dimensions of the N-type silicon channel but can be represented by $R_{BB}$.

These two series resistances produce a voltage divider network between the two base terminals of the unijunction transistor and since this channel stretches from $B_2$ to $B_1$, when a voltage is applied across the device, the potential at any point along the channel will be in proportion to its position between terminals $B_2$ and $B_1$. The level of the voltage gradient therefore depends upon the amount of supply voltage.When used in a circuit, terminal $B_1$ is connected to ground and the Emitter serves as the input to the device. Suppose a voltage $V_{BB}$ is applied across the UJT between $B_2$ and $B_1$ so that $B_2$ is biased positive relative to $B_1$. With zero Emitter input applied, the voltage developed across $R_{B1}$ (the lower resistance) of the resistive voltage divider can be calculated as:

Unijunction Transistor $R_{B1}$ Voltage

$V_{RB1} = R_{B1} / R_{B1} + R_{B2} X V_{BB}$

For a unijunction transistor, the resistive ratio of $R_{B1}$ to $R_{BB}$ is called the intrinsic stand-off ratio and is given the Greek symbol: η (eta). Typical standard values of η range from 0.5 to 0.8 for most common UJT's.

If a small positive input voltage which is less than the voltage developed across resistance, $R_{B1}$ ( $\eta V_{BB}$ ) is now applied to the Emitter input terminal, the diode p-n junction is reverse biased, thus offering a very high impedance and the device does not conduct. The UJT is switched "OFF" and zero current flows.However, when the Emitter input voltage is increased and becomes greater than $V_{RB1}$ (or $\eta V_{BB}$ + 0.7V, where 0.7V equals the p-n junction diode volt drop) the p-n junction becomes forward biased and the unijunction transistor begins to conduct. The result is that Emitter current, $\eta I_E$ now flows from the Emitter into the Base region.

The effect of the additional Emitter current flowing into the Base reduces the resistive portion of the channel between the Emitter junction and the $B_1$ terminal. This reduction in the value of $R_{B1}$resistance to a very low value means that the Emitter junction becomes even more forward biased resulting in a larger current flow. The effect of this results in a negative resistance at the Emitter terminal.

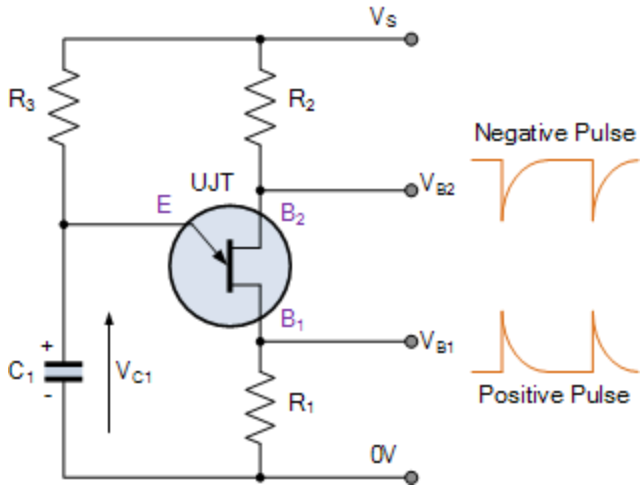
If the input voltage applied between the Emitter and $B_1$terminal decreases to a value below breakdown, the resistive value of$R_{B1}$ increases to a high value. Then the Unijunction Transistor can be thought of as a voltage breakdown device.So we can see that the resistance presented by $R_{B1}$ is variable and is dependant on the value of Emitter current, $I_E$. Then forward biasing the Emitter junction with respect to $B_1$ causes more current to flow which reduces the resistance between the Emitter, E and $B_1$.In other words, the flow of current into the UJT's Emitter causes the resistive value of $R_{B1}$ to decrease and the voltage drop across it, $V_{RB1}$must also decrease, allowing more current to flow producing a negative resistance condition.

**Unijunction Transistor Applications**

The most common application of a unijunction transistor is as a triggering device for scR and TRIAC , but other UJT applications include sawtoothed generators, simple oscillators, phase control, and timing circuits. The simplest of all UJT circuits is the Relaxation Oscillator producing non-sinusoidal waveforms.

In a basic and typical UJT relaxation oscillator circuit, the Emitter terminal of the unijunction transistor is connected to the junction of a series connected resistor and capacitor, RC circuit as shown below.

**Unijunction Transistor Relaxation Oscillator**

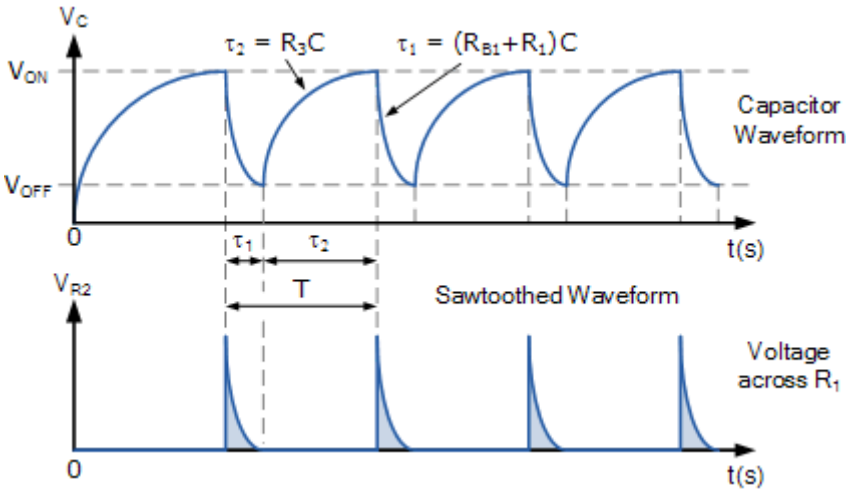



When a voltage (Vs) is applied, the unijunction transistor is "OFF" and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3. As the Emitter of the UJT is connected to the capacitor, when the charging voltage Vc across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The unijunction transistor is "ON". At this point the Emitter to B1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R1 taking place.

As the ohmic value of resistor R1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears acrossR1. Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R3, the discharging time is a lot less than the charging time as the capacitor discharges through the low resistance UJT.

When the voltage across the capacitor decreases below the holding point of the p-n junction ( $V_{OFF}$ ), the UJT turns "OFF" and no current flows into the Emitter junction so once again the capacitor charges up through resistor R3 and this charging and discharging process between$V_{ON}$ and $V_{OFF}$ is constantly repeated while there is a supply voltage, Vsapplied.

UJT Oscillator Waveforms




Then we can see that the unijunction oscillator continually switches "ON" and "OFF" without any feedback. The frequency of operation of the oscillator is directly affected by the value of the charging resistanceR3, in series with the capacitor C1 and the value of η. The output pulse shape generated from the Base1 (B1) terminal is that of a sawtooth waveform and to regulate the time period, you only have to change the ohmic value of resistance, R3 since it sets the RC time constant for charging the capacitor.

The time period, T of the saw tooth waveform will be given as the charging time plus the discharging time of the capacitor. As the discharge time, $\tau_1$ is generally very short in comparison to the larger RC charging time, $\tau_2$ the time period of oscillation is more or less equivalent to $T \cong \tau_2$. The frequency of oscillation is therefore given by $f = 1/T$.

For example, if the value of R3 was too large, (Megohms) the capacitor may not charge up sufficiently to trigger the Unijunction's Emitter into conduction but must also be large enough to ensure that the UJT switches "OFF" once the capacitor has discharged to below the lower trigger voltage.

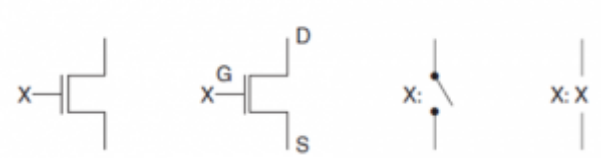
**CMOS**

CMOS (complementary metal-oxide-semiconductor) technology is used predominantly to create digital circuitry. The fundamental building blocks of CMOS circuits are P-type and N-type MOSFET transistors. A P-type MOSFET can be modeled as a switch that is closed when the input voltage is low (0 V) and open when the input voltage is high (5 V). A N-type MOSFET can be modeled as a switch that is closed when the input voltage is high (5 V) and open when the input voltage is low (0 V). The basic idea for

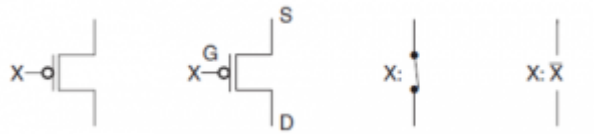
CMOS technology is to combine P-type and N-type MOSFETs such that there is never a conducting path from the supply voltage (5 V) to ground. As a consequence, CMOS circuits consume very little energy.

CMOS technology employs two types of transistor: n-channel and p-channel. The two differ in the characteristics of the semiconductor materials used in their implementation and in the mechanism governing the conduction of a current through them.

The transistor has three terminals: the gate (G), the source (S), and the drain (D). The voltage applied between G and S determines whether a path for current to flow exists between D and S. If a path exists, we say that the transistor is ON, and if a path does not exist, we say that the transistor is OFF. The n-channel transistor is ON if the applied gate-to-source voltage is H and OFF if the applied voltage is L. Here we will make the usual assumption that a 1 represents the H voltage range and a 0 represents the L voltage range. The notion of whether a path for current to flow exists is easily modeled by a switch. The switch consists of two fixed terminals corresponding to the S and D terminals of the transistor. In addition, there is a movable contact that, depending on its position, determines whether the switch is open or closed. The position of the contact is controlled by the voltage applied to the gate terminal G. Since we are looking at logic behavior, this control voltage is represented on the symbol by the input variable X on the gate terminal. For an n-channel transistor, the contact is open (no path exists) for the input variable X equal to 0 and closed (a path exists) for the input variable X equal to 1. Such a contact is traditionally referred to as being normally open, that is, open without a positive voltage applied to activate or close it.




The symbol for a p-channel transistor is shown in Figure below. The positions of the source S and drain D are seen to be interchanged relative to their positions in the n-channel transistor. The voltage applied between the gate G and the source S determines whether a path exists between the drain and source. The negation indicator or bubble appears as a part of the symbol. This is because, in contrast to the behavior of an n-channel transistor, a path exists between S and D in the p-channel transistor for input variable X equal to 0 (at value L) and does not exist for input variable X equal to 1 (at value H). This behavior is represented by the model which has a normally closed contact through which a path exists for X equal to 0. No path exists through the contact for X equal to 1.




The popular CMOS family include,

4000A,
4000B,
4000UB,
54/74C,
54/74HC,
54/74HCT,
54/74AC
54/74ACT

## CHARGE COUPLED DEVICE-CCD

CCD was developed in the year 1969 by Willard Boyle and George E. Smith at AT & T Bell Labs. It is a shift register device which can be used for the movement of electrical charge within the device. This movement can be from one area of the device to another and the digital value of the moved charge can be easily found out. When the signals are moved, one at a time from one place to another within the device, the value of the charge can be easily manipulated. There are capacitive bins in the device that allow the movement of charge.

**There are mainly two regions of a CCD**

### 1. Photoactive Region

The photoactive region mainly consists of a capacitor array. These arrays can be one-dimensional or two-dimensional depending on the type of device that uses the CCD. If a line scan camera is used, it introduces a one-dimensional capacitor array. It is called 1D because it captures the image in 1D form, that is, a single slice of the image. 2D is used mostly in video applications. This device captures the image in 2D form. The photoactive region is made out of an epitaxial layer of silicon. It is made by doping a boron ion on a substrate such as p++. Sometimes CCD's are also implanted with a phosphorus ion so as to give them an n-doping . This is often carried out in devices consisting of n-channels This is done in some areas of the silicon ion causing the movement of photo generated packets across them.

As soon as the silicon layer and substrates are made, a dielectric in the form of a gas oxide (mostly capacitor) is made to grow on top of them. Thus the separately lying gates will lie in a perpendicular angle to the channels. This is because the poly-silicon gates are undergoing chemical vapour deposition and then photolithography. Then the channel stop region and the charge carrying channel is made, and that too parallel to each other.

**2.Transmission Region**

After the image is projected onto the capacitor array, the control circuit comes into action. This circuit makes the capacitors send the appropriate signal to a shift register. The shift register converts each signal into a voltage sequence. This is later sampled, digitized and then stored in the memory.

**Applications of CCD**

**1.Astronomy**

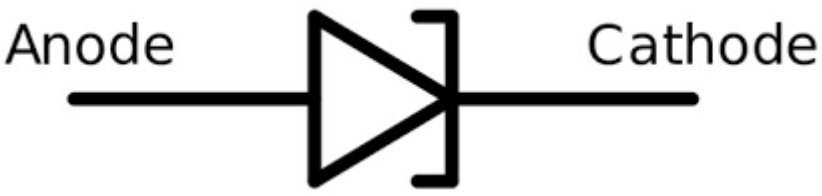
**2. Colour Cameras**

## TUNNEL DIODE

. A Tunnel diode is a heavily doped p-n junction diode in which the electric current decreases as the voltage increases.In tunnel diode, electric current is caused by "Tunneling". The tunnel diode is used as a very fast switching device in computers. It is also used in high-frequency oscillators and amplifiers. Tunnel diode was invented in 1958 by Leo Esaki.It is also known as Esaki diode which is named after Leo Esaki for his work on the tunneling effect.

In tunnel diode, the p-type semiconductor act as an anode and the n-type semiconductor act as a cathode.

Symbol



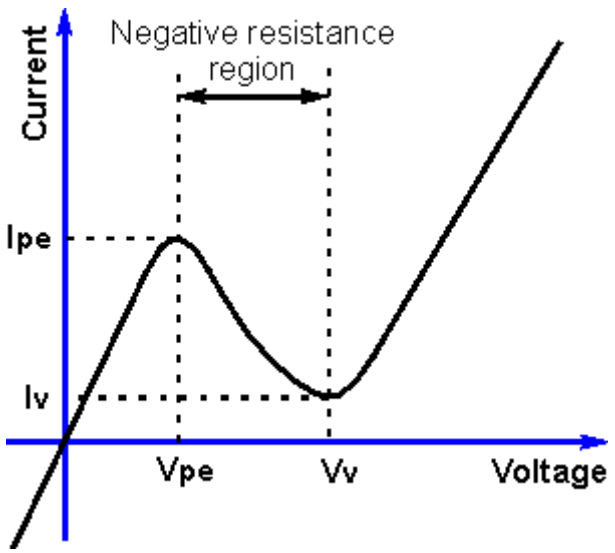

**Tunnelling mechanism & theory**

Tunnelling is an effect that is caused by quantum mechanical effects when electrons pass through a potential barrier. It can be visualised in very basic terms by them "tunnelling" through the energy barrier. The tunnelling only occurs under certain conditions. It occurs within tunnel diodes because of the very high doping levels employed.

At reverse bias, the electrons tunnel from the valence band in the p-type material to the conduction band in the n-type material, and the level of the current increase monotonically.For the forward bias situation there are a number of different areas. For voltages up to Vpe, electrons from the conduction band find increasing availability of empty states in the valence band and the level of current increases up to a point where the current equals Ipe.Once this point is reach, it is found that number of empty states available for electrons with the level of energy they are given by the increased voltage level starts to fall. This means that the current level falls in line with this. The overall current level falls away relatively swiftly, dropping to near zero.

As the current from the tunnelling effect falls, so the diffusion current, which is the same action as occurs in a normal PN junction diode starts to increase and steadily becomes the dominant mechanism.

Tunnel diode characteristics




**Tunnel diode IV characteristic**

The diagram towards the top of the page shows the tunnel diode IV characteristic. This has a form of 'N' shaped curve. With an area of negative resistance between the peak voltage, Vpe and the valley voltage Vv.

The characteristic curve for a tunnel diode shows an area of negative resistance. When forward biased the current in the diode rises at first, but later it can be seen to fall with increasing voltage, before finally rising again. In this diode , current flows in the reverse direction - the reverse breakdown voltage is actually zero and the diode conducts in the reverse direction.

The reason for this is that there are a number of different components to forming the overall curve.

- Normal diode current: This is the 'normal' current that would flow through a PN junction diode.
- Tunnelling current: This is the current that arises as a result of the tunnelling effect.
- Excess current: This is a third element of current that contributes to the overall current within the diode. It results from what may be termed excess current that results from tunnelling though bulk states in the energy gap, and means that the valley current does not fall to zero.

The values for these voltages depend upon the diode material and also upon its individual characteristics. One of the useful figures of merit for a tunnel diode characteristic is the peak to valley current ratio, Ipe / Iv. From the values in the table it can be seen that silicon has a very low value and as a result, this means that it is not normally one of the best options for a tunnel diode.

**Advantages of tunnel diodes**

- Long life
- High-speed operation
- Low noise
- Low power consumption

## POSSIBLE QUESTIONS

**PART-B (2 Marks)**

**1.** What is the difference between BJT and FET?

2. What is called Tunnel Diode?

3. What is called as tunneling effect?

4. What do you mean by charge coupled device?

5.What are the different mode of operations of MOSFET?

6. List out the advantages of CMOS.

7. List out the advantages of Tunnel diode.

8. Define transconductance.

9. What do ypu meant by negative resistance region?

10.What are the frequency limitations of MOSFET?

**PART-C ( 6 Marks)**

1.Explain working principle and characteristics of UJT.

2.Explain working principle and characteristics of JFET.

3.Explain working principle and characteristics of tunnel diode.

4.Explain working principle and characteristics of D MOSFET

5.Explain working principle and characteristics of E MOSFET.

6.Explain working principle and characteristics of CMOS.

7.Write short note on i) CCD ii) tunneling effect.

8.Explain briefly about charge coupled device.

9.Explain working principle of relaxation oscillator.

10.Explain working principle of MOSFET amplifier.

| KARPAGAM ACADEMY OF HIGHER EDUCATION,COIMBATORE-21 | | | | | |
|---|---|---|---|---|---|
| **DEPARTMENT OF PHYSICS** | | | | | |
| **CLASS: II B.Sc., PHYSICS (2017-2020)** | | | | | |
| **PART – A Online Examination (1 mark questions)**<br>**SUBJECT: PHYSICS OF DEVICES AND COMMUNICATION**<br>**SUBJECT CODE: 17PHU302** | | | | | |
| **UNIT - I** | | | | | |
| | **Option-1** | **Option-2** | **Option-3** | **Option-4** | **Key** |
| Junction Field Effect Transistors (JFET) contain how many diodes? | 4 | 3 | 2 | 1 | 2 |
| When not in use, MOSFET pins are kept at the same potential through the use of: | shipping foil | nonconductive foam | conductive foam | a wrist strap | conductive foam |
| D-MOSFETs are sometimes used in series to construct a cascode high-frequency amplifier to overcome the loss of: | low output impedance | capacitive reactance | high input impedance | inductive reactance | high input impedance |
| A "U" shaped, opposite-polarity material built near a JFET-channel center is called the: | gate | block | drain | heat sink | gate |
| In the constant-current region, how will the $I_{DS}$ change in an n-channel JFET? | As $V_{GS}$ decreases $I_D$ decreases | As $V_{GS}$ increases $I_D$ increases. | As $V_{GS}$ decreases $I_D$ remains constant | As $V_{GS}$ increases $I_D$ remains constant | As $V_{GS}$ decreases $I_D$ decreases |
| A MOSFET has how many terminals? | 2 or 3 | 5 | 6 | 3 or 4 | 3 or 4 |
| $I_{DSS}$ can be defined as: | the minimum possible drain current | the maximum possible current with $V_{GS}$ held at –4 V | the maximum possible current with $V_{GS}$ held at 0 V | the maximum drain current with the source shorted | the maximum possible current with $V_{GS}$ held at 0 V |
| What is the input impedance of a common-gate configured JFET? | very low | high | low | very high | very low |

| | | | | | |
|---|---|---|---|---|---|
| JFET terminal "legs" are connections to the drain, the gate, and the: | channel | source | substrate | cathode | source |
| A very simple bias for a D-MOSFET is called: | widening the channel | gate biasing | zero biasing | voltage-divider biasing | zero biasing |
| With the E-MOSFET, when gate input voltage is zero, drain current is: | at saturation | zero | $I_{DSS}$ | widening the channel | zero |
| When an input signal reduces the channel size, the process is called: | enhance ment | substrate connectin g | gate charge | depletion | depletion |
| Which JFET configuration would connect a high-resistance signal source to a low-resistance load? | source follower | common-source | common-drain | common-gate | source follower |
| How will electrons flow through a p-channel JFET? | from source to drain | from source to gate | from drain to gate | from drain to source | from drain to source |
| When $V_{GS}$ = 0 V, a JFET is: | saturated | an analog device | an open switch | cut off | saturated |
| When applied input voltage varies the resistance of a channel, the result is called: | saturizati on | polarizati on | cutoff | field effect | field effect |
| When is a vertical channel E-MOSFET used? | for high frequenci es | for high voltages | for high currents | for high resistances | for high currents |
| A UJT has ……. | Two pn junctions | one on junction | three pn junction | foue pn junction | one on junction |
| In a UJT, the p-type emitter is ……. doped | Lightly | Heavily | Moderatel y | very heavily | Heavily |
| When a UJT is turned ON, the resistance between emitter terminal and lower base terminal … | remains the same | increased | decreased | zero | increased |

| | | | | | |
|---|---|---|---|---|---|
| To turn on UJT, the forward bias on the emitter diode should be …… the peak point voltage | Less than | more than | zero | grater than or equal | more than |
| UJT is sometimes called ……. diode | Low resistance | high resistance | Single-base | double-base | double-base |
| When the temperature increases, the inter-base resistance (RBB) of a UJT …… | remains the same | increased | decreased | zero | increased |
| When the temperature increases, the intrinsic stand off ratio | remains the same | increased | decreased | zero | remains the same |
| Between the peak point and the valley point of UJT emitter characteristics we have …….. region | Saturation | Negative resistance | Cut-off | positive resistance | Negative resistance |
| The device that exhibits negative resistance region is | FET | UJT | Triac | Diac | UJT |
| The UJT may be used as | amplifier | sawtooth generator | rectifier | switch | sawtooth generator |
| Which of the following is not a characteristic of UJT? | Intrinsic stand off ratio | Negative resistance | Peak-point voltage | Bilateral conduction | Bilateral conduction |
| When the JFET is no longer able to control the current, this point is called the | breakdown region | depletion region | saturation point | pinch-off region | breakdown region |
| With a JFET, a ratio of output current change against an input voltage change is called | gain | transconductance | siemens | resistivity | transconductance |
| Which type of JFET bias requires a negative supply voltage? | feedback | source | gate | voltage divider | gate |
| The type of bias most often used with E-MOSFET circuits is: | constant current | drain-feedback | voltage-divider | zero biasing | drain-feedback |

| | | | | | |
|---|---|---|---|---|---|
| The output of the comparator for CMOS IC's is_____ | 0.5V | 1.2V | 2.5V | 4.5V | 2.5V |
| Which component is considered to be an "OFF" device? | transistor | JFET | D-MOSFET | E-MOSFET | E-MOSFET |
| In MOS transistors, _____ is used for their gate | metal | silicon-di-oxide | polysilicon | gallium | polysilicon |
| The gate region consists of | insulating layer | conducting layer | lower metal layer | p type layer | conducting layer |
| Source in MOS transistors is doped with _____ material | n-type | p-type | c-type | e-type | n-type |
| In N channel MOSFET which is the more negative of the elements? | source | gate | drain | source and drain | source |
| If the gate is given sufficiently large charge, electrons will be attracted to | drain region | channel region | switch region | bulk region | channel region |
| nMOS devices are formed in | p-type substrate of high doping level | n-type substrate of low doping level | p-type substrate of moderate doping level | n-type substrate of high doping level | p-type substrate of moderate doping level |
| Source and drain in nMOS device are isolated b | a single diode | two diodes | three diodes | four diodes | two diodes |
| In enhancement mode, device is in _____ condition | conducting | non conducting | partially conducting | insulating | non conducting |
| MOS transistor structure is | symmetrical | non symmetrical | semi symmetrical | pseudo symmetrical | symmetrical |
| nMOS is | donor doped | acceptor doped | no doping | insulating | acceptor doped |
| pMOS is | donor doped | acceptor doped | no doping | insulating | donor doped |

| | | | | | |
|---|---|---|---|---|---|
| Inversion layer in enhancement mode consists of excess of | positive carriers | negative carriers | both in equal quantity | neutral carriers | negative carriers |
| As source drain voltage increases, channel depth | increases | decreases | logarithmically increases | exponentially increses | decreases |
| If the n-MOS and p-MOS of the CMOS inverters are interchanged the output is measured at: | Source of the both transistor | Drains of the both transistor | Drain of n-MOS and source of p-MOS | Source of n-MOS and drain of p-MOS | Source of the both transistor |
| What will be the effect on output voltage if the positions of n-MOS and p-MOS in CMOS inverter circuit are exchanged? | Output is same | Output is reversed | Output is always high | Output is always low | Output is reversed |
| The average power dissipated in resistive load n-MOS inverter is: | 0 | VDD (VDD-VOL)/R | VDD (VDD-VOL)/2R | VDD (VDD-VIH)/2R | VDD (VDD-VOL)/2R |
| In the CMOS inverter the output voltage is measured across: | Drain of n-MOS transistor and groun | Source of p-MOS transistor and ground | Source of n-MOS transistor and source of p-MOS transistor | Gate of p-MOS transistor and Gate of n-MOS transistor | Drain of n-MOS transistor and groun |
| Tuneel diode operates in | Microwave region | low frequency region | visible | radio | Microwave region |
| The tunneling phenomenon is a carrier effect | majority | minority | no carrier | hole | majority |
| The enhancement mode n-MOS load inverter requires 2 different supply voltages to: | Keep load transistor in cutoff region | Keep load transistor in linear region | Keep load transistor in saturation region | Keep load resistor in saturation region | Keep load transistor in linear region |

| | | | | | |
|---|---|---|---|---|---|
| When the input of the CMOS inverter is equal to Inverter Threshold Voltage Vth, the transistors are operating in: | N-MOS is cutoff, p-MOS is in Saturation | P-MOS is cutoff, n-MOS is in Saturation | Both the transistors are in linear region | Both the transistors are in saturation region | Both the transistors are in saturation region |
| The switching threshold voltage VTH for an ideal inverter is equal to | (VDD-VOL)/2 | VDD | (VDD)/2 | 0 | (VDD)/2 |
| In dynamic CMOS logic _____ is used | two phase clock | three phase clock | one phase clock | four phase clock | one phase clock |
| In clocked CMOS logic, output in evaluated in | on period | off period | both periods | half of on period | both periods |
| In clocked CMOS logic, rise time and fall time are | faster | slower | faster first and then slows down | slower first and then speeds up | slower |
| In CMOS domino logic _____ is used | two phase clock | three phase clock | one phase clock | four phase clock | one phase clock |
| In CMOS domino logic _____ is possible | inverting structure | non inverting structure | inverting and non inverting structure | very complex design | non inverting structure |

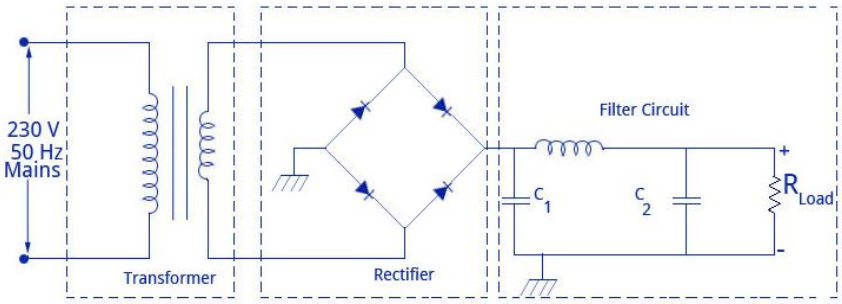
## UNIT-II

## SYLLABUS

Power supply and Filters: Block Diagram of a Power Supply, Qualitative idea of C and L Filters. IC Regulators, Line and load regulation, Short circuit protection. Active and Passive Filters, Low Pass, High Pass, Band Pass and band Reject Filters.
Multivibrators: Astable and Monostable Multivibrators using transistors.

## POWER SUPPLY

Almost all basic household electronic circuits need an unregulated AC to be converted to constant DC, in order to operate the electronic device. All devices will have a certain power supply limit and the electronic circuits inside these devices must be able to supply a constant DC voltage within this limit. That is, all the active and passive electronic devices will have a certain DC operating point (Q-point or Quiescent point), and this point must be achieved by the source of DC power. The DC power supply is practically converted to each and every stage in an electronic system. Thus a common requirement for all this phases will be the DC power supply. All low power system can be run with a battery. But, for long time operating devices, batteries could prove to be costly and complicated. The best method used is in the form of an unregulated power supply –a combination of a transformer, rectifier and a filter. The diagram is shown below.




**Unregulated Power Supply – Diagram**

As shown in the figure above, a small step down transformer is used to reduce the voltage level to the devices needs. The output of the transformer is a pulsating sinusoidal AC voltage, which is converted to pulsating DC with the help of a rectifier. This output is given to a filter circuit which reduces the AC ripples, and passes the DC components. But there are certain disadvantages in using an unregulated power supply.

**1. Poor Regulation –** When the load varies, the output does not appear constant. The output voltage changes by a great value due to the huge change in current drawn from the supply. This is mainly due to the high internal resistance of the power supply (>30 Ohms).

**2. AC Supply Main Variations –** The maximum variations in AC supply mains is give or take 6% of its rated value . But this value may go higher in some countries (180-280 volts). When the value is higher it's DC voltage output will differ largely.

**3. Temperature Variation –** The use of semiconductor devices in electronic devices may cause variation in temperature.

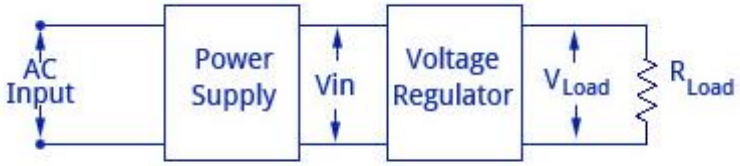
These variations in dc output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. For instance, in oscillators the frequency will shift, in transmitters output will get distorted, and in amplifiers the operating point will shift causing bias instability.

All the above listed problems are overcome with the help of a voltage regulator which is employed in conjunction with an unregulated power supply. Thus, the ripple voltage is largely reduced. Thus, the supply becomes a regulated power supply.

The internal circuitry of a regulated power supply also contains certain current limiting circuits which helps the supply circuit from getting fried from inadvertent circuits. Nowadays, all the power supplies use IC's to reduce ripples, enhance voltage regulation and for widened control options. Programmable power supplies are also available to allow remote operation that is useful in many settings.

## REGULATED POWER SUPPLY

Regulated power supply is an electronic circuit that is designed to provide a constant dc voltage of predetermined value across load terminals irrespective of ac mains fluctuations or load variations.



As shown in the figure, the two main parts of a regulated power supply are a simple power supply and a voltage regulating device. The power supply output is given as input to the voltage regulating device that provides the final output. The voltage output of the power supply remains constant irrespective of large variations in the input AC voltage or output load current.

The input AC voltage (230 Voltas Vrms), is supplied to a transformer. The output will be a stepped down ac output appropriate for the desired dc output. This ac voltage is then given to a bridge rectifier to produce a full-wave rectified output. This is then given to a pi-filter circuit to produce a dc voltage. The filter output may have some ac voltage variations and ripples. This is further filtered using a regulating circuit whose output will be a constant dc voltage. This regulated dc voltage is then given to a voltage divider, which supplies the different dc voltages that may be needed for different electronic circuits.

The potential divider is a single tapped resistor connected across the output terminals of the supply. The tapped resistor may consist of two or three resistors connected in series across the supply. A bleeder resistor may also be employed as a potential divider.

**Power Supply Characteristics**

The quality of the power supply is determined by various characteristics lik**e** load voltage, load current, voltage regulation, source regulation, output impedance, ripple rejection, and so on. Some of the characteristics are briefly explained below:

1. **Load Regulation** – The load regulation or load effect is the change in regulated output voltage when the load current changes from minimum to maximum value.

Load regulation = Vno-load – Vfull-load

Vno-load – Load Voltage at no load

Vfull-load – Load voltage at full load.

From the above equation it is clear that when Vno-load occurs the load resistance is infinite, that is, the out terminals are open circuited. Vfull-load occurs when the load resistance is of the minimum value where voltage regulation is lost.

% Load Regulation = [(Vno-load – Vfull-load)/Vfull-load] * 100

2. **Minimum Load Resistance** – The load resistance at which a power supply delivers its full-load rated current at rated voltage is referred to as minimum load resistance.

Minimum Load Resistance = Vfull-load/Ifull-load

The value of Ifull-load, full load current should never increase than that mentioned in the data sheet of the power supply.

3. **Source/Line Regulation** – In the block diagram, the input line voltage has a nominal value of 230 Volts but in practice, there are considerable variations in ac supply mains voltage. Since this ac supply mains voltage is the input to the ordinary power supply, the filtered output of the bridge rectifier is almost directly proportional to the ac mains voltage.

The source regulation is defined as the change in regulated output voltage for a specified rage of line voltage.

4. **Output Impedance** – A regulated power supply is a very stiff dc voltage source. This means that the output resistance is very small. Even though the external load resistance is varied, almost no change is seen in the load voltage. An ideal voltage source has an output impedance of zero.

5. **Ripple Rejection** – Voltage regulators stabilize the output voltage against variations in input voltage. Ripple is equivalent to a periodic variation in the input voltage. Thus, a voltage regulator attenuates the ripple that comes in with the unregulated input voltage. Since a voltage regulator uses negative feedback, the distortion is reduced by the same factor as the gain

**FILTER:**

An electrical filter is a circuit that can be designed to modify, reshape or reject all unwanted frequencies of an electrical signal and accept or pass only those signals wanted by the circuits designer. Electronic filters are mainly used in power supplies to filter out the ac components in the rectifier output.

A rectifier is actually required to produce pure d.c. supply for using at various places in the electronics circuits. However, the output of a rectifier is pulsating. That means it contains both a.c.component and d.c. component. If such a pulsating d.c. is applied in an electronics circuit, it will produce a hum. So the a.c. component in the pulsating rectifier output is undesirable and must be kept away from the load. To do so, a filter circuit is used which removes the a.c. component and allows only the d.c. component.

A filter circuit is a device which removes the a.c. component of rectifier output and allows only d.c. component to reach the load.

**Types of Filter Circuits**

The most commonly used filter circuits are:

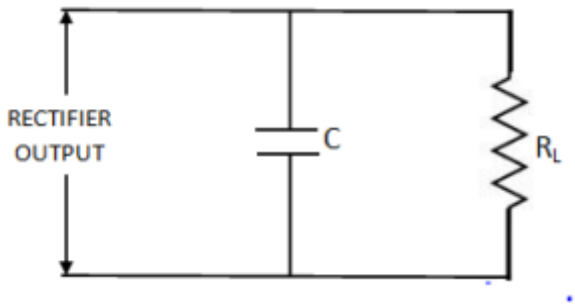
1. Capacitor Filter
2. Choke input Filter

A capacitor is used as the filter and this high value capacitor is shunted or placed across the load impedance. This capacitor, when placed across a rectifier gets charged and stores the charged energy during the conduction period. When the rectifier is not conducting, this energy charged by the capacitor is delivered back to the load. Through this energy storage and delivery process, the time duration during which the current flows through the load resistor gets increased and the ripples are decreased by a great amount. Thus for the ripple component with a frequency of 'f' megahertz, the capacitor 'C' will offer a very low impedance. The value of this impedance can be written as:

Shunt Capacitor Impedance = 1/2 fC

Thus the dc components of the input signal along with the few residual ripple components, is only allowed to go through the load resistance RLoad. The high amount of ripple components of current gets bypassed through the capacitor C.

The circuit diagram of a typical capacitor filter is shown in the figure .




The capacitor filter circuit consists of a capacitor C placed across the rectifier output in parallel with load resistance $R_L$. The pulsating d.c. output of the rectifier is applied across the capacitor.

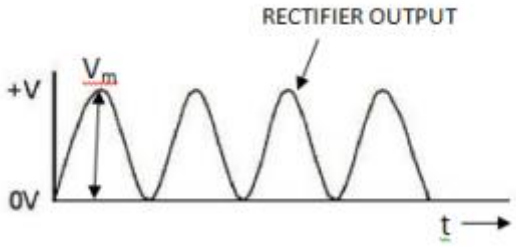



Figure-1

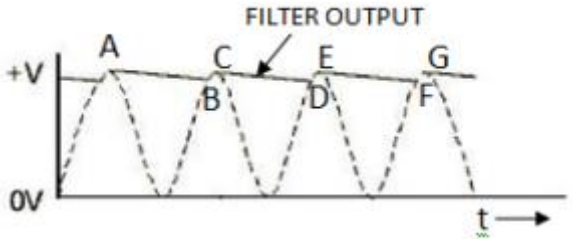



Figure-2

At the end of quarter cycle i.e. at point A in fig.2 the capacitor is charged to the peak value of the rectifier voltage i.e. $V_m$.

As the rectifier voltage now starts to decrease, the capacitor discharges through the load and voltage across it decreases. So voltage across $R_L$ also decreases. This is shown by the line AB in fig.2.The voltage across the load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor.This process is repeated again and again and the output voltage waveform becomes ABCDEFG as shown in the fig.2

**Advantages of Capacitor Filter**

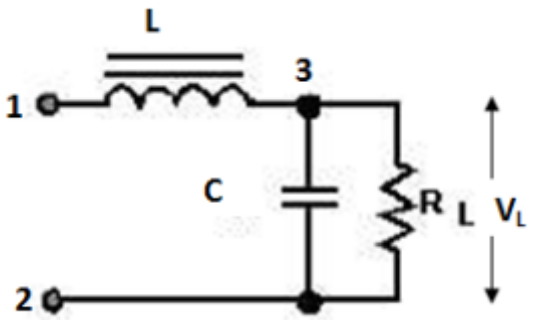
1. Capacitor filter circuits are extremely popular because of its low cost.
2. These filters are of very small size.
3. It has a little weight.
4. It has good characteristics.

For small load currents up to 50mA this type of filter is preferred. It is commonly used in transistor radio battery eliminators.

**Choke Input Filter- Inductor Filter**

The inductor carries the property of opposing the change in current that flows through it.In other words, the inductor offers high impedance to the ripples and no impedance to the desired dc components. Thus the ripple components will be eliminated. When the rectifier output current increases above a certain value, energy is stored in it in the form of a magnetic field and this energy is given up when the output current falls below the average value. Thus all the sudden changes in current that occurs in the circuit will be smoothened by placing the inductor in series between the rectifier and the load.

Fig.shows a typical choke input filter circuit. The rectifier output which is applied as input to the choke input filter is shown in fig.




The circuit of a choke input filter consists of a choke L connected in series with the rectifier output and a filter capacitor C, which is connected across the load resistance $R_L$. The pulsating output of the rectifier is applied across the terminal 1 and 2 of the filter circuit.

This pulsating output contains both a.c. and d.c. component. As we know, the choke L offers a high resistance to the passage of a.c. component and passes the d.c. component readily. So most of the a.c. component appears across the choke L , while all the d.c. component passes through the choke L on its way to the load. This results in the reduced pulsation at terminal 3 as most of the a.c. component are blocked by the choke L now.At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which are managed to pass through the choke L. Now, the filter capacitor by passes the a.c. component but opposes the d.c. component to flow through it. Therefore, only the d.c. component reaches the load $R_L$.

**`Voltage Regulators**

It is an integrated circuit whose basic purpose is to regulate the unregulated input voltage and provide with a constant, regulated output voltage**.**

**Types of Regulators**

Regulators can be classified into different categories, depending upon their working and type of connection.

**Depending upon the type of regulation**, the regulators are mainly divided into two types namely, line and load regulators.

- **Line Regulator** − The regulator which regulates the output voltage to be constant, in spite of input line variations, it is called as **Line regulator**.
- **Load Regulator** − The regulator which regulates the output voltage to be constant, in spite of the variations in load at the output, it is called as **Load regulator**.

**Depending upon the type of connection**, there are two type of voltage regulators. They are

- Series voltage regulator
- Shunt voltage regulator

A voltage regulator is one of the most widely used electronic circuitry in any device. A regulated voltage (without fluctuations & noise levels) is very important for the smooth functioning of many digital electronic devices. A common case is with micro controllers, where a smooth regulated input voltage must be supplied for the micro controller to function smoothly.

**Voltage regulators are of different types**

An IC based voltage regulator can be classified in different ways. A common type of classification is 3 terminal voltage regulator and 5 or multi terminal voltage regulator. Another popular way of classifying IC voltage regulators is by identifying them as linear voltage regulator & switching voltage regulator. There is a third set of classification as 1) Fixed voltage regulators (positive & negative) 2) Adjustable voltage regulators (positive & negative) and finally 3) Switching regulators. In the third classification, fixed & adjustable regulators are basically versions of linear voltage regulators.

**Fixed Voltage Regulators**

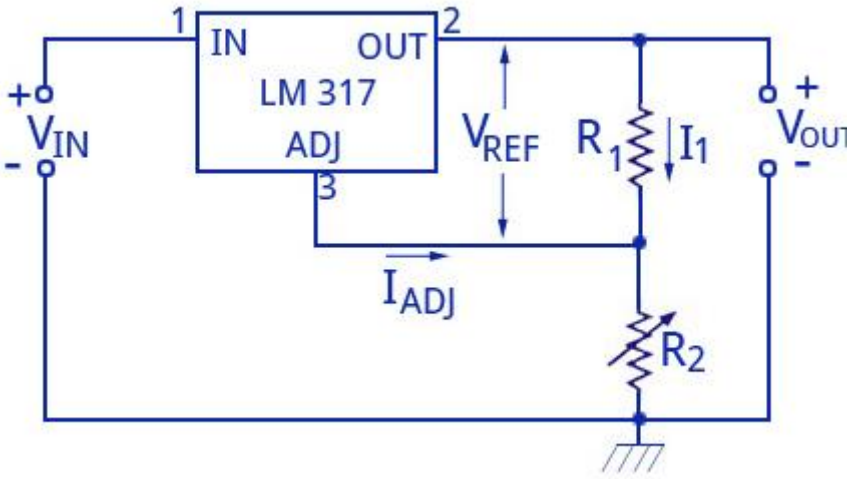
These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage. All those IC's in the

78XX series are fixed positive voltage regulators. In the IC nomenclature – 78XX ; the part XX denotes the regulated output voltage the IC is designed for. Examples:- 7805, 7806, 7809 etc.

A negative fixed voltage regulator is same as the positive fixed voltage regulator in design, construction & operation. The only difference is in the polarity of output voltages. These IC's are designed to provide a negative output voltage. Example:- 7905, 7906 and all those IC's in the 79XX series.

**Adjustable Voltage Regulator**

An adjustable voltage regulator is a kind of regulator whose regulated output voltage can be varied over a range. There are two variations of the same; known as positive adjustable voltage regulator and negative adjustable regulator. LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 volts to 57 volts. LM337 is an example of negative adjustable voltage regulator. LM337 is actually a complement of LM317 which are similar in operation & design; with the only difference being polarity of regulated output voltage.




There may be certain conditions where a variable voltage may be required. Right now we shall discuss how an LM317 adjustable positive voltage regulator IC is connected.

The resistors R1 and R2 determine the output voltage Vout. The resistor R2 is adjusted to get the output voltage range between 1.2 volts to 57 volts. The output voltage that is required can be calculated using the equation:

Vout = Vref (1+R2/R1) + Iadj R2

In this circuit, the value of Vref is the reference voltage between the adjustment terminals and the output taken as 1.25 Volt.

The value of Iadj will be very small and will also have a constant value. Thus the above equation can be rewritten as

Vout = 1.25 (1+R2/R1)

In the above equation, due to the small value of Iadj, the drop due to R2 is neglected.

The load regulation is 0.1 percent while the line regulation is 0.01 percent per volt. This means that the output voltage varies only 0.01 percent for each volt of input voltage. The ripple rejection is 80 db, equivalent to 10,000.

The LM 337 series of adjustable voltage regulators is a complement to the LM 317 series devices. The negative adjustable voltage regulators are available in the same voltage and current options as the LM 317 devices

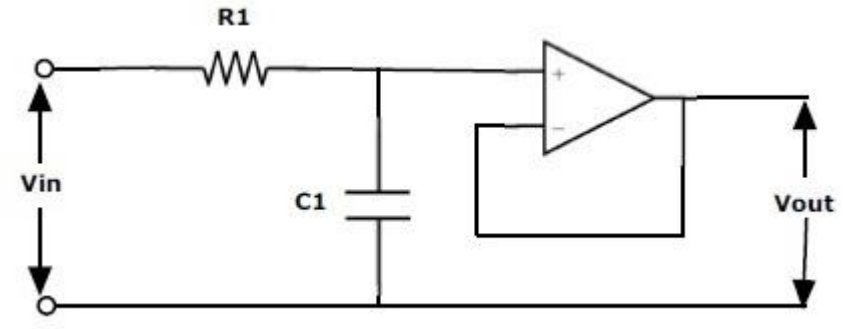
**Active Low Pass Filter:**

Low Pass filter is a filter which passes all frequencies from DC to upper cut-off frequency fH and rejects any signals above this frequency.

In ideal case, the frequency response curve drops at the cut-off frequency. Practically the signal will not drop suddenly but drops gradually from transition region to the stop band region. Cut-off frequency means the point where the response drops -3 dB or 70.7% from the pass band. Transition region means the area where falloff occurs. Stop band region means the area where the attenuation occurs mostly to the input signals. So this filter is also called as high-cut filter or treble cut filter.

The attenuation of the signal that is the amplitude of the output signal is lesser than amplitude of the input signal in the passive circuit. In order to overcome this disadvantage of passive filter active filter is designed. A Passive filter connected to the inverting or non-inverting op-amp gives us a simple active low pass filter.

First order active filter is formed by a single op-amp with RC circuit. A simple RC Passive Filter connected to the non-inverting terminal of an operational amplifier is shown below




This RC circuit will provide a low frequency path to the input of the amplifier. The amplifier acts as a buffer circuit providing unity gain output. This circuit has more input impedance value. Even though the input impedance of the op-amps high below the cut-off frequency, this input impedance is limited by the series impedance which is equal to $R+ 1/j\omega C$.

The output impedance of the op-amp which is connected in the circuit is always low. This circuit will provide high stability to filter. The main drawback of this configuration is voltage gain is unity. Even for this circuit also the output power is high since the input impedance is low.

The frequency response of Active low pass filter is same as that of the passive low pass filter, except that the amplitude of the output signals. The voltage gain of the non-inverting operational amplifier is given as

**AF = 1+ (R2/R1)**

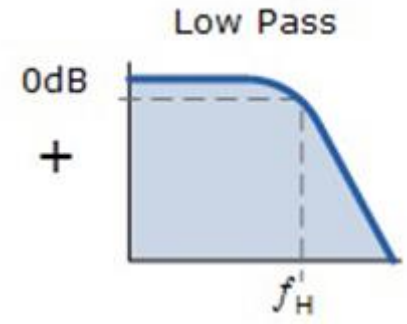
The gain of active low pass filter is given as

**Av = Vout / Vin = AF/ [$\sqrt{(1+(f/fc)^2)}$ ]**

Where

- AF is the pass band gain (1+ R2/R1)
- *f* is the frequency of input signal
- *fc* is the cut-off frequency

**Frequency Response:**



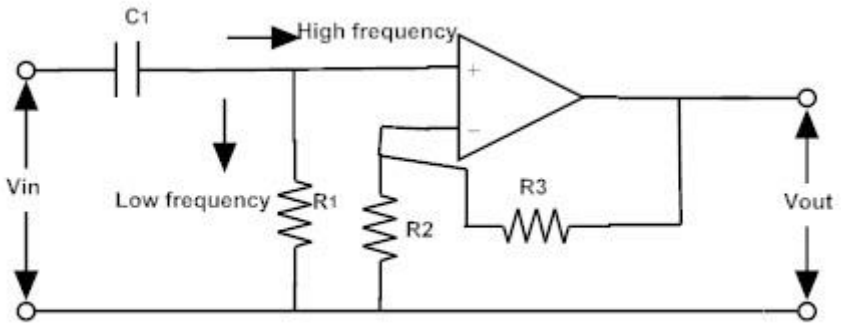

**Active High Pass Filter:**

A high pass filter will allow the frequencies which are higher than the cut-off frequency and attenuate the frequencies lower than the cut off frequency. In some cases this filter is also termed as 'Low-Cut' filter or 'Base-cut' filter. The amount of attenuation or the pass band range will depend on the designing parameters of the filter.

The pass band gain of an active filter is more than unity gain. The operation of the active high pass filter is same as passive high pass filter, but the main difference is that the active high pass filter uses operational an amplifier which provides amplification of the output signals and controls gain.

By connecting a passive RC high pass filter circuit to the inverting or non-inverting terminal of the op-amp gives us first order active high pass filter. The passive RC high pass filter circuit connected to the non-inverting terminal of the unity gain operational amplifier is shown below.

**Active High Pass Filter Circuit Diagram**




The simple Active high pass filter can be obtained by connecting a non-inverting or inverting operational amplifier to the passive high pass RC circuit. The frequency response of active high pass filter is same as that of passive low pass filter, except that the magnitude of the signal is increased by the gain of operational amplifier. In active high pass filter pass band is limited due to the open loop characteristics of operational amplifier.

The operation is same as that of the passive high pass filter, but the input signal is amplified by the amplifier at the output. The amount of amplification depends on the gain of the amplifier. The magnitude of the pass band gain is equal to $1 + (R_3/R_2)$. Where R3 is the feedback resistor in Ω (ohms) and $R_2$ is the input resistor.

The gain of active high pass filter is given as

$$\mathbf{Av = Vout / Vin = (AF (}\boldsymbol{f / fc}\mathbf{)) / (}\sqrt{[}\sqrt{\mathbf{(1+(}\boldsymbol{f/fc}\mathbf{)^2)}}\mathbf{ ]}$$

Where

- AF is the pass band gain (1+ R2/R1)

- *f* is the frequency of input signal
- *fc* is the cut-off frequency

Voltage gain in dB is given as

**Av (dB) = $20\log_{10}$ (Vout/Vin)**

**-3dB = $20\log_{10}$ (0.707 x Vout/Vin)**

For a first order Active high pass filter the frequency response curve increases at a rate of 20dB/decade or 6dB/octave until it reaches the cut-off frequency point. Same as like passive filter here also cut-off frequency can be calculated using the formula

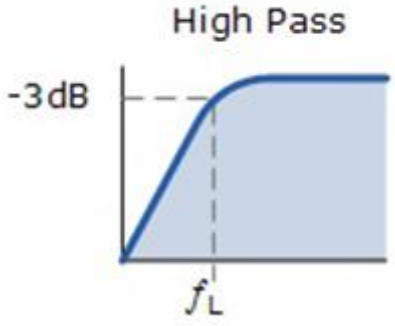
***fc* = 1 / (2πRC)**

In this filter the phase shift or phase angle of the output signal *leads* that of the input signal. At cut-off frequency phase angle value is equal to the +45°. This value can be calculated using the below formula.

**Phase angle Ø = $\tan^{-1}$ (1/ (2πRC))**

We can design a single stage active high pass filter using inverting amplifier configuration also. The applications of active high pass filters also same as that of passive high pass filter.

**Frequency Response:**

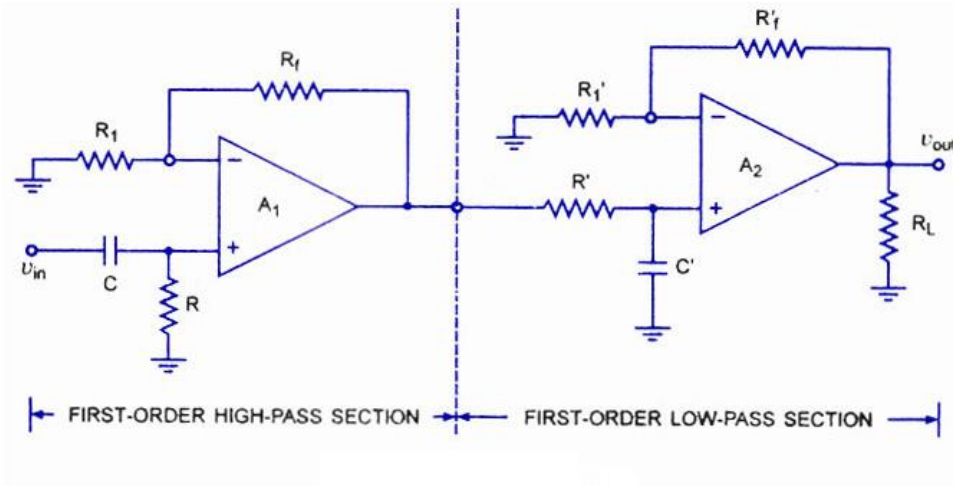



**Active Band Pass Filter:**

A Band Pass Filter is a circuit which allows only particular band of frequencies to pass through it. This Pass band is mainly between the cut-off frequencies and they are $f_L$ and $f_H$. Where $f_L$ is the lower cut-off frequency and $f_H$ is higher cut-off frequency. The centre frequency is denoted by '$f_C$' and it is also called as resonant frequency or peak frequency. The $f_L$ value must always be less than the value of $f_H$. The pass band of the filter is nothing but the bandwidth. The gain of the filter is maximum at resonant or centre frequency and this is referred as total pass band gain. This pass band gain is denoted by '$A_{max}$'.

That is Band pass filter is frequency selective filter used in electronic systems to allow a particular band or certain range of frequencies. This range of frequencies is set between two cut-off frequency points (*fL, fH)*.

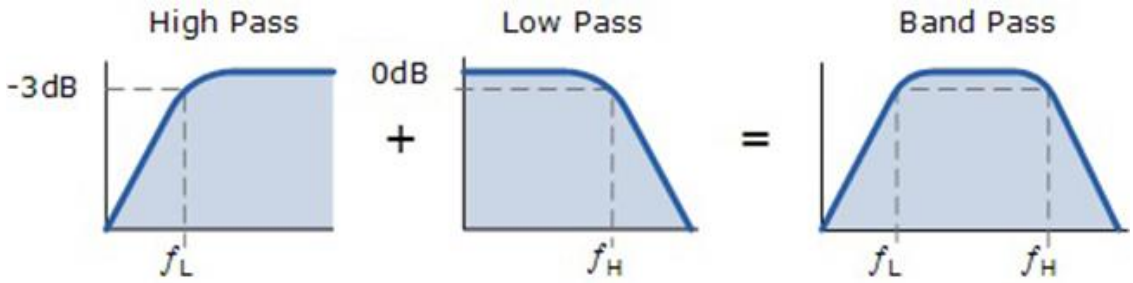
Simple Active pass band filer can be easily designed by combining or cascading a low pass filter with a high pass filter as shown below.




**Active Band Pass Filter Circuit Diagram**

The cascade connection of low pass filter and high pass filter produces a low "Quality factor" type filter which has wide pass band. The first stage of the circuit (high pass filter stage) blocks the very low frequency signals and low pass filter stage blocks the very high frequency signals. It produces the relatively flat pass band frequency response in which one half represents high pass filter response and other half represents the low pass filter response as shown below.

**Frequency response of band pass filter**




The higher cut-off frequency fH and lower cut-off frequency *fL* are calculated using the first order low pass and high pass filter cut-off frequency equations. The amplifier circuit provides isolation between two stages and increases overall gain of the circuit.

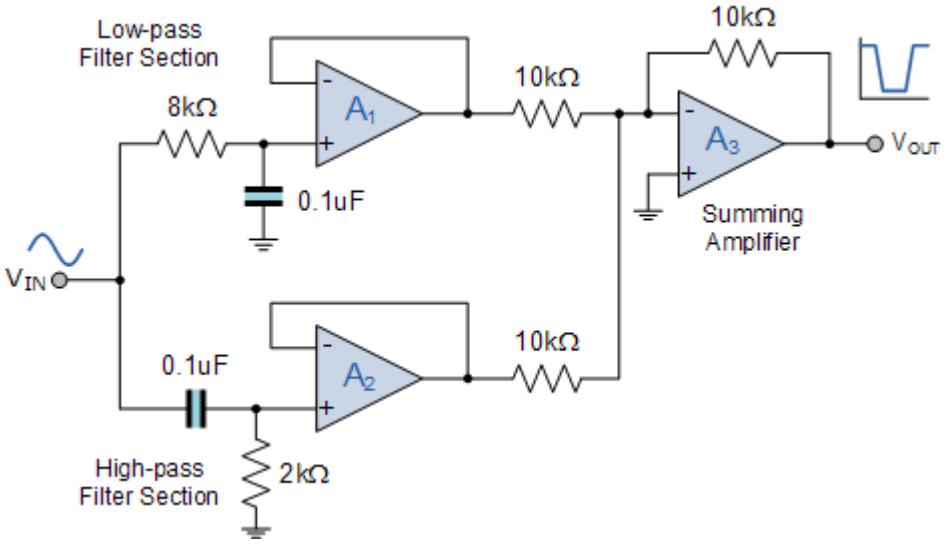
**Active Band Stop or Band Reject Filter:**

The Band Stop Filter**,** is another type of frequency selective circuit that functions in exactly the opposite way to the band pass filter. The band stop filter, also known as a band reject filter, passes all frequencies with the exception of those within a specified stop band which are greatly attenuated.

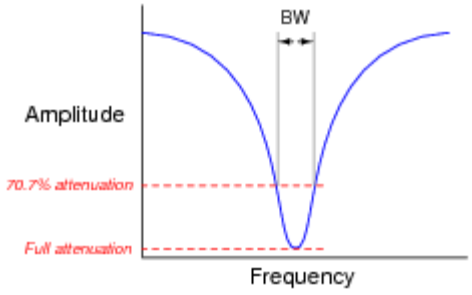
If this stop band is very narrow and highly attenuated over a few hertz, then the band stop filter is more commonly referred to as a notch filter, as its frequency response shows that of a deep notch with high selectivity (a steep-side curve) rather than a flattened wider band. The band stop (band reject or notch) filter is a second-order (two-pole) filter having two cut-off frequencies, commonly known as the -3dB or half-power points producing a wide stop band bandwidth between these two -3dB points.

Then the function of a band stop filter is too pass all those frequencies from zero (DC) up to its first (lower) cut-off frequency point $f_L$, and pass all those frequencies above its second (upper) cut-off frequency $f_H$, but block or reject all those frequencies in-between. Then the filters bandwidth, BW is defined as: $(f_H - f_L)$.

. The ideal band stop filter would have infinite attenuation in its stop band and zero attenuation in either pass band.




## Frequency response curve



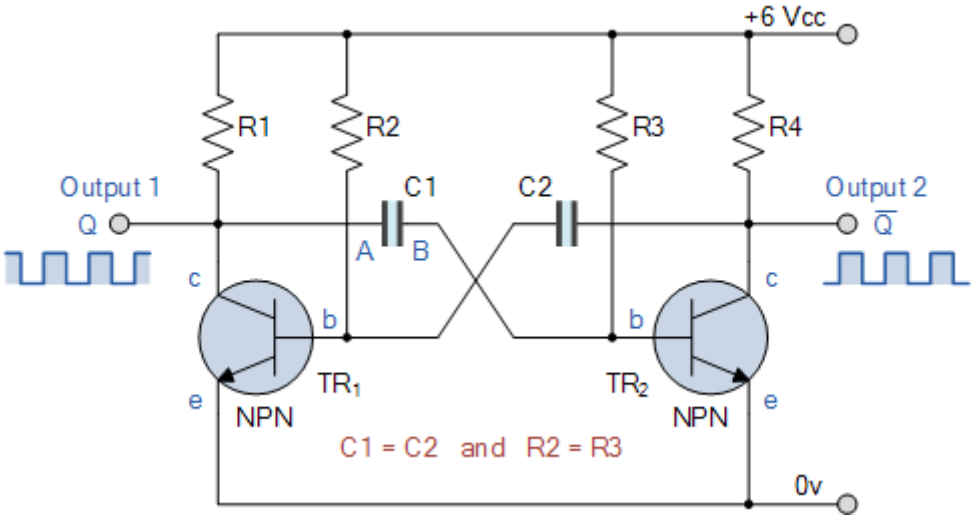

**MULTIVIBRATOR**

A multivibrator is an electronic circuit used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. A multivibrator circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. It is characterized by two amplifying devices cross-coupled by resistor and capacitors .

Multivibrators are classified according to the number of steady (stable) states of the circuit. A steady state exists when circuit operation is essentially constant that is, one transistor remains in conduction and the other remains cut off until an external signal is applied. The three types of multivibrators are the Astable, Monostable, and Bistable .

**Astable Multivibrator**

Regenerative switching circuits such as Astable Multivibrators are the most commonly used type of relaxation oscillator because not only are they simple, reliable and ease of construction they also produce a constant square wave output waveform.




The Astable Multivibrator is another type of cross-coupled transistor switching circuit that has NO stable output states as it changes from one state to the other all the time. The astable circuit consists of two switching transistors, a cross-coupled feedback network, and two time delay capacitors which allows oscillation between the two states with no external triggering to produce the change in state.

In electronic circuits, astable multivibrators are also known as Free-running Multivibrator as they do not require any additional inputs or external assistance to oscillate. Astable oscillators produce a continuous square wave from its output or outputs, (two outputs no inputs) which can then be used to flash lights or produce a sound in a loudspeaker. The basic transistor circuit for an Astable Multivibrator produces a square wave output from a pair of grounded emitter cross-coupled transistors.

Assume that transistor, $TR_1$ has just switched "OFF" (cut-off) and its collector voltage is rising towards Vcc, meanwhile transistor $TR_2$ has just turned "ON". Plate "A" of capacitor C1 is also rising towards the +6 volts supply rail of Vcc as it is connected to the collector of $TR_1$ which is now cut-off. Since $TR_1$ is in cut-off, it conducts no current so there is no volt drop across load resistor $R_1$.

The other side of capacitor, C1, plate "B", is connected to the base terminal of transistor $TR_2$ and at 0.6v because transistor $TR_2$ is conducting (saturation). Therefore, capacitor C1 has a potential difference of +5.4 volts across its plates, (6.0 – 0.6v) from point A to point B.Since $TR_2$ is fully-on, capacitor $C_2$ starts to

charge up through resistor$R_2$ towards Vcc. When the voltage across capacitor $C_2$ rises to more than 0.6v, it biases transistor $TR_1$ into conduction and into saturation.

The instant that transistor, $TR_1$ switches "ON", plate "A" of the capacitor which was originally at Vcc potential, immediately falls to 0.6 volts. This rapid fall of voltage on plate "A" causes an equal and instantaneous fall in voltage on plate "B" therefore plate "B" of C1 is pulled down to -5.4v (a reverse charge) and this negative voltage swing is applied the base of $TR_2$ turning it hard "OFF". One unstable state.

Transistor $TR_2$ is driven into cut-off so capacitor C1 now begins to charge in the opposite direction via resistor R3 which is also connected to the +6 volts supply rail, Vcc. Thus the base of transistor $TR_2$ is now moving upwards in a positive direction towards Vcc with a time constant equal to the C1 x R3 combination. However, it never reaches the value of Vcc because as soon as it gets to 0.6 volts positive, transistor $TR_2$ turns fully "ON" into saturation. This action starts the whole process over again but now with capacitor C2taking the base of transistor $TR_1$ to -5.4v while charging up via resistorR2 and entering the second unstable state.

Then we can see that the circuit alternates between one unstable state in which transistor $TR_1$ is "OFF" and transistor $TR_2$ is "ON", and a second unstable in which $TR_1$ is "ON" and $TR_2$ is "OFF" at a rate determined by the RC values. This process will repeat itself over and over again as long as the supply voltage is present.

The amplitude of the output waveform is approximately the same as the supply voltage, Vcc with the time period of each switching state determined by the time constant of the RC networks connected across the base terminals of the transistors. As the transistors are switching both "ON" and "OFF", the output at either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors.

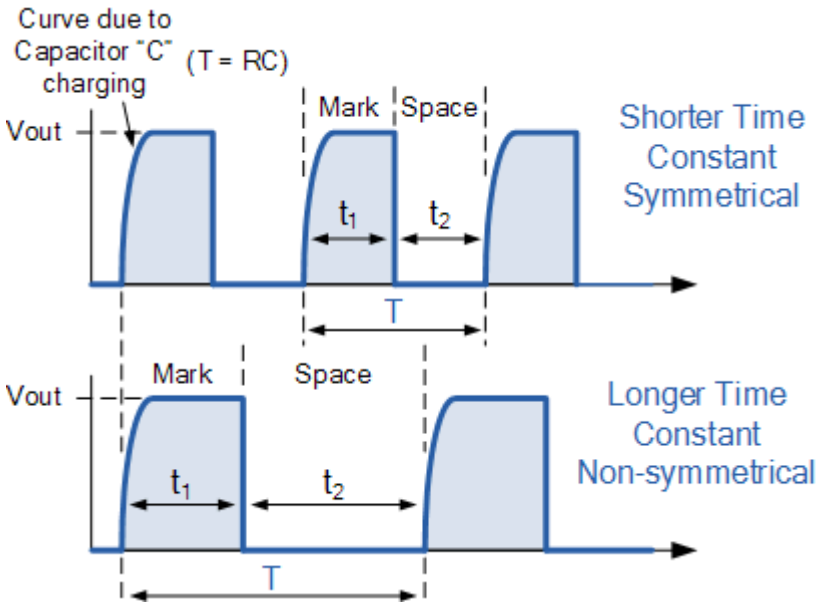
If the two time constants produced by C2 x R2 and C1 x R3 in the base circuits are the same, the mark-to-space ratio ( t1/t2 ) will be equal to one-to-one making the output waveform symmetrical in shape. By varying the capacitors, C1, C2 or the resistors, R2, R3 the mark-to-space ratio and therefore the frequency can be altered.

In astable multivibrator, the length of time that transistor $TR_2$ is "OFF" will be equal to 0.69T or 0.69 times the time constant of C1 x R3. Likewise, the length of time that transistor$TR_1$ is "OFF" will be equal to 0.69T or 0.69 times the time constant ofC2 x R2 and this is defined as.

Periodic Time , T =T1+ T2

T1 =0.69C1R3

T2= 0.69 C2 R2

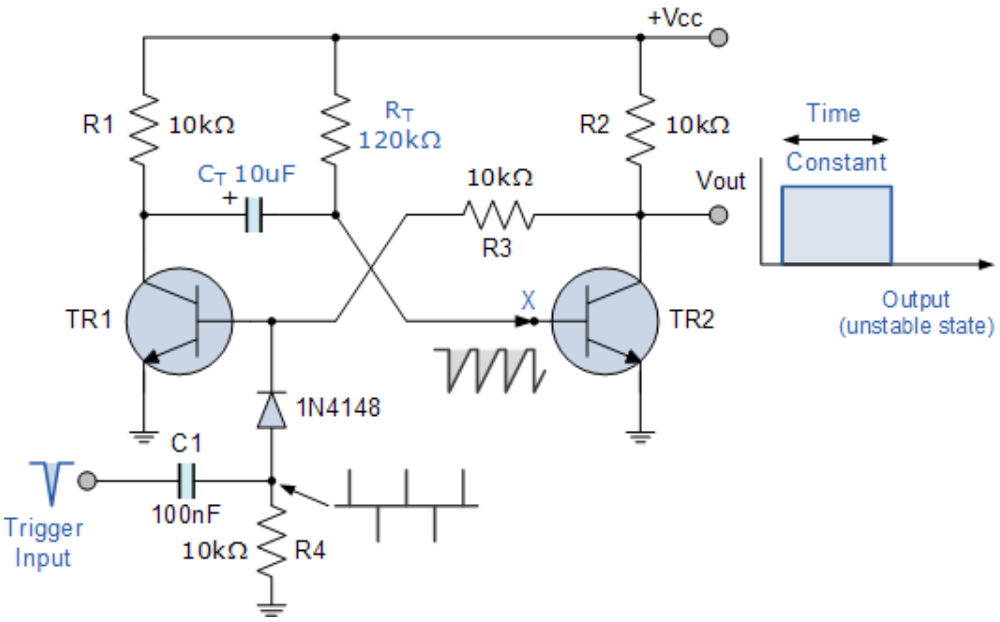



**Monostable Multivibrators**

Monostable Multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state.

The timing cycle of the monostable is determined by the time constant of the timing capacitor, $C_T$ and the resistor, $R_T$ until it resets or returns itself back to its original (stable) state. The monostable multivibrator will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, Monostable Multivibrators have only ONE stable state and go through a full cycle in response to a single triggering input pulse.

**Monostable Multivibrator Circuit**




The basic collector-coupled transistor Monostable Multivibrator circuit and its associated waveforms are shown above. When power is firstly applied, the base of transistor TR2 is connected to Vcc via the biasing resistor, $R_T$ thereby turning the transistor "fully-ON" and into saturation and at the same time turning TR1 "OFF" in the process. This then represents the circuits "Stable State" with zero output. The current flowing into the saturated base terminal of TR2 will therefore be equal to $Ib = (Vcc - 0.7)/R_T$.

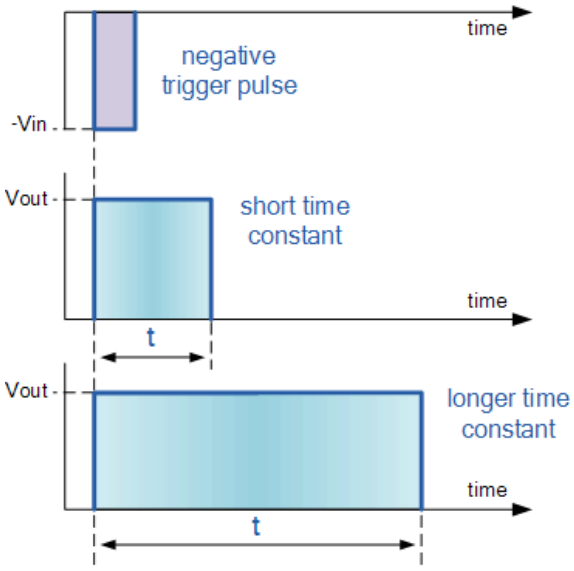
If a negative trigger pulse is now applied at the input, the fast decaying edge of the pulse will pass straight through capacitor, C1 to the base of transistor, TR1 via the blocking diode turning it "ON". The collector ofTR1 which was previously at Vcc drops quickly to below zero volts effectively giving capacitor $C_T$ a reverse charge of -0.7v across its plates. This action results in transistor TR2 now having a minus base voltage at point X holding the transistor fully "OFF". This then represents the circuits second state, the "Unstable State" with an output voltage equal to Vcc.

Timing capacitor, $C_T$ begins to discharge this -0.7v through the timing resistor $R_T$, attempting to charge up to the supply voltage Vcc. This negative voltage at the base of transistor TR2 begins to decrease gradually at a rate determined by the time constant of the $R_T$ $C_T$combination. As the base voltage of TR2 increases back up to Vcc, the transistor begins to conduct and doing so turns "OFF" again transistorTR1 which results in the monostable multivibrator automatically returning back to its original stable state awaiting a second negative trigger pulse to restart the process once again.

Monostable Multivibrators can produce a very short pulse or a much longer rectangular shaped waveform whose leading edge rises in time with the externally applied trigger pulse and whose trailing edge is dependent upon the RC time constant of the feedback components used. This RC time constant may be

varied with time to produce a series of pulses which have a controlled fixed time delay in relation to the original trigger pulse as shown below.

Monostable Multivibrator Waveforms




The time constant of Monostable Multivibrators can be changed by varying the values of the capacitor, $C_T$ the resistor, $R_T$ or both. Monostable multivibrators are generally used to increase the width of a pulse or to produce a time delay within a circuit as the frequency of the output signal is always the same as that for the trigger pulse input, the only difference is the pulse width.

## POSSIBLE QUESTIONS

**PART-A (2 marks)**

1.Define electronic filter.

2. What do you mean by astable multivibrator?

3.What do you mean by monostable multivibrator?

4.What do you mean by multivibrator?

5. What is called as regulated power supply?

6. What are the advantages of regulated power supply?

7.List out the difference between passive and active filters.

8. List out the difference between band pass and band stop filters.

9.What is called line regulation?

10. What is called load regulation?

**PART-C (6 Marks)**

1. Explain working principle of Power Supply with the help of Block Diagram.
2. Explain in low pass filter and plot the frequency response curve.
3. Write short note on C-filter and L-filter.
4. Explain the working of high pass filter and plot the frequency response curve
5. Explain working principle of Monostable multivibrator using transistor.
6. Explain in band pass filter and plot the frequency response curve.
7. Explain working principle of Astable multivibrator using transistor.
8. Explain band reject filter and plot the frequency response curve
9. Explain different type of IC voltage regulators.
10. Explain working principle of Regulated Power Supply with the help of Block Diagram.

| KARPAGAM ACADEMY OF HIGHER EDUCATION,COIMBATORE-21 | | | | | |
|---|---|---|---|---|---|
| DEPARTMENT OF PHYSICS | | | | | |
| CLASS: II B.Sc., PHYSICS (2017-2020) | | | | | |
| PART – A Online Examination (1 mark questions)<br>SUBJECT: PHYSICS OF DEVICES AND COMMUNICATION<br>SUBJECT CODE: 17PHU302 | | | | | |
| UNIT - II | | | | | |
| | **Option-1** | **Option-2** | **Option-3** | **Option-4** | **Key** |
| A _____ filter rejects all frequencies within a specified band and passes all those outside this band. | low-pass | high-pass | band-pass | band-stop | band-stop |
| A _____ filter significantly attenuates all frequencies below $f_c$ and passes all frequencies above $f_c$. | low-pass | high-pass | band-pass | band-stop | high-pass |
| The bandwidth in a _____ filter equals the critical frequency. | low-pass | high-pass | band-pass | band-stop | low-pass |
| Which filter exhibits a linear phase characteristic? | Bessel | Butterworth | Chebyshev | C-filter | Bessel |
| The critical frequency is defined as the point at which the response drops _____ from the passband. | -20dB | -3dB | -6dB | -40dB | -3dB |
| Which filter exhibits the most rapid roll-off rate? | Bessel | Butterworth | Chebyshev | C-filter | Chebyshev |
| Which filter has a maximally flat response? | Bessel | Butterworth | Chebyshev | C-filter | Butterworth |
| One important | low-pass | high-pass | band-pass | band- | band-stop |

| | | | | | |
|---|---|---|---|---|---|
| application of a state-variable _____ filter with a summing amplifier is to minimize the 60 Hz "hum" in audio systems. | | | | stop | |
| A _____ filter passes all frequencies within a band between a lower and an upper critical frequency and rejects all others outside this band. | low-pass | high-pass | band-pass | band-stop | band-pass |
| An electrical filter is a | Phase-selective circuit | Frequency-selective circuit | Filter-selective circuit | angle selective | Frequency-selective circuit |
| The problem of passive filters is overcome by using | Analog filter | Active filter | LC filter | A combination of analog and digital filters | Active filter |
| Find out the incorrect statement about active and passive filters | Gain is not attenuated in active filter | Passive filters are less expensive | Active filter does not cause loading of source | Passive filters are difficult to tune or adjust | Passive filters are less expensive |
| Ideal response of filter takes place in | Pass band and stop band frequency | Stop band frequency | Pass band frequency | none | Pass band frequency |
| A notch filter is a | Wide band pass filter. | Narrow band pass filter. | Wide band reject filter. | Narrow band reject filter. | Narrow band reject filter. |
| The region between the passband and the stopband is called the | Attenuation | Center | Transition | Ripple | Transition |

| | | | | | |
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| The center frequency of a bandpass filter is always equal to | The bandwidth | Geometric average of the cutoff frequencies | Bandwidth divided by Q | 3-dB frequenc y | Geometric average of the cutoff frequencies |
| The Q of a narrowband filter is always | small | equal to BW divided by f0 | less than 1 | greater than 1 | greater than 1 |
| A bandstop filter is sometimes called a | Snubber | Phase shifter | Notch filter | Time-delay circuit | Notch filter |
| The all-pass filter has | No passband | One stopband | the same gain at all frequencies | a fast roll-off above cutoff | the same gain at all frequencies |
| A first-order active-filter stage has | One capacitor | Two op amps | Three resistors | a high Q | One capacitor |
| The all-pass filter is sometimes called a | Tow-Thomas filter | Delay equalizer | KHN filter | State-variable filter | Delay equalizer |
| The multivibrator which generates square wave of its own is the …… multivibrator | astable | monostable | bistable | tristable | astable |
| With most monostable multivibrators, what is the Q output when no input trigger has occurred? | LOW | +5 V | SET | HIGH | LOW |
| An astable multivibrator requires: | balanced time constants | a pair of matched transistors | no input signal | dual J-K flip-flops | no input signal |
| What is the difference between an astable multivibrator and a monostable multivibrator | The astable is free running. | The astable needs to be clocked. | The monostable is free running. | bistable is free running | The astable is free running. |
| Monostable multivibrator is used in the application of___ | 555 timer | 556 timer | Op-amp | Ic741 | 555 timer |

| | | | | | |
|---|---|---|---|---|---|
| Astable multivibrator operating at 150Hz has a discharge time of 2.5m. Find the duty cycle of the circuit. | 50% | 75% | 90% | 37.50% | Burglar alarm |
| How to obtain symmetrical waveform in Astable multivibrator? | Use clocked RS flip-flop | Use clocked JK flip-flop | Use clocked D-flip-flop | Use clocked T-flip-flop | Use clocked JK flip-flop |
| The traffic light control is an application of _____ | IC 741 | IC 7805 | IC 555 | LM 311 | IC 555 |
| The _____ is the monostable multivibrator with a modulating input signal applied at pin 5 of timer | AM | FM | TDM | PWM | PWM |
| ree running frequency of Astable multivibrator? | f=1.45/ ($R_A$+2$R_B$)C | f=1.45(RA+2 RB)C | f=1.45C/ ($R_A$+2$R_B$) | f=1.45 $R_A$/ ( $R_A$+$R_B$) | f=1.45/ ($R_A$+2$R_B$)C |
| . …….multivibrator is a square wave oscillator | astable | monostable | bistable | tristable | astable |
| The monostable multivibrator circuit is not an oscillator because __ | its output switches between two states | it requires a trigger to obtain an output signal | it requires a sine wave input signal | the circuit does not require a dc power supply | it requires a trigger to obtain an output signal |
| What is another name for a bistable multivibrator? | an on-off switch | an oscillator | a flip-flop | amplifier | a flip-flop |
| How to achieve 50% duty cycle in adjustable rectangular wave generator? | $R_1 < R_2$ | R1 > R2 | $R_1 = R_2$ | $R_1 \geq R_2$ | $R_1 = R_2$ |
| Multivibrator is an | amplifier | oscillator | switch | diode | oscillator |
| The pulse width | supply | timing resistor | UTP | timing | supply |

| | | | | | |
|---|---|---|---|---|---|
| out of a one-shot multivibrator increases when the: | voltage increases | decreases | decreases | capacitance increases | voltage increases |
| An astable multivibrator has | No stable state | Two stable state | three stable state | four stable state | No stable state |
| A bistable multivibrator has … | One stable state | Two stable state | three stable state | four stable state | Two stable state |
| A monostable vibrator has | One stable state | Two stable state | three stable state | four stable state | One stable state |
| The multivibrator which generates square wave of its own is the …… multivibrator | monostable | astable | bistable | oscillator | astable |
| In a multivibrator, we have ……. feedback. | Negative | zero | 100 % posivite | 100 % negative | 100 % negative |
| Multivibrators belong to the category of | Square wave oscillators | Triangular wave oscillators | Ramp wave oscillators | Sinusoidal oscillators | Square wave oscillators |
| Which among the following can be used to detect the missing heart beat? | monostable | pulse stretching | Schmitt triggering | astable | monostable |
| In a bistable multivibrator circuit, commutating capacitor is used | To increase the base storage charge | To provide ac coupling | o increase the speed of response | To provide the speed of oscillations | o increase the speed of response |
| How does a monostable multivibrator used as frequency divider? | Using square wave generator | Using triangular wave generator | Using sawtooth wave generator | Using sine wave generator | Using square wave generator |
| The 7812 regulator IC | 5 V | –5 V | 12 V | –12 V | 12 V |

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| provides | | | | | |
| Voltage regulators keep a constant _____ output voltage when the input or load varies within limits. | ripple | dc | ac | ac&dc | dc |
| Switching regulator efficiencies can be greater than _____ percent. | 60 | 70 | 80 | 90 | 90 |
| f the value of full-load voltage is the same as the no-load voltage, the voltage regulation calculated is _____ %, which is the best expected. | 0 | 100 | 50 | 75 | 0 |
| A Multivibrrator produce | squre wave | sine wave | triangular wave | ramp | squre wave |
| A Zener diode utilises …… characteristic for voltage regulation | Forward | Reverse | No baising | zer biasing | Reverse |
| Which among the following are regarded as three-pin voltage regulator ICs? | Fixed voltage regulators | current regulators | Switching regulators | Linear regulators | Fixed voltage regulators |
| Which type of IC voltage regulator exhibits continuous variation in the impedance of transistor in order to supply the desired load current? | Fixed voltage regulators | current regulators | Switching regulators | Linear regulators | Linear regulators |
| In LM317 voltage regulator, what is the minimum | 1V | 3V | 5V | 10V | 3V |

| | | | | | |
|---|---|---|---|---|---|
| value of voltage required between its input & output in order to supply power to an internal circuit? | | | | | |
| In LM317 voltage regulator, the protective diodes do not allow the filter capacitors to discharge through _____current points. | low | High | moderate | very high | low |
| In a linear IC voltage regulator, series pass transistor always operates in _____ region | Active | Saturation | Cut-off | equlibrium | Active |
| Switching regulators are series type regulators, which has _____ power dissipation & _____ efficiency. | increased, increased | increased, reduced | reduced, increased | reduced, reduced | reduced, increased |
| Pulse stretching, time-delay, and pulse generation are all easily accomplished with which type of multivibrator circuit? | astable | monostable | bistable | multistable | monostable |
| Which of the following is not a form of multivibrator? | astable | monostable | bistable | tristable | tristable |
| The % load regulation of a power supply should be ideally _____ & practically _ | zero, small | small, zero | zero, large | large, zero | zero, small |
| | | | | | |
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| | | | | | |

## UNIT-III

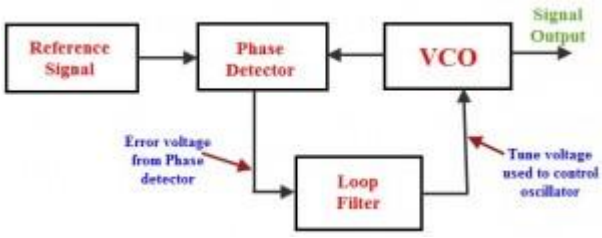
## SYLLABUS

Phase Locked Loop(PLL): Basic Principles, Phase detector(XOR & edge triggered), Voltage Controlled Oscillator (Basics, varactor). Loop Filter– Function, Loop Filter Circuits, transient response, lock and capture. Basic idea of PLL IC (565 or 4046).
**Processing of Devices:** Basic process flow for IC fabrication, Electronic grade silicon. Crystal plane and orientation. Defects in the lattice. Oxide layer. Oxidation Technique for Si. Metallization technique. Positive and Negative Masks. Optical lithography. Electron lithography. Feature size control and wet anisotropic etching. Lift off Technique. Diffusion and implantation.

### Phase locked loop

Phase-locked loop is used as a control system to control different operations in many communication systems, computers and many electronic applications. It is used to generate an output signal which has a phase related to input signal phase.

There are different types of PLLs such as Analog or Linear PLL, Digital PLL, Software PLL, Neuronal PLL and all digital PLL.




Basically PLL is a form of servo loop and a basic PLL consists of three major elements, namely phase comparator/detector, loop filter and voltage controlled oscillator.

- ***Phase comparator / detector:*** As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals.
  **Loop filter:** This filter is used to filter the output from the phase comparator in the PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line. It also governs many of the characteristics of the loop and its stability.

- ***Voltage controlled oscillator (VCO):*** The voltage controlled oscillator is the circuit block that generates the output radio frequency signal. Its frequency can be controlled and swung over the operational frequency band for the loop

The major concept behind the PPL operation is comparision of the phases of two signals (generally input and output signal phases are compared). Thus, the phase difference between the input and output signal can be used for controlling the loop frequency.

In many communication systems, PLL is used for different purposes:

- For following the phase or frequency modulation, it is used as Demodulator.
- To track or synchronize the two signals with different frequencies.
- To remove large noises from tiny signals.

The voltage-controlled oscillator of PLL produces a signal and this signal from the VCO is given to the phase detector. The phase detector compares this signal with the reference signal and thus, produces an error voltage or difference voltage. This error signal of the phase detector is fed to the low-pass filter for removing high-frequency elements of the signal -if any, and for governing many properties of the loop. Then, the output of the loop filter is fed to supply the tuning voltage for the control terminal of the voltage controlled oscillator.The change in this tuning voltage is sensed to reduce the phase difference between the two signals (input and output) and thus, the frequency between them. Initially the PLL does not lock and the error voltage drags the VCO frequency towards the reference until the error can not be reduced any further and then the loop gets locked.

The actual error between the two signals (input and output) is reduced to very small levels using an amplifier in between the voltage-controlled oscillator and a phase detector. If the PLL is locked, then a steady-state error voltage will be produced. This steady-state error voltage represents that there is no phase difference change between the reference signal and VCO. Thus, we can say that the frequency of the two signals (input and output signals) is exactly same

.

Phase locked loop basics

A phase locked loop, PLL, is basically of form of servo loop. Although a PLL performs its actions on a radio frequency signal, all the basic criteria for loop stability and other parameters are the same. When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.The fact that a steady error voltage is present means that the phase difference between

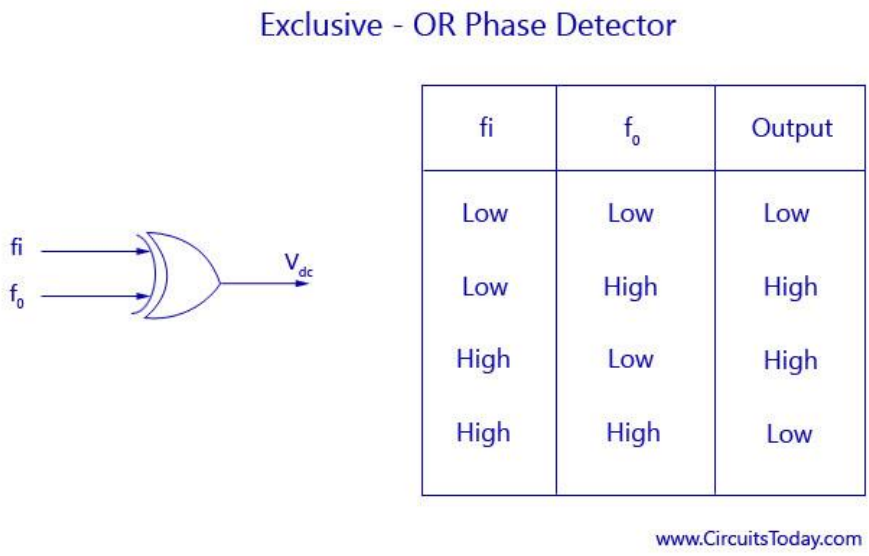
the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

**Phase Detector**

This comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies. The phase detector used in PLL may be of analog or digital type. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors are of the digital type. One of the most commonly used analog phase detector is the double balanced mixer circuit. Some of the common digital type phase detectors are

**Exclusive OR Phase Detector**

An exclusive OR phase detector is shown in the figure below.

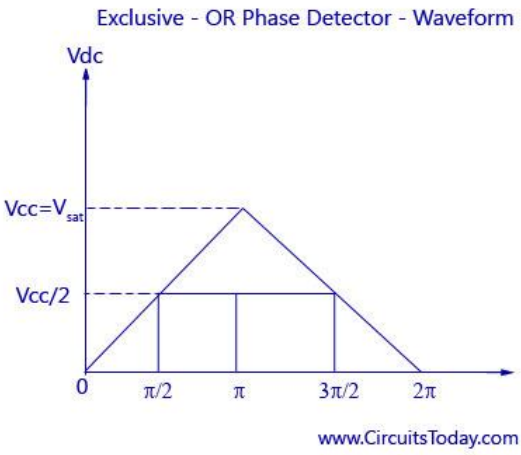



| fi | $f_0$ | Output |
|---|---|---|
| Low | Low | Low |
| Low | High | High |
| High | Low | High |
| High | High | Low |

Exclusive-OR Phase Detector

It is obtained as a CMOS IC of type 4070. Both the frequencies are provided as an input to the EX OR phase detector. Obeying the EX-OR concept the output becomes HIGH only if either of the inputs fi or fo becomes HIGH. All other conditions will produce a LOW output. Let us consider a waveform where the input frequency leads the output frequency by θ degrees. That is, fi and fo has a phase difference of θ degrees. The dc output voltage of the comparator will be a function of the phase difference between its two inputs.

The figure shows the graph of DC output voltage as a function of the phase difference between fi and fo. The output DC voltage is maximum when the phase detector is 180°.This type of phase detector is used when both fi and fo are square waves.




Exclusive-OR Phase Detector-Waveform

**Edge Triggered Phase Detector**

Edge triggered phase detector is used when fi and fo are pulse waveforms with less than 50% duty cycles. The figure of such a phase detector using an R-S Flip Flop is shown below. Two NOR Gate (CD4001) are cross-coupled to form an R-S Flip Flop. The output of the phase detector changes it's logic state by triggering of the R-S Flip Flop. That is, the output of the phase detector changes its logic state on the positive edge of the input fi and fo. The advantage of such a detector can be understood from the graph below. It is clear that the DC output voltage is linear over 360°.

**Monolithic Phase Detectors**

The monolithic type phase detector uses a CMOS type 4044 IC ,Which is highly advantages as the harmonic sensitivity and duty cycle problems are neglected and the circuit will be respond only to the transition in the input signals. This is the most preferred phase detector in the critical applications as the phase error and the output error voltage are independent of variations in the amplitude and duty cycles of the input waveforms.

**Characteristics of Phase Locked Loop**

1. **Acquisition and Tracking**

For a PLL to know the phase of the input signal, first it has to be in the phase locked state. Also, the VCO center frequency $\omega_0$ is usually different from the frequency $\omega_i$ of the input signal. So at first, the VCO frequency has to be tuned to the input frequency by the feedback loop. This process is called frequency pull in. Now inorder to adjust the VCO phase with the input phase, the PLL has to go to the Phase Locked State.

2. **Pull in Range**

It is the frequency difference change between the input and VCO frequencies.

$$\omega_P = I\omega_i - \omega_0 I$$

3. **Lock in Range**

It is the frequency ranges were the PLL achieves the phase locked condition.

$$\omega_L = |\omega i - \omega 0|$$

4. **Hold in Range**

The hold-in range $?\omega_H = |\omega i - \omega 0|$ is determined by the lower and upper values of $\omega i$, for which the phase-locked condition is lost.

5. **LOOP GAIN**

It is the amount of phase change between output and the input signal for the required shift in the frequency of input signal.

Loop gain = KoKD

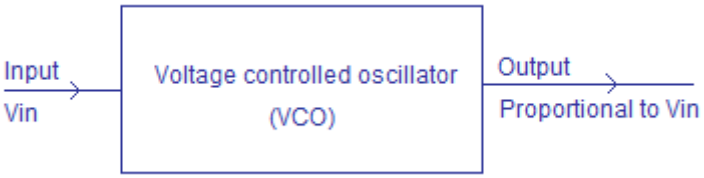
KD = phase detector sensitivity (V/radian), Ko = oscillator sensitivity (radians per sec/V).

6. **Free- Running Frequency**

The VCO frequency at which no any control signal applied is called as Free- Running Frequency.

## VCO (Voltage controlled oscillator).

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Voltage controlled oscillators are commonly used in frequency (FM), pulse (PM) modulators and phase locked loops (PLL). Another application of the voltage controlled oscillator is the variable frequency signal generator itself. Block diagram of a typical voltage controlled oscillator is shown below



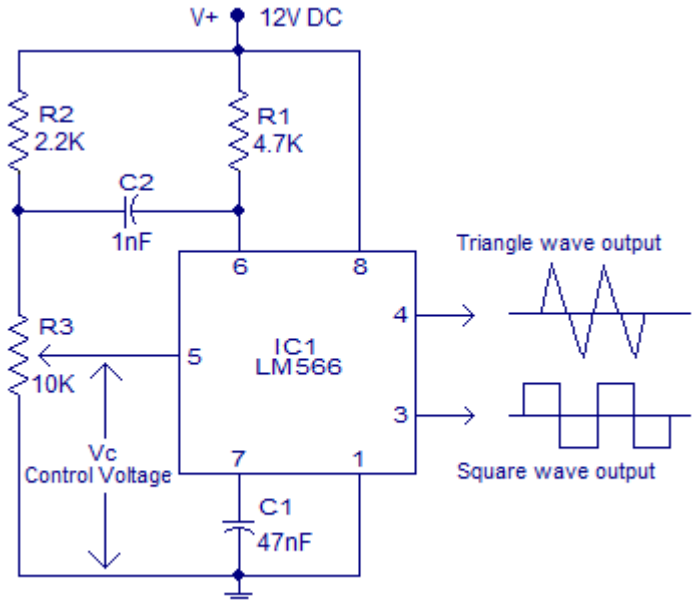
Voltage controlled oscillators can be broadly classified into linear voltage controlled oscillators and relaxation type voltage controlled oscillators. Linear voltage controlled oscillators are generally used to produce a sine wave. In such oscillators an LC tank circuit is used for producing oscillations. An active element like transistor is used for amplifying the output of the LC tank circuit, compensating the energy lost in the tank circuit and for establishing the necessary feedback conditions. Here a varactor (varicap) diode is used in place of the capacitor in the tank circuit.

Varactor diode is type of semiconductor diode whose capacitance across the junction can be varied by varying the voltage across the junction. Thus by varying the voltage across the varicap diode in the tank circuit, the output frequency of the VCO can be varied.

Relaxation type voltage controlled oscillators are used to produce a sawtooth or triangular waveform. This is achieved by the gradual charging and sudden discharge of a capacitor connected appropriately to an active element (UJT, PUT etc) or a monolitic IC (LM566 etc).Now a days relaxation type VCOs are generally realized using monolithic ICs.

**Voltage controlled oscillator using LM566 IC.**

LM566 is a monolithic voltage controlled oscillator from National semiconductors. It can be used to generates square and triangle waveforms simultaneously. The frequency of the output waveform can be adjusted using an external control voltage. The output frequency can be also programmed using a set of external resistor and capacitor. Typical applications of LM566 IC are signal generators, FM modulators, FSK modulators, tone generators etc. The LM566 IC can be operated from a single supply or dual supply. While using single supply, the supply voltage range is from 10V to 24V. The IC has a very linear modulation characteristics and has excellent thermal stability. The circuit diagram of a voltage controlled oscillator using LM566 is shown in the figure below.



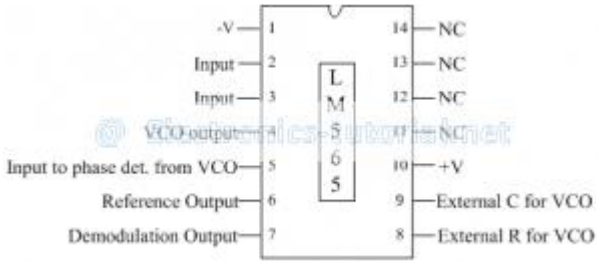

Resistor R1 and capacitor C1 forms the timing components. Capacitor C2 is used to prevent the parasitic oscillations during VCO switching. Resistor R3 is used to provide the control voltage Vc. Triangle and square wave outputs are obtained from pins 4 and 3 respectively. Output frequency of the VCO can be obtained using the following equation:

Fout = $2.4(V^+-V5)/(R1C1V^+)$ . Where Fout is the output frequency, R1 and C1 are the timing components and $V^+$ is the supply voltage.

**PLL IC 565**

The PLL IC 565 is usable over the frequency range 0.1 Hz to 500 kHz. It has highly stable centre frequency and is able to achieve a very linear FM detection. The output of VCO is capable of producing TTL compatible square wave. The dual supply is in the range of ±6V to ±12V. The IC can also be operated from single supply in the range 12V to 24V.

The following figure shows the pin-out and the internal block schematic of PLL IC LM 565.



It is a 14 pin IC, operated from a dual power supply +V (at pin no. 10) and –V (at pin no. 1).

Pin no 2 & 3 -> Signal input for phase detector.

Pin no 4 ->VCO output is available

Pin no 4 & 5 are shorted externally so that VCO output is applied for phase detection. In some applications PLL loop is broken and some circuit is to be connected between pin no 4 and 5.

Pin no 6-> reference dc voltage is available.

Pin no 7 -> demodulated output.If input signal between pin no 2 and 3 is FM signal then at pin no 7 we get FM demodulation output.

Pin no 8 and 9 -> external R1 and C1 for VCO (determines free running frequency of VCO)

Internal resistance R2 and external capacitor C2 forms a LPF. The value of internal resistance R2 is 3.6kΩ.

**Features of IC 565:**

1) Extreme stability of center frequency typically 200ppm.

2) Wide range of operating voltage ±6V to ±12V.

3) Very high linearity of demodulated output typically 0.2%

4) Centre frequency of VCO is programmable by means of resistor, capacitor or voltage.

5) TTL compatible square wave output.

6) Highly linear triangular wave output available at pin no.9

7) Loop can be broken between pin no.4 and 5 and external circuit can be added.

8) Frequency adjustable over the range 1:10 with single capacitor.

## IC Fabrication Process Steps

The fabrication of integrated circuits consists basically of the following process steps:

- **Lithography:** The process for pattern definition by applying thin uniform layer of viscous liquid (photo-resist) on the wafer surface. The photo-resist is hardened by baking and than selectively removed by projection of light through a reticle containing mask information.
- **Etching:** Selectively removing unwanted material from the surface of the wafer. The pattern of the photo-resist is transferred to the wafer by means of etching agents.
- **Deposition:** Films of the various materials are applied on the wafer. For this purpose mostly two kind of processes are used, physical vapor deposition (PVD) and chemical vapor deposition (CVD).
- **Chemical Mechanical Polishing:** A planarization technique by applying a chemical slurry with etchant agents to the wafer surface.

- **Oxidation:** In the oxidation process oxygen (dry oxidation) or $H_2O$ (wet oxidation) molecules convert silicon layers on top of the wafer to silicon dioxide.
- **Ion Implantation:** Most widely used technique to introduce dopant impurities into semiconductor. The ionized particles are accelerated through an electrical field and targeted at the semiconductor wafer.
- **Diffusion:** A diffusion step following ion implantation is used to anneal bombardment-induced lattice defects.

## Defects in the Crystal Structure of Materials

A crystal has a perfect order in the structural arrangement. The atoms or constituent particles in a crystalline solid occupies fixed lattice points. Such crystals are called ideal crystals. In most of the crystals, some deviations from complete order are seen. These deviations lead to defects in solid. The defect or disorder can also be due to the presence of impurity in the crystal lattice. Thus,

Any departure from perfectly ordered arrangement of atoms in crystal is called imperfection or defect.

We know that ordered arrangement of a solid imparts some unique properties to the solids. Imperfections modify existing properties of a solid and also impart some new properties to the solids. The imperfections can be of two types:

i. Electronic imperfections
ii. Atomic imperfections or point defects

**Electronic imperfections**

In a pure crystal (ionic or covalent) at 0 K, the electrons are present in the lowest energy state. But at higher temperatures (above 0 K), some of the electrons may occupy the higher energy states. For example, in pure silicon, above 0 K, some of the bonded electrons are thermally excited to higher energy level and at their place holes are created. The holes and electrons can freely more within a crystal giving rise to electrical conductivity. The direction of movement of holes is opposite to that of the electrons. These holes and free electrons give rise to electronic imperfection in the solids.

**Atomic imperfections**

As the name suggests, atomic imperfections in a solid are due to anomalous arrangement of atoms in the crystal lattice. The points in the crystal lattice where constituent particles are arranged are called lattice points. Thus, in

atomic imperfections, some of the constituent particles are not present at their lattice points. Atomic imperfections are thus also called point defects. Thus,

When deviations exist from the regular arrangement around an atom or a group of atoms in a crystalline substance, the defects are called atomic or point defects.

he point defects arise due to one of the following reasons:

i. Some constituent particles are missing from their normal positions. The unoccupied positions are called vacancies and the resulting defect is called vacancy defect.
ii. Some of the constituent particles are missing form their positions and shift to some interstitial site and the resulting defect is called interstitial defect.

Vacancy and interstitial defects occur in non-ionic solids, i.e. atomic, molecular and metallic solids.

**Defects in ionic solids**

Simple vacancy and interstitial defects are not possible in ionic solids as electrical neutrality will get disturbed. In ionic solids, such defects occur with some modifications so that electrical neutrality is not disturbed.
Point defects in ionic crystals may be classified into the following three types.

i. Stoichiometric defects
ii. Non-stoichiometric defects
iii. Impurity defects

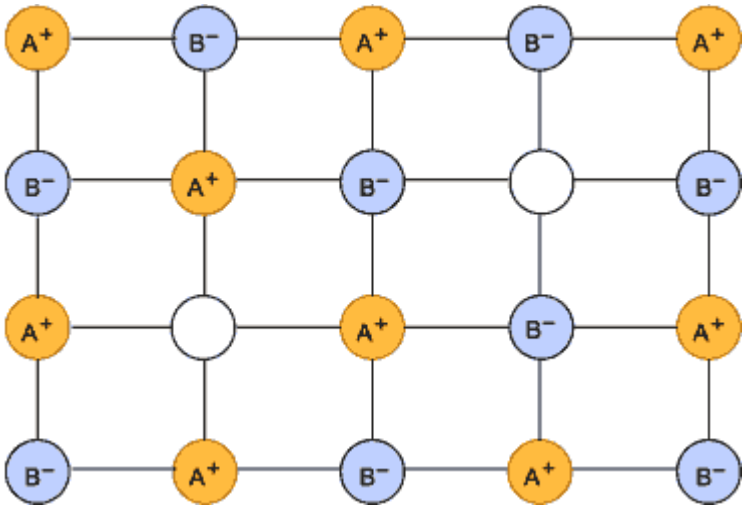
**Stoichiometric defects**

An ionic crystal has a fixed ratio of anion and cation, which can be seen from its formula. This fixed ratio is calledstoichiometry of that compound. If a defect in the crystal is such that the ratio between the cation and anion remains same as represented by its formula, the defect is called stoichiometric defect. Stoichiometric defects are further divided into two types:

i. Schottky defect
ii. Frenkel defect

**Schottky defect**

This defect was discovered by German scientist Schottky in 1930. In an ionic crystal of the type $A^+B^-$, if equal number ofcations and anions are missing from their lattice points so that the electrical neutrality of the crystal is maintained, the defect caused is called Schottky defect. In Schottky defect, vacancies are created due to absence of cation or anion. This defect is represented in the figure given below.



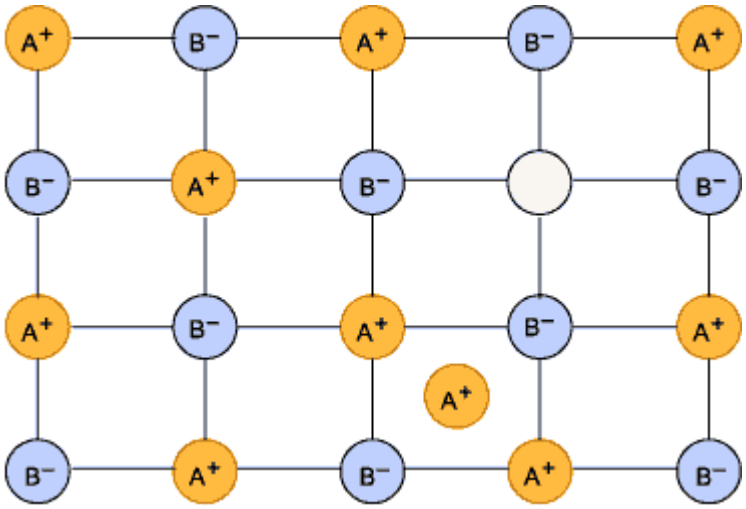

Schottky defects are usually observed in strongly ionic compounds having,

i. high coordination number
ii. ions (cations and anions) of almost similar sizes

NaCl, KCl, CsCl show Schottky defects. Since all of them have comparable ionic sizes or high coordination number. Since ions are lost in this type of defect, there is a loss of mass but the volume remains same. Hence, the density of the solid having Schottky defect decreases.

**Frenkel defect**

This defect was discovered by Russian scientist Frenkel in 1926. When a defect is caused by missing of an ion from its lattice points and occupying an interstitial site, the electrical neutrality as well as the stoichiometry of the compound are maintained. This defect is a combination of vacancy defect and interstitial defect. This type of defect is called Frenkeldefect. This defect is represented in the figure given below.




This defect generally occurs in compounds in which,

i. coordination number is low
ii. anions are much larger in size than cations

Since cations are usually smaller in size, it is more common to find the cations occupying interstitial sites. This defect is found in AgCl, AgBr, ZnS, etc. Since no ions are missing from the lattice (crystal) as a whole, there is no change in the density of the solid.

**Non-stoichiometric defects**

Non-stoichiometric defects are the defects due to which the ratio of the cations to the anions becomes different from that indicated by the ideal chemical formula. For example, vanadium oxide has the formula $VO_x$ where x lies between 0.6 and 1. Similarly, FeO has an excess of oxide ions and actual formula is $Fe_{0.95}O$ and the structure is called Wustite. It may be noted that in case of non-stoichiometric defects also the electrical neutrality of the crystal is maintained.

Non-stoichiometric defects are of two types depending upon whether positive ions are in excess or negative ions are in excess. These defects are also called metal excess defect and metal deficiency defect, respectively.

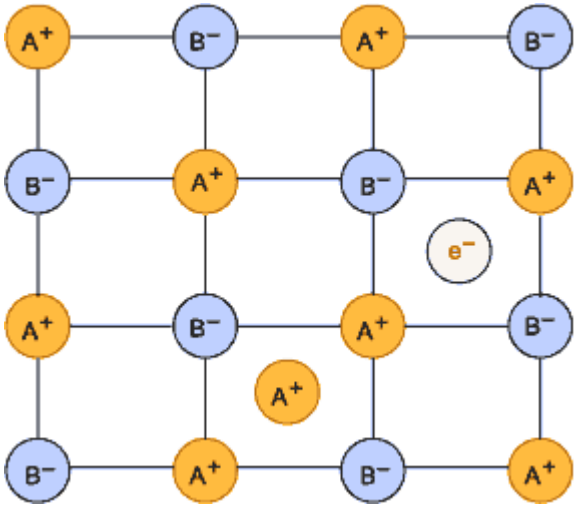
a. **Metal excess defects**

In metal excess defects, the positive ions are in excess. This may occur in two ways:

o **By anion vacancies**

An anion (or negative ion) is missing from the lattice point in this case. The vacant site thus produced is occupied by an electron ($e^-$) to maintain the electrical neutrality. This

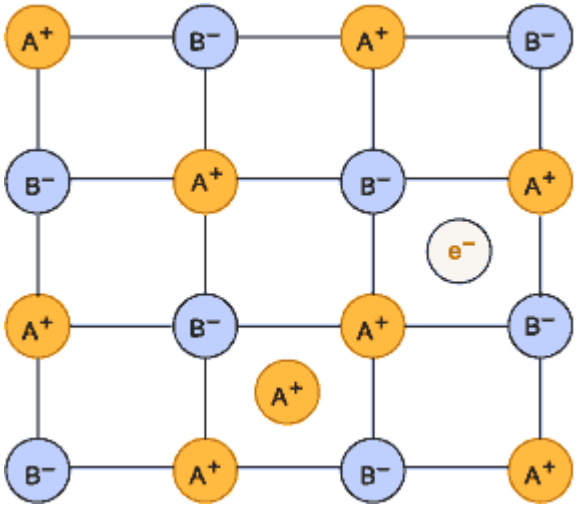
defect is represented in the figure given below.




The vacancies where these electrons are trapped are called F-centres. The letter 'F' means Farbe, which in German means colour. Thus, it is evident that these F-centres should be responsible for colour of the crystal, which is true. For example, metal excess causes NaCl to appear yellow. Let us see how this happens. When NaCl is heated in an atmosphere of Na vapour, the excess of Na atoms deposit on the surface of the NaCl crystal. $Cl^-$ ions then diffuse to the surface to combine with Na atoms to form NaCl again. For this recombination to happen Na atom should ionize to $Na^+$. The electron released during the ionization diffuses back into the crystal to occupy the vacant sites created by migration of $Cl^-$ ions. This electron absorbs white light and thus NaCl appears yellow in colour. Similarly, LiCl appears pink due to excess of $Li^+$ and KCl appears violet due to excess of $K^+$. This defect is similar to Schottkydefect as here also density of the crystal decreases. Thus, crystals having Schottky defect may also show this kind of defect.

**By the presence of extra cations in the interstitial sites**

Metal excess can also be obtained by having extra cations in the interstitial sites. The increased positive charge is balanced by the presence of extra electrons in some other interstitial site. This defect is represented in the figure given below.




This defect is similar to Frenkel defect in the sense that ions are present in the interstitial site and thus, such defects are found in crystals having Frenkel defect.

Example includes ZnO, when ZnO is heated, it loses oxygen and turns yellow due to following reactions.

$$O \longrightarrow Zn^{2+} + \frac{1}{2}O_2 + 2e^-$$

o

The excess of $Zn^{2+}$ ions thus formed are trapped in the crystal structure in the interstitial sites and the electrons produced also diffuse into the crystal to occupy interstitial sites.

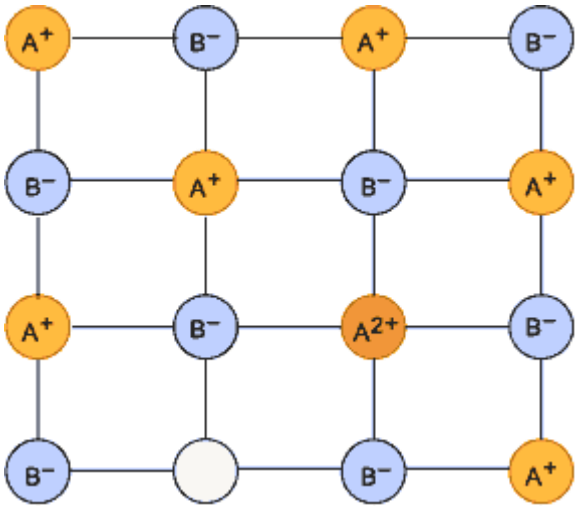
Crystals with either type of metal excess have free electrons and thus, act as semi-conductors.

b. **Metal deficient defects**

Metal deficient defects occur due to the presence of less number of positive ions than negative ions. These defects can also arise in two ways.

**By cation vacancies**

In some crystals, the positive ions (cations) may be missing from their original lattice points. The vacancy thus created will cause the crystal to carry a negative charge. This extra negative charge can be balanced by the presence of the cation having higher charge in some neighbouring sites.This defect is represented in the figure given below.

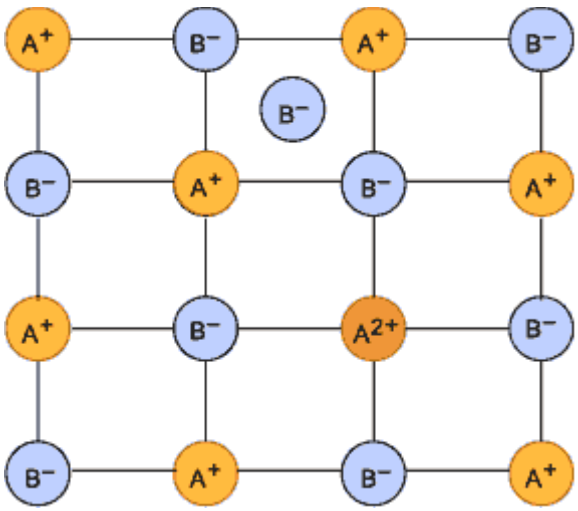



o

Since, the same metal ion should have higher charge, these defects are possible in metals, which show variable oxidation sates, i.e. transition elements. Common examples of compounds showing this kind of defect are FeO, FeS and NiO. In case of iron pyrites (FeS), two out of three $Fe^{2+}$ ions in the lattice may be converted into $Fe^{3+}$ state and the third $Fe^{2+}$ may be missing from its lattice site. Thus, the crystal remains electrically neutral and contain both $Fe^{2+}$ and $Fe^{3+}$ ions. Interconversion of $Fe^{2+}$ and $Fe^{3+}$ ions is possible in such situation by exchange of electrons. As a result, the crystal has metalliclusture.

o **By the presence of extra anions in the interstitial sites**

In such a case, an extra anion may occupy the interstitial site. The extra negative charge of crystal is then balanced by the conversion of the metal ions present at lattice points to higher oxidation states. This defect is represented in the figure given below.




o

Such kind of defects is very rare because usually negative ions are of larger size and thus,

cannot easily fit into the interstitial sites.

Metal deficient defects cause movement of electrons by interconversion of cations between two oxidation states and thus, the crystals having such defects can act as semi-conductors.

**Impurity defects**

Defects or imperfections that arise due to the presence of a foreign atom at a lattice point (instead of the host atom) or at vacant interstitial site are called impurity defects.

A substitutional solid solution is obtained when the impurity is present at the lattice point whereas an interstitial solid solution is obtained when the impurity occupies an interstitial site. The formation of the former depends upon the electronic structure of the impurity while that of the latter on the size of the impurity.

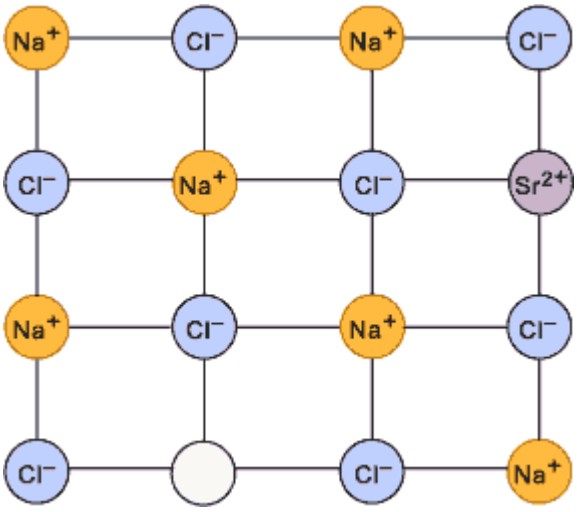
- **Introducing impurity defect in covalent solids**

Substitutional solid solutions of group 14 elements like Ge or Si are obtained when impurities of group 13 (such as Ga and Al) or group 15 (such as P and As) are added. The group 15 elements have one excess valence electron, compared to group 14 elements after forming four covalent bonds with group 14 elements. The excess electrons give rise to electronic conduction. On the other hand, a group 13 elements have one electron less than that of group 14 elements. Thus, a group 13 element, when present as an impurity, forms only three covalent bonds and an electron deficient bond which has a hole. Such holes impart electrical conductivity to the crystal.

This process of introducing defects by incorporating small amount of foreign impurity in the host crystal is called **doping.** Thus, as seen above, doping increases the electrical conductivity of the material. Thus, impurity-doped Si and Ge act as semiconductors.

- **Introducing impurity defect in ionic solids**

In ionic solids, the impurities are introduced by adding impurity of ions. If the impurity ions are in different oxidation state from that of host ions, vacancies are created. For example, addition of $SrCl_2$ as impurity to NaCl, yields a substitutional solid solution in which $Sr^{2+}$ ion occupies some of the lattice points of $Na^+$ ions. For the introduction of every $Sr^{2+}$ ion, there is removal of two $Na^+$ ions to maintain the electrical neutrality and as a result, one of these lattice points is occupied by $Sr^{2+}$ ion and at other vacancy is created.




These vacancies result in higher electrical conductivity of the solid.

Another example is addition of $CdCl_2$ as impurity to AgCl. Here, $Cd^{2+}$ ion occupies some of the lattice points of $Ag^+$ ions.

**Growth and Properties of Oxide Layers on Silicon**

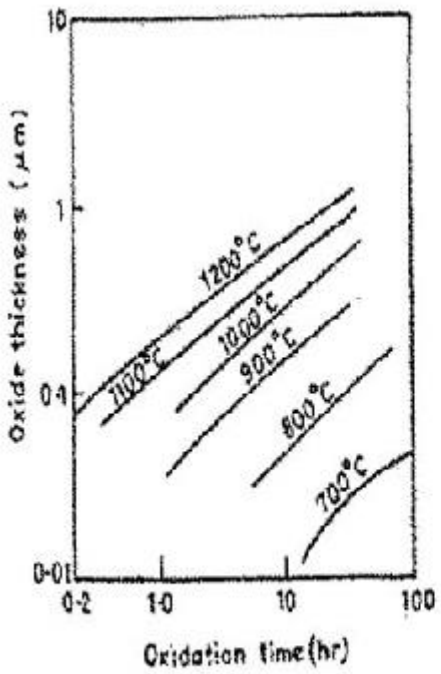
Silicon dioxide (silica) layer is formed on the surface of a silicon wafer by thermal oxidation at high temperatures in a stream of oxygen.

$$\mathbf{Si+02 = SiO_2\ (solid)}$$

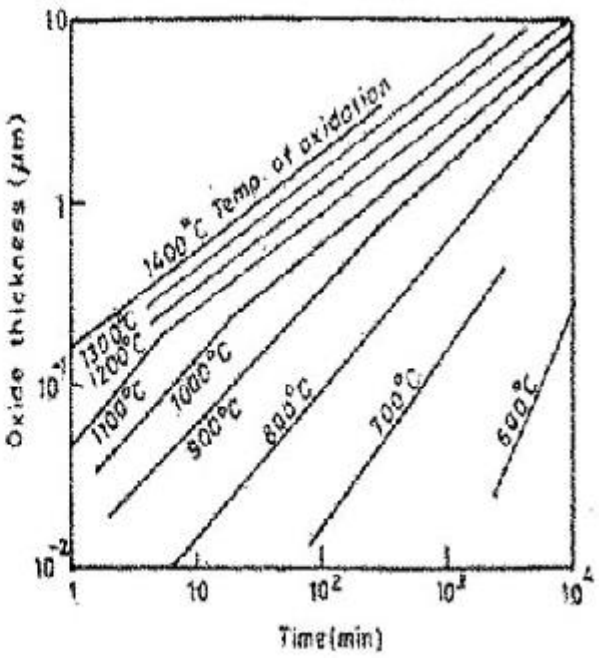
The oxidation furnace used for this reaction is similar to the diffusion furnace. The thickness of the oxide layer depends on the temperature of the furnace, the length of time that the wafers are in it, and the flow rate of oxygen. The rate of oxidation can be significantly increased by adding water vapour to the oxygen supply to the oxidizing furnace.

$$\mathbf{Si + 2H_2O = SiO_2 + 2H_2}$$

The time and temperature required to produce a particular layer thickness arc obtained from empirically determined design curves, of the type shown in the figures given below corresponding to dry- oxygen atmosphere and also corresponding to steam atmosphere.




Growth rate of $SiO_2$ in a dry oxygen atmosphere.




Growth rate of $SiO_2$ in a steam atmosphere which is much greater than in dry oxygen.

In the past, steam was obtained by boiling ultra-high-purity water and passing it into the high-temperature furnace containing the silicon wafers; however, present day technologies generally use hydrogen and oxygen which are ignited in the furnace tube to form the ultra high-purify water vapour.

The process of silicon oxidation takes place many times during the fabrication of an IC. Once silicon has been oxidized the further growth of oxide is controlled by the thickness of the initial or existing oxide layer.

**Growth Rate of Silicon Oxide Layer**

The initial growth of the oxide is limited by the rate at which the chemical reaction takes place. After the first 100 to 300 A of oxide has been produced, the growth rate of the oxide layer will be limited principally by the rate of diffusion of the oxidant ($0_2$ or $H_20$) through the oxide layer, as shown in the figures given below.

The rate of diffusion of $O_2$ or $H_2O$ through the oxide layer will be inversely proportional to the thickness of the layer, so that we will have that

$$dx/dt = C/x$$

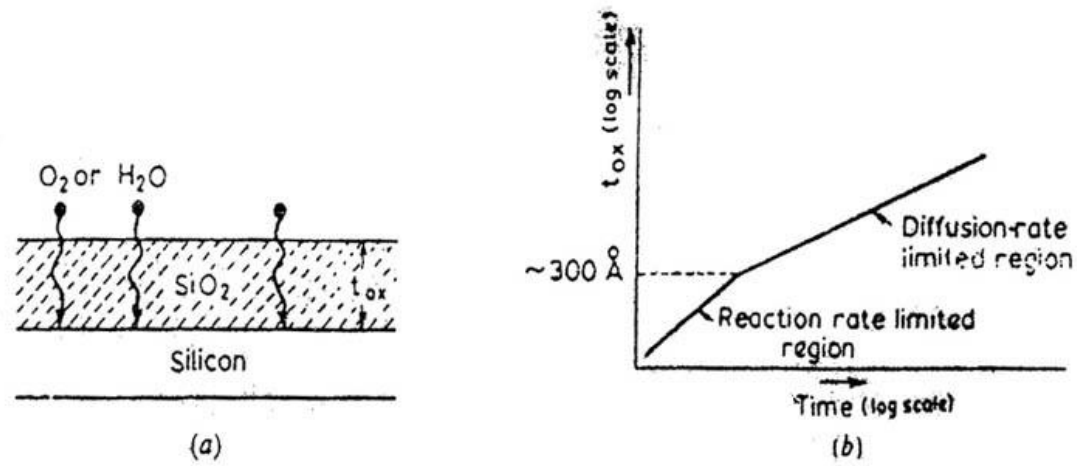
where x is the oxide thickness and C is a constant of proportionality. Rearranging this equation gives

$$xdx = Cdt$$

Integrating this equation both sides yields, $x^2/2 = Ct$

Solving for the oxide thickness x gives, $x = \sqrt{2Ct}$

We see that after an initial reaction-rate limited linear growth phase the oxide growth will become diffusion-rate limited with the oxide thickness increasing as the square root of the growth time. This is also shown in the figure below.




(*a*) Oxidation of silicon
(*b*) Oxide-thickness ($t_{ox}$) versus time for thermal oxidation of silicon.
The rate of diffusion of $O_2$ or $H_2O$ through the oxide layer will be inversely proportional to the thickness

The rate of oxide growth using $H_2O$ as the oxidant will be about four times faster than the rate obtained with $O_2$. This is due to the fact that the $H_2O$ molecule is about one-half the size of the $O_2$ molecule, so that the rate of diffusion of $H_2O$ through the $SiO_2$layer will be much greater than the $O_2$ diffusion rate

**Electronic grade silicon**

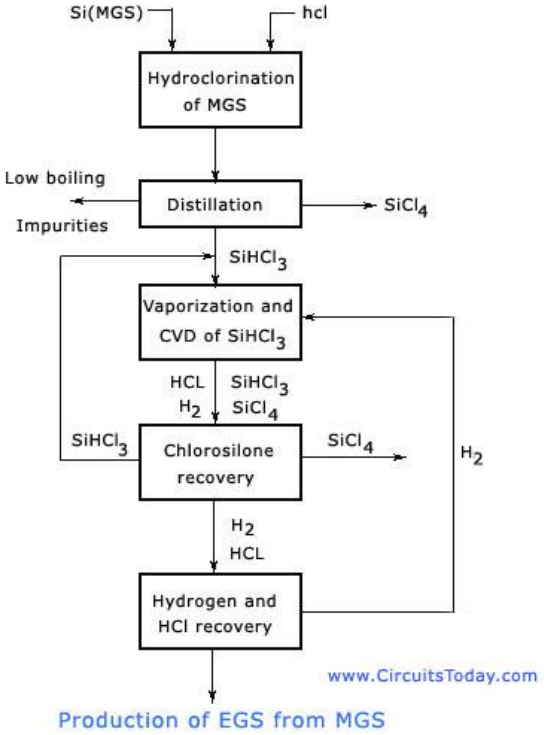
1. EGS is the raw material for the preparation of single crystal silicon.
2. It is a polycrystalline material of high purity and requires doping elements to be in parts per billion range.
3. Major impurities - boron,phosphorous,carbon.
4. 1st step is metallurgical grade silicon (MGS) production in submerged electrode arc furnace.The furnace is charged with quartzite and carbon.
5. Reactions taking place in furnace are :

- SiC (solid) + SiO2 (solid) -> Si (liquid) + SiO (gas) +CO (gas)
- Si (solid) + 3HCl (gas) -> SiHCl3 (gas) + H2 (gas) + heat
- 2H2 (gas) + 2SiHCl3 (gas) -> 2Si (solid) + 6HCl (gas)
- SiH4 (gas) + heat -> Si (solid) + 2H2 (gas)

**Production of Electronic Grade Silicon (EGS)**

Electronic-Grade Silicon (EGS) is the raw material that is used for the preparation of single-crystal silicon. EGS is actually a polycrystalline material of high purity. EGS has some major impurities like boron, carbon, and residual donors. The pure EGS will have doping elements in the parts per billion (ppb) range, and carbon less than 2 parts per million pppm .

The step by step procedure regarding the production of EGS is shown in the block diagram below.




Production of EGS

The process starts by the production of Metallurgical Grade Silicon (MGS) by charging it with quartzite and carbon in an arc furnace. Quartzite is a relatively pure form of sand (SiQ2), and carbon is obtained in the form of coal, coke, and wood chips.

The overall reaction in the furnace is given below.

**SiC+Si02 = Si + SiO + CO**

The MGS after being drawn off, has to be solidified at a purity of 98%. But this purity is not enough for the manufacture of semiconductor devices. So, the MGS has to be pulverized mechanically and reacted with anhydrous hydrogen chloride (HCI) to form trichlorosilane (SiHCI3). The reaction is shown below.

**Si + 3HCl = SiHCI3 + H2**

With the help of a catalyst, the reaction takes place at a nominal temperature of 300°C. The reaction creates products like silicon tetrachloride (SiCl4) and the chlorides of impurities. At this point the purification process occurs. The purification process has to be done by fractional distillation method as the products trichlorosilane and unwanted chlorides are liquids at room temperature. The purified SiHCI3 is subjected to chemical vapor deposition (CVD**).** The chemical reaction is a hydrogen reduction of SiHCl3.

The chemical reaction is shown below.

**2SiHCl3 + 2H2 = 2Si + 6HCl**

The reaction takes place in a CVD reactor. A resistance heated Si-rod (4-mm diameter), called a slim-rod, is used as the nucleation point for the deposition of silicon. Through the process rods of EGC are obtained. which are up to 0.2 meters (or more) in diameter and several meters in length. EGS can be cut from these rods as single chunks or crushed into nuggets.

In order to achieve high overall efficiency, a feedback or recycling of reaction of by-products is done. This is also shown in the figure above.

EGS can also be produced by pyrolysis method in which silane (SiH4) will be reacted with heat. The reaction takes place at a high temperature of 900°C. The main advantage of using silane instead of trichlorosilane is the lower production cost and less production of harmful reaction by-products.

**SiH4 + HEAT = Si + 2H2**

In this process the CVD reactor is operated at about 900°C and supplied with silane instead of trichlorosilane. The advantages of producing EGS from silane are lower cost and less harmful reaction by-products.

**Metallization**

Metallization is the final step in the wafer processing sequence. Metallization is the process by which the components of IC's are interconnected by aluminium conductor. This process produces a thin-film metal layer that will serve as the required conductor pattern for the interconnection of the various components on the chip. Another

use of metallization is to produce metalized areas called bonding pads around the periphery of the chip to produce metalized areas for the bonding of wire leads from the package to the chip. The bonding wires are typically 25 micro meters diameter gold wires, and the bonding pads are usually made to be around 100×100 micro meters square to accommodate fully the flattened ends of the bonding wires and to allow for some registration errors in the placement of the wires on the pads.

Aluminium (At) is the most commonly used material for the metallization of most IC's, discrete diodes, and transistors. The film thickness is as about 1 micro meters and conductor widths of about 2 to 25 micro meters are commonly used. The use of aluminium offers the following advantages:

- It has as relatively good conductivity.
- It is easy to deposit thin films of Al by vacuum evaporation.
- It has good adherence to the silicon dioxide surface.
- Aluminium forms good mechanical bonds with silicon by sintering at about 500°C or by alloying at the eutectic temperature of 577°C.
- Aluminium forms low-resistance, non-rectifying (that is, ohmic) contacts with p-type silicon and with heavily doped n-type silicon.
- It can be applied and patterned with a single deposition and etching process.

**Aluminium has certain limitations:**

During packaging operation if temperature goes too high, say 600°C, or if there is overheating due to current surge, Al can fuse and can penetrate through the oxide to the silicon and may cause short circuit in the connection. By providing, adequate process control and testing, such failures can be minimized.

The silicon chip is usually mounted in the package by a gold perform or die backing that alloys with the silicon. Gold lead wires have been bonded to the aluminium film bonding pads on the chip, since package lead are usually gold plated. At elevated temperatures, a reaction between the metal of such systems causes formation of intermetallic compounds, known as the purple plague. Purple plague is one of six phases that can occur when gold and aluminium inter-diffuse. Because of dissimilar rate of diffusion of gold and aluminium, voids normally occur in the form of the purple plague. These voids may result in weakened bonds, resistive bonds or catastrophic failure. The problem is generally solved by using aluminium lead wires, or another metal system, in circuits that will be subjected so elevated temperatures. One method is to deposit gold over an under layer of chromium. The chromium acts as a diffusion barrier to the gold and also adheres well to both oxide and gold. Gold has poor adhesion to oxide because it does not oxide itself. However, the chromium-gold process is comparatively expensive, and it has an uncontrollable reaction with silicon during alloying.

Aluminium suffers from electromigration which can cause considerable material transport in metals. It occurs because of the enhanced and directional mobility of atoms caused by the direct influence of the electric field and the collision of electrons with atoms, which leads to momentum transfer. In thin-film conductors that carry sufficient current density during device operations, the mode of material transport can occur at much lower temperature (compared to bulk metals) because of the presence of grain boundaries, dislocations and point defects that aid the material transport. Eecctromigration-induced failure is the most important mode of failure in Al lines.

In general the desired properties of the metallization for IC can be listed as follows.

- Low resistivity.
- Easy to form.
- Easy to etch for pattern generation.
- Should be stable in oxidizing ambient , oxidizable.
- Mechanical stability; good adherence, low stress.
- Surface smoothness.
- Stability throughout processing including high temperature sinter, dry or wet oxidation, gettering, phosphorous glass (or any other material) passivation, metallization.
- No reaction with final metal, aluminium.
- Should not contaminate device, wafers, or working apparatus.
- Good device characteristics and life times.
- For window contacts-low contact resistance, minimum junction penetration, low electromigration.

**Metallization Processes**

Metallisation process can be classified info two types:

1. CVD and
2. Physical Vapour Deposition

Both these methods have three identical steps.

- Converting the condensed phase (generally a solid) into a gaseous or vapour phase.
- Transporting the gaseous phase from the source to the substrate, and
- Condensing the gaseous source on the substrate.

In both methods the substrate is away from the source.

**Lift-off Process**

The lift-off process is an alternative metallization patterning technique. In this process a positive photoresist is spun on the wafer and patterned using the standard photolithographic process. Then the metallization thin film is deposited on top of the remaining photoresist. The wafers are then immersed in suitable solvent such as acetone and at the same time subjected to ultrasonic agitation. This causes swelling and dissolution of the photoresist. As the photoresist comes off it lifts off the metallization on top of it, for the lift-off process to work, the metallization film thickness must generally be somewhat less than the photoresist thickness. This process can, however produce a very fine line-width metallization pattern, even with metallization thickness that are greater than the line width.

**Lithography**

Lithography (or patterning) refers to the series of steps that establish the shapes, dimensions, and location of the various components of the integrated circuit (IC).

When a sample of crystalline silicon is covered with silicon dioxide, the oxide-layer acts as a barrier to the diffusion of impurities, so that impurities separated from the surface of the silicon by a layer of oxide do not diffuse into the silicon during high-temperature processing. A p-n junction can thus be formed in a selected location on the sample by first covering the sample with a layer of oxide [oxidation step] removing the oxide in the selected region, and then performing a predeposition and diffusion step. The selective removal of the oxide in the desired area is performed with photolithography. Thus, the areas over which diffusions are effective are defined by the oxide layer with windows cut in it, through which diffusion can take place. The windows are produced by the photolithographic process. This process is the means by which microscopically small electronic circuits and devices can be produced on silicon wafers resulting in as many as 10000 transistors on a 1 cm x 1 cm chip.

In fact photolithography or optical lithography is a kind of lithography. The lithography technique was first used in the late $18^{th}$ century by people interested in art. A lithograph is a less expensive picture

made from a flat, specially prepared stone or metal plate and the lithography is art of making lithographs. Therefore, lithography for IC manufacturing is analogous to the lithography of the art world. In this process the exposing radiation, such as ultraviolet (UV) light in case of photolithography, is transmitted through the clear parts of the mask. The circuit pattern of opaque chromium blocks some of die radiation. This type of chromium/glass mask is used with UV light. Other types of exposing radiations are electrons, X-rays, or ions. Thus for IC manufacturing we have following types of lithography. Photolithography has been explained in this post. To know about the other types of lithographic process, click on the link below.

1. **Photolithography**
2. **Electron-beam Lithography**
3. **X-ray lithography**
4. **Ion-beam lithography**

In IC fabrication a number of masks are employed. Except for the first mask, every mask must be aligned to the pattern produced by the previous mask. This is done using mask aligner. The mask aligner may be contact type or proximity type or projection type. Accordingly we have three types of printing. They are

- Contact printing
- Proximity printing
- Projection printing

**Photolithographic (Optical Lithography) Process Steps**

**1. Photoresist Application (Spinning)**

A drop of light-sensitive liquid called photoresist is applied to the centre of the oxidized silicon wafer that is held down by a vacuum chuck. The wafer is then accelerated rapidly to a rotational velocity in the range 3000 to 7000 RPM for some 30 to 60 seconds. This action spreads the solution in a thin, nearly uniform coat and spins off the excess liquid. The thickness of the coat so obtained is in the range 5000 to 10000 A, as shown in the figure below. The thickness of the photoresist layer will be approximately inversely proportional to the square root of the rotational velocity.

Sometimes prior to the application of the photoresist the silicon wafers are given a “bake-out” at a temperature Of at least 100°C to drive off moisture from the wafer surfaces so as to obtain better adhesion of the photoresist. Typical photoresist used is Kodak Thin Film Resist (KTFR).

**2. Prebake**

The silicon wafers coated with photoresist are now put into an oven at about 80°C for about 30 to 60 minutes to drive off solvents in the photoresist and to harden it into a semisolid film.

**3. Alignment and Exposure**

The coated wafer, as above, is now placed in an apparatus called a mask aligner in very close proximity (about 25 to 125 micro meters) to a photomask. The relative positions of the wafer and the photomasks are adjusted such that the photomask is correctly lined up with reference marks or a pre-existing pattern on the wafer.

The photomask is a glass plate, typically about 125 mm square and about 2 mm thick. The photomask has a photographic emulsion or thin film metal (generally chromium) pattern on one side. The pattern has clear and opaque areas. The alignment of the photomask to the wafer is often required to be accurate to within less than 1 micro meter, and in some cases to within 0.5 micro meters. After proper alignment has been achieved, the wafer is brought into direct contact with the photomask. Photomask making will be described separately.

A highly collimated ultraviolet (UV) light is then turned on and the areas of the silicon wafer that are not covered by the opaque areas of the photomask are exposed to ultraviolet radiation, as shown in the figure. The exposure time is generally in the range 3 to 10 seconds and is carefully controlled such that the total UV radiation dosage in watt-seconds or joules is of the required amount.

**4. Development**

Two types of photoresist exist- negative photoresist and positive photoresist. In the present description negative photoresist is used in which the areas of the photoresist that are exposed the ultraviolet radiation become polymerized. The polymerization process increases the length of the organic chain molecules that make up the photoresist. This makes the resist tougher and makes it essentially insoluble in the developer solution. The resisting photoresist pattern after the development process will therefore be a replication of the photomask pattern, with the clear areas on the photomask corresponding to the areas where the photoresist remains on the wafers, as shown in the figure below.

An opposite type of process occurs with positive photoresist. Exposure to UV radiation results in depolymerization of the photoresist. This makes these exposed areas of the photoresist readily soluble in the

developer solution, whereas the unexposed areas are essentially insoluble. The developer solution will thus remove the exposed or depolymerized regions of the photoresist, whereas the unexposed areas will remain on the wafer. Thus again there is a replication of the photomask pattern, but this time the clear areas of the photomask produce the areas on the wafer from which the photoresist has been removed.

**5. Postbake**

After development and rinsing the wafers are usually given a postbake in an oven at a temperature of about 150°C for about 30 to 60 minutes to toughen further the remaining resist on the wafer. This is to make it adhere better to the wafer and to make it more resistant to the hydrofluoric acid [HF] solution used for etching of the silicon dioxide.

**6. Oxide Etching**

The remaining resist is hardened and acts as a convenient mask through which the oxide layer can be etched away to expose areas of semiconductor underneath. These exposed areas are ready for impurity diffusion.

For etching of oxide, the wafers are immersed in or sprayed with a hydrofluoric [HF] acid solution. This solution is usually a diluted solution of typically 10: 1, $H_2O$ : HF, or more often a 10 : 1 NH4F [ammonium fluoride]: HF solution. The HF solutions will etch the $SiO_2$ but will not attack the underlying silicon, nor will it attack the photoresist layer to any appreciable extent. The wafers are exposed to the etching solution ion enough to remove the $SiO_2$ completely in the areas of the wafer that are not covered by the photoresist as shown in the figure.

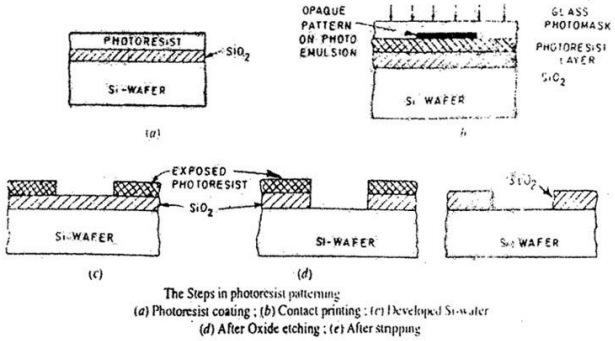
The duration of oxide etching should be carefully controlled so that all of the oxide present only in the photoresist window is removed. If etching time is excessively prolonged, it will result in more undercutting underneath the photoresist and widening of the oxide opening beyond what is desired.

The above oxide etching process is termed **wet etching process**since the chemical reagents used are in liquid form. A newer process for oxide etching is a dry etching process called **plasma etching**. Another dry etching process is ion milling.

**7. Photoresist Stripping**

Following oxide etching, the remaining resist is finally removed or stripped off with a mixture of sulphuric acid and hydrogen peroxide and with the help of abrasion process. Finally a step of washing and

drying completes the required window in the oxide layer. The figure below shows the silicon wafer ready for next diffusion.




Photolithographic Process Steps

Negative photoresists, as above, are more difficult to remove. Positive photoresists can usually be easily removed in organic solvents such as acetone.

The photolithography may employ contact, proximity, or projection printing. For IC production the line width limit of photolithography lies near 0.4 micro meters, although 0.2 micro meters features may be printed under carefully controlled conditions. At present, the photolithography occupies the primary position among various lithographic techniques.

**Photoresists**

O ne of the major factors in providing increasingly complex devices has been improvement in photolithographic art. A large part of this improvement has been due to high quality photoresist, materials as improved techniques of coating, baking, exposing and developing photoresists.

The principal constituents of a photoresist solution are a polymer, a sensitizer and a suitable solvent system Polymers have properties of excellent film forming and coating. Polymers generally used are polyvinyl cinnamate, partially cyclized isoprene family and other types are phenol formaldehyde.

When photoresist is exposed to light, sensitizer absorbs energy and initiates chemical changes in the resist. The sensitizers are chromophoric organic molecules. They greatly enhance cross linking of the photoresist. Cross linking of polymer or long chain formation of considerable number of monomers makes high molecular weight molecules on exposure to light radiation, termed as photo-polymerization. Typical

sensitizers are carbonyl compounds, Benzoin, Benzoyl peroxide, Benzoyl disulphide, nitrogen compounds and halogen compounds.

The solvents used to keep the polymers in solution are mixture of organic liquids. They include aliphetic esters such as butyl acetate and cellosolve acetate, aromatic hydrocarbons like xylene and Ethylbenzene, chlorinated hydrocarbons like chlorobenzene and methylene chloride and ketones such as cyclohexanone. The same solvents are used as thinners and developers.

**Characteristics of Good Photoresist**

To achieve faithful registration of the mask geometry over the substrate surface, the resist should satisfy following conditions.

- Uniform film formation
- Good adhesion to the substrate
- Resolution
- Resistance to wet and dry etch processes

**Types of Photoresist**

Polymers film is either photosensitive or capable or reacting with the pholysis product of additional compound so that the solubility increases or decreases greatly by exposure to UV (ultra-violet) radiation. According to the changes that take place, photoresists are termed negative or positive. Materials which are rendered less soluble in a developer solution by illumination^ yield a negative pattern of the mask and are called negative photoresists. Conversely, positive photoresists become more soluble when subjected to light and therefore yield a positive image of the mask.

**Negative Photoresist**

Kodak negative photoresist contain polyvinyl cinnametes. KPR is being used in printing circuit boards. KTFR is widely used in fabrication of ICs. It provides good adhesion to silicon dioxide and metal surfaces. It gives well etch results to different etchant solutions. For finer resolution, thinner coating of KTFR is used. To achieve controlled and uniform thickness, the viscosity of resist is suitably lowered using thinners.Another negative photoresist is Kodak Microneg 747 which provides high scan speeds at high aperature giving high throughput and resolution.

**Positive Photoresist**

Positive Photoresists have solved the problem of resolution and substrate protection. Photo resists can be used at a coating thickness of 1 micro meter that eliminates holes and minimises defects from dust.Positive photoresist is inherently of low solubility (polymerized) material. The base polymer is active by itself. A sensitizer, when absorbs light, makes the base resist soluble in an alkali developer. Positive photoresists are Novolac resins. Typical solvents are cellosolve acetate, butyl acetate, xylene and toluene.

**Resist requirements for VLSI**

For fine line geometries in VLSI circuits, the resist requirements become more stringent. The resist properties should meet the required demand of high resolution. Here the resist should exhibit

- High sensitivity for partial exposure tool chosen
- Dry developing, dry compatibility
- Vertical profile control

**Photomask Fabrication**

Photolithography is used to produce windows in the oxide layer of the silicon wafer, through which diffusion can take place. For this purpose photomask is required. In this section we shall discuss various techniques of mask fabrication. The pattern appearing on the mask is required to be transferred to the wafer. For this purpose various exposure techniques are employed. We will also discuss these techniques.

**Mask Making**

IC fabrication is done by the batch processing, where many copies of the same circuit are fabricated on a single wafer and many wafers are fabricated at the same time. The number of wafers processed at one time is called the lot size and many vary between 20 to 200 wafers. Since each IC chip is square and the wafer is circular, the number of chips per wafer is the number of complete squares of a given size that can fit inside a circle.

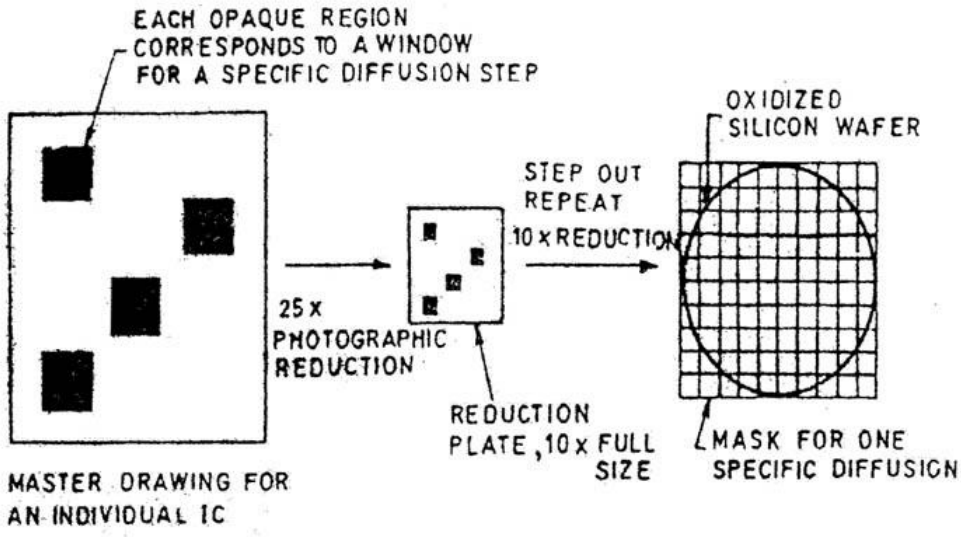
The pattern for the mask is designed from the circuit layout. Many years ago, bread boarding of the circuit was typical. In this, the circuit was actually built and tested with discrete components before its integration. At present, however, when LSI and VLSI circuits contain from a thousand to several hundred

thousand components, and switching speeds are of such high order where propagation delay time between devices is significant, bread boarding is obviously not practical. Present-day mask layout is done with the help of computer.

The photographic mask determines the location of all windows in the oxide layer, and hence areas over which a particular diffusion step is effective. Each complete mask consists of a photographic plate on which each window is represented by an opaque are, the remainder being transparent. Each complete mask will not only include all the windows for the production of one stage of a particular IC, but in addition, all similar areas for all such circuits on the entire silicon as shown in the figure below.

It will be obvious that a different mask is required for each stage in the production of an array of IC's on a wafer. There is also a vital requirement for precise registration between one mask and the other in series, to ensure that there is no overlap between components, and that each section of a particular transistor is formed in precisely the correct location.

T o make a mask for one of the production stages, a master is first prepared which is an exact replica of that portion of the final mask associated with one individual integrated circuit, but which is 250x [say] enlargement of the final size of IC. The figure below shows a possible master for the production of a mask to define a particular layer of diffusion for a hypothetical circuit. Art work at enlarge size avoids large tolerance errors. Large size also permits the art work to be dealt easily by human operator. In the design of the art work, the locations of all components that is, resistor, capacitor, diode, transistor and so on, are determined on the surface of the chip. Therefore, six or more layout drawings are required. Each drawing shows the position of Windows that are required for a particular step of the fabrication. For complex circuit the layout is generated by the use of computer-aided graphics.




Producing one of a series of photographic masks required for the manufacture of an array of ICs. Figures are not to scales.

Photomask Fabrication

The master, typically of order 1 m x 1 m, is prepared from cut and strip plastic material which consists of two plastic films, one photographically opaque called Rubilith and the other transparent [mylar], which are laminated together. The outline of the pattern required is cut in the red coating of Rubilith (which is opaque) using a machine controlled cutter on an illuminated drafting table. The opaque film is then peeled off to reveal transparent areas, each representing a window region in die final mask.

The next step is to photograph the master using back illumination, to produce a 25 x reduced sub-master plate. This plate is used in a step and repeat camera which serves the dual purpose of reducing the pattern by a further 10 x to finished size and is also capable of being stepped mechanically to produce an array of identical patterns on the final master mask, each member of the many corresponding to one complete IC. Instead of the photographic plate being transported mechanically in discrete steps, better accuracy may be achieved by using continuous plate movement; discrete exposures then being made by an electronically synchronized flash lamp which effectively freezes the motion.

The entire sequence just described can be done with plates containing a photosensitive emulsion; typically the emulsion is considered too vulnerable to abrasion and tears. For this reason, masks are often made of harder materials such as chrome or iron oxide.

For very complex circuits automated mask generation equipment is used. In this, a computer controlled light flashes to build up the pattern on a photographic film by a series of line or block exposures,

the resulting film is then reduced and handled in a step and repeat system to create the production mask. Alternatively, the master mask can be generated by an electron beam exposure system, again controlled by computer.

**Various Printing Techniques**

Photolithography comprises the formation of images with visible or U V radiation in a photoresist using contact proximity, or projection printing. Here we will discuss about these printing techniques.

**1. Contact Printing**

In this printing technique, the photomask is pressed against the resist coated wafer with a pressure typically in the range of 0.05 atm to 0.3 atm and exposure by light of wavelength near 400 micro meters. A resolution of less than 1 micro meter linewidth is possible, but it may vary across the wafer because of spatial non-uniformity of the contact. To provide better contact over the whole wafer, a thin (0.2 mm) flexible mask has been used.

**2. Proximity Printing**

In proximity or shadow printing, there exists a gap between mask and wafer in the range of 20 to 50 micro meters. This has the advantage of longer mask life because there is no contact between the mask and the wafer. In the proximity printing, the mask and wafer are both placed in an equipment called a projection aligner. Looking through a microscope, an operator brings the mask into close proximity [say 10 to 20 micro meters] to the wafer and properly aligns the wafer and mask using alignment mark on the mask and the wafer. UV light is then projected through the mask on to the entire resist coated wafer at one time. This mask that is used is a full wafer x 1 mask. The resolution of this process is a function of the wavelength of the light source and the distance between the mask and the wafer. Typically, the resolution of proximity printing is 2 to 4 micro meter and is therefore not suitable for a process requiring less than a 2 um minimum line width.

**3. Projection Printing**

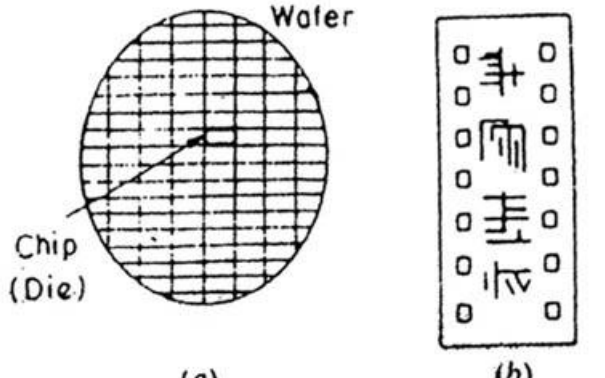
In this case the image is actually projected with the help of a system of lenses, onto the wafer. The mask can be used a large number of times, substantially reducing the mask cost per wafer. Theoretically a mask can be used an unlimited-number of times, but actual usage is limited to about 100,000 times because the mask must be cleaned due to dust accumulation, and it is scratched at each cleaning. This is costliest of

the conventional systems, however mask life is good, and resolution obtained is higher than proximity printing together with large separation between mask and wafer.

**Automated Mask Generation**

As discussed above, layouts of electronic circuit are drawn on large mylar sheets. They can also be drawn on a CRT screen by which layouts are stored digitally in a magnetic tape (or disk). In this case we need to prepare many layouts since each layout represents a pattern on each mask to be used during fabrication. Since the layouts are to be stored digitally, it is required to convert the layouts drawn on mylar sheets into digital data. This is performed by a digitizer with the aid of a computer. Then different portions of each layout are displayed on a CRT one by one and inspected for further mistakes. After all the corrections have been made, a reticle, which is a small photographic plate of the layout image, is prepared from each layout stored on the magnetic tape.

Depending upon the type of equipment used, the mask to be fabricated contains one IC chip pattern which is repeated as many times as there are on the wafer. Alternatively, the mask consists of only magnified chip pattern as shown in the figure below.




(a) Full water mask ×1 mask with chip pattern repeated for each chip location (b) Single chip pattern at ×5 or ×10 magnification.

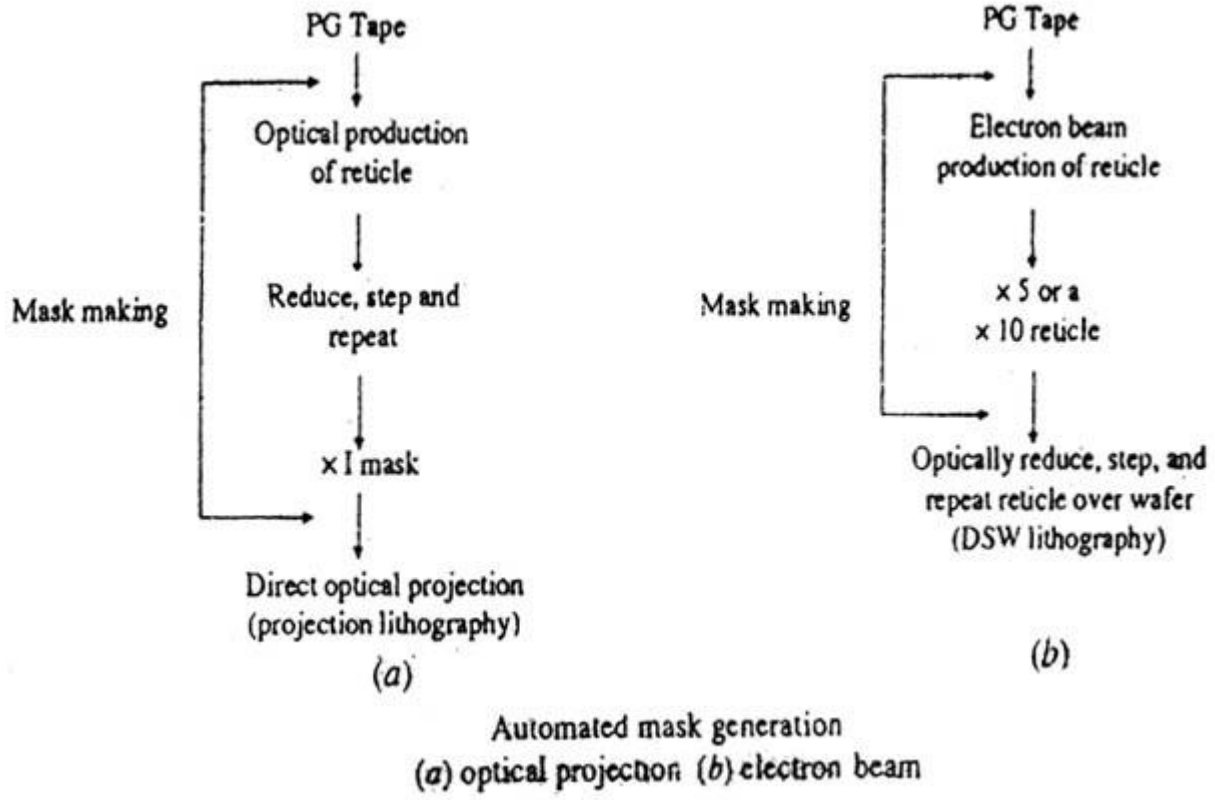
Automated Mask generation

The two most common approaches to automated mask making or generation are

- Using optical projection and
- Using electron beam

A pattern generator (PG) tape is used as the Input to both approaches. The PG tape, contains the digitized data necessary to control the light source or electron beam that is used to write a pattern on a photosensitive glass plate. An Ax10 pattern for a single chip (called a x10 reticle) is first produced. This reticle is then photo enlarged by a factor of 15, yielding x 150 blowback, which is used for visual checking. A x 1 mask of the type shown in the figure is then produced from the x 10 reticle by optical reduction and projection onto a second photosensitive plate. The same pattern is stepped and repeated on this plate as many as there are chips on the wafer. This step and repat operation is performed by photo repeater. The glass plate is then developed yielding a x 1 mask which is called a master mask and looks like a tile floor where each rectangular tile has the same layout image of the chp. During the step and repeat process the position and angle of the reticle are precisely aligned with the help of two fiducial marks incorporated in the PG files of all layouts in the same relative position with respect to the entire chip. The master mask plate is then placed in close proximity to the wafer and optically projected on to a resist-coated wafer during the lithographic process.

The figure below shows the second approach. This employs electron-beam mask generation equipment winch generates the mask plate in one step. The layout data are converted into a hit map of 1’s and 0’s on a raster image. The electron beam sweeps the row in a repeating S pattern, blanking or unblanking the beam according to the input bit value, 0 or 1. In the figure, the x10 reticle is optically reduced and stepped directly onto the wafer. This is referred to as direct-step on wafer (DSW) lithography.




Automated Mask Generation Process

The main advantage of electron-beam pattern generator is speed in the case of complex chips. A large, dense chip can require 20 hours or more of optical pattern generator time, but only two hours or less of electron-beam pattern generator time.

**Electron-beam lithography**

Electron-beam lithography provides better resolution then photolithography. This is possible because of small wavelength of the 10-50 KeV electrons. The resolution of electron-beam lithography system is not limited by diffraction, but by electron scattering in the resist and by the various aberrations of the electron optics. The electron-beam exposure system (EBES) machine has proved to be the best photomask pattern generator. However, the pattern writing is in serial form. Therefore, the throughput is much less than for optical systems. In the earlier years of development, electron-beam lithography was employed in the production of low-volume integrated circuits.

**Resists**

There is a formation of bonds or cross-links between polymer chains when negative resist is exposed to electron beam. However, bond breaking occurs in positive resist when it is exposed. The electron-beam induced cross-links between molecules of negative resist make the polymer less soluble in the developer solution. Resist sensitivity increases with increasing molecular weight. In positive resist the bond breaking process predominates. Thus exposure leads to lower molecular weight and greater solubility.

The polymer molecules in the unexposed resist will have a distribution of length or molecular weight and thus a distribution of sensitivities to radiation.The narrower the distribution, the higher will be the contrast. High molecular weight and narrow distribution are advantageous.The resist resolution is limited by swelling of the resist in the developer and electron scattering. Swelling is of more concern for the negative resist and this occurs in all types of lithography, that is, optical, electron, or X-ray. Swelling leads to poor adhesion of resist to the substrate. This problem becomes less severe as resist thickness is reduced.

There is also a fundamental process limitation on resolution. When electrons are incident on a resist or other material, they inter the material and lose energy by scattering, thus producing secondary electrons and X-rays. This limits the resolution to an extent that depends on resist thickness, beam energy, and substrate composition.

For thinner resist layers the resolution is better. Minimum thickness, however, is set by the need to keep defect density low and by resistance to etching as used while device processing. For photomasks where the surface is fiat and only a thin layer of chrome must be etched with a liquid etchant, resist thickness in the range of 0.2 to 0.4 micro meters are used. In case of more severe dry gas plasma etching process employed, thickness of 0.5 micro meters to 2 micro meters are required. One way to overcome this problem is to use a multilayer resist structure in which the thick bottom layer consists of the process-resistant polymer. A three-layer resist structure may be used in which the uppermost layer is used to pattern a thin intermediate layer, such as $SiO_2$ which serves as a mask for etching the thick polymer below. For electron lithography a conducting layer can be substituted for the $SiO_2$ layer to prevent charge build-up that can lead to beam placement errors.

Multilayer resist structure also alleviates the problem of proximity effect encountered during electron-beam exposure. In this, an exposed pattern element adjacent to another element receives exposure not only from the incident electron beam but also from scattered electrons from the adjacent elements. A two- layer resist structure is also used. In such structure, both the thin upper and the thick lower layer are

positive electron resist, but they are developed in different solvents. The thick layer can be overdeveloped to provide the undercut profile that is ideal for lift-off process.

**Electron Optics**

The first widespread use of electron-beam pattern generators has been in photomask making as discussed in previous section. The EBES machine, as stated earlier, has proved to be the best photomask pattern generator. Scanning electron-beam pattern generators are similar to scanning electron microscopes, from which they are derived. A basic probe-forming electron optical system may consist of two or more magnetic lenses and provisions for scanning the image and blanking the beam on the wafer image plane. Typical image spot sizes are in the range from 0.1 to 2 micro meters. This is for from the diffraction limits. Hence diffraction can be ignored. However, abberations of the final lens and of the deflection system will increase the size of the spot and can change its shape as well.

**Electron Projection Printing**

Electron projection system provides high resolution over a large field with high throughput. Rather than a small beam writing the pattern in serial fashion, a large beam provides parallel exposure of large area pattern. In a 1:1 projection system parallel electric and magnetic fields image electrons onto the wafer. The mask is of quartz and is patterned with chrome. It is covered with CsI on the side facing the wafer. Photoelectrons are generated on the mask/cathode by backside UV illumination.

The advantages of the projection system are stable mask, good resolution, fast step-repeat exposure with low sensitivity electron resists, large field, and fast alignment. The limitations of the system include proximity effects of electrons and shorter life of cathode.

**Electron Proximity Printing**

This is a step-repeat system in which a silicon membrane stencil mask containing one chip pattern is shadow printed onto the wafer. The mask cannot accommodate re-entrant geometries. Registration is accomplished by reference to alignment mask on each chip. An advantage of electron proximity printing is its ability to measure and compensate for mask distortions. Proximity effects must be treated by changing the size of pattern elements. The main limitation of the system is the need for two masks for each pattern.

**Diffusion of Dopant Impurities**

The process of junction formation, that is transition from p to n type or vice versa, is typically accomplished by the process of diffusing the appropriate dopant impurities in a high temperature furnace. Impurity atoms are introduced onto the surface of a silicon wafer and diffuse into the lattice because of their tendency to move from regions of high to low concentration. Diffusion of impurity atoms into silicon crystal takes place only at elevated temperature, typically 900 to 1100°C.

Although these are rather high temperatures, they are still well below the melting point of silicon, which is at 1420°C. The rate at which the various impurities diffuse into silicon will be of the order of 1 micro meter per hour at a temperature range stated above, and the penetration depth that are involved in most diffusion processes will be of the order of 0.3 to 30 micro meter. At room temperature the diffusion process will be so extremely slow such that the impurities can be considered to be essentially frozen in place.

A method of p-n junction formation which was popular in the early days is the grown junction technique. In this method the dopant is abruptly changed in the melt during the process of crystal growth. A convenient technique for making p-n junction is the alloying of a metal containing doping atoms on a semiconductor with the opposite type of dopant. This is called the alloyed junction technique. The p-n junction using epitaxial growth is widely used in ICs. An epitaxial grown junction is a sharp junction. In terms of volume of production, the most common technique for forming p-n junctions is the impurity diffusion process. This produces diffused junction. Along with diffusion process the use of selective masking to control junction geometry, makes possible the wide variety of devices available in the form of IC's. Selective diffusion is an important technique in its controllability, accuracy and versatility.

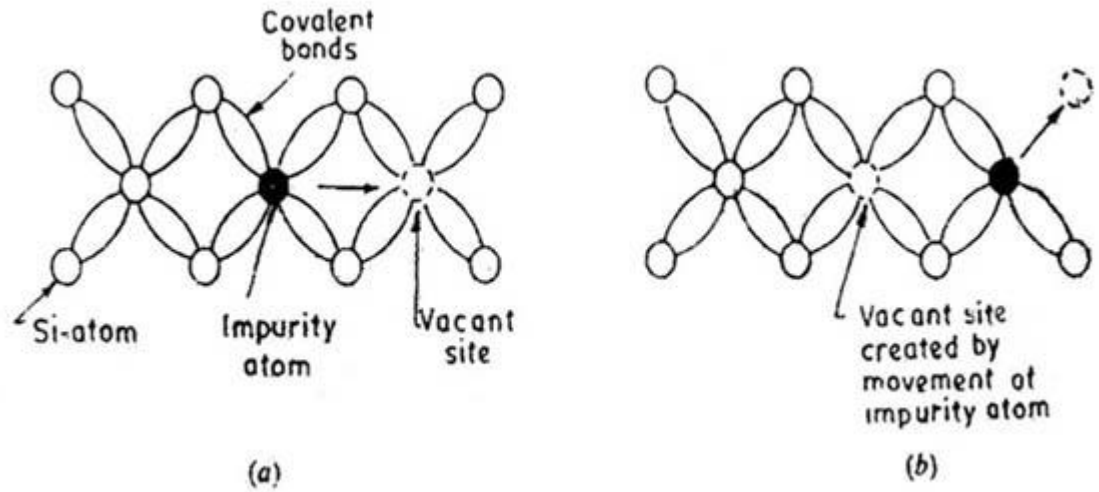
**Nature of Impurity Diffusion**

The diffusion of impurities into a solid is basically the same type of process as occurs when excess carriers are created non-uniformly in a semiconductor which cause carrier gradient. In each case, the diffusion is a result of random motion, and particles diffuse in the direction of decreasing concentration gradient The random motion of impurity atoms in a solid is, of course, rather limited unless the temperature is high. Thus diffusion of doping impurities into silicon is accomplished at high temperature as stated above.

There are mainly two types of physical mechanisms by which the impurities can diffuse into the lattice. They are

**1. Substitutional Diffusion**

At high temperature many atoms in the semiconductor move out of their lattice site, leaving vacancies into which impurity atoms can move. The impurities, thus, diffuse by this type of vacancy motion and occupy lattice position in the crystal after it is cooled. Thus, substitutional diffusion takes place by replacing the silicon atoms of parent crystal by impurity atom. In other words, impurity atoms diffuse by moving from a lattice site to a neighbouring one by substituting for a silicon atom which has vacated a usually occupied site as shown in the figure below.




Substitutional Diffusion By Dopant Impurities

Substitutional diffusion mechanism is applicable to the most common diffusants, such as boron, phosphorus, and arsenic. These dopants atoms are too big to fit into the interstices or voids, so the only way they can enter the silicon crystal is to substitute for a Si atom.

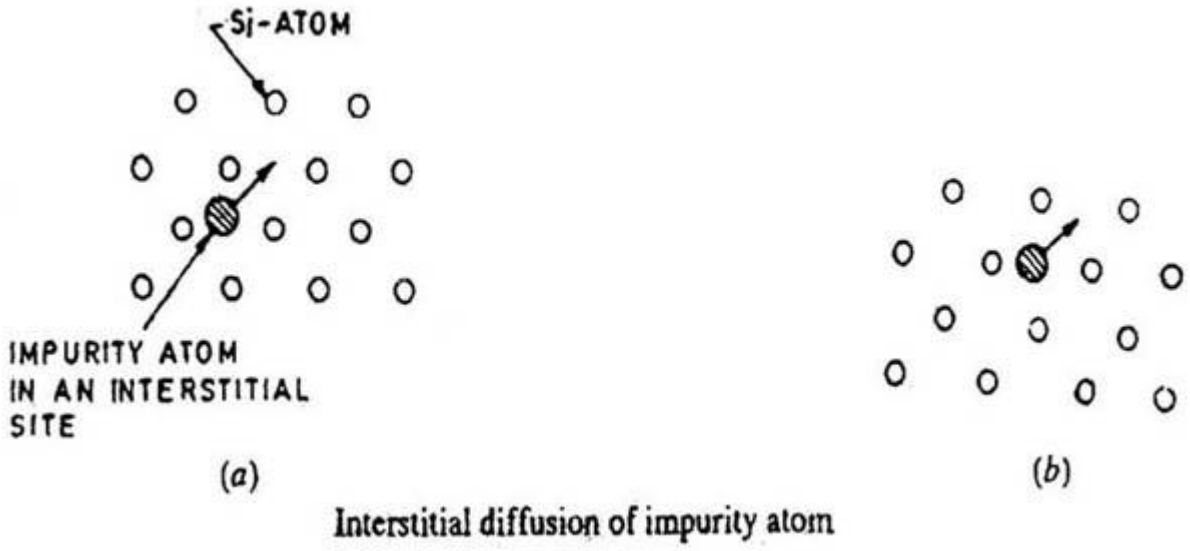
In order for such an impurity atom to move to a neighbouring vacant site, it has to overcome energy barrier which is due to the breaking of covalent bonds. The probability of its having enough thermal energy to do this is proportional to an exponential function of temperature. Also, whether it is able to move is also dependent on the availability of a vacant neighbouring site and since an adjacent site is vacated by a Si atom due to thermal fluctuation of the lattice, the probability of such an event is again an exponent of temperature.

The jump rate of impurity atoms at ordinary temperatures is very slow, for example about 1 jump per $10^{50}$ years at room temperature! However, the diffusion rate can be speeded up by an increase in temperature. At a temperature of the order 1000 degree Celsius, substitutional diffusion of impurities is practically realized in sensible time scales.

**2. Interstitial Diffusion**

In such, diffusion type, the impurity atom does not replace the silicon atom, but instead moves into the interstitial voids in the lattice. The main types of impurities diffusing by such mechanism are Gold, copper, and nickel. Gold, particularly, is introduced into silicon to reduce carrier life time and hence useful to increase speed at digital IC's.

Because of the large size of such metal atoms, they do not usually substitute in the silicon lattice. To understand interstitial diffusion, let us consider a unit cell of the diamond lattice of the silicon which has five interstitial voids. Each of the voids is big enough to contain an impurity atom. An impurity atom located in one such void can move to a neighbouring void, as shown in the figure below.




Interstitial diffusion of impurity atom

Interstitial Diffusion of Impurity Atom

In doing so it again has to surmount a potential barrier due to the lattice, this time, most neighbouring interstitial sites are vacant so the frequency of movement is reduced. Again, the diffusion rate due to this process is very slow at room temperature but becomes practically acceptable at normal operating temperature of around 1000 degree Celsius. It will be noticed that the diffusion rate due to interstitial movement is much greater than for substitutional movement. This is possible because interstitial diffusants can fit in the voids between silicon atoms. For example, lithium acts as a donor impurity in silicon, it is not normally used because it will still move around even at temperatures near room temperature, and thus will not be frozen in place. This is true of most other interstitial diffusions, so long-term device stability cannot be assured with this type of impurity.

**Fick's Laws of Diffusion**

The diffusion rate of impurities into semiconductor lattice depends on the following

- Mechanism of diffusion
- Temperature
- Physical properties of impurity
- The properties of the lattice environment
- The concentration gradient of impurities
- The geometry of the parent semiconductor

The behaviour of diffusion particles is governed by Fick's Law, which when solved for appropriate boundary conditions, gives rise to various dopant distributions, called profiles which are approximated during actual diffusion processes.

In 1855, Fick drew analogy between material transfer in a solution and heat transfer by conduction. Fick assumed that in a dilute liquid or gaseous solution, in the absence of convection, the transfer of solute atoms per unit area in a one-dimensional flow can be described by the following equation

$$\mathbf{F = -D\ \partial N(x,t)/\partial x = -\partial F(x,t)/\partial x}$$

where F is the rate of transfer of solute atoms per unit area of the diffusion flux density (atoms/$cm^2$-sec). N is the concentration of solute atoms (number of atoms per unit volume/$cm^3$), and x is the direction of solute flow. (Here N is assumed to be a function of x and t only), t is the diffusion time, and D is the diffusion constant (also referred to as diffusion coefficient or diffusivity) and has units of $cm^2$/sec.

The above equation is called Fick's First law of diffusion and states that the local rate of transfer (local diffusion rate) of solute per unit area per unit time is proportional to the concentration gradient of the solute, and defines the proportionality constant as the diffusion constant of the solute. The negative sign appears due to opposite direction of matter flow and concentration gradient. That is, the matter flows in the direction of decreasing solute concentration.

Fick's first law is applicable to dopant impurities used in silicon. In general the dopant impurities are not charged, nor do they move in an electric field, so the usual drift mobility term (as applied to electrons and holes under the influence of electric field) associated with the above equation can be omitted. In this equation N is in general function of x, y, z and t.

The change of solute concentration with time must be the same as the local decrease of the diffusion flux, in the absence of a source or a sink. This follows from the law of conservation of matter. Therefore we can write down the following equation

$$\partial N(x,t)/\partial t = -\partial F(x,t)/\partial x$$

Substituting the above equation to 'F'. We get

$$\partial N(x,t)/\partial t = \partial/\partial x[D*\partial N(x,t)/\partial x]$$

When the concentration of the solute is low, the diffusion constant at a given temperature can be considered as a constant.

Thus the equation becomes,

$$\partial N(x,t)/\partial t = D[\partial^2 N(x,t)/\partial x^2]$$

This is Ficks second law of distribution.

**Diffusion Profiles**

Depending on boundary equations the Ficks Law has two types of solutions. These solutions provide two types of impurity distribution namely constant source distribution following complimentary error function (erfc) and limited source distribution following Gaussian distribution function.

**Constant Source (erfc) Distribution**

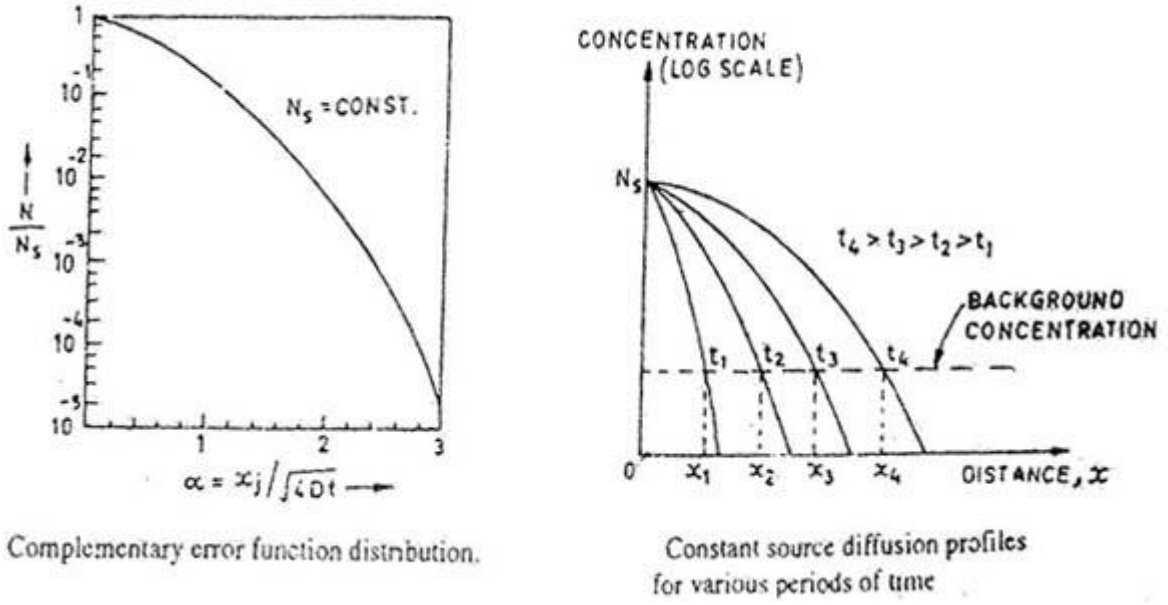
In this impurity distribution, the impurity concentration at the semiconductor surface is maintained at a constant level throughout the diffusion cycle. That is,

$$N(o,t) = N_S = \text{Constant}$$

The solution to the diffusion equation which is applicable in this situation is most easily obtained by first considering diffusion inside a material in which the initial concentration changes in same plane as x=0, from $N_S$ to 0. Thus the equation can be written as

$$N(o,t) = N_S = \text{Constant and } N(x,t) = 0$$

Shown below is a graph of the complementary error function for a range of values of its argument. The change in concentration of impurities with time, as described by the equation is also shown in the figure below. The surface concentration is always held at $N_S$, falling to some lower value away from the surface. If a sufficiently long time is allowed to elapse, it is possible for the entire slice to acquire a dopant level of $N_S$ per $m^3$.




Complementary error function distribution.

Constant source diffusion profiles for various periods of time

Complimentary Error Function

If the diffused impurity type is different from the resistivity type of the substrate material, a junction is formed at the points where the diffused impurity concentration is equal to the background concentration already present in the substrate.In the fabrication of monolithic IC's, constant source diffusion is commonly used for the isolation and the emitter diffusion because it maintains a high surface concentration by a continuous introduction of dopant.There is an upper limit to the concentration of any impurity that can be accommodated at the semiconductor wafer at some temperature. This maximum concentration which determines the surface concentration in constant source diffusion is called the solid solubility of the impurity.

**Limited Source Diffusion or Gaussian Diffusion**

Here a predetermined amount of impurity is introduced into the crystal unlike constant source diffusion. The diffusion takes place in two steps.

**1. Predeposition Step** – In this step a fixed number of impurity atoms are deposited on the silicon wafer during s short time.

**2. Drive-in step** – Here the impurity source is turned off and the amounts of impurities already deposited during the first step are allowed to diffuse into silicon water.

The essential difference between the two types of diffusion techniques is that the surface concentration is held constant for error function diffusion. It decays with time for the Gaussian type owing to a fixed available doping concentration Q. For the case of modelling the depletion layer of a p-n junction, the erfc is modelled as a step junction and the Gaussian as a linear graded junction. In the case of the erfc, the surface concentration is constant, typically the maximum solute concentration at that temperature or solid solubility limit.

**Parameters which affect diffusion profile**

- **Solid Solubility** – In deciding which of the availability impurities can be used, it is essential to know if the number of atoms per unit volume required by the specific profile is less than the diffusant solid solubility.
- **Diffusion temperature** – Higher temperatures give more thermal energy and thus higher velocities, to the diffused impurities. It is found that the diffusion coefficient critically depends upon temperature. Therefore, the temperature profile of diffusion furnace must have higher tolerance of temperature variation over its entire area.
- **Diffusion time** – Increases of diffusion time, t, or diffusion coefficient D have similar effects on junction depth as can be seen from the equations of limited and constant source diffusions. For Gaussian distribution, the net concentration will decrease due to impurity compensation, and can approach zero with increasing diffusion tunes. For constant source diffusion, the net Impurity concentration on the diffused side of the p-n junction shows a steady increase with time.

  **Surface cleanliness and defects in silicon crystal –** The silicon surface must be prevented against contaminants during diffusion which may interfere seriously with the uniformity of the diffusion profile. The crystal defects such as dislocation or stacking faults may produce localized impurity concentration. This results in the degradation of junction characteristics. Hence silicon crystal must be highly perfect.

**Basic Properties of the Diffusion Process**

Following properties could be considered for designing and laying out ICs.

- When calculating the total effective diffusion time for given impurity profile, one must consider the effects of subsequent diffusion cycles.

- The erfc and Gaussian functions show that the diffusion profiles are functions of (x/ √Dt). Hence, for a given surface and background concentration, the junction depth x1 and x2 associated with the two separate diffusions having different times and temperature
- **Lateral Diffusion Effects** – The diffusions proceed sideways from a diffusion window as well as downward. In both types of distribution function, the side diffusion is about 75 to 80 per cent of the vertical diffusion.

**Dopants and their Characteristics**

The dopants selection affects IC characteristics. Boron and phosphorus are the basic dopants of most ICs. Arsenic and antimony, which are highly soluble in silicon and diffuse slowly, are used before epitaxial processing or as a second diffusion. Gold and silver diffuse rapidly. They act as recombination centres and thus reduce carrier life time.

Boron is almost an exclusive choice as an acceptor impurity in silicon since other p-type impurities have limitations as follows :

Gallium has relatively large diffusion coefficient in $Si0_2$, and the usual oxide window-opening technique for locating diffusion would be inoperative, Indium is of little interest because of its high acceptor level of 0.16 eV, compared with 0.01 eV for boron, which indicates that not all such acceptors would be ionized at room temperature to produce a hole. Aluminium reacts strongly with any oxygen that is present in the silicon lattice.

The choice of a particular n-type dopant is not so limited as for p-type materials. The n-type impurities, such as phosphorus, antimony and arsenic, can be used at different stages of IC processing. The diffusion constant of phosphorus is much greater than for Sb and As, being comparable to that for boron, which leads to economies resulting from shorter diffusion times.

**Dopants in VLSI Technology**

The common dopants in VLSI circuit fabrication are boron, phosphorus. and arsenic. Phosphorus is useful not only as an emitter and base dopant, but also far gettering fast-diffusing metallic contaminants, such as Cu and An, which cause junction leakage current problems. Thus, phosphorus is indispensable in VLSI technology. However, n-p-n transistors made with arsenic-diffused emitters have better low-current gain characteristics and better control of narrow base widths than those made with phosphorus-diffused emitters. Therefore, in V LSI, the use of phosphorus as an active dopant in small, shallow junctions and low-

temperature processing will be limited to its use as the base dopant of p-n-p device and as a gettering agent. Arsenic is the most frequently used dopant for the source and drain regions in n-channel MOSFETs.

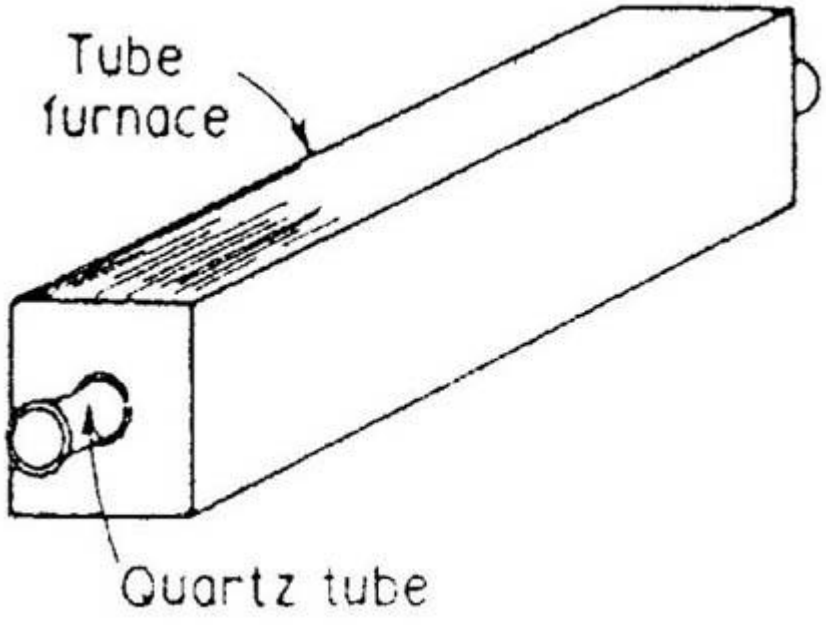
**Diffusion Systems**

Impurities are diffused from their compound sources as mentioned above. The method impurity delivery to wafer is determined by the nature of impurity source; Two-step diffusion is widely technique. Using this technique, the impurity concentration and profiles can be carefully controlled. The type of impurity distribution (erfc or Gaussian) is determined by the choice of operating conditions.

The two-step diffusion consists of a deposition step and a drive-in step. In the former step a constant source diffusion is carried out for a short time, usually at a relatively low temperatures, say, 1000°C. In the latter step, the impurity supply is shutoff and the existing dopant is allowed to diffuse into the body of the semiconductor, which is now held at a different temperature, say 1200°C, in an oxidizing atmosphere. The oxide layer which forms on tire surface of the wafer during this step prevents further impurities from entering, or those already deposited, from diffusing out. The final impurity profile is a function of diffusion condition, such as temperature, time, and diffusion coefficients, for each step.

- **Diffusion Furnace**

For the various types of diffusion (and also oxidation) processes a resistance-heated tube furnace is usually used. A tube furnace has a long (about 2 to 3 meters) hollow opening into which a quartz tube about 100,150 mm in diameter is placed as shown in the figure below.




Diffusion Furnace

The temperature of the furnace is kept about1000°C. The temperature within the quartz furnace tube can be controlled very accurately such that a temperature within 1/2°C of the set-point temperature can be maintained uniformly over a "hot zone" about 1 m in length. This is achieved by three individually controlled adjacent resistance elements. The silicon wafers to be processed are stacked up vertically into slots in a quartz carrier or "boat" and inserted into the furnace lube.

**Diffusion Of p-Type Impurity**

Boron is an almost exclusive choice as an acceptor impurity in silicon. It has a moderate diffusion coefficient, typically of order I0-16 m2/sec at 1150°C which is convenient for precisely controlled diffusion. It has a solid solubility limit of around 5 x 1026 atoms/m3, so that surface concentration can be widely varied, but most reproducible results are obtained when the concentration is approximately 1024/m3, which is typical for transistor base diffusions.

- **Boron Diffusion using $B_2H_6$ (Diborane) Source**

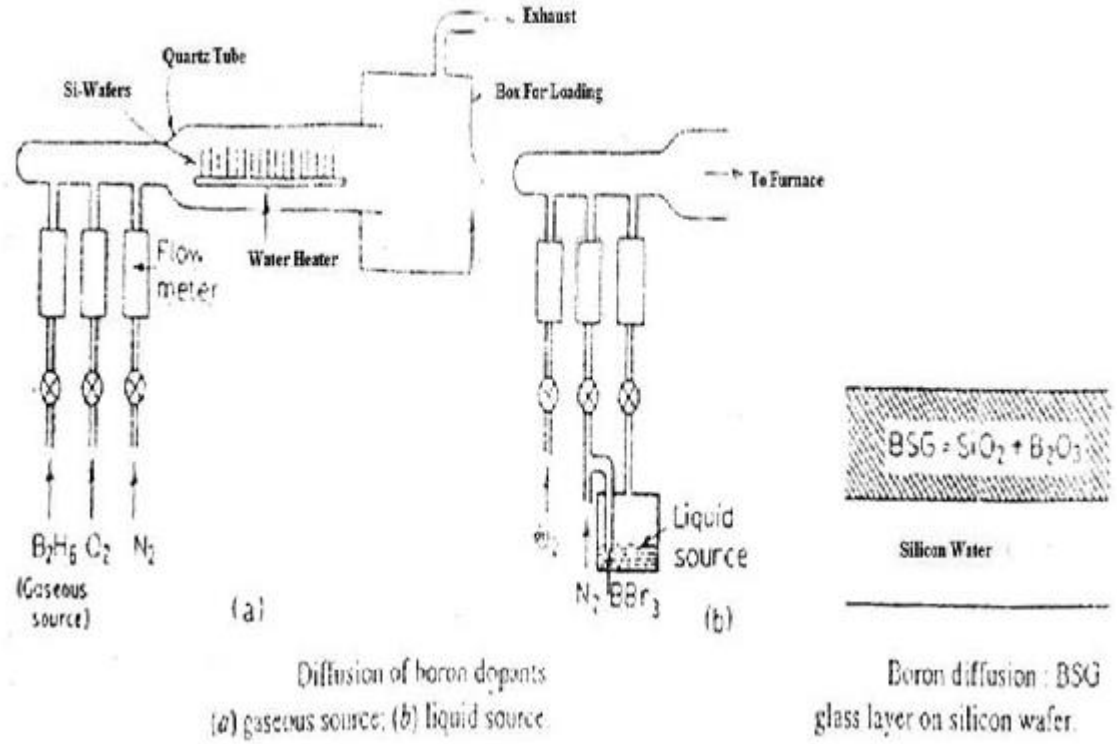
This is a gaseous source for boron. This can be directly introduced into the diffusion furnace. A number of other gases are metered into the furnace. The principal gas flow in the furnace will be nitrogen ($N_2$) which acts as a relatively inert gas and is used as a carrier gas to be a dilutent for the other more reactive gases. The $N_2$, carrier gas will generally make up some 90 to 99 percent of the total gas flow. A small amount of oxygen

and very small amount of a source of boron will make up the rest of the gas flow. This is shown in the figure below. The following reactions will be occurring simultaneously at the surface of the silicon wafers:

**$Si + 0_2 = SiO_2$ (silica glass)**

**$2B_2H_6 + 30_2 = B_2O_3$ (boron glass) + $6H_2$**

This process is the chemical vapour deposition (CVD) of a glassy layer on (lie silicon surface which is a mixture of silica glass ($Si0_2$) and boron glass ($B_20_3$) is called borosilica glass (BSG). The BSG glassy layer, shown in the figure below, is a viscous liquid at the diffusion temperatures and the boron atoms can move around relatively easily.




Diffusion of boron dopants (a) gaseous source; (b) liquid source

Boron diffusion : BSG glass layer on silicon wafer.

Diffusion Of Dopants

Furthermore, the boron concentration in the BSG is such that the silicon surface will be saturated with boron at the solid solubility limit throughout the time of the diffusion process as long as BSG remains present. This is constant source (erfc) diffusion. It is often called deposition diffusion. This diffusion step is referred as pre-deposition step in which the dopant atoms deposit into the surface regions (say 0.3 micro meters depth) of the silicon wafers. The BSG is preferable because it protects the silicon atoms from pitting

or evaporating and acts as a "getter" for undesirable impurities in the silicon. It is etched off before next diffusion as discussed below.

The pre-deposition step, is followed by a second diffusion process in which the external dopant source (BSG) is removed such that no additional dopants cuter the silicon. During this diffusion process the dopants that are already in the silicon move further in and are thus redistributed. The junction depth increases, and at the same time the surface concentration decreases. This type of diffusion is called drive-in, or redistribution, or limited-source (Gaussian diffusion).

- **Boron Diffusion using $BBr_3i$ (Boron Tribromide) Source**

This is a liquid source of boron. In this case a controlled flow of carrier gas ($N_2$,) is bubbled through boron tribromide, as shown in the figure below, which with oxygen again produces boron trioxide (BSG) at the surface of the wafers as per following reaction :

$$4BBr_3 + 30_2 = B20_3 + 2Br_2$$

**Diffusion of n-Type Impurity**

For phosphorus diffusion such compounds as PH3 (phosphine) and POCl3 (phosphorus oxychloride) can be used. In the case of a diffusion using PoCI3, the reactions occurring at the silicon wafer surfaces will be:

$$Si + 02 = SiO2 \text{ (silica glass)}$$

$$4POCl + 30_2 = 2P_20_5 + 6Cl_2$$

This will result in the production of a glassy layer on the silicon wafers (hat is a mixture of phosphorus glass and silica glass called phosphorosilica glass (PSG), which is a viscous liquid at the diffusion temperatures. The mobility of the phosphorus atoms in this glassy layer and the phosphorus concentration is such that the phosphorus concentration at the silicon surface will be maintained at the solid solubility limit throughout the time of the diffusion process (similar processes occur with other dopants, such as the case of arsenic, in winch arsenosilica glass is formed on the silicon surface.

The rest of the process for phosphorus diffusion is similar to boron diffusion, that is, after deposition step, drive-in diffusion is carried out.

$P_20_5$ is a solid source for phosphorus impurity and can be used in place of $POCl_3$. However $POCl_3$ offers certain advantages overP205 such as easier source handling, simple furnace requirements, similar glassware for low and high surface concentrations and better control of impurity density from wafer to wafer and from run to run.

**POSSIBLE QUESTIONS**

**PART-B ( 2Marks)**

1. What is called PLL?
2. What are the basic circuit elements of PLL?
3. What do you mean by diffusion?
4. Define Metallization.
5. What is called Lift off Technique.?
6. What are the advantages of Loop Filter Circuits?
7. What are Defects in the lattice?
8. What is called lithography?
9. What is called Positive and Negative Masks?
10. Write the importance of Electronic grade silicon in IC fabrication.

**PART-C (6 Marks)**

1. Discuss crystal plane and defects in crystal lattice
2. Explain the working principle of PLL
3. Explain the working principle of voltage controlled oscillator.
4. Discuss optical lithography technique and its applications
5. Discuss basic idea of PLL IC 565
6. Explain Electron lithography
7. Explain the princpiple of IC fabrication
8. Explain the working principle of Edge triggered Phase detector.
9. Explain Optical lithography technique.
10. Explain the principle of Metalization Techniques.

**KARPAGAM ACADEMY OF HIGHER EDUCATION,COIMBATORE-21**

**DEPARTMENT OF PHYSICS**

**CLASS: II B.Sc., PHYSICS (2017-2020)**

**PART – A Online Examination (1 mark questions)**
**SUBJECT: PHYSICS OF DEVICES AND COMMUNICATION**
**SUBJECT CODE: 17PHU302**

**UNIT - III**

| | Option-1 | Option-2 | Option-3 | Option-4 | Key |
|---|---|---|---|---|---|
| The _____ is a miniature, low cost electronic circuit consisting of active and passive components that are joined on a single crystal chip. | Integrated Resistor | Integrated Capacitor | Integrated Circuit | Integrated Inductor | Integrated Circuit |
| The number of gates fabricated using MSI is | 3 to 30 | 30 to 300 | 300 to 3000 | 3000 to 30,000 | 30 to 300 |
| The type of metal used for interconnections in the fabrication of IC is | Iron | Boron | Aluminium | Brass | Aluminium |
| The chips can be separated by using diamond cut tools to cut lines into the surface of the wafer along the rectangular grid by a method known as | Thermal | co-ordinatograph | etching | cleaving | cleaving |
| The formation of resistor in the isolation region of epitaxial layer during emitter diffusion is known as | Diffused Resistor | Epitaxial Resistor | Pinched Resistor | Thin film Resistor | Diffused Resistor |
| The process which is subjected to intense bombardment by ions of a heavy inert gas for the deposition of thin film is | Vacuum Evaporation | Gas plating | Silk screening | Cathode sputtering | Cathode sputtering |
| Cost reduction in IC is due to _____ processing | Oxidation | Batch | Photolithography | Diffusion | Batch |
| System reliability of an IC can be increased by elimination of | Mask | Etching | Solder joints | Cleaving | Solder joints |

| | | | | | |
|---|---|---|---|---|---|
| Operating speed of an IC can be increased due to the absence of | Parasitic resistance | diffused resistance | Junction capacitance | Parasitic capacitance | Parasitic capacitance |
| During a epitaxial growth, the graphite is heated to a temperature of | 1200*c | 1420*c | 1600*c | 1750*c | 1200*c |
| The thickness of oxide layer in the order of ___ | 0.02 to 2um | 0.2 to 2 um | 2 to 20 um | 20 to 200 um | 0.02 to 2 um |
| In oxidation process, Silicon wafers are heated to a temperature of ____ | 600-800*c | 800-950*c | 950-1115*c | 1115-1200*c | 950-1115*c |
| Using photolithography process,_____ transistors are fabricated on a 1cm*1cm chip | 1000 | 10000 | 100 | 10 | 10000 |
| In photolithography _____ is used to remove SiO2 layer. | Masking | Diffusion | Photoetching | Oxidation | Photoetching |
| The ions during ion implantation are accelerated by energies between____ | 1 kv to 10 kv | 10 kv to 100kv | 10 kv to 200 kv | 20 kv to 250 kv | 20 kv to 250 kv |
| During Diffusion,the cleaned wafers are maintained at a temperature of | 1200*c | 1000*c | 1420*c | 1800*c | 1000*c |
| After diffusion of impurities,the photoresist is removed by using | H2So4 | Hcl | CaCl4 | NaCl | H2So4 |
| The_____produces thin metal film layer to make inter connections of various components on the chip | Oxidation | Diffusion | Ion Implantation | Metallization | Metallization |
| The pressure in the chamber during metallization in maintained at____ | 760 to rr | 720 to rr | 840 to rr | 960 to rr | 760 to rr |
| During metallization,unwanted aluminium is etched away using _____ | Hcl | NaCl | CaCl2 | H3Po4 | H3Po4 |
| The thickness of SiO2 layer is____ | 0.02-2um | 2-20um | 2.8-10um | 20-28um | 0.02-2um |

| | | | | | |
|---|---|---|---|---|---|
| The higher collecter series resistance of an integrated transistor can be reduced by ___ layer | depletion | Oxidation | Buried | Isolation | Buried |
| The type of diode that is used as a clamp between base and collector of a transistor during fabrication is | Schottky | Tunnel | Varactor | Zener | Schottky |
| The missing link in the chain of IC components is____ | Resistors | Capacitors | Transistors | Inductors | Inductors |
| The thickness of thin film IC's vary between____ | 50-20,000A* | 50-100A* | 50-200A* | 50-2000A* | 50-20,000A* |
| The thickness of thinfilm IC's vary between | 1,00,000-1,25,000A* | 1,25,000-6,25,000A* | 50-200A* | 10000-25000A* | 1,25,000-6,25,000A* |
| How many gates per chip are used in first generation Integrated Circuits? | 3-30 | 30-3000 | 3000-30000 | 3-30000 | 3-30 |
| ICs are generally made of | Silicon | germanium | iron | copper | Silicon |
| ICs are the most commonly used | Thin films | Monolithic | Hybrid | transistor | Monolithic |
| The most popular form of IC package is | DIL | Flatpack | TO-5 | TO-7 | Flatpack |
| Which device is used for diagnostic purposes and for recording? | Low pass filter | Monolithic PLL | Voltage Controlled Oscillator | PLL | Voltage Controlled Oscillator |
| Write the equation for time period of VCO? | (2×Vcc×CT)/i | (Vcc CT)/(2×i) | (Vcc×CT×i)/2 | (2×Vcc)/(i×CT) | (Vcc CT)/(2×i) |
| The output frequency of the VCO can be changed by changing | External tuning resistor | External tuning capacitor | Modulating input voltage | All of the mentioned | External tuning capacitor |
| Choose the VCO for attaining higher output frequency. | NE566 | SE566 | MC4024 | MC4000 | MC4024 |
| At which state the phase-locked loop tracks any change in input frequency? | Free running state | Capture state | Phase locked state | monostable | Phase locked state |
| What is the function of | Improves | Removes | Tracks the | Changes | Removes |

| | | | | | |
|---|---|---|---|---|---|
| low pass filter in phase-locked loop? | low frequency noise | high frequency noise | voltage changes | the input frequency | high frequency noise |
| What is the need to generate corrective control voltage? | To maintain the lock | To remove lock | remove high frequency | improve signal to noise ratio | To maintain the lock |
| What is the need to generate corrective control voltage? | To track the frequency change | To remove lock | remove high frequency | improve signal to noise ratio | To track the frequency change |
| What is the need to generate corrective control voltage? | To shift the VCO frequency | To remove lock | remove high frequency | improve signal to noise ratio | To shift the VCO frequency |
| At what range the PLL can maintain the lock in the circuit? | Lock in range | Input range | Feedback loop range | out put range | Lock in range |
| Varactor diode is majorly used in the | networking | database | tuning circuit | amplifing | tuning circuit |
| A semiconductor device operated in reverse-bias mode whose capacitance can change in response to a modulating signal is the | zener diode | tunnel diode | varactor diode | unijunction transistor | varactor diode |
| VCO stands for | Voltage Capacitor Oscillator | Voltage Controlled Oscillator | Voltage Charing Oscillator | Varying Capacitor Oscilloscope | Voltage Controlled Oscillator |
| The range of frequencies over which the PLL can maintain lock with the incoming signal is called as | phase detector | lock-in range | capture range | pull-in time | lock-in range |
| The range of frequencies over which the PLL can acquire lock with the input signal is called as | capture range | phase detector | lock-in range | pull-in time | capture range |
| The total time taken by PLL to establish lock is known as | phase detector | capture range | pull-in time | lock-in range | pull-in time |
| Most phase modulators are capable of producing an amount of phase shift essentially limited to | ± 5° | ± 10° | ± 15° | ± 20° | phase detector |
| hich of the following is | phase | parallel | voltage- | low-pass | phase- |

| | | | | | |
|---|---|---|---|---|---|
| not a basic element of a phase-locked loop circuit? | detector | tuned circuit | controlled oscillator | filter | locked loops |
| Oscillators whose frequencies are controlled by an external input voltage are generally referred to as | phase-locked loops | crystal oscillators | voltage-controlled oscillators | Colpitts | |
| The active components in an IC are … | Resistors | Capacitors | Transistors and diodes | transformers | Transistors and diodes |
| The SiO2 layer in an IC acts as | Resistors | An insulating layer | Capacitors | Mechanical output | An insulating layer |
| Which of the following is most difficult to fabricate in an IC? | Resistors | Capacitors | Transistors | diodes | Capacitors |
| What is the conversion ratio of the phase detector in 565 PLL | 0.14 | 0.35 | 0.4458 | 0.7 | 0.4458 |
| What happens when VCO output is 90o out of phase with respect to input signal? | Perfect lock | Attenuation | Shift in phase of comparator | Error signal is removed | Perfect lock |
| How to overcome the problem associated with switch type phase detective? | Increase loop gain depending on input signal | decrease loop gain depending on input signal | Phase shift is made linear | Limit the amplifier of input signal | Limit the amplifier of input signal |
| Which among the following has better capture tracking & locking characteristics? | XOR phase detector | X NOR phase detector | Edge triggered phase detector | Analog phase detector | Edge triggered phase detector |
| In communication circuits, PLL is currently applicable for | Demodulation | modulation | amplification | filtering | Demodulation |
| In the locked state of PLL, the phase error between the input & output is | Zero | maxcimum | minimum | moderate | minimum |
| In PLL, the capture range is always _____the lock range. | > | < | equal to | 0 | equal to |
| In a linear IC voltage regulator, series pass transistor always operates in _____ region. | Active | Saturation | cut-off | inactive | Active |

## UNIT-IV

## SYLLABUS

**Digital Data Communication Standards:**
Serial Communications: RS232, Handshaking, Implementation of RS232 on PC.
Universal Serial Bus (USB): USB standards, Types and elements of USB transfers. Devices (Basic idea of UART). Parallel Communications: General Purpose Interface Bus (GPIB), GPIB signals and lines, Handshaking and interface management, Implementation of a GPIB on a PC. Basic idea of sending data through a COM port.

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SERIAL COMMUNICATIONS:

Computers transfer data in two ways: parallel and serial. In parallel data transfers, often 8 or more lines are used to transfer data to a device that is only a few feet away. Examples of parallel transfers are printers and hard disks; each uses cables with many wire strips. Although in such cases a lot of data can be transferred in a short amount of time by using many wires in parallel, the distance cannot be great. To transfer to a device located many meters away, the serial method is used. In serial communication, the data is sent one bit at a time, in contrast to parallel communication, in which the data is sent a byte or more at a time.

When a microprocessor communicates with the outside world, it provides the data in byte-sized chunks. In some cases, such as printers, the information is simply grabbed from the 8-bit data bus and presented to the 8-bit data bus of the printer. This can work only if the cable is not too long, since long cables diminish and even distort signals. Furthermore, an 8-bit data path is expensive. For these reasons, serial communication is used for transferring data between two systems located at distances of hundreds of feet to millions of miles apart.

Serial communication is the process of sending/receiving data in one bit at a time.

Serial Transmission Modes

Serial data can be transferred in two modes – asynchronous and synchronous.


Serial Communication Terminologies

1. MSB/LSB: this stands for Most Significant Bit (or Least Significant Bit).
2. Simplex Communication: In this mode of serial communication, data can only be transferred from transmitter to receiver and not vice versa.
3. Half Duplex Communication: this means that data transmission can occur in only one direction at a time, i.e. either from master to slave, or slave to master, but not both.
4. Full Duplex Communication: full duplex communication means that data can be transmitted from the master to the slave, and from slave to the master as the same time!
5. Baud Rate: according to Wikipedia, baud is synonymous to symbols per second or pulses per second. It is the unit of symbol rate, also known as baud or modulation rate. However, though technically incorrect, in the case of modem manufacturers baud commonly refers to bits per second.

The UART:

The Universal Asynchronous Receiver/Transmitter (UART) controller is the key component of the serial communications subsystem of a computer. The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.

Serial transmission is commonly used with modems and for non-networked communication between computers, terminals and other devices. There are two primary forms of serial transmission: Synchronous and Asynchronous. Depending on the modes that are supported by the hardware, the name of the communication sub-system will usually include a `A` if it supports Asynchronous communications, and a `S` if it supports Synchronous communications. Both forms are described below.

Synchronous serial transmission

Synchronous serial transmission requires that the sender and receiver share a clock with one another, or that the sender provide a strobe or other timing signal so that the receiver knows when to "read" the next bit of the data. In most forms of serial Synchronous communication, if there is no data available at a given

instant to transmit, a fill character must be sent instead so that data is always being transmitted. Synchronous communication is usually more efficient because only data bits are transmitted between sender and receiver, and synchronous communication can be more costly if extra wiring and circuits are required to share a clock signal between the sender and receiver.

A form of Synchronous transmission is used with printers and fixed disk devices in that the data is sent on one set of wires while a clock or strobe is sent on a different wire. Printers and fixed disk devices are not normally serial devices because most fixed disk interface standards send an entire word of data for each clock or strobe signal by using a separate wire for each bit of the word. In the PC industry, these are known as Parallel devices.The standard serial communications hardware in the PC does not support Synchronous operations. This mode is described here for comparison purposes only.

Asynchronous Serial Transmission

Asynchronous transmission allows data to be transmitted without the sender having to send a clock signal to the receiver. Instead, the sender and receiver must agree on timing parameters in advance and special bits are added to each word which are used to synchronize the sending and receiving units.When a word is given to the UART for Asynchronous transmissions, a bit called the "Start Bit" is added to the beginning of each word that is to be transmitted. The Start Bit is used to alert the receiver that a word of data is about to be sent, and to force the clock in the receiver into synchronization with the clock in the transmitter. These two clocks must be accurate enough to not have the frequency drift by more than 10% during the transmission of the remaining bits in the word.

After the Start Bit, the individual bits of the word of data are sent, with the Least Significant Bit (LSB) being sent first. Each bit in the transmission is transmitted for exactly the same amount of time as all of the other bits, and the receiver“looks” at the wire at approximately halfway through the period assigned to each bit to determine if the bit is a 1 or a 0.

For example, if it takes two seconds to send each bit, the receiver will examine the signal to determine if it is a `1` or a `0`after one second has passed, then it will wait two seconds and then examine the value of the next bit, and so on.The sender does not know when the receiver has “looked” at the value of the bit. The sender only knows when the clock says to begin transmitting the next bit of the word.When the entire data word has been sent, the transmitter may add a Parity Bit that the transmitter generates. The Parity

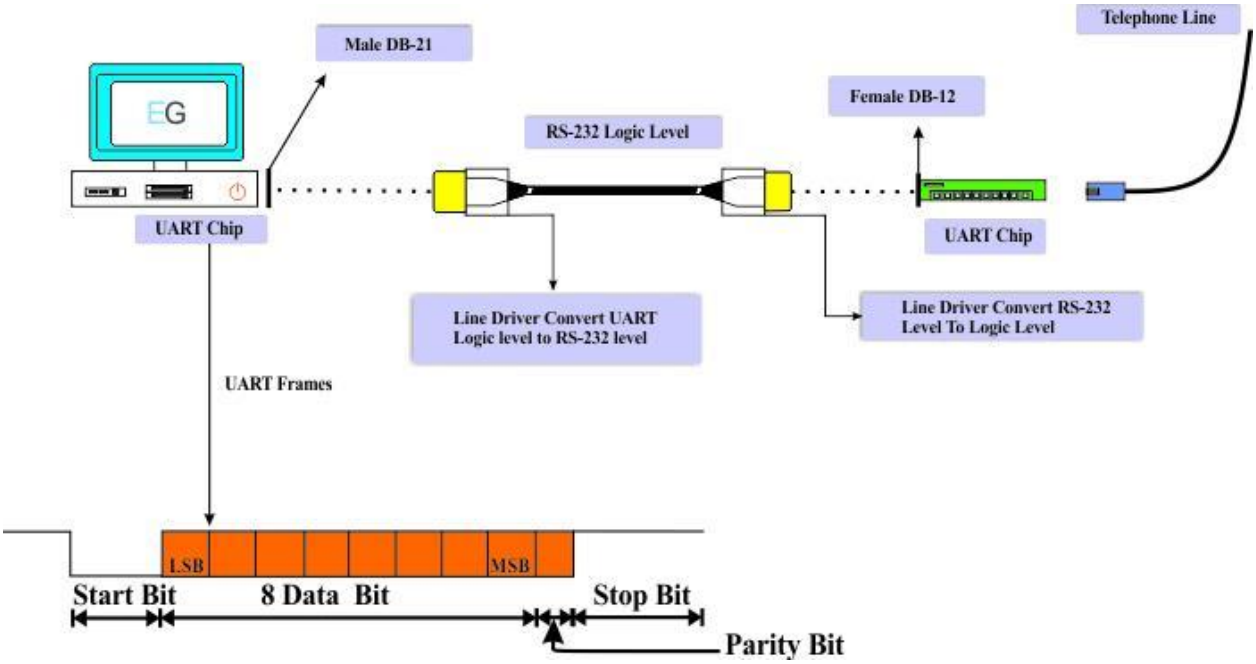
Bit may be used by the receiver to perform simple error checking. Then at least one Stop Bit is sent by the transmitter.

When the receiver has received all of the bits in the data word, it may check for the Parity Bits (both sender and receiver must agree on whether a Parity Bit is to be used), and then the receiver looks for a Stop Bit. If the Stop Bit does not appear when it is supposed to, the UART considers the entire word to be garbled and will report a Framing Error to the host processor when the data word is read. The usual cause of a Framing Error is that the sender and receiver clocks were not running at the same speed, or that the signal was interrupted.Regardless of whether the data was received correctly or not, the UART automatically discards the Start, Parity and Stop bits. If the sender and receiver are configured identically, these bits are not passed to the host.If another word is ready for transmission, the Start Bit for the new word can be sent as soon as the Stop Bit for the previous word has been sent.

Because asynchronous data is “self synchronizing”, if there is no data to transmit, the transmission line can be idle.

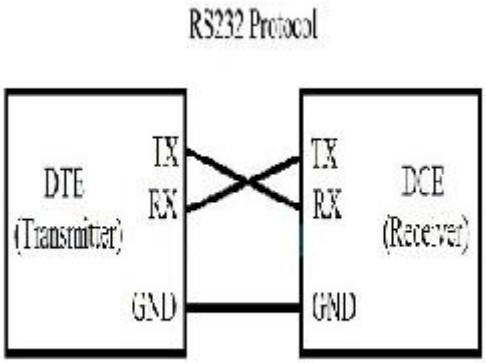
**RS232 - "RECOMMENDED STANDARD 232"**

RS-232 is a standard communication protocol for linking computer and its peripheral devices to allow serial data exchange. In simple terms RS232 defines the voltage for the path used for data exchange between the devices. It specifies common voltage and signal level, common pin wire configuration and minimum, amount of control signals. As mentioned above this standard was designed with specification for electromechanically teletypewriter and modem system and did not define elements such as character encoding, framing of characters, error detection protocols etc that are essential features when data transfer takes place between a computer and a printer. Without which it could not be adopted to transfer data between a computer and a printer. To overcome this problem a single integrated circuit called as UART known as universal asynchronous receiver/transmitter is used in conjunction with RS232.




RS232 is one of the most widely used techniques to interface external equipment with computers. RS232 is a Serial Communication Standard developed by the Electronic Industry Association (EIA) and Telecommunications Industry Association (TIA).

In general it is an interface between Data terminal equipment and Data communication equipment".




DTE stands for data terminal equipment is an end instrument that convert user information into signals or reconverts the receive signal. It is a functional unit of station that serves as data source or data sink and provides for communication control function according to the link protocol. A male connector is used in DTE and has pin out configuration.

DCE-A DCE stands for data communication equipments. It sits between the DTE and data transmission circuit for example modem. A DCE device uses a female connector which has holes on the surface to hold male connector.

A minimum of three signals are required for communication between a DTE and a DCE devices. These signals are a transmission line, a reception line and ground. These two devices communicate with each other by handshaking. It allows a DTE and a DCE device system to acknowledge each other before sending the data. Thai is RS232 defines the signals connecting between DTE and DCE.

Handshaking is a process in which a DTE device sends a signal to a DCE device to establish a connection between the devices before the actual transfer of data. It sets the parameters of communication channel established between two equipments before normal communication over the channel begins. It follows physical establishment of the channel and precedes normal information transfer. Handshaking makes it possible to connect relatively heterogeneous systems or equipment over a communication channel without the need for human intervention to set parameters. This same concept is used in RS232 to allow two devices communicate with each other before the actual exchange of information.

All these terms put together gives a complete picture of a RS232 system starting from DTE to DCE with UART, line drivers and RS232 as conjunction between them.

. The RS-232 standard states that DTE devices use a 25-pin male connector, and DCE devices use a 25-pin female connector. You can therefore connect a DTE device to a DCE using a straight pin-for-pin connection. However, to connect two like devices, you must instead use a null modem cable. Null modem cables cross the transmit and receive lines in the cable, and are

Male RS232 DB25


| Pin Number | Direction of signal: |
|---|---|
| 1 | Protective Ground |

| | |
|---|---|
| 2 | Transmitted Data (TD) Outgoing Data (from a DTE to a DCE) |
| 3 | Received Data (RD) Incoming Data (from a DCE to a DTE) |
| 4 | Request To Send (RTS) Outgoing flow control signal controlled by DTE |
| 5 | Clear To Send (CTS) Incoming flow control signal controlled by DCE |
| 6 | Data Set Ready (DSR) Incoming handshaking signal controlled by DCE |
| 7 | Signal Ground Common reference voltage |
| 8 | Carrier Detect (CD) Incoming signal from a modem |
| 20 | Data Terminal Ready (DTR) Outgoing handshaking signal controlled by DTE |
| 22 | Ring Indicator (RI) Incoming signal from a modem |

The TD (transmit data) wire is the one through which data from a DTE device is transmitted to a DCE device. This name can be deceiving, because this wire is used by a DCE device to receive its data. The TD line is kept in a mark condition by the DTE device when it is idle. The RD (receive data) wire is the one on which data is received by a DTE device, and the DCE device keeps this line in a mark condition when idle.

RTS stands for Request To Send. This line and the CTS line are used when "hardware flow control" is enabled in both the DTE and DCE devices. The DTE device puts this line in a mark condition to tell the remote device that it is ready and able to receive data. If the DTE device is not able to receive data (typically because its receive buffer is almost full), it will put this line in the space condition as a signal to the DCE to stop sending data. When the DTE device is ready to receive more data (i.e. after data has been removed from its receive buffer), it will place this line back in the mark condition. The complement of the RTS wire is CTS, which stands for Clear To Send. The DCE device puts this line in a mark condition to tell the DTE device that it is ready to receive the data. Likewise, if the DCE device is unable to receive data, it will place this line in the space condition. Together, these two lines make up what is called RTS/CTS or "hardware"

flow control. WinWedge supports this type of flow control, as well as Xon/XOff or "software" flow control. Software flow control uses special control characters transmitted from one device to another to tell the other device to stop or start sending data. With software flow control the RTS and CTS lines are not normally used.

DTR stands for Data Terminal Ready. Its intended function is very similar to the RTS line. DSR (Data Set Ready) is the companion to DTR in the same way that CTS is to RTS. Some serial devices use DTR and DSR as signals to simply confirm that a device is connected and is turned on. WinWedge sets DTR to the mark state when the serial port is opened and leaves it in that state until the port is closed. The DTR and DSR lines were originally designed to provide an alternate method of hardware handshaking. It would be pointless to use both RTS/CTS and DTR/DSR for flow control signals at the same time. Because of this, DTR and DSR are rarely used for flow control.

CD stands for Carrier Detect. Carrier Detect is used by a modem to signal that it has a made a connection with another modem, or has detected a carrier tone.

The last remaining line is RI or Ring Indicator. A modem toggles the state of this line when an incoming call rings your phone.

The Carrier Detect (CD) and the Ring Indicator (RI) lines are only available in connections to a modem. Because most modems transmit status information to a PC when either a carrier signal is detected (i.e. when a connection is made to another modem) or when the line is ringing, these two lines are rarely used.

**What is Handshaking?**

The method used by RS-232 for communication allows for a simple connection of three lines: TX,RX,andground.

For the data to be transmitted, both sides have to be clocking the data at the same baud rate. Although, this method is sufficient for most applications, it is limited in being able to respond to problems such as the receiver getting overloaded. In RS-232: Software Handshaking, Hardware Handshaking, and Xmodem are present.

a. **Software Handshaking:** The first form of handshaking we will discuss is software handshaking. This style uses actual data bytes as control characters, similar to the way GPIB uses command strings. The lines necessary are still the simple three line set of TX, RX, and round since the control characters are sent over the transmission line like regular data. The function SetXMode allows the user to enable or

disable the use of two control characters, XON and XOFF. These characters are sent by the receiver of the data to pause the transmitter

As an example, assume that the transmitter begins to transmit data at a high baud rate. During the transmission, the receiver finds that the input buffer is becoming full due to the CPU being busy with other duties. To temporarily pause the transmission, the receiver sends XOFF, typically decimal 19 or hex 13, until the input buffer has been emptied. Once the receiver is ready for more data it sends XON, typically decimal 17 or hex 11, to resume communication. LabWindows will send XOFF when its input buffer becomes half full. In addition, in case the XOFF transmission was corrupted, LabWindows will also transmit XOFF when the buffer has reached 75% and 90% capacity. Obviously, the transmitter must also be following this protocol for it to succeed.

The biggest drawback to this method is also the most important fact to keep in mind: decimal 17 and 19 are now off limits for data values. In ASCII transmissions this typically does not matter since these values are non-character values; however, if the data is being transmitted via binary, it is very likely that these values could be transmitted as data and the transmission would fail.

b. **Hardware Handshaking:** The second method of handshaking is to use actual hardware lines. Like the TX and RX lines, the RTS/CTS and DTR/DSR lines work together with one being the output and the other the input. The first set of lines are RTS (Request to Send) and CTS (Clear to Send). When a receiver is ready for data, it will assert the RTS line indicating it is ready to receive data. This is then read by the sender at the CTS input, indicating it is clear to send the data. The next set of lines are DTR (Data Terminal Ready) and DSR (Data Set Ready). These lines are used mainly for modem communication. They allow the serial port and the modem to communicate their status. For example, when the modem is ready for data to be sent from the PC, it will assert the DTR line indicating that a connection has been made across the phone line. This is read in through the DSR line and the PC can begin to send data. The general rule of thumb is that the DTR/DSR lines are used to indicate that the system is ready for communication where the RTS/CTS lines are used for individual packets of data.

c. Whenthe PC sends data:
The RS-232 library must detect that its CTS line is high before sending data.
When the PC receives data:
If the port is opened and the input queue has room for data, the library raises RTS and DTR.
If the port's input queue is 90% full, the library lowers RTS and leaves DTR high.
If the port's input queue is nearly empty, the library raises RTS and leaves DTR high.

If the port is closed, the library lowers RTS and DTR.

d. **XModem Handshaking:** The last mode discussed here is the XModem file transfer protocol. This protocol is very common in modem communication. Although it is often used for modem communication, the XModem protocol can be used directly between other devices if they both follow the protocol. In LabWindows, the actual implementation of XModem is hidden from the user. As long as the PC is connected to another device using XModem protocol, the LabWindows' XModem functions can be used to transfer files from one site to another. The functions are XModemConfig, XModemSend, and XModemReceive.

XModem uses a protocol based on the following parameters: start_of_data, end_of_trans, neg_ack, ack, wait_delay, start_delay, max_tries, packet_size. These parameters need to be agreed upon by both sides. Standard XModem has a standard definition of these; however, they can be modified through the XModemConfig function in LabWindows to meet any requirement. The way that these parameters are used in XModem is by having the neg_ack character sent by the receiver. This tells the sender that it is ready to receive data. It will try again with start_delay time in-between each try until either it reaches max_tries or receives start_of_data from the sender. If it reaches max_tries it will inform the user that it was unable to communicate with the sender. If it does receive start_of_data from the sender, it will read the packet of information that follows. This packet contains the packet number, the complement of the packet number as an error check, the actual data packet of packet_size bytes, and a checksum on the data for more error checking. After reading the data, the receiver will call wait_delay and then se nd ack back to the sender. If the sender does not receive ack, it will re-send the data packet max_tries or until it receives ack. If it never receives the ack, it informs the user that it has failed to transfer the file.

Since the data must be sent in packets of packet_size bytes, when the last packet is sent, if there is not enough data to fill the packet, the data packet is padded with ASCII NUL (0) bytes. This can cause the received file to be larger than the original. It is also important to remember not to use XON/XOFF with the XModem protocol since the packet number from the XModem transfer is very likely to increment to the XON/OFF control character values, which would cause a breakdown in communication.

**USB**

Universal Serial Bus, USB is a plug-and-play interface that allows a computer to communicate with peripheral and other devices. USB-connected devices cover a broad range; anything from keyboards and mice, to music players and flash drives.

**USB standards**

- USB1.1: This was the original version of the USB, Universal Serial Bus and was released in September 1998 after a few problems with the USB 1.0 specification released in January 1996 were resolved.. It provided a Master / Slave interface and a tiered star topology which was capable of supporting up to 127 devices and a maximum of six tiers or hubs. The master or "Host" device is normally a PC with the slaves or "Devices" linked via the cable.

  One of the aims of the USB standard was to minimise the complexity within the Device by enabling the Host to perform the processing. This meant that devices would be cheap and readily accessible.

  The data transfer rates of USB 1.1 are defined as:

  - Low speed: 1.5 Mbps
  - Full speed: 12 Mbps

  The cable length for USB 1.1 is limited to 5 metres, and the power consumption specification allows each device to take up to 500mA, although this is limited to 100mA during start-up.

  USB 1.1 does not allow extension cables or the inclusion of pass-through monitors (due to timing and power limitations).

- USB 2.0: The USB 2.0 standard is a development of USB 1.1 which was released in April 2000. The main difference when compared to USB 1.1 was the data transfer speed increase up to a "High Speed" rate of 480 Mbps. However it should be noted that even though devices are labelled USB 2.0, they may not be able to meet the full transfer speed.
- USB 3.0: This improved USB standard which was first demonstrated at the Intel Developer Forum in September 2007. The major feature is what is termed the SuperSpeed bus, which provides a fourth

transfer mode which gives data transfer rates of 4.8 Gbit/s. Although the raw throughput is 4 Gbit/s, data transfer rates of 3.2 Gbit/s, i.e.0.4 GByte/s more after protocol overhead are deemed acceptable within the standard. The standard is also backwards compatible with USB 2.0.

Often USB ports on computers, etc. may have the USB symbol with 'SS' added, i.e. SS USB. SS USB denotes USB 3, i.e. Super Speed USB. Read More

- Wireless USB The concept for wireless USB is that, as the name suggests, it provides a wire-less connection over which data can be transferred. This USB standard has not been as widely adopted.

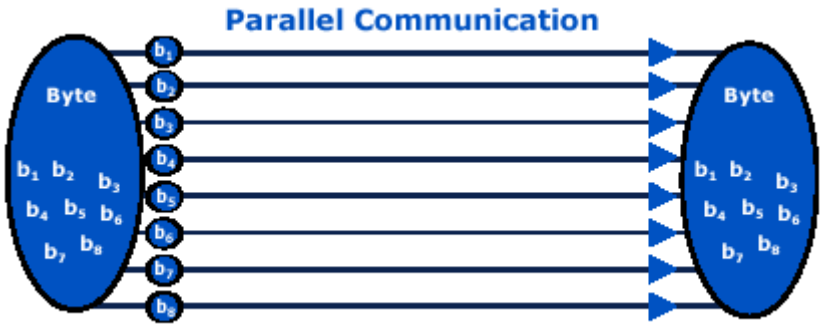
**There are four basic types of data transaction that can be made within USB.**

- Control: This type of data transaction within the overall USB protocol is used by the host to send commands or query parameters. The packet lengths are defined within the protocol as 8 bytes for Low speed, 8-64 bytes for Full, and 64 bytes for High Speed devices.
- Interrupt: The USB protocol defines an interrupt message. This is often used by devices sending small amounts of data, e.g. mice or keyboards. It is a polled message from the host which has to request specific data of the remote device
- Bulk: This USB protocol message is used by devices like printers for which much larger amounts of data are required. In this form of data transfer, variable length blocks of data are sent or requested by the Host. The maximum length is 64-byte for full speed Devices or 512 bytes for high speed ones. The data integrity is verified using cyclic redundancy checking, CRC and an acknowledgement is sent. This USB data transfer mechanism is not used by time critical peripherals because it utilises bandwidth not used by the other mechanisms.
- Isochronous: This form of data transfer is used to stream real time data and is used for applications like live audio channels, etc. It does not use and data checking, as there is not time to resend any data packets with errors - lost data can be accommodated better than the delays incurred by resending data. Packet sizes can be up to 1024 bytes.

## PARALLEL COMMUNICATION

The parallel port greatly increases transfer speeds by using an eight wire connector which transmits the eight bits in a byte of data simultaneously, thus sending an entire byte of data in the time it takes to send a single

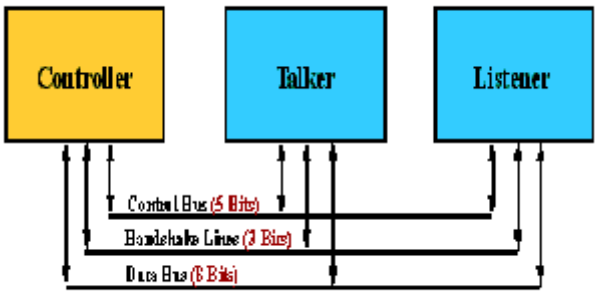
bit in a serial system. This byte of data is supplemented by several other handshaking signals, each sent on its own wire, which ensure that data transfer takes place smoothly.




**GPIB General-Purpose-Interface-Bus**

Definition

General Purpose Interface Bus: A standard bus for controlling electronic instruments with a computer. Also called IEEE-488 bus because it is defined by ANSI/IEEE Standards 488-1978, and 488.2-1987. Also called HP-IB, a trademarked term of Hewlett-Packard, which invented the protocol.




Synonyms

- General Purpose Interface Bus
- IEEE-488
- HP-IB
- 488

**Basic GPIB concept**

The GPIB or IEEE 488 bus is a very flexible system, allowing data to flow between any of the instruments on the bus, at a speed suitable for the slowest active instrument. Up to fifteen instruments may be connected together with a maximum bus length not exceeding 20 m.

There must also be no more than 2 m between two adjacent instruments on the bus. It is possible to purchase GPIB cards to incorporate into computers that do not have the interface fitted. As GPIB cards are relatively cheap, this makes the inclusion of a GPIB card into the system a very cost effect method of installing it.

Devices have a unique address on the bus. Instruments are allocated addresses in the range 0 to 30, and no two instruments on the same bus should have the same address. The addresses on the instruments can be changed and this may typically be done via the front panel, or by using switches often located on the rear panel.

Active extenders allow longer buses, with up to 31 devices theoretically possible.

In the original HPIB protocol, transfers utilise three wire handshaking system. Using this the maximum data rate achievable is around 1 Mbyte per second, but this is always governed by the speed of the slowest device. A later enhancement often referred to as HS-488 relaxes the handshaking conditions and enables data rates up to about 8 Mbytes / second.

The connector used for the IEEE 488 bus is standardized as a 24-way Amphenol 57 series type. This provides an ideal physical interface for the standard. The IEEE 488 or GPIB connector is very similar in format to those that were used for parallel printer ports on PCs although the type used for the GPIB has the advantage it has been changed so that several connectors can be piggy-backed. This helps the physical setting up of the bus and prevents complications with special connection boxes or star points.

General-purpose interface bus (GPIB), has provided a standard, high-speed interface for communication between instruments and controllers from a multitude of vendors. GPIB is used across a wide variety of industrial instrument control applications.

**1.The IEEE 488.1 Specification**

The GPIB is a digital 8-bit parallel communications interface with data transfer rates up to 1 Mbyte/s. The bus supports one System Controller, usually a computer, and up to 15 additional instruments. Because the

GPIB is an 8-bit parallel interface with fast data transfer rates, it gained popularity in other applications such as intercomputer communication and peripheral control.

2. **The IEEE 488.2 Specification**

IEEE Standard 488.2-1987 encouraged a new level of growth and acceptance of the IEEE 488 bus or GPIB by addressing problems that had arisen from the original IEEE 488 standard. IEEE 488.2 was drafted on the premise that it stay compatible with the existing IEEE 488.1 standard. The overriding concept used in the IEEE 488.2 specification for the communication between Controllers and instruments is that of "precise talking" and "forgiving listening." In other words, IEEE 488.2 exactly defined how both IEEE 488.2 Controllers and IEEE 488.2 instruments talk so that a completely IEEE 488.2-compatible system can be highly reliable and efficient. The standard also required that IEEE 488.2 devices be able to work with existing IEEE 488.1 devices by accepting a wide range of commands and data formats as a Listener.

The IEEE 488.2 standard defined control sequences that specify the exact IEEE 488.1 messages that are sent from the Controller as well as the ordering of multiple messages. IEEE 488.2 defined 15 required control sequences and four optional control sequences, as shown in Table 1. The IEEE 488.2 control sequences describe the exact states of the GPIB and the ordering of command messages for each defined operation. IEEE 488.2 control sequences remove the ambiguity of the possible bus conditions, so instruments and Controllers are much more compatible. By exactly defining the state of the bus and how devices should respond to specific messages, IEEE 488.2 solves such system development problems.

- Listener: A listener is an entity connected to the bus that accepts instructions from the bus. An example of a listener is an item such as a printer that only accepts data from the bus
- Talker: This is an entity on the bus that issues instructions / data onto the bus.

Assembling GPIB Instrument Control System

A basic GPIB Instrument Control system consists of four parts:

1. PC
2. GPIB controller
3. GPIB cable

4. GPIB instrument

Setting up the PC. PCI-based GPIB controller boards offer a simple, seamless bridge between the PC and the GPIB instrument. Additionally, stand-alone GPIB controllers communicate via serial, USB, or Ethernet/LXI. As a result GPIB instruments can transmit their data across the room or around the world. Additionally, the National Instruments Instrument Driver Network has more than 7000 instrument drivers to choose from, as well as tutorials on how to use them to control your instrument.

Configuring the Controller. Depending on the GPIB controller manufacturer, some kind of instrument control software driver will need to be installed before the device will function. National Instruments GPIB controllers come with their own GPIB driver and Measurement & Automation Explorer (MAX). MAX scans for connected instruments, confirms communication, and creates the necessary handles for programming. Connecting GPIB Controller to Instrument. Once the controller is installed and working properly, the GPIB cable can be connected from the controller to the instrument. In accordance with the IEEE 488.2 standard, with a single controller you can control up to 15 different instruments connected in either a daisy-chain or star topology.

## POSSIBLE QUESTIONS

**PART-A( 2Marks)**

1. What do you mean by serial communication?
2. What do you mean by parallel communication?
3. Define baudrate.
4. What are the basic GPIB Instrument Control system elements?
5. What is called USB?
6. What is called UART
7. What is called Synchronous mode of transmission
8. What is called Asynchronous mode of transmission
9. What is called Software handshaking
10. What is called Hardware handshaking

**PART-C( 6Marks)**

1. Explain the working principle of RS232
2. Explain handshaking and interface management in GPIB
3. Explain the working principle of USB
4. Explain handshaking and Implementation of RS232 on PC
5. Explain the working principle of UART
6. Explain the Implementation of a GPIB on a PC
7. Write short note on Parallel and serial communications.
8. Explain the basic GPIB Instrument Control system elements
9. Write short note on i) Synchronous mode of transmission ii) Asynchronous mode of transmission
10. Write short note on i) USB ii) UART.

**KARPAGAM ACADEMY OF HIGHER EDUCATION,COIMBATORE-21**

**DEPARTMENT OF PHYSICS**

**II B.Sc., PHYSICS (2017-2020)**

**PHYSICS OF DEVICES AND COMMUNICATION (17PHU302 )**

**UNIT - IV**

| | **Option-1** | **Option-2** | **Option-3** | **Option-4** | **Key** |
|---|---|---|---|---|---|
| The transfer rate, when the USB is operating in low-speed of operation is | 5 Mb/s | 12 Mb/s | 2.5 Mb/s | 1.5 Mb/s | 1.5 Mb/s |
| THe high speed mode of operation of the USB was introduced by _ | ISA | USB 3.0 | USB 2.0 | ANSI | USB 2.0 |
| The sampling process in speaker output is a _____ process. | Asynchronous | Synchronous | Isochronous | noisy | Isochronous |
| The USB device follows _____ structure | List | Huffmann | Hash | Tree | Tree |
| The I/O devices form the _____ of the tree structure. | Leaves | Subordinate roots | Left sub trees | Right sub trees | Leaves |
| When the USB is connected to a system, its root hub is connected to | PCI BUS | SCSI BUS | Processor BUS | IDE | Processor BUS |

| | | | | | |
|---|---|---|---|---|---|
| the _____. | | | | | |
| The devices connected to USB is assigned an ____ adrress. | 9 bit | 4bit | 8 bit | 7 bit | 8 bit |
| A USB pipe is a _____ channel. | Simplex | Half-Duplex | Full-Duplex | Duplex | Full-Duplex |
| he transmission over the USB is divided into | Frames | Pages | Packets | Tokens | Frames |
| The _____ signal is used to indiacate the beginning of a new frame. | Start | SOF | BEG | UEG | SOF |
| The power specification of usb is | 5V | 10v | 20v | 13v | 5V |
| The first feild of any packet is | PID | ADDR | ENDP | CRC16 | PID |
| The last field in the packet is _ | PID | ADDR | ENDP | CRC | PID |
| The data packets can contain data upto | 512 bytes | 256 bytes | 1024 bytes | 2 KB | 1024 bytes |
| The serial communication is | cheaper communication | high cost | low data | low sensitivity | cheaper communication |
| The serial communication is used for | short distance communication | long distance communication | short and long distance communication | communication for a certain range of distanc | long distance communication |
| The number of bits transmitted or received | transmission rate | reception rate | transceiver rate | baud rate | baud rate |

| | | | | | |
|---|---|---|---|---|---|
| per second is defined as | | | | | |
| The task of converting the byte into serial form and transmitting it bit by bit along with start, stop and parity bits is carried out by | reception unit | serial communicatio n unit | transmission unit | reception unit | transmissi on unit |
| The common unit shared by the receiver unit and transmission unit of serial communicati on unit is | SCON(Serial Port Control) Register | Parallel buffer unit | 2 bit serial data interface | Parallel port | SCON(Se rial Port Control) Register |
| The common unit shared by the receiver unit and transmission unit of serial communicati on unit is | SBUF(Serial Buffer) register | Parallel buffer unit | 2 bit serial data interface | Parallel port | SBUF(Se rial Buffer) register |
| The common unit shared by the receiver unit and transmission unit of serial communicati on unit is | 8-bit serial data interface | Parallel buffer unit | 2 bit serial data interface | Parallel port | 8-bit serial data interface |
| During | receive buffer | receive buffer | receive buffer | receive buffer | receive |

| | | | | | |
|---|---|---|---|---|---|
| serial reception, the buffer that receives serial bits and converts to a byte is | 0 | 2 | 1 | 3 | buffer 1 |
| If SM0=1, SM1=0, then the transceiver selected is | 8-bit synchronous | 9-bit synchronous | 9-bit asynchronous | 8-bit asynchronous | 9-bit asynchronous |
| In mode 2, the baud rate depends only on | SMOD bit | SCON bit | oscillator clock frequency | SMOD bit and oscillator clock frequency | SMOD bit and oscillator clock frequency |
| The mode that offers the most secured parity enabled data communication at lower baud rates is | mode 2 | mode 0 | mode 1 | mode 3 | mode 2 |
| With what frequency UART operates( where f denoted the crystal frequency )? | f/12 | f/32 | f/144 | f/384 | f/384 |
| UART stands for: | Universal asynchronization receiver/transmitter | Universal asynchronous receiver/transmitter | United asynchronous receiver/transmitter | Universal automatic receiver/transmitter | Universal asynchronous receiver/transmitter |
| How is data detected in a UART? | counter | timer | clock | first bit | clock |
| Which of the signal is set to one, if no data is | READY | START | STOP | TXD | TXD |

| | | | | | |
|---|---|---|---|---|---|
| transmitted? | | | | | |
| What rate can define the timing in the UART? | bit rate | baud rate | speed rate | voltage rate | baud rate |
| How is baud rate supplied? | baud rate voltage | external timer | peripheral | internal timer | external timer |
| Which is the most commonly used UART? | 8253 | 8254 | 8259 | 8250 | 8250 |
| What does ADS indicate in 8250 UART? | address signal | address terminal signal | address strobe signal | address generating signal | address terminal signal |
| Which of the following signals are active low in the 8250 UART? | BAUDOUT | DDIS | INTR | MR | BAUDOUT |
| Which of the signal can control bus arbitration logic in 8250? | BAUDOUT | DDIS | INTR | MR | DDIS |
| Which of the following is used to reset the device in 8250? | BAUDOUT | DDIS | INTR | MR | MR |
| Which provides an input clock for the receiver part of the UART 8250? | BAUDOUT | DDIS | INTR | RCLK | RCLK |
| Which of the following can be used for long | I2C | parallel port | SPI | RS232 | RS232 |

| | | | | | |
|---|---|---|---|---|---|
| distance communication? | | | | | |
| Which of the following can affect the long distance communication? | clock | resistor | Capacitors | diodes | diodes |
| Which are the serial ports of the IBM PC? | COM1 | COM4 and COM4 | COM1 and COM2 | COM3 | COM1 and COM2 |
| Which of the following can provide hardware handshaking ? | RS232 | parallel port | counter | timer | RS232 |
| Which of the following have an asynchronous data transmission ? | I2C | parallel port | SPI | RS232 | RS232 |
| How many areas does the serial interface have? | 1 | 2 | 3 | 4 | 2 |
| The RS232 is also known as | UART | SPI | hysical interface | electrical interface | hysical interface |
| Which of the following is not a serial protocol? | I2C | parallel port | SPI | RS232 | RS232 |
| The _____ circuit enables the generation of the ASCII code when the key is | Generator | Debouncing | Encoder | Logger | Encoder |

| | | | | | |
|---|---|---|---|---|---|
| pressed. | | | | | |
| To overcome multiple signals being generated upon a single press of the button, we make use of _ | Generator circuit | Debouncing circuit | Encoder | Logger | Debouncing circuit |
| The disadvantage of using parallel mode of communication is _ | It is costly | Leads to erroneous data transfer | Security of data | low cost | It is costly |
| In a 32 bit processor, the A0 bit of the address line is connected to _____ of the parallel port interface. | Valid bit | Idle bit | Interrupt enable bit | Status or data register | Status or data register |
| In the output interface of the parallel port, along with the valid signal _____ is also sent. | Data | Idle signal | Interrupt | Acknowledge signal | Idle signal |
| DDR stands for, | Data Direction Register | Data Decoding Register | Data Decoding Rate | Data Diverting Register | Data Direction Register |
| In a general 8-bit parallel interface, the INTR line is connected to | Status and Control unit | Control unit | DDR | Register select | Status and Control unit |

| | | | | | |
|---|---|---|---|---|---|
| Programmable peripheral input-output port is other name for | serial input-output port | parallel input-output port | serial input port | parallel output port | parallel input-output port |
| Baud means? | The number of bits transmitted per unit time | The number of byted transmitted per unit time | The rate at which the signal changes | The rate at which will not signal changes | The rate at which the signal changes |
| Storage device that plug directly into a computer's USB port. | jump/flash/thumb drive | floppy | DVD | CKHVW | jump/flash/thumb drive |
| Parallel port can transfer ____ bits of data at a time: | 2 | 4 | 8 | 16 | 8 |
| Parallel Port can not connect: | Printers | Scanners | Telephones | Monitors | Monitors |
| Which is the fastest port for data transfer: | USB | Serial | Parallel | FireWire | FireWire |

## UNIT-V

## SYLLABUS

Introduction to CRO: Block Diagram of CRO. Applications of Oscilloscope: (1) Study of Waveform, (2) Measurement of Voltage, Current, Frequency and Phase Difference. Power Supply: Half-wave Rectifiers. Centre-tapped and Bridge Full-wave Rectifiers Calculation of Ripple Factor and Rectification Efficiency, Basic idea about capacitor filter, Zener Diode and Voltage Regulation Timer IC: IC 555 Pin diagram and its application as Astable and Monostable Multivibrator.

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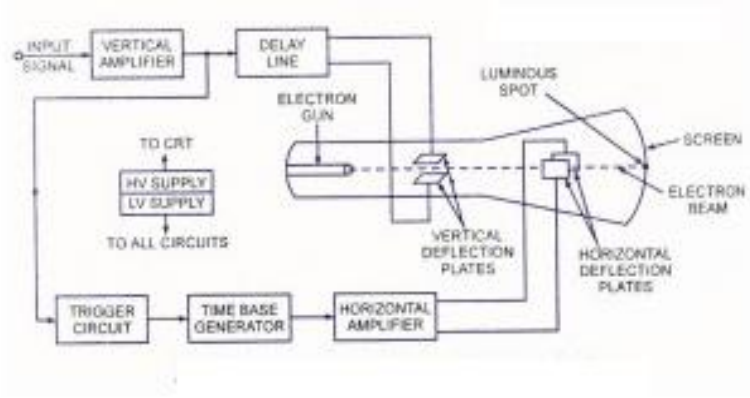
**Introduction to CRO:**

An Oscilloscope is an electronic device generally used to obtain the wave-form of different signals applied to it, which depicts the instantaneous values of an electrical parameter, an Oscilloscope on the other hand expands the time window for the observer to have a better picture regarding the properties of the signal applied to it.




It generates the electron beam, accelerates the beam to a high velocity, deflects the beam to create the image, and contains a phosphor screen where the electron beam eventually becomes visible. For accomplishing these tasks various electrical signals and voltages are required, which are provided by the power supply circuit of the oscilloscope. Low voltage supply is required for the heater of the electron gun for generation of electron beam and high voltage, of the order of few thousand volts, is required for cathode ray

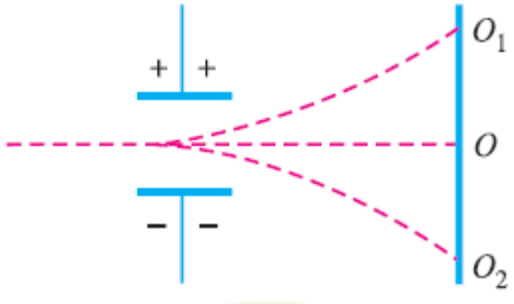
tube to accelerate the beam. Normal voltage supply, say a few hundred volts, is required for other control circuits of the oscilloscope.

Horizontal and vertical deflection plates are fitted between electron gun and screen to deflect the beam according to input signal. Electron beam strikes the screen and creates a visible spot. This spot is deflected on the screen in horizontal direction (X-axis) with constant time dependent rate. This is accomplished by a time base circuit provided in the oscilloscope. The signal to be viewed is supplied to the vertical deflection plates through the vertical amplifier, which raises the potential of the input signal to a level that will provide usable deflection of the electron beam. Now electron beam deflects in two directions, horizontal on X-axis and vertical on Y-axis. A triggering circuit is provided for synchronizing two types of deflections so that horizontal deflection starts at the same point of the input vertical signal each time it sweeps.

**Cathode Ray Tube**

When high velocity electron beam strikes the screen, a spot of light appears at the point of impact. The colour of the spot depends upon the nature of fluorescent material.As the cathode is heated, it produces a large number of electrons.These electrons pass through the control grid on their way to the screen.The control grid controls the amount of current flow as in standard vacuum tubes. If negative potential on the control grid is high, fewer electrons will pass through it. Hence the electron beam will produce a dim spot of light on striking the screen. Reverse will happen when the negative potential on the control grid is reduced.Therefore, the intensity of the light spot on the screen can be controlled by changing the negative potential on the control grid.

After leaving the control grid, the electron beam comes under the influence of focusing and accelerating anodes.Since, the two anodes are at high positive potential, therefore, they produce a field which acts as electrostatic lens to converge the electron beam at a point on the screen.After leaving the accelerating anode, the electron beam comes under the influence of vertical and horizontal deflection plates.When no voltage is applied to these deflection plates, the electron beam produces a spot of light at the centre as shown by point O in fig below on the screen.




If the voltage is applied to the vertical deflection plates only, the electron beam and so as the spot of light will be deflected upwards i.e. point O1. And if the potential on the plates is reversed, the spot of light will be deflected downwards i.e. point O2.

Similarly, the spot of light can be deflected horizontally by applying voltage across the horizontal deflection plates.The cathode ray tube or CRT is a vacuum tube of special geometrical shape which converts an electrical signal into a visual one.A CRT makes available a large number of electrons which are accelerated to high velocity and are brought to focus on a fluorescent screen where it produces a spot when strikes it. The electron beam is deflected during its journey in response to the applied electrical signal. As a result, the electrical signal waveform is displayed visually.

**Glass Envelope**

It is a conical highly evacuated glass housing which maintains vacuum inside it and supports various electrodes.The inner wall of CRT between the neck and screen are usually coated with a conducting material known as aquadag. This coating is electrically connected to the accelerating anode so that the electrons which accidentally strike the walls are returned to the anode. This prevents the walls from charging to a high negative potential.

**Electron Gun Assembly**

The electron gun assembly consists of an indirectly heated cathode, a control grid, a focusing anode and an accelerating anode and it is used to produce a focused beam of electrons. The control grid is held at negative potential w.r.t. cathode. However, the two anodes are held at high positive potential w.r.t. cathode. The cathode consists of a nickel cylinder coated with oxide coating and provides a large number of electrons. The control grid encloses the cathode and consists of a metal cylinder with a tiny circular opening to keep the electron beam small. By controlling the positive potential on it, the focusing anode focuses the electron beam into a sharp pin point. Due to the positive potential of about 10,000 V on the accelerating anode which is much larger than on the focusing diode, the electron beam is accelerated to a high velocity. In this way,

the electron gun assembly forms a narrow, accelerated electron beam which produces a spot of light when it strikes the screen.

**Deflection Plate Assembly**

It consists of two sets of deflecting plates within the tube beyond the accelerating anode and is used for the deflection of the beam. One set is called as vertical deflection plates and the other set is called horizontal deflection plates. The vertical deflection plates are mounted horizontally in the tube. On application of proper potential to these plates, the electron beam can be made to move up and down vertically on the screen. The horizontal deflection plates are mounted vertically in the tube. On application of proper potential to these plates, the electron beam can be made to move right and left horizontally on the screen.

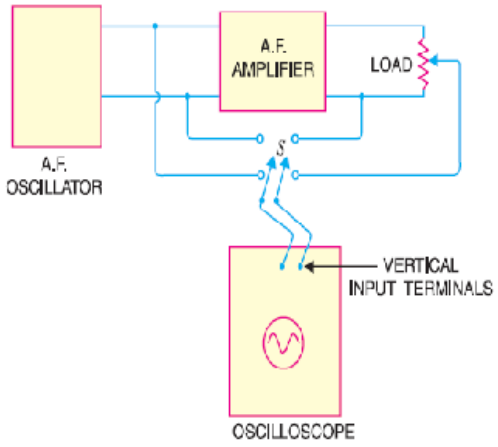
*Screen*

The screen is coated with some fluorescent materials such as zinc orthosilicate, zinc oxide etc and is the inside face of the tube.

**Applications of CRO**

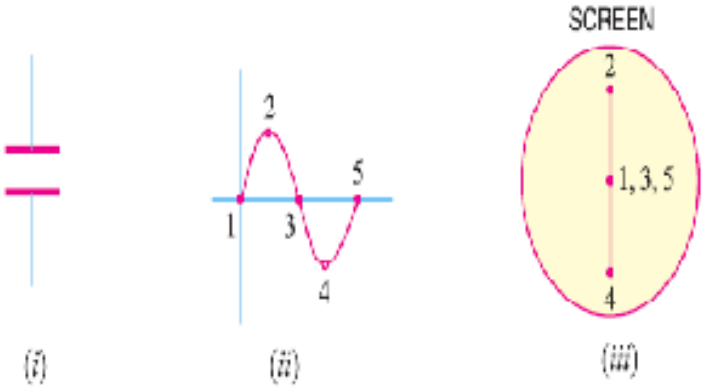
1) **Study of wave form**

One of the important application of CRO is to observe the wave shapes of voltages in various type of electronic circuits. To do this, the signal under study is applied to vertical input terminals i.e. the vertical deflection plates of the oscilloscope. The sweep circuit is set to internal so that saw tooth wave is applied to the horizontal input terminals i.e. the horizontal deflection plates. Then various controls are adjusted to get sharp and well defined signal waveform on the screen. Fig below shows the circuit for studying the performance of an audio frequency amplifier.

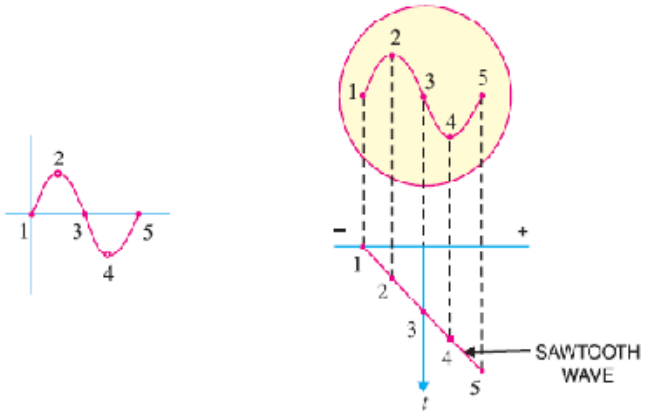



With the help of switch S, the output and input of amplifier is applied in turn to the vertical input terminals of the CRO . If the waveforms are identical in shape, the fidelity of the amplifier is excellent.

When a sinusoidal voltage is applied to the vertical deflection plates, it makes the plates alternately positive and negative. Thus, in the positive half cycle, upper plate is positive and lower plate is negative and in the negative half cycle, the plate polarities are reversed. As a result, the spot moves up and down at the same rate as the frequency of the applied voltage. Since the frequency of the applied voltage is 50 Hz, hence we will see a continuous vertical line 2-1-4 on the screen as shown in fig below. This line gives no indication of the manner in which the voltage is alternating hence we cannot get the wave shape.




When the signal voltage is applied to the vertical plates and saw-tooth wave to the horizontal plates, we get the exact pattern of the signal on the screen as shown in fig. below.




When the signal is at the instant 1, its amplitude is zero, and at this instant maximum negative voltage is applied to the horizontal plates. As a result the beam appears at extreme left on the screen as shown in fig.When the signal is at instant 2, its amplitude is maximum, but the negative voltage on the horizontal plates is decreased at this instant. Hence, the beam is deflected upwards by the signal and towards right by the saw tooth wave. As a result, the beam strikes the screen at 2. In a similar manner, the beam strikes the screen at 3,4 and 5 and we get the exact pattern of the signal on the screen.

**Voltage Measurement**

When the signal is applied to the vertical deflection plates only, a vertical line appears on the screen. The height of the line is proportional to the peak-to-peak voltage of the applied signal. To measure the voltage on CRO, the following steps are followed :

1. Shut off the internal horizontal sweep generator
2. Attach a tracing paper to the face of the oscilloscope. Mark off the paper with vertical and horizontal lines in the form of graph.
3. Now, calibrate the oscilloscope against a known voltage. Apply the known voltage to the vertical input terminals. Since, the sweep circuit is off, you will get a vertical line. Adjust the vertical gain till a good deflection is obtained. Let the deflection sensitivity is V volts/mm.
4. Keeping the vertical gain unchanged, apply the unknown voltage to be measured, to the vertical input terminals of the oscilloscope.
5. Measure the length of the vertical line obtained. Let it be l mm.
6. Now the unknown voltage = l×V volts.

**Frequency Measurement**

Using a CRO , the unknown frequency can be accurately determined following the below steps :

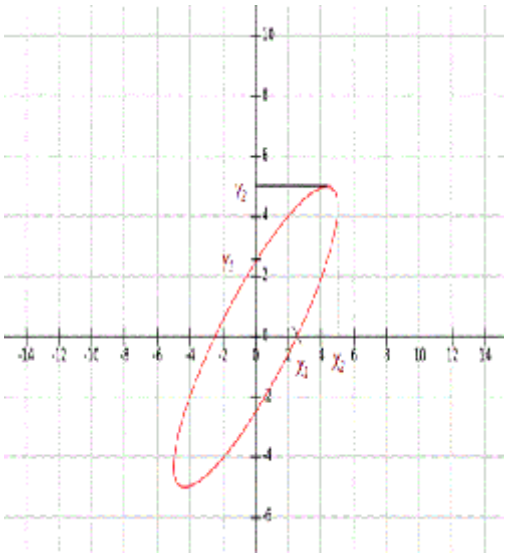
1. A known frequency is applied to the horizontal input and unknown frequency to the vertical input.
2. The various controls are adjusted.
3. A pattern with loops is obtained.
4. The number of loops cut by the horizontal line gives the frequency on the vertical plates($f_V$) and the number of loops cut by the vertical line gives the frequency on the horizontal plates($f_H$).

So,

$f_V / f_H$= No. of loops cut by the horizontal line/No. of loops cut by the vertical line

**Calculation of the phase difference between two Sinusoidal Signals having same frequency**

When two sinusoidal signals of same frequency and magnitude are applied two both pairs of deflecting plates of CRO, the Lissajous pattern changes with change of phase difference between signals applied to the CRO.



There are two cases to determine the phase difference ø between two signals applied to the horizontal & vertical plates,

In this condition the phase difference will be,

$$\emptyset = sin^{-1}\left(\frac{x_1}{x_2}\right) = sin^{-1}\left(\frac{y_1}{y_2}\right)$$

Another possibility of phase difference,

$$\emptyset' = 360^0 - \emptyset$$

From Above given Lissajous pattern

$$x_1 = 2.25 \;\&\; x_2 = 4.5$$

$$\text{Hence, } \emptyset = sin^{-1}\left(\frac{x_1}{x_2}\right) = sin^{-1}\left(\frac{2.25}{4.5}\right) = 30^0$$

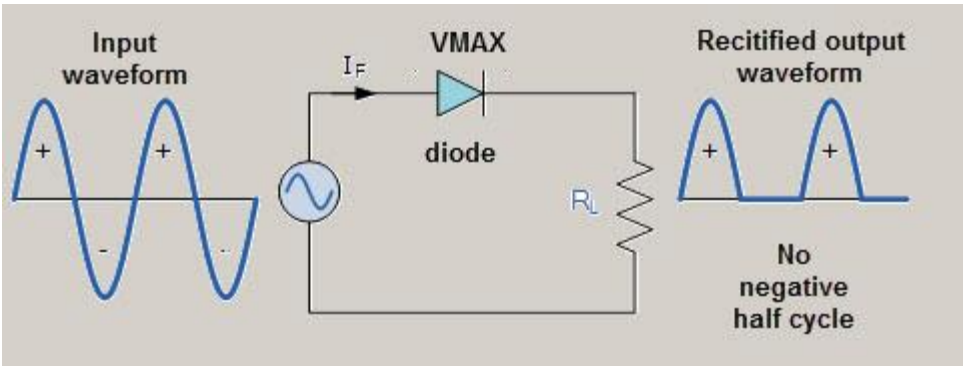
Another Possibility of Phase Difference,

$$\emptyset' = 360^0 - \emptyset = 360^0 - 30^0 = 330^0$$

**POWER SUPPLY:**

**Half wave rectification:**

Rectifier is an electronic device which coverts the alternating current to unidirectional current, in other words rectifier converts the AC voltage to DC voltage.




Average output Voltage($V_{DC}$): Measure of DC content in the output Voltage. Consider above output wave form of HWR with $V_m$ as output peak voltage and period is 0 to 2∏.

**Working of Half Wave Rectifier**

During the positive half cycle the diode is under forward bias condition and it conducts current to RL (Load resistance). A voltage is developed across the load, which is same as the input AC signal of the positive half cycle.

Alternatively, during the negative half cycle the diode is under reverse bias condition and there is no current flow through the diode. Only the AC input voltage appears across the load and it is the net result which is possible during the positive half cycle. The output voltage pulsates the DC voltage.

During the positive half cycle, when the secondary winding of the upper end is positive with respect to the lower end, the diode is under forward bias condition and it conducts current. During the positive half cycles, the input voltage is applied directly to the load resistance when the forward resistance of the diode is assumed to be zero. The wave forms of output voltage and output current are same as that of the AC input voltage.

During the negative half cycle, when the secondary winding of the lower end is positive with respect to the upper end, the diode is under reverse bias condition and it does not conduct current. During the negative half cycle, the voltage and current across the load remains zero. The magnitude of the reverse current is very small and it is neglected. So, no power is delivered during the negative half cycle.

A series of positive half cycles is the output voltage that is developed across the load resistance. The output is a pulsating DC wave and to make the smooth output wave filters, which should be across the load, are used. If the input wave is of half cycle, then it is known as a half wave rectifier.

**Regulation**

Regulation is the difference between no-load voltage to full-load voltage with respect to the full-load voltage, and the percentage voltage regulation is given as

$$\%\text{Regulation} = \{(V_{\text{no-load}} - V_{\text{full-load}}) / V_{\text{full-load}}\} * 100$$

**Peak Inverse Voltage (PIV)**

It is the maximum voltage that the rectifying diode has to withstand, during the reverse biased period. When the diode is reverse biased, during the negative half cycle, there will be no current flow through the load resistor RL. Hence, there will be no voltage drop through the load resistance RL which causes the entire input voltage to appear across the diode. Thus $V_{SMAX}$, the peak secondary voltage, appears across the diode. Therefore, Peak Inverse Voltage (PIV) of half wave rectifier = $V_{SMAX}$

**Efficiency:** The efficiency is defined as the ratio of input AC to the output DC.

$$\text{Efficiency, } \eta = P_{dc} / P_{ac}$$

DC power delivered to the load, $P_{dc} = I^2_{dc} R_L = ( I_{max/pi} )^2 R_L$

AC power input to the transformer, $P_{ac}$ = Power dissipated in junction of diode + Power dissipated in load resistance $R_L$

$$= I^2_{rms} R_F + I^2_{rms} R_L = \{I^2_{MAX}/4\}[R_F + R_L]$$

$$\text{Rectification Efficiency, } \eta = P_{dc} / P_{ac} = \{4/ ^2\}[RL/ (R_F + R_L)] = 0.406/\{1+ R_{F/RL} \}$$

If $R_F$ is neglected, the efficiency of half wave rectifier is 40.6%.

**Ripple factor**: It is defined as the amount of AC content in the output DC. It nothing but amount of AC noise in the output DC. Less the ripple factor, performance of the rectifier is more. The ripple factor of half wave rectifier is about 1.21 (full wave rectifier has about 0.48). It can be calculated as follows:

The effective value of the load current I is given as sum of the rms values of harmonic currents I1, I2, I3, I4 and DC current Idc.

$$I^2 = I^2_{dc} + I^2_1 + I^2_2 + I^2_4 = I^2_{dc} + I^2_{ac}$$

$$\text{Ripple factor, is given as } \gamma = I_{ac} / I_{dc} = (I^2 - I^2_{dc}) / I_{dc} = \{( I_{rms} / I_{dc}^2)-1\} = K_f^2 - 1)$$

Where Kf is the form factor of the input voltage. Form factor is given as

$$K_f = I_{rms} / I_{avg} = (I_{max}/_2)/ (I_{max}/pi) = pi/2 = 1.57$$

$$\text{So, ripple factor, } \gamma = (1.57^2 - 1) = 1.21$$

**FULL WAVE RECTIFIER**

Center **Tapped** Full Wave Rectifier Working:

The primary winding of the center tap transformer is applied with the Ac voltage. Thus the two diodes connected to the secondary of the transformer conducts alternatively. For the positive half cycle of the input diode D1 is connected to the positive terminal and D2 is connected to the negative terminal. Thus diode D1 is in forward bias and the diode D2 is reverse biased. Only diode D1 starts conducting and thus current flows from diode and it appears across the load RL. So positive cycle of the input is appeared at the load.

During the negative half cycle the diode D2 is applied with the positive cycle. D2 starts conducting as it is in forward bias. The diode D1 is in reverse bias and this does not conduct. Thus current flows from diode D2 and hence negative cycle is also rectified, it appears at the load resistor RL.

By comparing the current flow through load resistance in the positive and negative half cycles, it can be concluded that the direction of the current flow is same. Thus the frequency of rectified output voltage is two times the input frequency. The output that is rectified is not pure, it consists of a dc component and a lot of ac components of very low amplitudes.

Peak Inverse Voltage (PIV) of Centre Tap Full Wave Rectifier:

PIV is defined as the maximum possible voltage across a diode during its reverse bias. During the first half that is positive half of the input, the diode D1 is forward bias and thus conducts providing no resistance at all. Thus, the total voltage Vs appears in the upper-half of the ac supply, provided to the load resistance R. Similarly, in the case of diode D2 for the lower half of the transformer total secondary voltage developed appears at the load. The amount of voltage that drops across the two diodes in reverse bias is given as

$$\text{PIV of D2} = Vm + Vm = 2Vm$$

$$\text{PIV of D1} = 2Vm$$

Vm is the voltage developed across upper and lower halves.

Peak Inverse Voltage (PIV) of Centre Tap Full Wave Rectifier:

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$$\text{PIV of D1} = 2Vm$$

Vm is the voltage developed across upper and lower halves.

**RIPPLE FACTOR**

The pulsating output of a rectifier can be considered to contain a dc component and ac component called the ripples. The ripple current is undesirable and its value should be the smallest possible in order to make the rectifier effective.

The ripple voltage or current is measured in turn of the ripple factor which is defined as the ratio of the effective value of the ac components of voltage (or current) present in the output from the rectified to the direct or average value of the output voltage (or current)

The effective value of the load current is given as

$$I^2 = I_{dc}^2 + I_1^2 + I_2^2 + I_4^2 + \ldots\ldots = I_{dc}^2 + I_{ac}^2$$

Where $I_1$, $I_2$, $I_4$ etc. are the rms values of fundamental, second, fourth etc. harmonics and $I_{ac}^2$ is the sum of the square of the rms Value of the ac components.

$$\text{So ripple factor, } \gamma = I_{ac}/I_{dc} = \sqrt{\{(I^2 + I_{dc}^2)/I_{dc}\}} = \sqrt{[\{I_{rms}/I_{dc}\}^2 - 1]} = \sqrt{(K_f^2 - 1)}$$

Where $K_f$ is the form factor of the input voltage. For half-wave rectifier, from factor is given as

$$K_f = I_{rms} / I_{av} = (I_{max}/\sqrt{2})/(2I_{max}/\pi) = \pi/2\sqrt{2} = 1.11$$

Now, Ripple factor is given as

$$\gamma = \sqrt{(K_f^2 - 1)} = \sqrt{(1.11^2 - 1)} = 0.482$$

**Efficiency :**The efficiency of a full wave rectifier is defined as the ratio of DC power output to the applied input AC power. Therefore, it is given as;

$\eta$ = DC Power Output / AC power input

**BRIDGE FULL WAVE RECTIFIER**

A bridge rectifier is a type of full wave rectifier which uses four or more diodes in a bridge circuit configuration to efficiently convert the Alternating Current (AC) into Direct Current (DC).

**Bridge rectifier construction**

The construction diagram of a bridge rectifier is shown in the below figure. The bridge rectifier is made up of four diodes namely $D_1$, $D_2$, $D_3$, $D_4$ and load resistor $R_L$. The four diodes are connected in a closed loop (Bridge) configuration to efficiently convert the Alternating Current (AC) into Direct Current (DC). The main advantage of this bridge circuit configuration is that we do not require an expensive center tapped transformer, thereby reducing its cost and size.

The input AC signal is applied across two terminals A and B and the output DC signal is obtained across the load resistor $R_L$ which is connected between the terminals C and D.The four diodes $D_1$, $D_2$, $D_3$, $D_4$ are arranged in series with only two diodes allowing electric current during each half cycle. For example, diodes $D_1$ and $D_3$ are considered as one pair which allows electric current during the positive half cycle whereas diodes $D_2$ and $D_4$ are considered as another pair which allows electric current during the negative half cycle of the input AC signal.

When input AC signal is applied across the bridge rectifier, during the positive half cycle diodes $D_1$ and $D_3$ are forward biased and allows electric current while the diodes $D_2$ and $D_4$ are reverse biased and blocks electric current. On the other hand, during the negative half cycle diodes $D_2$ and $D_4$ are forward biased and allows electric current while diodes $D_1$ and $D_3$ are reverse biased and blocks electric current.

During the positive half cycle, the terminal A becomes positive while the terminal B becomes negative. This causes the diodes $D_1$and $D_3$ forward biased and at the same time, it causes the diodes $D_2$ and $D_4$ reverse biased.The current flow direction during the positive half cycle is shown in the figure A (I.e. A to D to C to B).

During the negative half cycle, the terminal B becomes positive while the terminal A becomes negative. This causes the diodes $D_2$and $D_4$ forward biased and at the same time, it causes the diodes $D_1$ and $D_3$ reverse biased.

The current flow direction during negative half cycle is shown in the figure B (I.e. B to D to C to A).

From the above two figures (A and B), we can observe that the direction of current flow across load resistor $R_L$ is same during the positive half cycle and negative half cycle. Therefore, the polarity of the output DC signal is same for both positive and negative half cycles. The output DC signal polarity may be either completely positive or negative. In our case, it is completely positive. If the direction of diodes is reversed then we get a complete negative DC voltage. Thus, a bridge rectifier allows electric current during both positive and negative half cycles of the input AC signal.

**Ripple factor**

The smoothness of the output DC signal is measured by using a factor known as ripple factor. The output DC signal with very fewer ripples is considered as the smooth DC signal while the output DC signal with high ripples is considered as the high pulsating DC signal.

Ripple factor is mathematically defined as the ratio of ripple voltage to the pure DC voltage.

The ripple factor for a bridge rectifier is given by

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

The ripple factor of the bridge rectifier is 0.48 which is same as the center tapped full wave rectifier.

**Rectifier efficiency**

The rectifier efficiency determines how efficiently the rectifier converts Alternating Current (AC) into Direct Current (DC).

High rectifier efficiency indicates a most reliable rectifier while the low rectifier efficiency indicates a poor rectifier.

Rectifier efficiency is defined as the ratio of the DC output power to the AC input power.

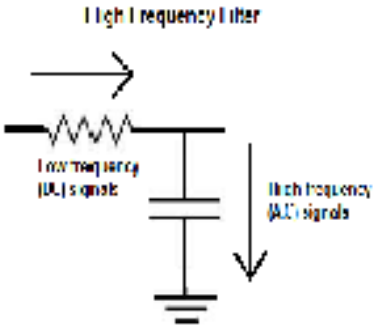
$$\eta = \frac{\text{DC output power}}{\text{AC input power}} = \frac{P_{DC}}{P_{AC}}$$

The maximum rectifier efficiency of a bridge rectifier is 81.2% which is same as the center tapped full wave rectifier.

**CAPACITOR FILTER**

A filter capacitor is a capacitor which filters out a certain frequency or range of frequencies from a circuit.

**Filter Capacitor Circuit To Block DC and Pass AC**



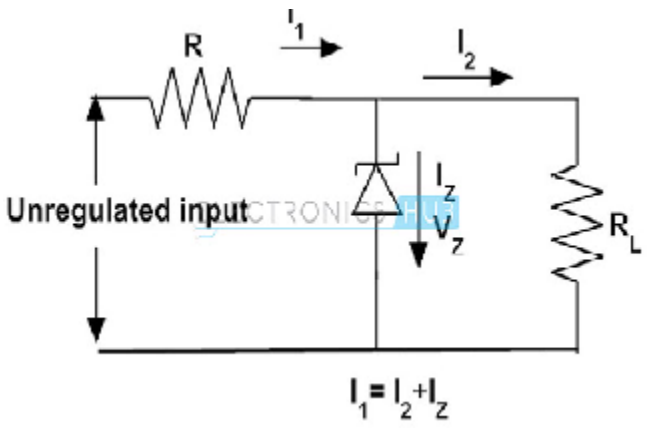

Being that capacitors have offer very high resistance to low frequency signals and low resistance to high frequency signals, it acts as a high pass filter, which is a filter which passes high frequency signals and blocks low frequency signals.

This capacitor, when placed across a rectifier gets charged and stores the charged energy during the conduction period. When the rectifier is not conducting, this energy charged by the capacitor is delivered back to the load. Through this energy storage and delivery process, the time duration during which the current flows through the load resistor gets increased and the ripples are decreased by a great amount. Thus for the ripple component with a frequency of 'f' megahertz, the capacitor 'C' will offer a very low impedance. Thus the dc components of the input signal along with the few residual ripple components, is only allowed to go through the load resistance R Load. The high amount of ripple components of current gets bypassed through the capacitor C.

**ZENER DIODE AND VOLTAGE REGULATION**

Zener diode is a special purpose p-n junction diode, which operates under reverse biased condition. It is used to regulate voltages in a d.c. circuit. The primary objective of the zener diode is to maintain a constant voltage.

There is a series resistor connected to the circuit in order to limit the current into the diode. It is connected to the positive terminal of the d.c. Supply such that it is reverse biased and can also work in breakdown condition. Zener Diodes have a sharp reverse breakdown voltage and breakdown voltage will be constant for a wide range of currents. Thus we will connect the zener diode parallel to the load such that the applied voltage will reverse bias it. Thus if the reverse bias voltage across the zener diode exceeds the knee voltage, the voltage across the load will be constant.




The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_Z$(min) value in the reverse breakdown region. It permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the Zener voltage. The Zener diode specially made to have a reverse voltage breakdown at a specific voltage. Its characteristics are otherwise very similar to common diodes. In breakdown the voltage across the Zener diode is close to constant over a wide range of currents thus making it useful as a shunt voltage regulator.

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current. The resistor is selected so that when the input voltage is at $V_{IN}$(min) and the load current is at $I_L$(max) that the current through the Zener diode is at least $I_z$(min). Then for all other combinations of input voltage and load current the Zener diode conducts

the excess current thus maintaining a constant voltage across the load. The Zener conducts the least current when the load current is the highest and it conducts the most current when the load current is the lowest.

If there is no load resistance, shunt regulators can be used to dissipate total power through the series resistance and the Zener diode. Shunt regulators have an inherent current limiting advantage under load fault conditions because the series resistor limits excess current.

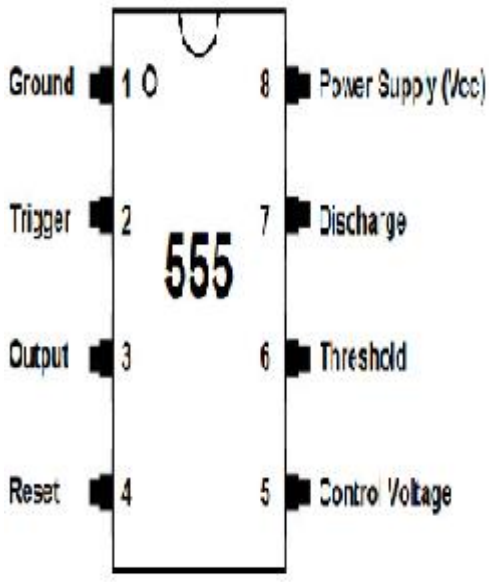
A Zener diode of break down voltage $V_z$ is reverse connected to an input voltage source $V_i$ across a load resistance $R_L$ and a series resistor $R_S$. The voltage across the zener will remain steady at its break down voltage $V_Z$ for all the values of zener current $I_Z$ as long as the current remains in the break down region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across $R_L$, whenever the input voltage remains within a minimum and maximum voltage.

**Basically there are two type of regulations such as**:

a. **Line Regulation:** In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.
b. **Load Regulation:** In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

**TIMER IC -555**

**PIN DIAGRAM**



**GND Pin**

Pin-1 is a GND pin which is used to supply a zero voltage to the IC.

**Trigger Pin**

Pin-2 is a trigger pin which is used to convert the FF from set to RST (reset). The output of the timer depends on the amplitude of the external trigger pulse that is applied to the trigger pin.

**Output Pin**

Pin-3 is an output pin.

**Reset Pin**

Pin-4 is a RST pin. When the negative pulse is applied to this pin to disable or reset, and false triggering can be neglected by connecting to VCC.

**Control Voltage Pin**

Pin-5 is the control voltage pin used to control the pulse width of the output waveform and also the levels of threshold and trigger. When an external voltage is applied to this pin, then the output waveform will be modulated

**Threshold Pin**

Pin-6 is the threshold pin, when the voltage is applied to threshold pin, then it contrasts with a reference voltage. The set state of the FF can be depends on the amplitude of this pin.

**Discharge Pin**

Pin-7 is the discharge pin, when the output of the open collector discharges a capacitor between the intervals, then it toggles the output from high to low.

**Supply Terminal**

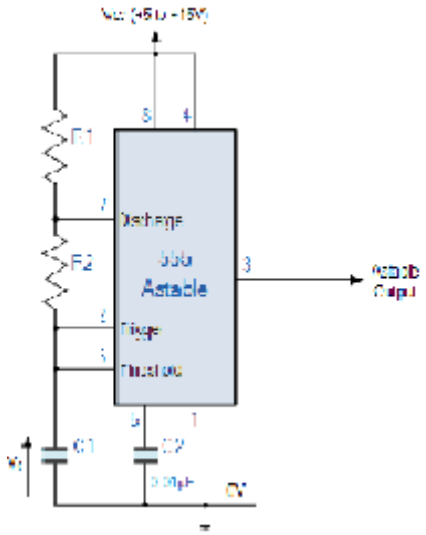
Pin-8 is the voltage supply pin which is used to supply the voltage to the IC with respect to the ground terminal.

**Operating Modes of 555 Timer IC**

The operating modes of a 555 timer are astable, and monostable.

**ASTABLE MULTIVIBRATOR**

Astable multivibrator is also called as Free Running Multivibrator. It has no stable states and continuously switches between the two states without application of any external trigger.




In the 555 Oscillator circuit above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the discharge terminal, pin 7.

Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the 0.693(R1+R2)C combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the0.693(R2.C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc – 1.5V and whose output “ON” and “OFF” time periods are determined by the capacitor and resistors combinations. The individual times required to complete one charge and discharge cycle of the output is therefore given as:

$$T1= 0.693(R1+R2)C$$

And

$$T2 =0.693xR2xC$$

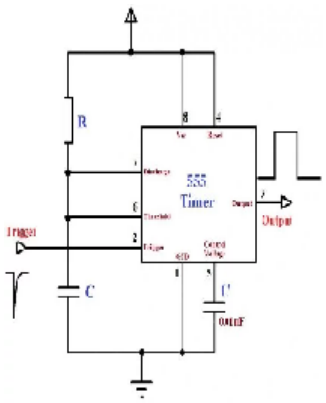
$$T = T1+T2 = 0.693(R1+2R2)$$

$$F=1/T = 1.44/(R1+2R2)C$$

## MONOSTABLE MULTIVIBRATOR

A monostable multivibrator (MMV) often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable).

### Working




Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor- C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 $V_{CC}$, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward +$V_{CC}$ through resistance $R_A$ with a time constant equal to $R_AC$. When the increasing capacitor voltage becomes slightly greater than +2/3 $V_{CC}$, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure.

Thus the output returns back to stable state from quasi-stable state. The output of the Monostable Multivibrator remains low until a trigger pulse is again applied. Then the cycle repeats.

The time during which the timer output remains high is given as

$$t_p = 1.0986 R_A C$$

where $R_A$ is in ohms and C is in farads.

## POSSIBLE QUESTIONS

**PART-A (2 Marks)**

**1.**Define rectification.

2. What is called half wave rectifier?

3. What is called full wave rectifier?

4. What are the applications of CRO?

5.What called multivibrator?

6.Define ripple factor.

7. Define efficiency of rectifier.

8.What are the difference between astable and monostable multivibrator.

9. Draw the pin diagram of IC555.

10.What do you mean by UTP and LTP?

**PART-C (6Marks)**

1. Explain the working principle of CRO with the help of diagram
2. Explain the working principle of centre tapped rectifier and calculate its efficiency and ripple factor
3. Explain the working principle of 555 timer with the help of diagram
4. Explain the working principle of bridge tapped rectifier and calculate its efficiency and ripple factor
5. Explain working principle of Astable multivibrator using IC 555
6. Explain the working principle of half wave rectifier and calculate its efficiency and ripple factor
7. Define voltage regulation. Explain the working principle of zener diode as a voltage regulator
8. Explain working principle of Mono stable multivibrator using IC 555
9. Discuss different applications of cathode ray oscilloscope.
10. Write short note on Astable and monostable multivibrator.

| KARPAGAM ACADEMY OF HIGHER EDUCATION,COIMBATORE-21 | | | | | |
|---|---|---|---|---|---|
| DEPARTMENT OF PHYSICS | | | | | |
| II B.Sc., PHYSICS (2017-2020) | | | | | |
| PHYSICS OF DEVICES AND COMMUNICATION (17PHU302 ) | | | | | |
| UNIT - V | | | | | |
| | **Option-1** | **Option-2** | **Option-3** | **Option-4** | **Key** |
| A Zener diode utilises …… characteristic for voltage regulation | Forward | Reverse | No baising | zer biasing | Reverse |
| Which of the following might not be needed in a power supply? | The transformer | The filter. | The rectifier. | amplifier | amplifier |
| The part of a power supply immediately preceding the regulator is: | The transformer | The filter. | The rectifier. | ac input | The filter. |
| Which of the following would make the best filter for a power supply? | A capacitor in series. | A choke in series. | A capacitor in series and a choke in parallel. | A capacitor in parallel and a choke in series. | A capacitor in series and a choke in parallel. |
| If you needed exceptionally good ripple filtering for a power supply, the best approach would be to: | Connect several capacitors in parallel. | Use a choke-input filter | Connect several chokes in series. | Use two capacitor/choke sections one after the other. | Use two capacitor/choke sections one after the other. |
| To service a power supply with which you are not completely familiar, you should: | Install bleeder resistors. | Use proper fusing. | Leave it alone and have a professional work on it. | Use a voltage regulator. | Leave it alone and have a professional work on it. |
| A current surge takes place when a power supply is first turned on because | The transformer core is suddenly magnetized | The diodes suddenly start to conduct | The filter capacitor(s) must be initially charged. | Arcing takes place in the power switc | The filter capacitor(s) must be initially charged. |

| | | | | | |
|---|---|---|---|---|---|
| | . | | | | |
| In. a supply designed to provide high power at low voltage, the best rectifier design would probably be: | Half-wave. | Full-wave, center-tap. | Bridge. | Voltage multiplier. | Full-wave, center-tap. |
| In an unregulated power supply, if input a.c. voltage increases, the output voltage | remains the same | increases | decreases | zero | increases |
| A power supply which has voltage regulation of …….. is unregulated power supply | 0% | 5% | 10% | 8% | 10% |
| Commercial power supplies have voltage regulation | of 10% | of 15% | of 25% | within 1% | within 1% |
| An ideal regulated power supply is one which has voltage regulation of | 0% | 5% | 10% | 8% | 0% |
| CRO gives the visual representation of time varying signals. The display of the signal is | One dimensional | Two dimensional | Three dimensional | Four dimensional | Two dimensional |
| Principally CRO is a | Ammeter | Voltmeter | Wattmeter | Watt-hour meter | Voltmeter |
| Which part is called as heart of CRO? | CRT | . Sweep generator | Trigger circuit | Amplifier | CRT |
| The light emitted by the zinc silicate coated | Green colour | Yellow colour | Blue colour | . White colour | Green colour |

| | | | | | |
|---|---|---|---|---|---|
| fluorescent screen of cathode ray tube is usually of | | | | | |
| If the bombardment of electrons ceases i.e. when the signal becomes zero then the light emitted by the screen will | Disappear immediatel y | . Persist for some time then it will disappear | Will not disappear at all | exist | . Persist for some time then it will disappear |
| In terms of the division on screen, the voltage of the waveform in CRO is | Average voltage | RMS voltage | Peak to peak voltage | Maximum voltage | Peak to peak voltage |
| If the two input waveforms f equal amplitude and 90 degree phase difference is applied to the CRO then the Lissajous patterns obtained will be | Straight line tilted at 45 degree with respect to X-axis | Circle | Ellipse | Vertical straight line | Circle |
| Number of electrons from grid reaching screen determines the | brightnes s level | sound quality | picture quality | noise reduction | brightness level |
| In C.R.O, grid is connected to the | positive potential | negative potential | AC source | DC source | negative potential |
| Material which gives light as a result of bombardment of fast moving electrons is | Carbon | Graphene | Potassium | Phosphorus | Phosphorus |
| The pin 7th of IC 555 timer is used as_____ | Output | Trigger | Discharge | threshold | Discharge |

| | | | | | |
|---|---|---|---|---|---|
| Monostable multivibrator is used in the application of___ | 555 timer | 556 timer | Op-amp | Ic741 | 555 timer |
| A monostable 555 timer has the following number of stable states: | 0 | 1 | 2 | 3 | 1 |
| An astable 555 timer has the following number of stable states: | 0 | 1 | 2 | 3 | 0 |
| Which mode of operation is being used when a 555 timer chip has two external resistors and an external capacitor? | monostable | pulse stretching | Schmitt triggering | astable | astable |
| 555 Timer is used for the application of ____ | Amplifier | Burglar alarm | Transformer | Charging | Burglar alarm |
| What is the function of the comparators in the 555 timer circuit | to compare the output voltages to the internal voltage divider | to compare the input voltages to the internal voltage divider | to compare the output voltages to the external voltage divider | to compare the input voltages to the external voltage divider | to compare the input voltages to the internal voltage divider |
| The bias voltage applied to the lower comparator of IC 555 timer is_____ | Vcc | 1/3Vcc | 2/3Vcc | 1/2Vcc | 1/3Vcc |
| The bias voltage applied to the upper comparator of IC 555 timer is_____ | Vcc | 1/3Vcc | 2/3Vcc | 1/2Vcc | 2/3Vcc |
| In cathode ray oscilloscope, spots are formed on screen having | anode | cathode | grid | matrix | grid |

| | | | | | |
|---|---|---|---|---|---|
| Cathode ray oscilloscope displays graph of waveforms based on | current | voltage | potential difference | temperature | voltage |
| Output of sweep and time base generator will be | sinusoidal waveform | cos waveform | saw tooth waveform | square wave | saw tooth waveform |
| Electronic device named as cathode ray oscilloscope is known as | graph plotting device | plotting device | printing device | writing device | graph plotting device |
| A Zener diode is used as a …… voltage regulating device | Shunt | Series | Series-shunt | series-series | Shunt |
| For increasing the voltage rating, zeners are connected in | Parallel | Series-parallel | Series | Shunt | Series |
| In a Zener voltage regulator, the changes in load current produce changes in … | Zener current | Zener voltage | Zener voltage as well as Zener current | diode voltage | Zener current |
| A Zener voltage regulator is used for …… load currents | High | Very high | Moderate | Small | Small |
| A Zener voltage regulator will cease to act as a voltage regulator if Zener current becomes | Less than load current | Zero | More than load current | one | Zero |
| A Zener regulator …… in the power supply | Increases the ripple | Decreases the ripple | Neither increases nor decreases the ripple | Data insufficient | Decreases the ripple |
| A 555 timer in monostable application mode can be used for | Pulse position modulation | Frequency shift keying | Speed control and measurement | Digital phase detector | Speed control and measurement |

| | | | | | |
|---|---|---|---|---|---|
| In an unregulated power supply, if load current increases, the output voltage | Remains the same | Decreases | Increases | zero | Decreases |
| In an unregulated power supply, if input a.c. voltage increases, the output voltage | Remains the same | Decreases | Increases | zero | Remains the same |
| A power supply which has voltage regulation of …….. is unregulated power supply | 0% | 5% | 10% | 8% | 10% |
| An ideal regulated power supply is one which has voltage regulation of | 0% | 5% | 10% | 8% | 0% |
| What is true about the breakdown voltage in a Zener diode? | It decreases when load current increases | It destroys the diode | It equals current times the resistance | It is approximately constant | It is approximately constant |
| The load voltage is approximately constant when a Zener diode is | Forward biased | Unbiased | Reverse biased | Operating in the breakdown region | Operating in the breakdown region |
| The PIV rating of each diode in a bridge rectifier is …….. that of the equivalent centretap rectifier. | one-half | the same as | twice | four times | one-half |
| For the same secondary voltage, the output voltage from a centre-tap rectifier is …….. | one-half | the same as | twice | four times | one-half |

| | | | | | |
|---|---|---|---|---|---|
| than that of bridge rectifier. | | | | | |
| The maximum efficiency of a half-wave rectifier is …….. | 40.60% | 81.20% | 50% | 25% | 40.60% |
| There is no need of transformer in | half-wave rectifier | Full-wave, | center-tap. | diode | center-tap. |
| The ripple factor of a half-wave rectifier is | 2 | 1.21 | 2.5 | 0.48 | 0.48 |
| A 10 V power supply would use ……. as filter capacitor. | paper capacitor | mica capacitor | electrolytic capacitor | air capacitor | electrolytic capacitor |
| A 1,000 V power supply would use …….. as a filter capacitor | paper capacitor | mica capacitor | electrolytic capacitor | air capacitor | paper capacitor |
| In a CRO which of the following is not a part of electron gun | cathode | grid | accelerating anode | X - Y plates | X - Y plates |
| An oscilloscope cannot be used to indicate | Frequency | Peak signal voltage | Energy | Wave shape | Wave shape |
| In a dual trace oscilloscope, the display appears segmented when | Low frequency signals are observed in Alternate mode | Low frequency signals are observed in Chop mode | High frequency signals are observed in Alternate mode | High frequency signals are observed in Chop mode | High frequency signals are observed in Chop mode |
| What does the discharge transistor do in the 555 timer circuit? | charge the external capacitor to stop the timing | charge the external capacitor to start the timing over again | discharge the external capacitor to stop the timing | discharge the external capacitor to start the timing over again | discharge the external capacitor to start the timing over again |
| The monostable | its output | it requires a | it requires a | the circuit | it requires a |

| | | | | | |
|---|---|---|---|---|---|
| multivibrator circuit is not an oscillator because | switches between two states | trigger to obtain an output signal | sine wave input signal | does not require a dc power supply | trigger to obtain an output signal |
| Determine the time period of a monostable 555 multivibrator. | T= 0.33RC | T= 1.1RC | T= 3RC | T= RC | T= 1.1RC |