KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University)
(Established Under Section 3 of UGC Act 1956)
Coimbatore - 641021.
(For the candidates admitted from 2017 onwards)

DEPARTMENT OF PHYSICS

SUBJECT :DIGITAL, ANALOG CIRCUITS AND INSTRUMENTATION

SEMESTER : V

SUBJECT CODE: 16PHU503A CLASS : III B.Sc.PHYSICS

OBJECTIVE

The aim of this paper is to give information about different digital and analog circuits, and their uses.

UNIT-I: Digital Circuits

Difference between Analog and Digital Circuits. Binary Numbers. Decimal to Binary and Binary to Decimal Conversion, AND, OR and NOT Gates (Realization using Diodes and Transistor). NAND and NOR Gates as Universal Gates. XOR and XNOR Gates.

De Morgan's Theorems. Boolean Laws. Simplification of Logic Circuit using Boolean Algebra. Fundamental Products. Minterms and Maxterms. Conversion of a Truth Table into an Equivalent Logic Circuit by (1) Sum of Products Method and (2) Karnaugh Map.

Binary Addition. Binary Subtraction using 2's Complement Method). Half Adders and Full Adders and Subtractors, 4-bit binary Adder-Subtractor.

UNIT-II: Semiconductor Devices and Amplifiers:

Semiconductor Diodes: P and N type semiconductors. Barrier Formation in PN Junction Diode. Qualitative Idea of Current Flow Mechanism in Forward and Reverse Biased Diode. PN junction and its characteristics. Static and Dynamic Resistance. Principle and structure of (1) LEDs, (2) Photodiode, (3) Solar Cell. Bipolar Junction transistors: n-p-n and p-n-p Transistors.

UNIT III

Characteristics of CB, CE and CC Configurations. Active, Cutoff & Saturation regions Current gains α and β. Relations between α and β. Load Line analysis of Transistors. DC Load line & Q-point. Voltage Divider Bias Circuit for CE Amplifier. h-parameter Equivalent Circuit. Analysis of single-stage CE amplifier using hybrid Model. Input & output Impedance. Current, Voltage and Power gains. Class A, B & C Amplifiers

UNIT-IV Operational Amplifiers (Black Box approach):

Characteristics of an Ideal and Practical Op-Amp (IC 741), Open-loop and closed-loop Gain. CMRR, concept of Virtual ground. Applications of Op-Amps: Inverting and non-inverting Amplifiers, Adder, Subtractor, Differentiator, Integrator, Zero crossing detector.

Sinusoidal Oscillators: Barkhausen's Criterion for Self-sustained Oscillations. Determination of

Frequency of RC Oscillator

UNIT-V: Instrumentations: Introduction to CRO: Block Diagram of CRO. Applications of CRO: (1) Study of Waveform, (2) Measurement of Voltage, Current, Frequency, and Phase Difference. Power Supply: Half-wave Rectifiers. Centre-tapped and Bridge Full-wave Rectifiers Calculation of Ripple Factor and Rectification Efficiency, Basic idea about capacitor filter, Zener Diode and Voltage Regulation. Timer IC: IC 555 Pin diagram and its application as Astable and Monostable Multivibrator.

Suggested Readings

1) Integrated Electronics, J. Millman and C.C. Halkias, 1991, Tata Mc-Graw Hill.
2) Electronic devices & circuits, S. Salivahanan & N.S. Kumar, 2012, Tata Mc-Graw Hill
3) Microelectronic Circuits, M.H. Rashid, 2nd Edn., 2011, Cengage Learning.
4) Modern Electronic Instrumentation and Measurement Tech., Helfrick and Cooper, 1990, PHI Learning
5) Digital Principles and Applications, A.P. Malvino, D.P. Leach and Saha, 7th Ed., 2011, Tata McGraw Hill
6) Microelectronic circuits, A.S. Sedra, K.C. Smith, A.N. Chandorkar, 2014, 6th Edn., Oxford University Press.
7) Fundamentals of Digital Circuits, A. Anand Kumar, 2nd Edition, 2009, PHI Learning Pvt. Ltd.
8) OP-AMP & Linear Digital Circuits, R.A. Gayakwad, 2000, PHI Learning Pvt. Ltd.

7. Aaron, M. Tenenbaum., Moshe, J. Augenstein., & Yedidyah Langsam. (2003). Data Structures Using Java. New Delhi: PHI.
8. Robert Lafore. (2003). Data Structures and Algorithms in Java(2^{nd} ed.). New Delhi: Pearson/ Macmillan Computer Pub.
9. John Hubbard. (2009). Data Structures with JAVA(2nd ed.) . New Delhi: McGraw Hill Education (India) Private Limited.
10. Goodrich, M., & Tamassia, R. (2013). Data Structures and Algorithms Analysis in Java(4th ed.). New Delhi: Wiley.

WEB SITES:

1.http://en.wikipedia.org/wiki/Data_structure

2.http://www.cs.sunysb.edu/~skiena/214/lectures/

3.www.amazon.com/Teach-Yourself-Structures-Algorithms

Journals:

1.Suchait Gaurav "Algorithm for Stack with Random Operations (Stack Using Random Array Operations)" International Journal of Innovative Research & Development" Volume 2, Issue 8, August 2013

2.Karuna, Garima Gupta" Dynamic Implementation Using Linked List" International Journal Of Engineering Research & Management Technology"Volume 1, Issue-5, September - 2014

3.Parth Patel, Deepak Garg "Comparison of Advance Tree Data Structures" International Journal of Computer Applications" Volume 41, issue-2, March 2012

4.Ms ROOPA K,Ms RESHMA J "A Comparative Study of Sorting and Searching Algorithms "International Research Journal of Engineering and Technology "Volume: 05 Issue: 01 | Jan-2018

5.B. Madhuravani, D. S. R Murthy "Cryptographic Hash Functions: SHA Family" International Journal of Innovative Technology and Exploring Engineering" Volume-2, Issue-4, March 2013.

Prepared by Dr P.Tamil Selvan,Mrs N.Manonmani ,Dept of CS,CA&IT,KAHE 4/4

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LECTURE PLAN
DEPARTMENT OF PHYSICS

S No	Lecture Duration (Hr)	Topics to be covered	Support materials
UNIT I			
1.	1Hr	Difference between Analog and Digital Circuits. Binary Numbers.	T1,T2,T3
2.	1Hr	Decimal to Binary and Binary to Decimal Conversion	T4,T5
3.	1Hr	AND, OR and NOT Gates (Realization using Diodes and Transistor). NAND and NOR Gates as Universal Gates. XOR and XNOR Gates	T10,T11
4.	1Hr	De Morgan's Theorems. Boolean Laws. Simplification of Logic Circuit using Boolean Algebra	T15,T16
5.	1Hr	Fundamental Products. Minterms and Maxterms	-
6.	1Hr	Conversion of a Truth Table into an Equivalent Logic Circuit	T24
7.	1Hr	(1) Sum of Products Method and (2) Karnaugh Map	T18,T19
8.	1Hr	Binary Addition. Binary Subtraction using 2's Complement Method). Half Adders and Full Adders and Subtractors, 4-bit binary Adder-Subtractor.	T32,T33
9.	1Hr	Revision	
	Total No Of Hours Planned For Unit 1=9		
UNIT II			
1.	1Hr	Semiconductor Diodes	
2.	1Hr	P and N type semiconductors	
3.	1Hr	Barrier Formation in PN Junction Diode	
4.	1Hr	Qualitative Idea of Current Flow Mechanism	
5.	1Hr	Forward and Reverse Biased Diode. PN	

		junction and its characteristics	
6.	1Hr	Static and Dynamic Resistance. Principle and structure of (1) LEDs	
7.	1Hr	Principle and structure of Photodiode, Solar cell	
8.	1Hr	Bipolar Junction transistors: n-p-n and p-n-p Transistors.	
9.	1Hr	Revision	
	Total No Of Hours Planned For Unit II =9		
UNIT III			
1.	1Hr	Characteristics of CB configuration	
2.	1Hr	Characteristics of CE configuration	
3.	1Hr	Characteristics of CC configuration	
4.	1Hr	Active, Cutoff & Saturation regions Current gains α and β. Relations between α and β	
5.	1Hr	Load Line analysis of Transistors. DC Load line & Q-point	
6.	1Hr	Voltage Divider Bias Circuit for CE Amplifier. h-parameter Equivalent Circuit.	
7.	1Hr	Analysis of single-stage CE amplifier using hybrid Model.	
8.	1Hr	Input & output Impedance. Current, Voltage and Power gains. Class A, B & C Amplifiers	
9.	1Hr	Revision	
	Total No Of Hours Planned For Unit III =9		
UNIT IV			
1.	1Hr	Characteristics of an Ideal Op-Amp (IC 741)	
2.	1Hr	Characteristics of Practical Op-Amp (IC 741)	
3.	1Hr	Open-loop and closed-loop Gain. CMRR	
4.	1Hr	Concept of Virtual ground. Applications of Op-Amps	
5.	1Hr	Inverting and non-inverting Amplifiers	
6.	1Hr	Adder, Subtractor, Differentiator, Integrator,	
7.	1Hr	Zero crossing detector	
8.	1Hr	Barkhausen's Criterion for Self-sustained Oscillations. Determination of Frequency of RC Oscillator	
9.	1Hr	Revision	
	Total No Of Hours Planned For Unit IV = 9		
UNIT V			
1.	1Hr	**Instrumentations:** Introduction to CRO: Block Diagram of CRO	
2.	1Hr	Applications of CRO: (1) Study of	

		Waveform,	
3.	1Hr	Measurement of Voltage, Current, Frequency, and Phase Difference Power Supply	
4.	1Hr	Half-wave Rectifiers	
5.	1Hr	Centre-tapped and Bridge Full-wave Rectifiers	
6.	1Hr	Calculation of Ripple Factor	
7.	1Hr	Rectification Efficiency,	
8.	1Hr	Basic idea about capacitor filter, Zener Diode and Voltage Regulation. Timer IC: IC 555 Pin diagram and its application as Astable and Monostable Multivibrator.	
9.	1Hr	Revision	
10.	1Hr	Previous year Question Paper Discussion	
11.	1Hr	Previous year Question Paper Discussion	
12.	1Hr	Previous year Question Paper Discussion	
	Total No Of Hours Planned For Unit IV = 12		

UNIT-I

SYLLABUS

Digital Circuits :Difference between Analog and Digital Circuits. Binary Numbers. Decimal to Binary and Binary to Decimal Conversion, AND, OR and NOT Gates (Realization using Diodes and Transistor). NAND and NOR Gates as Universal Gates. XOR and XNOR Gates.
De Morgan's Theorems. Boolean Laws. Simplification of Logic Circuit using Boolean Algebra. Fundamental Products. Minterms and Maxterms. Conversion of a Truth Table into an Equivalent Logic Circuit by (1) Sum of Products Method and (2) Karnaugh Map.
Binary Addition. Binary Subtraction using 2's Complement Method). Half Adders and Full Adders and Subtractors, 4-bit binary Adder-Subtractor.

1. Difference between Analog and Digital Circuits

Analog Circuits	Digital Circuits
These circuits operate on continuous valued signals(commonly referred to as analog signals).	These circuits operate on signals that exist only at two levels i.e. 0's and 1's (binary number system).
Analog circuits are difficult to design since each component has to be placed by hand as automation techniques for designing these circuits fail to do the job efficiently.	On the other hand digital circuits are easy to design since automation technique can be applied at various levels of circuit design. This involves minimum human interaction.
No conversion of input signals are required before processing i.e. input signal is analog, the circuit directly performs various logical operations and produces an analog output.	In digital circuits, the input signals are converted from analog to digital form before it is processed, i.e. the digital circuit is capable of processing digital signals only, and produces output which is again converted back from digital to analog signals so that the output gives meaning full results that can be understood by humans.
In analog circuits, since there are no conversions involved at the input or at the output side there is no loss of information that is available for processing.	Due to the conversion process at the input side(analog to digital) and at the output side, some amount of information is lost during the conversion process.
The man power available to design analog circuits is very low, this results in long time to market the finished products.	The available man power to design digital circuits is significantly large compared to that of analog circuit designers.
Analog circuits are mostly custom made and lacks flexibility.	Digital circuits have high degree of flexibility.

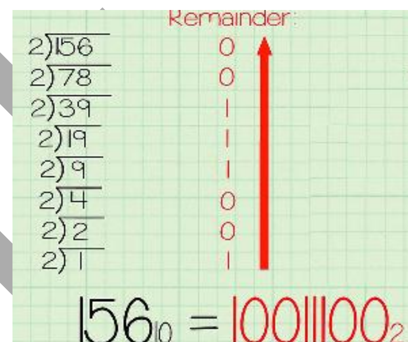
Binary numbers

In mathematics and digital electronics, a binary number is a number expressed in the base-2 numeral system or binary numeral system, which uses only two symbols: typically 0 (zero) and 1 (one).

The base-2 numeral system is a positional notation with a radix of 2. Each digit is referred to as a bit. Because of its straightforward implementation in digital electronic circuitry using logic gates, the binary system is used by almost all modern computers and computer-based devices.

Decimal to binary conversion

The decimal (base ten) numeral system has ten possible values (0,1,2,3,4,5,6,7,8, or 9) for each place-value. In contrast, the binary (base two) numeral system has two possible values represented as 0 or 1 for each place-value.[1] Since the binary system is the internal language of electronic computers, serious computer programmers should understand how to convert from decimal to binary



Example

Decimal to binary conversion examples

- $(51)_{10} = (110011)_2$
- $(217)_{10} = (11011001)_2$
- $(8023)_{10} = (1111101010111)_2$

Binary to Decimal conversion

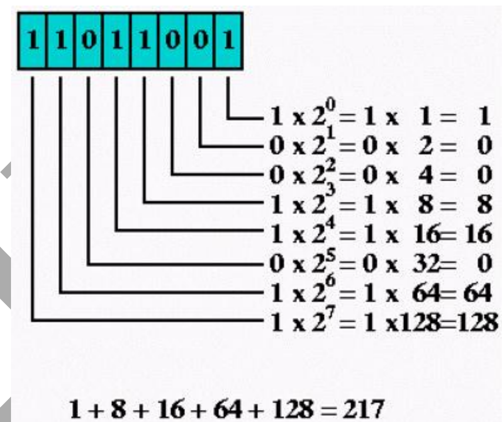
An easy method of **converting decimal** to**binary** number equivalents is to write down the**decimal** number and to continually divide-by-2 (two) to give a result and a remainder of either a “1” or a “0” until the final result equals zero. So for example. **Convert** the **decimal** number 294_{10}into its **binary** number equivalent.

Binary to decimal conversion examples

- $(10011)_2 = (19)_{10}$
- $(110101)_2 = (53)_{10}$
- $(10001011)_2 = (139)_{10}$

Algorithm to convert Binary to Decimal

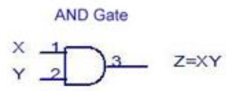
Binary Number	Decimal Number	Binary Number	Decimal Number
0	0	1111	15
1	1	10000	16
10	2	10001	17
11	3	10010	18
100	4	10011	19
101	5	10100	20
110	6	10101	21
111	7	10110	22
1000	8	10111	23
1001	9	11000	24
1010	10	11001	25
1011	11	11010	26
1100	12	11011	27
1101	13	11100	28
1110	14	11101	29



AND Gate

An AND gate requires two or more inputs and produce only one output. The AND gate produces an output of logic 1 state when each of the inputs are at logic 1 state and also produces an output of logic 0 state even if any of its inputs are at logic 0 state. The symbol for AND operation is '.', or we use no symbol for representing. If the inputs are of X and Y, then the output can be expressed as Z=XY. The AND gate is so named because, if 0 is called "false" and 1 is called "true," the gate performs in the same way as the logical "and" operator. The AND gate is also named as all or nothing gate. The logic symbols and truth tables of two-input and three-input AND gates are given below

2 Input AND Gate

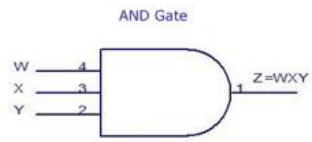


TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

2 Input AND Gate – Truth Table

3 Input AND Gate



TRUTH TABLE

INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3 Input AND Gate – Truth Table

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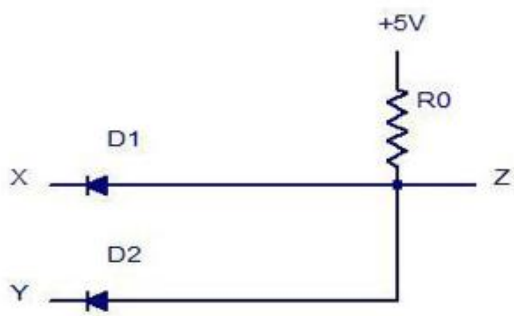
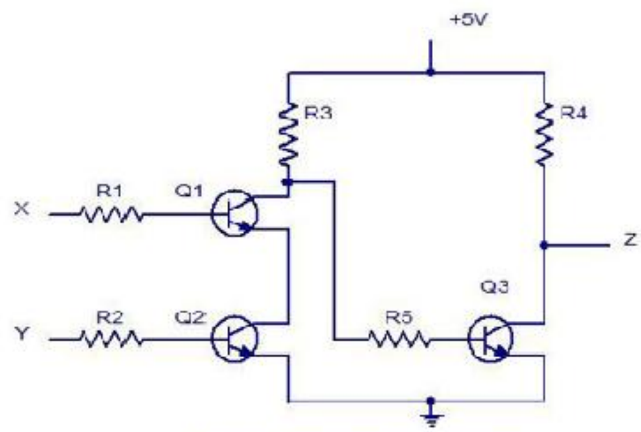


2 Input Diode AND Gate



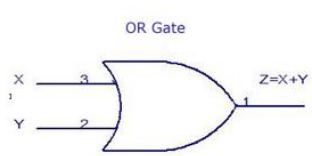
2 Input Transistor AND Gate

2 INPUT DIODE AND TRANSISTOR AND GATE

OR GATE

Similar to AND gate, an OR gate may also have two or more inputs but produce only one output. The OR gate produces an output of logic 1 state even if any of its inputs is in logic 1 state and also produces an output of logic 0 state if any of its inputs is in logic 0 state. The symbol for OR operation is '+'. If the inputs are of X and Y, then the output can be represented as Z=X+Y. An OR gate may also be defined as a device whose output is 1, even if one of its input is 1. OR gate is also called as any or all gate. It is also called as an inclusive OR gate because it consists of the condition of 'both the inputs can be present'. The logic symbols and truth table for two-input and three-input OR gates are given below.

2 Input OR Gate

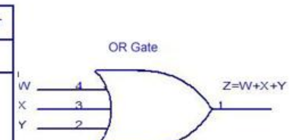


TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

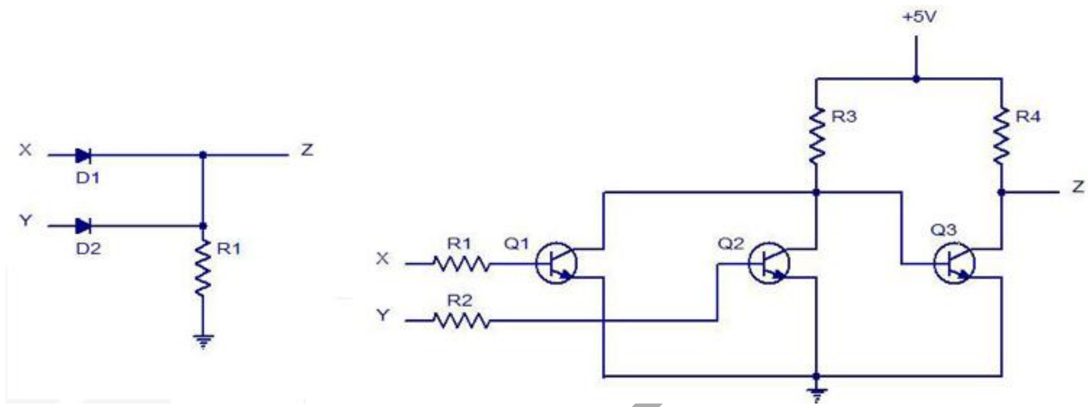
2 Input OR Gate – Truth Table

3 Input OR Gate



TRUTH TABLE

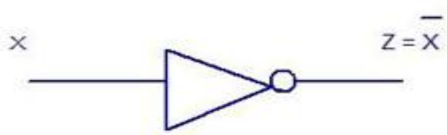
INPUTS			OUTPUT
W	X	Y	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



2 INPUT DIODE AND TRANSISTOR OR GATE

NOT GATE

The NOT gate is also called as an inverter, simply because it changes the input to its opposite. The NOT gate is having only one input and one corresponding output. It is a device whose output is always the compliment of the given input. That means, the NOT gate produces an output of logic 1 state when the input is of logic 0 state and also produce the output of logic 0 state when the input is of logic 1 state. The NOT operation is denoted by '-'(bar). When the input variable to the NOT gate is represented by 'X' and the output is represented by 'Z'. In the NOT operation it can be read as 'Z is equal to X bar'. The logic symbol and truth table are given below:

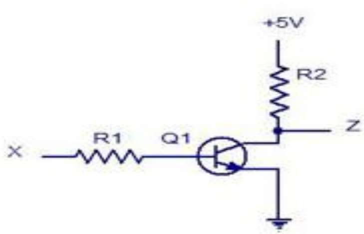


TRUTH TABLE

INPUT	OUTPUT
X	Z
0	1
1	0

NOT Gate – Truth Table

Transistor Inverter NOT Gate



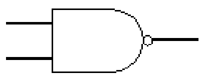
Transistor Inverter NOT Gate

TRUTH TABLE

INPUT	OUTPUT
X	Z
0 V	5 V
5 V	0 V

The *NAND gate* operates as an AND gate followed by a NOT gate. It acts in the manner of the logical operation "and" followed by negation. The output is "false" if both inputs are "true." Otherwise, the output is "true."

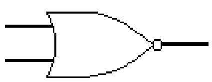
NAND gate



Input 1	Input 2	Output
		1
	1	1
1		1
1	1	

The *NOR gate* is a combination OR gate followed by an inverter. Its output is "true" if both inputs are "false." Otherwise, the output is "false."

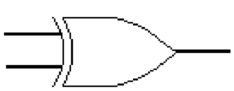
NOR gate



Input 1	Input 2	Output
		1
	1	
1		
1	1	

The *XOR* (*exclusive-OR*) *gate* acts in the same way as the logical "either/or." The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true." Another way of looking at this circuit is to observe that the output is 1 if the inputs are different, but 0 if the inputs are the same.

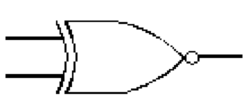
XOR gate



Input 1	Input 2	Output
	1	1
1		1
1	1	

The *XNOR (exclusive-NOR) gate* is a combination XOR gate followed by an inverter. Its output is "true" if the inputs are the same, and"false" if the inputs are different.

XNOR gate



Input 1	Input 2	Output
		1
	1	
1		
1	1	1

De Morgan's Theorems

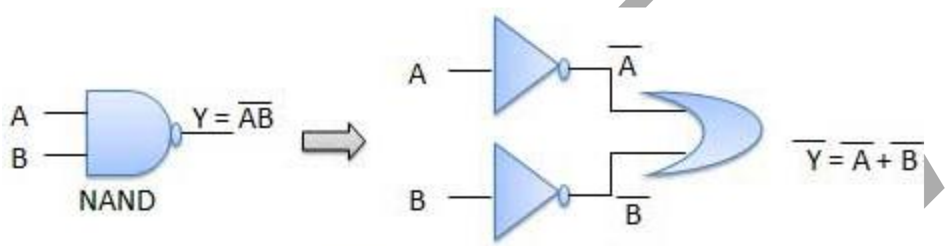
De Morgan has suggested two theorems which are extremely useful in Boolean Algebra. The two theorems are discussed below.

Theorem 1

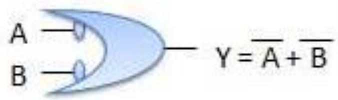
$\overline{A.B} = \overline{A} + \overline{B}$

NAND = Bubbled OR

- The left hand side (LHS) of this theorem represents a NAND gate with inputs A and B, whereas the right hand side (RHS) of the theorem represents an OR gate with inverted inputs.
- This OR gate is called as **Bubbled OR**.



NAND ≡ Bubbled OR



Bubbled OR

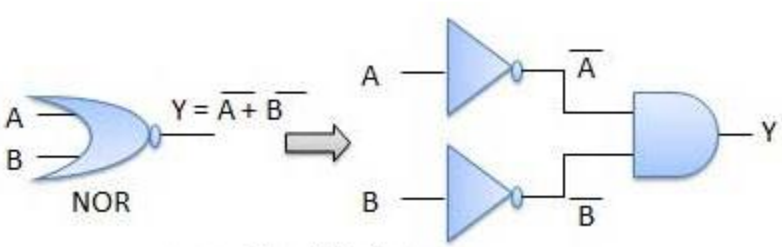
Table showing verification of the De Morgan's first theorem

A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Theorem 2

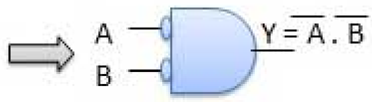
$\overline{A + B} = \overline{A}.\overline{B}$ NOR = Bubbled AND

- The LHS of this theorem represents a NOR gate with inputs A and B, whereas the RHS represents an AND gate with inverted inputs.



NOR ≡ Bubbled AND

- This AND gate is called as **Bubbled AND**.



Bubbled AND

Table showing verification of the De Morgan's second theorem

A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\,.\,\overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Boolean Laws

There are six types of Boolean Laws.

Commutative law

Any binary operation which satisfies the following expression is referred to as commutative operation.

(i) $A.B = B.A$ (ii) $A + B = B + A$

Commutative law states that changing the sequence of the variables does not have any effect on the output of a logic circuit.

Associative law

This law states that the order in which the logic operations are performed is irrelevant as their effect is the same.

(i) $(A.B).C = A.(B.C)$ (ii) $(A + B) + C = A + (B + C)$

Distributive law

Distributive law states the following condition.

$A.(B + C) = A.B + A.C$

AND law

These laws use the AND operation. Therefore they are called as **AND** laws.

(i) $A.0 = 0$ (ii) $A.1 = A$

(iii) $A.A = A$ (iv) $A.\overline{A} = 0$

OR law

These laws use the OR operation. Therefore they are called as **OR** laws.

(i) $A + 0 = A$ (ii) $A + 1 = 1$

(iii) $A + A = A$ (iv) $A + \overline{A} = 1$

Inversion law

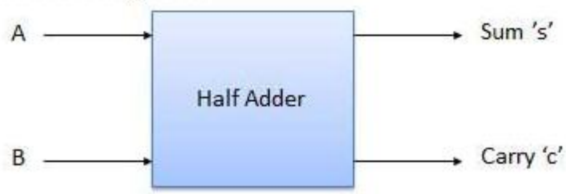
This law uses the NOT operation. The inversion law states that double inversion of a variable results in the original variable itself.

$\overline{\overline{A}} = A$

Half Adder

Half adder is a combinational logic circuit with two inputs and two outputs. The half adder circuit is designed to add two single bit binary number A and B. It is the basic building block for addition of two **single** bit numbers. This circuit has two outputs **carry** and **sum**.

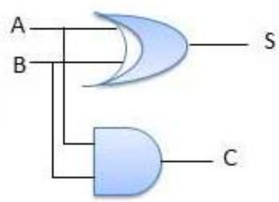
Block diagram



Truth Table

Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

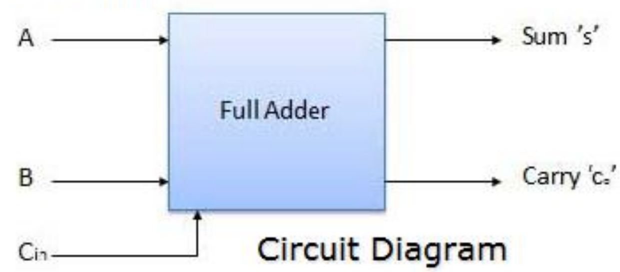
Circuit Diagram



Full Adder

Full adder is developed to overcome the drawback of Half Adder circuit. It can add two one-bit numbers A and B, and carry c. The full adder is a three input and two output combinational circuit.

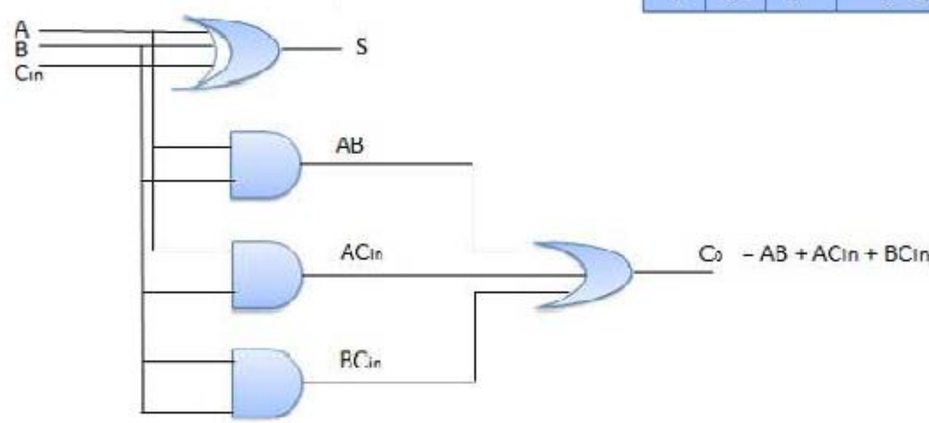
Block diagram



Truth Table

Inputs			Output	
A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit Diagram



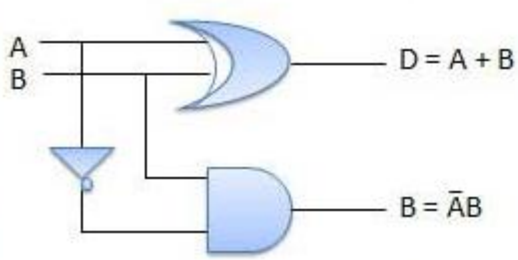
Half Subtractors

Half subtractor is a combination circuit with two inputs and two outputs (difference and borrow). It produces the difference between the two binary bits at the input and also produces an output (Borrow) to indicate if a 1 has been borrowed. In the subtraction (A-B), A is called as Minuend bit and B is called as Subtrahend bit.

Truth Table

Inputs		Output	
A	B	(A – B)	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Circuit Diagram



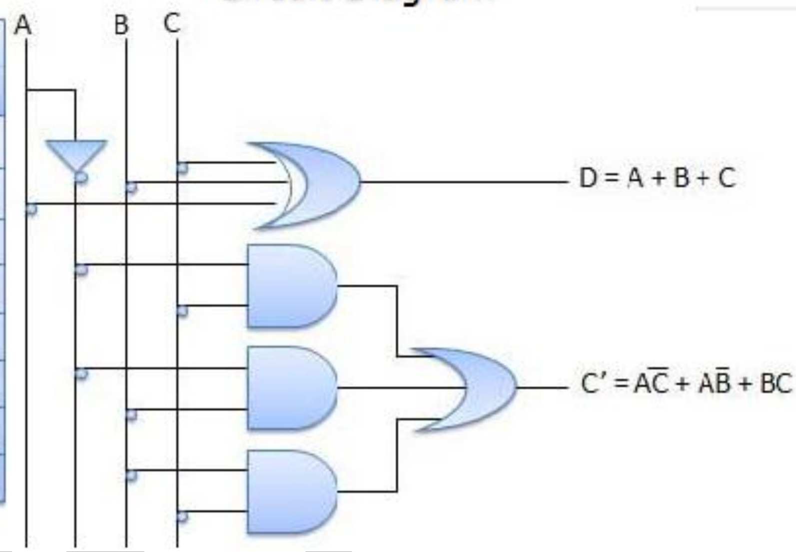
Full Subtractors

The disadvantage of a half subtractor is overcome by full subtractor. The full subtractor is a combinational circuit with three inputs A,B,C and two output D and C'. A is the 'minuend', B is 'subtrahend', C is the 'borrow' produced by the previous stage, D is the difference output and C' is the borrow output.

Truth Table

Inputs			Output	
A	B	C	(A-B-C)	C
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Circuit Diagram



Possible questions

Part –B

1. Convert the binary number 1101010101_2 into decimal.
2. Convert the binary numbers to decimal numbers. a) 1100101001010111_2 b) 111111000101101001_2
3. Give logic symbol and truth tables for XOR and XNOR gates.
4. What is Boolean algebra?
5. Draw the truth table of AND and OR gate.
6. Prove A+BC = (A+B) (A+C)
7. What is the Half-Adder?
8. What is the Half-Subtractor?
9. State Commutative law.
10. State Distributive law.

Part –C

11. List the laws of laws of Boolean algebra.
12. State and prove DeMorgan's theorem.
13. Draw logic symbols and truth table of AND, OR, NOT, NAND and NOT logic gates.
14. Explain the basic laws of Boolean algebra with truth tables
15. Construct half adder and half subtractor using XOR gates.
16. Explain the various logic gates with their truth tables.
17. Solve following problems using K-map:
    (i) $Y=\Sigma(2,3,12,14,15)$ (ii) $Y=\Sigma(0,2,5,7,8,10,13,15)$
    (iii)$Y=F(A,B,C,D) = \Sigma(1,5,6,7,11,12,13,15)$
    Explain full adder and half adder.
18. Using K-Map solve following problems:
    a. $F(A,B,C,D) = \Sigma(0,1,4,6,7,8,9,10,11,15)$
    b. $Y=\Sigma(0,2,5,7,8,10,13,15)$
19. Solve following problems using K-map:
    (i) $Y=F(A,B,C,D)= \Sigma(1,3,7,11,15)+\Sigma_d(0,2,5,8)$
20. Using K-Map solve following problems:
    a. $F(A,B,C,D) = \Sigma(0,1,4,6,7,8,9,10,11,15)$

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(For Candidates Admitted From 2017 Onwards)

DEPARTMENT OF PHYSICS

UNIT I: Objective Type/Multiple choice Questions each Question carries one Mark

Sl.No	Question	OPTION A	OPTION B	OPTION C	OPTION D	ANSWER
1	Which gate has two or more input signals in which all input must be high to get a high output?	OR	NAND	AND	NOR	AND
2	A NOR gate has a high output only when the input bits are	low	high	some low some high	None of the above	low
3	A NOR gate is logically equivalent to an OR gate followed by an	AND	NAND	XOR	INVERTER	INVERTER
4	Boolean expression for NOR gate with two inputs x and y can be written as	(x+y)’	x . y	x+y	xy’ + x’y	(x+y)’
5	Boolean expression for NAND gate with two inputs x and y can be written as	xy	x+y	x’+y’	None of the above	x+y
6	In a four input NAND gate, if all the inputs are 1, the output is	4	¼	1	0	0
7	NAND gates can be used as which type gates?	NOT	OR	AND	All of the above	All of the above
8	An OR gate can be imagined as	switches connected in series	switches connected in parallel	MOS transistors connected in series	None of the above	switches connected in parallel
9	Which gate is known as Universal gate?	NOT	AND	NAND	OR	NAND
10	Any Boolean expression can be implemented using	only NOR gates	only NAND gates	only AND gates	only XOR gates	only NAND gates
11	Which digits are used to represent high & low level in digital circuits?	1 0	0 1	0 0	1 1	1 0

12	Complement of a Variable is represented by __________ over the Letter.	slash	bar	dot	hyphen	bar
13	What is the value for 1+1 in Boolean Addition?	2	10	1	0	1
14	Multiplication in Boolean algebra is the same as the ___________ function	AND	OR	NOT	NOR	AND
15	The operation of an inverter is_________	Complement Input variable	add +1 to input variable	add –1 to input variable	minus input variable	Complement Input variable
16	____________is same as Inversion.	complementation	exclusive	AND	OR	complementation
17	The output of an AND gate is 1(High) only when both inputs are ___________	1 0	0 0	1 1	0 1	1 1
18	The output of an OR gate is 1(High) only when any one or more of the inputs are ___________	high	low	medium	high	high
19	NAND is a complement of ___________	NOT	AND	OR	NOR	AND
20	NOR is a complement of ___________	NOT	AND	OR	NAND	OR
21	Commutative Law of Addition of 2 variables is written as	A+B=B+A	B+A=B+A	A+B=A + B	AB=AB	A+B=B+A
22	Commutative Law of Multiplication of 2 variables is written as	AB=BA	BA=BA	AB=AB	AB=A+B	AB=BA
23	Associative law of addition is stated as	A + (B + = (A++C	(A + + C = (A++C	(A+ C = A (B+	AB+C = A+BC	A + (B + = (A++C
24	Associative law of multiplication is stated as	A (B=(A C	ABC=ACB	AB = BA	ABC=CAB	A (B=(A C
25	Distributive Law is stated as	A (B+ = AB + AC	AB + AC = ABC	AB + C= AC + B	(A + C = AB + AC	A (B+ = AB + AC
26	In Boolean algebra A + 0 =?	A	0	–A	1	A

27	In Boolean algebra A + 1 =?	A	0	–A	1	1
28	In Boolean algebra A .0 =?	A	0	–A	1	0
29	In Boolean algebra A .1 =?	A	0	–A	1	A
30	In Boolean algebra A +A =?	A	0	–A	1	A
31	In Boolean algebra A + $\bar{A}$ =?	A	0	–A	1	1
32	In Boolean algebra A .A =?	A	0	–A	1	A
33	In Boolean algebra A. $\bar{A}$ =?	A	0	–A	1	0
34	In Boolean algebra A + AB =?	A	0	–A	1	A
35	In Boolean algebra A + $\bar{A}$B =?	A	0	B	A + B	A + B
36	In Boolean algebra (A +(A + =?	A	0	B	A +BC	A +BC
37	The Complement of a product =	Sum of the Complements	Product of the Complement	Complement of the sum	Product	Sum of the Complements
38	The Complement of a Sum =	Sum of the Complements	Product of the Complement	Complement of the sum	Sum	Sum of the Complements
39	Sum of Product expression is	two or more AND functions OR together	two or more OR functions AND together	two or more AND functions NOR together	two or more OR functions NOR together	two or more AND functions OR together
40	Product of Sum expression is	AND of two or more OR functions	OR of two or more AND functions	AND of two or more NAND functions	OR of two or more NAND functions	AND of two or more OR functions
41	Boolean expression can be simplified using	Associative law	rules and laws of Boolean algebra	Distributive law	None of the above	rules and laws of Boolean algebra

42	Sum of products expression is implemented with ________	AND-OR logic	OR-AND logic	NAND logic	NOR logic	AND-OR logic
43	The output of an exclusive – OR gate is HIGH when inputs have	Same state	Opposite State	Complement State	Alternate State	Opposite State
44	The output of an exclusive – NOR gate is HIGH when inputs have	Same state	Opposite State	Complement State	Alternate State	Same state
45	Any Logic Expression can be implemented using	NAND / NOR	AND / OR	X-OR / OR	NAND / AND	NAND / NOR
46	What are the common internal gate failures?	open input or output & shorted input or output	open input or output & Loaded input or output	open input or output & driving input or output	open input or output & bad input or output	open input or output & shorted input or output
47	The interconnecting paths represent a common electrical point is known as ____________.	Cell	Node	Point	Junction	Junction
48	The coincidence circuit is otherwise called as	Exclusive-NOR	Exclusive – OR	Exclusive – AND	Exclusive – NAND	Exclusive – OR
49	NAND & NOR gates are called as	Universal Gates	Functional gates	Logical Gates	Combinational gates	Universal Gates
50	Sum of products can be done using	demorgan's theorem	algebric theorem	demorgan's postulate	algebric postulate	demorgan's theorem
51	Two variables will be represented by	eight minterms	six minterms	five minterms	four minterms	four minterms
52	The output of AND gates in SOP is connected to	NOT gates	OR gates	AND gates	XOR gates	OR gates
53	Sum of minterms of Boolean functions give conditions in which function is	dont care	variable	0	1	1

54	The minterms in a karnaugh map are marked with a	y	x	0	1	1
55	Small circle in a NAND circuit represents	input	bits	output	complement	complement
56	Tabulation method is adopted for giving simplified function in	subtraction of sum	sum of products	product of sums	subtraction of product	product of sums
57	Each square in a karnaugh map represents a	points	values	minterm	maxterm	minterm
58	Sum of products can be done using	demorgan's theorem	algebric theorem	demorgan's postulate	algebric postulate	demorgan's theorem
59	The binary code of the decimal number 73 is	1010001	1000100	1100101	1001001	1001001
60	What is the binary equivalent of decimal 269?	100001100	100001010	101001011	100001101	100001101
61	A binary number with 4 bits is called a__________:	Bit	Bytes	Nibble	None of these	Nibble
62	A binary number with 8 bits is called as a____________:	Bytes	Bits	Nibble	All of these	Bytes
63	0,1,2 ,3 ,4,5,6 ,7,8 and 9 numerals are called:	Arabic numerals	String numerals	Digit numerals	None of these	Arabic numerals
64	In the adder circuit the two outputs are ____________.	Sum & carry	Carry & borrow	Carry & borrow	Sum & difference	Sum & carry
65	In the subtractor circuit the two outputs are ____________.	Sum & carry	Sum & borrow	Sum & difference	Difference & borrow	Difference & borrow
66	A four bit adder adds ____________ 4-bit numbers.	2	4	5	6	2
67	The four bit adder requires ____________ full adders.	2	4	6	8	4

68	A Karnaugh map is a systematic way of reducing which type of expression?	product-of-sums	exclusive NOR	sum-of-products	those with overbars	sum-of-products
69	Which of the following combinations cannot be combined into K-map groups?	corners in the same row	corners in the same column	diagonal	overlapping combinations	diagonal
70	Why XOR gate is called an inverter?	Because of the same input	Because of the same output	It behaves like a NOT gate	None of the Mentioned	It behaves like a NOT gate
71	The systematic reduction of logic circuits is accomplished by:	using Boolean algebra	symbolic reduction	TTL logic	using a truth table	
72	Which of the examples below expresses the distributive law of Boolean algebra?	(A + + C = A + (B +	A(B + = AB + AC	A + (B + = AB + AC	A(B = (A + C	A(B + = AB + AC
73	Use Boolean algebra to find the most simplified SOP expression for F = ABD + CD + ACD + ABC + ABCD.	F = ABD + ABC + CD	F = CD + AD	F = BC + AB	F = AC + AD	F = ABD + ABC + CD

UNIT-II

Semiconductor Devices and Amplifiers: Semiconductor Diodes: P and N type semiconductors. Barrier Formation in PN Junction Diode. Qualitative Idea of Current Flow Mechanism in Forward and Reverse Biased Diode. PN junction and its characteristics. Static and Dynamic Resistance. Principle and structure of (1) LEDs, (2) Photodiode, (3) Solar Cell. Bipolar Junction transistors: n-p-n and p-n-p Transistors.

Conductor
A material that allows electricity to pass through it is known as conductor. Charges are allowed to move freely in the conductor. E.g.: Usually metals are conductors.
Insulator
A material which does not allow electricity to pass through it is known as insulator. Charges are not allowed to move in insulator. E.g.: Plastic, wood are insulators.
Semiconductors
A material that can behave as a conductor as well as an insulator is known as semiconductor.
E.g.: germanium, silicon etc.
Conductivity
The measurement of charges which are allowed to flow in a material is known as conductivity of the material.
Resistivity
The measurement of the resisting power i.e. restriction to the flow of charge in the material, is called as resistivity.
conductivity = 1/resistivity

Material	Resistivity	Conductivity
Conductors	10-2 to 10-8 Ωm	102 to 108 Sm-1
Semiconductors	10-5 to 106 Ωm	105 to 10-6 Sm-1
Insulators	1011 to 1019 Ωm	10-11 to 10-19 Sm-1

Observations
Conductors have high conductivity and very low resistivity.
Insulator have low conductivity and high resistivity.
Semiconductors have conductivity and resistivity in between the conductor and insulator.
Types of Semiconductors
Elemental Semiconductors: Silicon (Si), Germanium (Ge)
Compound Semiconductors: There can be three types of Compound semiconductors –

- Inorganic semiconductors: Cadmium sulphide (Cd S), Gallium arsenide (Ga As), Cadmium selenide (Cd Se), Indium phosphide (In P).
- Organic semiconductors: Anthracene, Phthalocyanine.
- Organic Polymers: Polypyrrole, Polyaniline, Polythiophene.

Energy Level

In an isolated atom, the energy processed by the electrons in the same orbit is almost equal. When the atoms are placed in a crystal form the energy level of each electron changes due to the effect of other closely placed atoms.

There are two types of electrons present in an atom

- **Valence electron** − An atom requires eight electrons in the outer most orbit to be stable. So the atom shares electrons with another atom to attain stability, this is known as valence fulfilment. In valence fulfilment the electron that is shared between the two atoms is known as valence electron.

- **Free electron** − If an electron receives energy externally such as due to heat the electron moves out of the valence band and becomes free. The free electron has a greater energy than the valence electron.

When electric current is passed through the material the free electrons move towards the positive direction of current resulting in conduction of current through the material.

In crystal formation the energy level of electron can be categorised into two distinct energy levels or energy bands.

Valence Band − Valence band contains valence electrons. The valence band can be completely filled with electrons or sometimes partially filled with electrons but it is never empty. As these are valence electrons they are not affected by the electric filled.

Conduction Band − Conduction band contains free electrons. It can be empty or partially filled with electrons. As these are free electrons they conduct electricity through the material.

Forbidden Band / Energy Gap (E_g) − The forbidden band is completely empty as there are no electrons in it. To move an electron from the valence band to the conduction band an energy equal to the energy gap is required.

N type Semiconductors

When Si or Ge crystal is doped with pentavalent impurity we get n type semiconductor.

Example of pentavalent atom: Phosphorous (P), Arsenic (As), Antimony (Sb).

Pentavalent atom has 5 electrons in its valence shell. Figure shows the structure of n type semiconductor. Every pentavalent dopant atom finds 4 neighboring Si atoms. It shares its 4 valence electrons with four Si atoms to form octet and Si atoms become stable.
Since valence orbit can hold maximum 8 electrons, the 1 extra electron of dopant atom is not the part of covalent bonding and hence it becomes free electron. The free electron of phosphorous atom has energy 0.01eV less than the conduction band energy of Silicon. At room temperature these free electrons move to the conduction band and are available for conduction of electricity.
Due to these extra free electrons in the crystal structure, the number of electrons become greater than the number of holes in the crystal.

Note − Number of holes will decrease but will never become zero, there would be a small number of holes present in the crystal.
Relationship between the number of electrons and number of holes is given by -
ne × nh = ni2
Where,
ne = number of electrons.
nh = number of holes.
ni = total number of charge carriers.

Conduction band is crowded by electrons and holes in the valence band are decreased in N type semiconductor. In N type semiconductor electrons are majority charge carriers and holes are minority charge carriers. Since every pentavalent dopant atom donates 1 electron for conduction; it is called donor type dopant. As we can control the number of dopant i.e. we can control the number of free electrons and hence control the conductivity of semiconductor.

P-Type Semiconductors

When Si or Ge crystal or intrinsic semiconductor is doped with measured quantity of trivalent impurity such as indium(In), boron (B), aluminum (Al), we get p type semiconductor. The trivalent atom has three electrons in valence shell. Every trivalent dopant atom shares its 3 electrons with 3 neighboring Si atoms to form covalent bond. But, the bond between dopant atom and 4th neighbor is not completed as trivalent atom has no more electron to share. Hence creating a vacancy that acts as a hole. This hole has tendency to accept any electron in its close vicinity. For this reason, trivalent impurity is called as an acceptor type dopant. At room temperature, an electron from neighboring atom can jump into the hole. This hole disappears and new hole is created at the position of displaced electron.

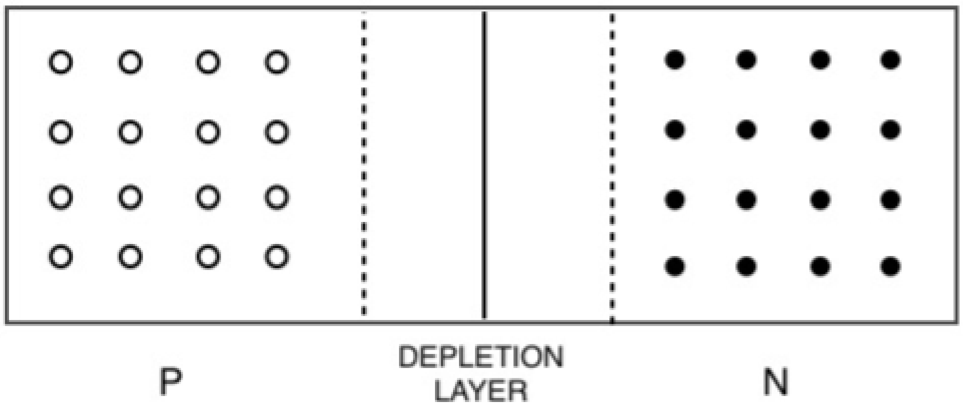
As this semiconductor has large number of holes and conductivity is because of positively charged holes, it is called p type semiconductor. In P type semiconductor holes are majority charge carriers and electrons are minority charge carriers. The number of holes is comparatively very large than the number of electrons.

$$\mathbf{n_h >> n_e}$$

Though P type semiconductor has large numbers of holes, its net charge is zero.

P-N Junction

When half part of a Si crystal is doped with trivalent impurity and half with pentavalent impurity, we get P-N junction diode.The border where p-region meets with n-region is called the junction.



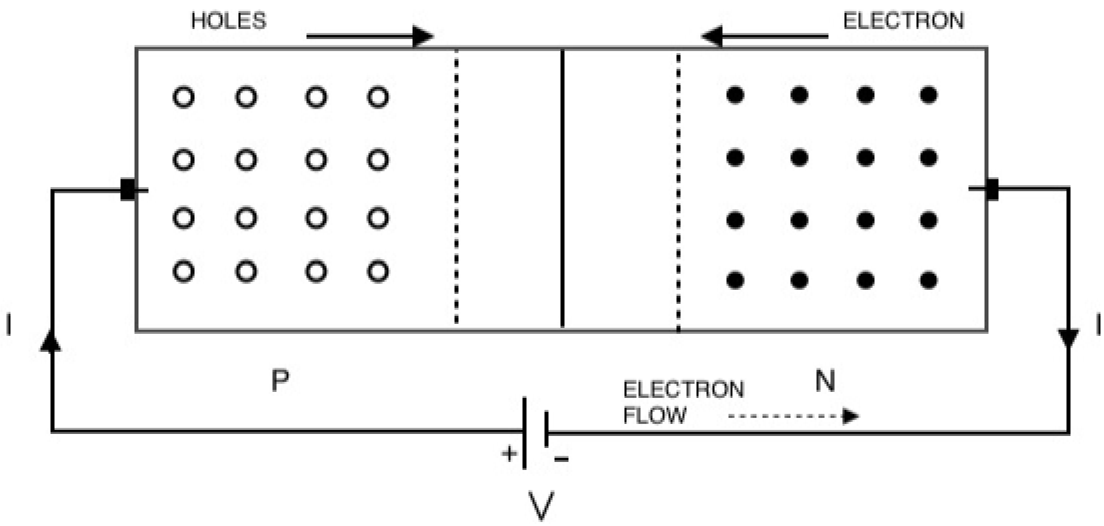
P and N type junction develops a depletion-layer around it due to the recombination of electrons from N-side and holes on P-side. No charge carriers are present in this region as combination of holes and electrons create neutral atoms, hence depletion-layer has high resistance. No charge carriers from either side is allowed to cross the depletion layer. Due to losing electrons 'N' develops a positive charge layer, and 'P' develops a negative charge layer. Hence an electric field or potential difference is developed between the two. This potential difference prevents the flow of majority charge carriers across the junction, hence called as potential barrier. When no external source is connected to diode it is said to be unbiased diode. Majority charge carriers i.e. holes in the P side and electrons in the N side cannot flow through the depletion-layer, but minority charge carriers i.e. electrons in P side and holes in N side can flow through depletion-layer. P-N junction diode acts as an insulator.

Biasing of P-N Junction

Biasing in the process of applying potential difference to the semiconductor. Biasing is achieved by applying EMF across the P-N junction diode.
Biasing can be of two types –
Forward biasing
Reverse biasing

Forward biasing

When positive terminal of the battery is connected to P-side and negative terminal to N-side it is called forward biasing and the diode is said to be forward biased.



When forward biased, electrons from N-side and holes from P-side are pushed towards the junction. The depletion layer's width decreases. As depletion layer decreases, potential barrier also decreases. The potential difference within the P-N junction diode is known as induced potential ($V_{induced}$) and potential difference applied externally is called applied potential ($V_{applied}$).

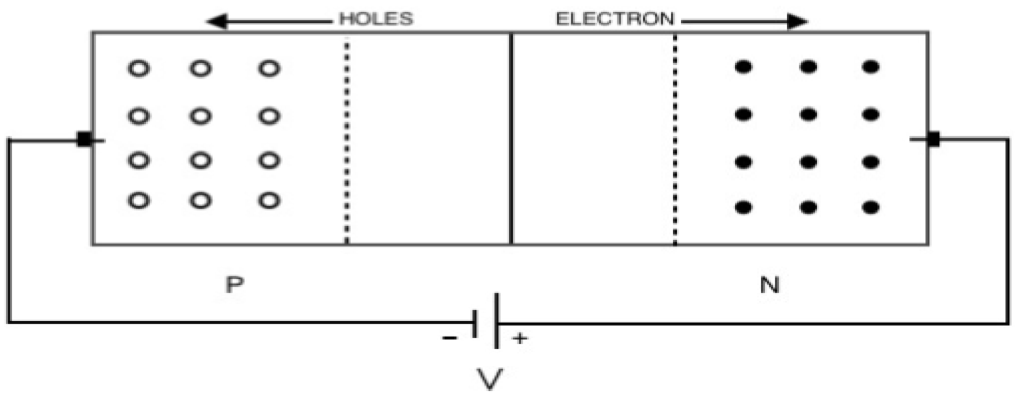
Total Potential Difference = $V_{Induced}$ + $V_{Applied}$

The direction of both the potential are opposite to each other therefore, as the applied potential increases it reduces the effect of induced potential. When the applied potential is equal to the induced potential then, the net potential equals to zero and the depletion layer vanishes.

As there is no depletion layer, large number of electrons and holes cross the junction. They recombine and large current flows through the diode. After recombining, the electrons travel as valence electrons then leave the Pregion and enter positive terminal of the source. A continuous current flows in the diode. That is, on forward biasing, P-N junction diode acts as conductor.

Reverse Biasing Of P-N Junction

When positive terminal of the battery is connected to N-side and negative terminal to P-side, it is known as reverse biasing and the diode is said to be reversed biased.



In reverse biasing, free electrons and holes move away from the junction. Hence, increasing the width of depletion layer. As the depletion layer increases, potential barrier also increases.

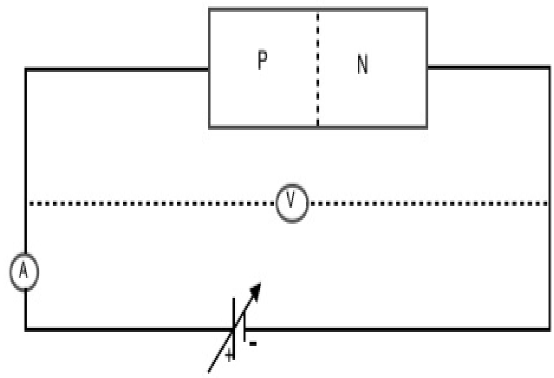
In reverse biasing the induced and applied potential are in the same direction i.e. the net potential will increase with the increasing applied potential. Higher will be the net potential in the diode, higher will be the resistance. Majority charge carriers cannot move across the junction, hence current will not be allowed to flow across the diode. That is, on reverse biasing, P-N junction diode acts as insulator. The current flowing in the reverse biased circuit due to the minority charge carrier is known as reverse current.

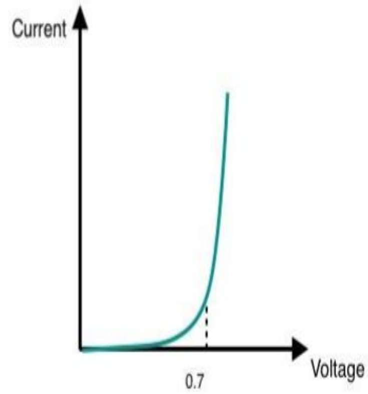
Characteristic Of P-N Junction

To study V-I characteristic of diode the external source is connected to diode through rheostat so that variable voltage can be applied to diode. A voltmeter is connected parallel to diode to read diode voltage and current meter is connected in series with diode to measure resulting current. Characteristics can be studied separately for forward biasing and reverse biasing.

Forward characteristic

When forward biased (Si diode), initially current does not flow until biasing is less than potential barrier (0.7 V) but it increases suddenly beyond 0.7 V and current is directly proportional to voltage.





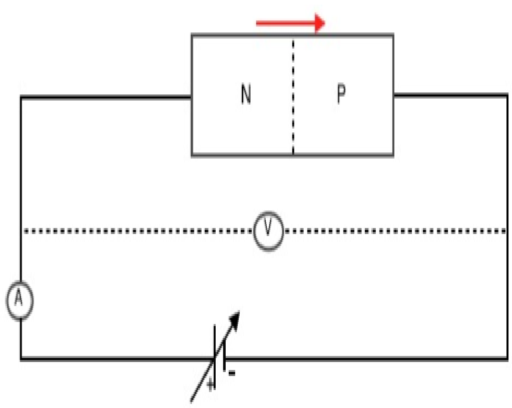
Resistance in forward biasing is dynamic resistance which is given by -

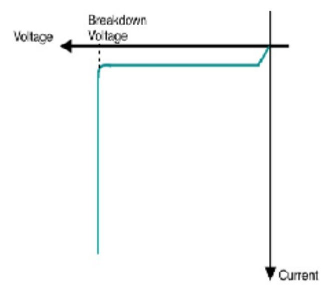
$$\mathbf{R = \Delta v/\Delta i}$$

Resistance in forward biasing in the range of few ohm to ten kilo ohm.

Reverse characteristic

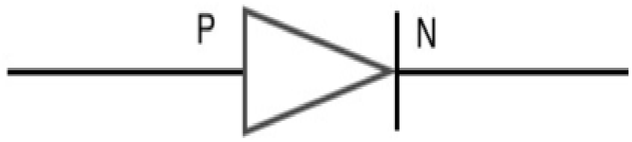
When the diode is reverse biased, there is no crossing of majority carriers and current is approximately zero.





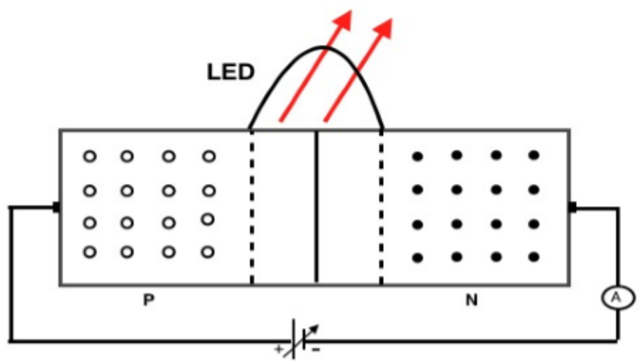
A very small current of the order nA flows because of minority carriers in depletion region. This current is called reverse current.When reverse biasing increases, at a particular high value, the reverse current increases suddenly and a large amount of atoms are broken down in the depletion layer. This is called breakdown of diode. If this reverse current is not controlled, p-n junction gets damaged due to excess heating. The reverse voltage, at which the diode breakdown occur is called breakdown voltage (V_{BR}). For general purpose diode, the reverse voltage is always kept below the breakdown voltage.Resistance in forward biasing is in the range of thousand kilo ohm.

Symbol for P-N junction

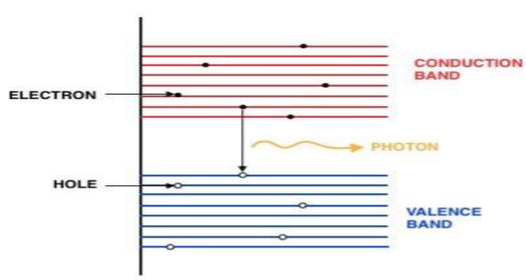


Light Emitting Diode(LED)

Light emitting diode is a special type of P-N junction diode that has energy gap greater than 1.8eV.

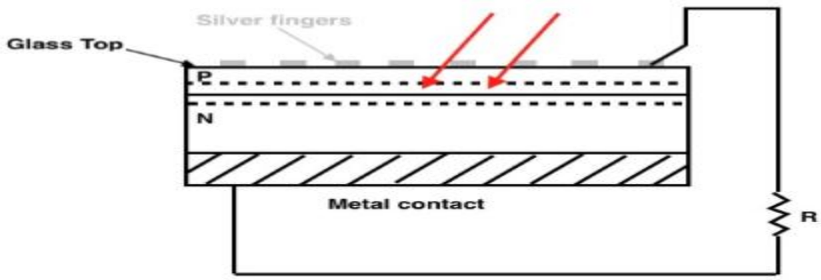


When the free electrons fall from conduction band to valence band, the energy equal to band gap (E_g) is released in the form of photons. The photon has energy **E = hv**, for the photon to be visible to human eye it should have a frequency **v** greater than visible light hence, the energy gap should have a value greater than 1.8eV hence, Silicon and Germanium cannot be used. Light emitting diodes are used in forward bias. This results in reduction of depletion layer allowing the free electrons to recombine with the holes i.e. minority charge carriers recombine and release energy slightly less than energy gap. This gives light of different colors. Gallium-Arsenide LED emits infrared light. Ga-As-P LED emits red and yellow light. Ga-P LEDs emit red, green light. LEDs cannot be used in reverse biased because if we reach the breakdown voltage a large amount of current will flow through it and the LED will burn out. Their reverse breakdown voltage is low about 5V.



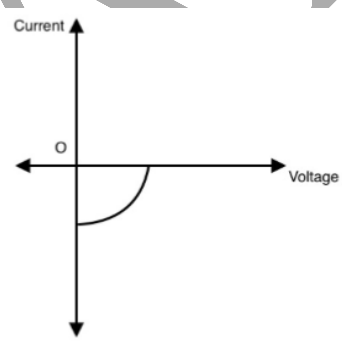
Solar-Cell

Solar cell, which is also known as photovoltaic cell, converts solar (light) energy directly into electrical energy.



V-I characteristic of solar cell

Solar cell is a P-N junction diode that has very thin layer of P-type semiconductor (thickness is in μm) so that light can reach the junction. The photon that is reaching the junction should have energy greater than the energy gap. Metallic contacts are formed on both the layers for external circuit connections. At the top silver fingers are used, as silver is the best conductor and they are used to absorb photo electrons. This displacement of charges sets up a potential difference across two regions, with P-side as positive and N-side as negative. If external load RL is connected, current flows through it and we get electrical energy. Typically, a solar cell can generate photo voltage from 0.5 V to 1.2 V.



Applications of solar cell

- Charging storage batteries.
- Charging satellite batteries.
- Pumps and other electronic appliances in the far-off areas use solar cell.
- Radiophones.

Transistor

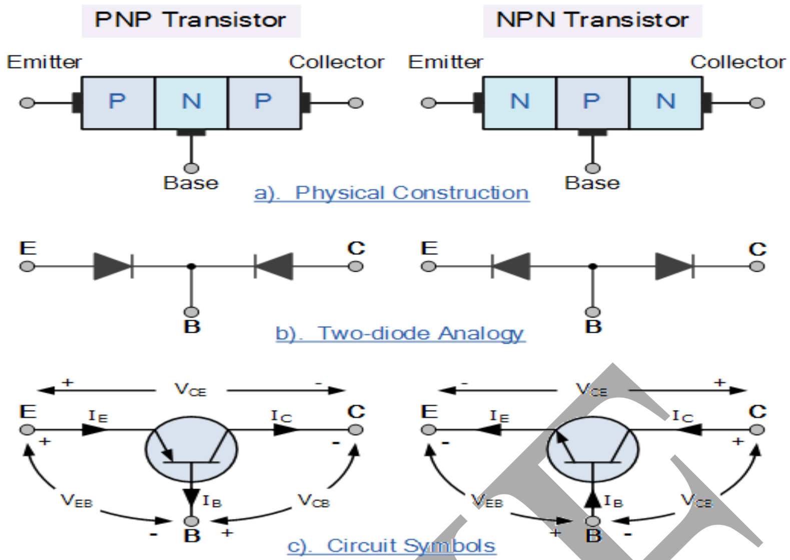
If we now join together two individual signal diodes back-to-back, this will give us two PN-junctions connected together in series that share a common **P** or **N** terminal. The fusion of these two diodes produces a three layer, two junction, three terminal device forming the basis of a **Bipolar Junction Transistor**, or **BJT** for short. Transistors are three terminal active devices made from different semiconductor materials that can act as either an insulator or a conductor by the application of a small signal voltage. The transistor's ability to change between these two states enables it to have two basic functions: "switching" (digital electronics) or "amplification" (analogue electronics). Then bipolar transistors have the ability to operate within three different regions:

1) Active Region – the transistor operates as an amplifier and $Ic = \beta.Ib$
2) Saturation – the transistor is "Fully-ON" operating as a switch and Ic = I(saturation)
3) Cut-off – the transistor is "Fully-OFF" operating as a switch and Ic = 0

A Typical Bipolar Transistor

The word Transistor is an acronym, and is a combination of the words Transfer aristorused to describe their mode of operation way back in their early days of development. There are two basic types of bipolar transistor construction, PNP and NPN, which basically escribes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. The **Bipolar Transistor** basic construction consists of two PN-junctions producing three connecting terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP andNPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type.

Bipolar Transistor Construction



The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

Possible Questions

Part –B

1. What is PN junction ?
2. What is depletion region?
3. Define diode.
4. Define semiconductor,
5. What is static resistance ?
6. What is dynamic resistance?
7. Write the application of solar cell.
8. Write the application of Photo diode.
9. Write the application of LED.
10. Give the symbol of LED.
11. Give the symbol of Solar Cell.
12. What is called solar cell?

Part –C

1. Explain the current flow mechanism in forward and reveres bias condition.
2. Explain in detail about P and N type semiconductors.
3. Explain Barrier Formation in PN Junction Diode.
4. Explain working principle and structure of LED.
5. Explain working principle and structure of Solar Cell
6. Explain working principle and structure of Photodiode.
7. What is LED? Explain the operation of a LED and write its applications.
8. Explain in detail about n-p-n and p-n-p transistors.

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(For Candidates Admitted From 2017 Onwards)

DEPARTMENT OF PHYSICS

UNIT II: Objective Type/Multiple choice Questions each Question carries one Mark

SL	Question	OPTION A	OPTION B	OPTION C	OPTION D	KEY
1	A zener diode has ………..	one pn junction	two pn junctions	three pn junctions	four junction	one pn junction
2	A zener diode is used as …………….	an amplifier	a voltage regulator	a rectifier	a multivibrator	voltage regulator
3	The doping level in a zener diode is …………… that of a crystal diode	the same as	less than	more than	equal	more than
4	A zener diode is always ……….. connected	reverse	forward	both forward and reverse	opposite	reverse
5	In the breakdown region, a zener didoe behaves like a ………….. source.	constant voltage	constant current	constant resistance	variable voltage	constant voltage
6	A zener diode is destroyed if it…………..	is forward biased	is reverse biased	carrier more than rated current	carrier is less than rated current	carrier more than rated current
7	A zener diode is …………………. device	a non-linear	a linear	an amplifying	unilateral	a non-linear
8	If the PIV rating of a diode is exceeded,	the diode conducts poorly	the diode is destroyed	the diode behaves like a zener diode	diode conducts normally	the diode is destroyed
9	The ……………….. filter circuit results in the best voltage regulation	choke input	capacitor input	resistance input	inductance input	choke input
10	The maximum efficiency of a half-wave rectifier is	40.6 %	50.00%	35%	80%	40.60%

11	The most widely used rectifier is ………………	half-wave rectifier	centre-tap full-wave rectifier	bridge full-wave rectifier	filter	bridge full-wave rectifier
12	If the junction temperature of LED is increased the radiant output power:	Decreases	Increases	same	propotional	decreases
13	The LED is usually made of materials like:	GaAs	CU	C	Al	GaAS
14	What does LED stands for	Light emitting doide	Light emitting detector	light energy disply	light emitting disply	Light emitting doide
15	The most commonly used semiconductor in the manufacture of a transistor is …………	germanium	Silicon	Aluminium	galium	Silicon
16	A zener diode is used as …………….	an amplifier	a voltage regulator	a rectifier	a multivibrator	voltage regulator
17	A zener diode is destroyed if it…………..	is forward biased	is reverse biased	carrier more than rated current	carrier is less than rated current	carrier more than rated current
18	The ……………….. filter circuit results in the best voltage regulation	choke input	capacitor input	resistance input	inductance input	choke input
19	If the junction temperature of LED is increased the radiant output power:	Decreases	Increases	same	propotional	decreases
20	The arrow in the symbol of a transistor indicates the direction of	electron current in the emitter	electron current in the collector	hole current in the emitter	donor ion current	hole current in the emitter
21	In what range of voltages is the transistor in the linear region of its operation?	$0 < V_{CE}$	$0.7 < V_{CE} < V_{CE(max)}$	$V_{CE(max)} > V_{CE}$	Vce.	$0.7 < V_{CE} < V_{CE(max)}$
22	The arrow in the symbol of a transistor indicates the direction of	electron current in the emitter	electron current in the collector	hole current in the emitter	donor ion current	hole current in the emitter
23	In a transistor, signal is transferred from a …………… circuit	high resistance to low resistance	low resistance to high resistance	high resistance to high resistance	. low resistance to low resistance	low resistance to high resistance

24	As the temperature of a transistor goes up, the base-emitter resistance ……………	Decreases	Increases	same	propotional	decreases
25	In what range of voltages is the transistor in the linear region of its operation?	$0 < V_{CE}$	$0.7 < V_{CE} < V_{CE(max)}$	$V_{CE(max)} > V_{CE}$	Vce.	$0.7 < V_{CE} < V_{CE(max)}$
26	What is (are) general-purpose/small-signal transistors case type(s)?	TO-18	TO-92	TO-39	TO-92,TO-18 ,TO-39	TO-92,TO-18 ,TO-39
27	The magnitude of dark current in a phototransistor usually falls in what range?	mA	µA	nA	pA	nA
28	First solar cell was invented in 1883 by	George Fritts.	Jefferson Fritts.	Charles Fritts.	Fornster Fritts.	Charles Fritts.
29	Most of the majority carriers from the emitter ………………..	recombine in the base	recombine in the emitter	pass through the base region to the collector	recombine in collector	pass through the base region to the collector
30	The current IB is …………	electron current	hole current	donor ion current	acceptor ion current	electron current
31	In a transistor …	IC = IE + IB	IB = IC + IE	IE = IC – IB	IE = IC + IB	IE = IC + IB
32	The value of α of a transistor is ……	1	>1	<1	0	<1
33	The output impedance of a transistor is …	low	high	0	very low	high
34	If the value of α is 0.9, then value of β is ………..	90	10	30	55	90
35	The leakage current in CE arrangement is ……………. that in CB arrangemen	more than	less than	the same as	equal	more than
36	The collector-base junction in a transistor has …	forward bias at all times	reverse bias at all times	low resistance	high resistance	reverse bias at all times

37	The emitter-base junction in a transistor has …	forward bias at all times	reverse bias at all times	low resistance	high resistance	forward bias at all times
38	The term photo voltaic comes from ________	Spanish	Greek	German	English	Greek
39	The volt is the units of emf that was named after its inventor _________	Alessandro volta	Alxender volta	Alexa volta	Alexandro volta	Alessandro volta
40	The term photo voltaic is in use since _________	1840	1844	1849	1850	1849
41	The region where the electrons and holes diffused across the junction is called ________	Depletion Junction	Depletion region	Depletion space	Depletion boundary	Depletion region
42	The amount of photo generated current increases slightly with increase in _________	Temperature	Photons	Diode current	Shunt current	Temperature
43	Solar cells are made from bulk materials that are cut into wafer of _________ thickness.	120-180µm	120-220µm	180-220µm	180-240µm	180-240µm
44	__________ photo voltaic devices in the form of thin films.	Cadmium Telluroide	Cadmium oxide	Cadmium sulphide	Cadmium sulphate	Cadmium Telluroide
45	__________ is a direct band gap material	Copper Indium Gallium Selenide	Copper Selenide	Copper Gallium Telluride	Copper Indium Gallium Diselenide	Copper Indium Gallium Selenide
46	Dye-sensitized solar cells are made from ________ organic dye.	Ruthium melallo	Aniline	Safranine	Induline	Ruthium melallo
47	Quantum dot solar cells are based on _______	Gratzel cell	Solar cell	Voltaic cell	Galvanic cell	Gratzel cell
48	The quantum dot used are _______	Cds	CdTe	PbO	GaAs	Cds

49	____________ has more sophisticated structure than p-i-n photodiode.	Avalanche photodiode	p-n junction diode	Zener diode	Varactor diode	Avalanche photodiode
50	________ is fully depleted by employing electric fields.	Avalanche photodiode	P-I-N diode	Varactor diode	P-n diode	Avalanche photodiode
51	At high gain, avalanche buildup time _________	Is negligible	Very less	Increases gradually	Dominates	Dominates

UNIT-III

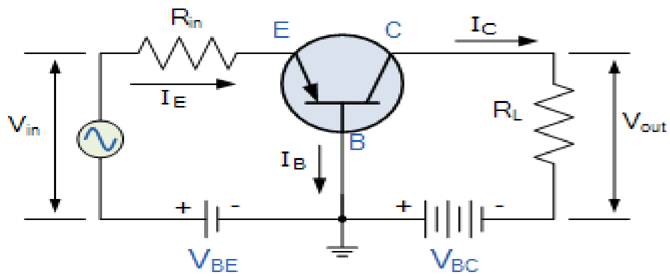
SYLLABUS

UNIT III
Characteristics of CB, CE and CC Configurations. Active, Cutoff & Saturation regions Current gains α and β. Relations between α and β. Load Line analysis of Transistors. DC Load line & Q-point. Voltage Divider Bias Circuit for CE Amplifier. h-parameter Equivalent Circuit. Analysis of single-stage CE amplifier using hybrid Model. Input & output Impedance. Current, Voltage and Power gains. Class A, B & C Amplifiers

The Common Base (CB) Configuration

As its name suggests, in the **Common Base** or grounded base configuration, the BASE connection is common to both the input signal AND the output signal with the input signal being applied between the base and the emitter terminals. The corresponding output signal is taken from between the base and the collector terminals as shown with the base terminal grounded or connected to a fixed reference voltage point.
The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less than the emitter current input resulting in a current gain for this type of circuit of "1" (unity) or less, in other words the common base configuration "attenuates" the input signal.

The Common Base Transistor Circuit



This type of amplifier configuration is a non-inverting voltage amplifier circuit, in that the signal voltages Vin and Vout are "in-phase". This type of transistor arrangement is not very common due to its unusually high voltage gain characteristics. Its input characteristics represent that of a forward biased diode while the output characteristics represent that of an illuminated photo-diode.

Also this type of bipolar transistor configuration has a high ratio of output to input resistance or more importantly "load" resistance (RL) to "input" resistance (Rin) giving it a value of "Resistance Gain". Then the voltage gain (Av) for a common base configuration is therefore given as:

Common Base Voltage Gain

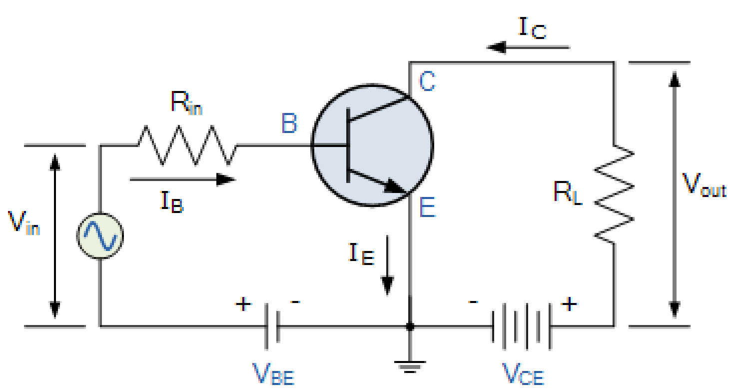
$$A_V = \frac{Vout}{Vin} = \frac{I_C \times R_L}{I_E \times R_{IN}}$$

Where: Ic/Ie is the current gain, alpha (α) and RL/Rin is the resistance gain.
The common base circuit is generally only used in single stage amplifier circuits such as microphone pre-amplifier or radio frequency (Rf) amplifiers due to its very good high frequency response.

The Common Emitter (CE) Configuration

In the **Common Emitter** or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the "normal" method of bipolar transistor connection. The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.

The Common Emitter Amplifier Circuit



In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib.

As the load resistance (RL) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, (β). As the emitter current for a common emitter configuration is defined asIe = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity. Since the electrical relationship between these three currents, Ib, Ic and Ieis determined by the physical construction of the transistor itself, any small change in the base current (Ib), will result in a much larger change in the collector current (Ic). Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminal. By combining the expressions for both Alpha, α and Beta, β the mathematical relationship between these parameters and therefore the current gain of the transistor can be given as:

$$\text{Alpha}, (\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta}, (\beta) = \frac{I_C}{I_B}$$

$$\therefore I_C = \alpha . I_E = \beta . I_B$$

$$\text{as:} \ \alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

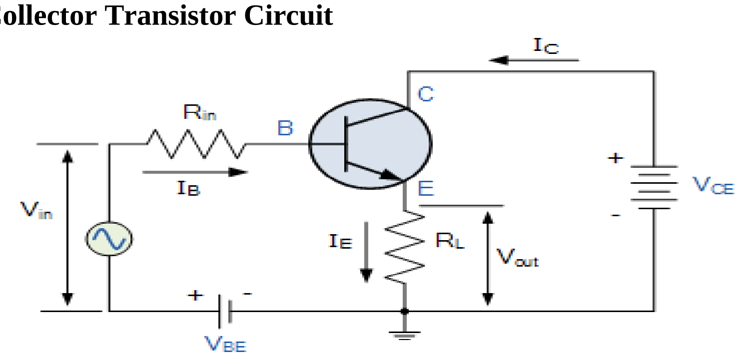
$$I_E = I_C + I_B$$

Where: "Ic" is the current flowing into the collector terminal, "Ib" is the current flowing into the base terminal and "Ie" is the current flowing out of the emitter terminal. Then to summarise a little. This type of bipolar transistor configuration has a greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal is 180^o "out-of-phase" with the input voltage signal.

The Common Collector (CC) Configuration

In the **Common Collector** or grounded collector configuration, the collector is now common through the supply. The input signal is connected directly to the base, while the output is taken from the emitter load as shown. This type of configuration is commonly known as a**Voltage Follower** or **Emitter Follower** circuit. The common collector, or emitter follower configuration is very useful for impedance matching applications because of the very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

The Common Collector Transistor Circuit



The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. In the common collector configuration the load resistance is situated in series with the emitter so its current is equal to that of the emitter current. As the emitter current is the combination of the collector AND the base current combined, the load resistance in this type of transistor configuration also has both the collector current and the input current of the base flowing through it. Then the current gain of the circuit is given as:

The Common Collector Current Gain

$$I_E = I_C + I_B$$

$$A_i = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B}$$

$$A_i = \frac{I_C}{I_B} + 1$$

$$A_i = \beta + 1$$

This type of bipolar transistor configuration is a non-inverting circuit in that the signal voltages of Vin and Vout are "in-phase". It has a voltage gain that is always less than "1" (unity). The load resistance of the common collector transistor receives both the base and collector currents giving a large current gain (as with the common emitter configuration) therefore, providing good current amplification with very little voltage gain.

We can now summarise the various relationships between the transistors individual DC currents flowing through each leg and its DC current gains given above in the following table.

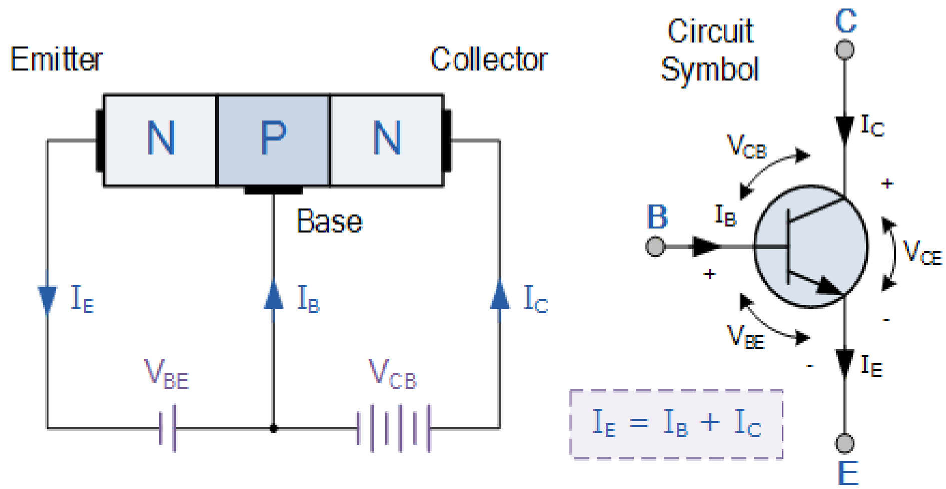
Relationship between DC Currents and Gains

$I_E = I_B + I_C$ $I_C = I_E - I_B$ $I_B = I_E - I_C$	$\alpha = \frac{I_C}{I_E} = \frac{\beta}{1+\beta}$ $\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$
$I_B = \frac{I_C}{\beta} = \frac{I_E}{1+\beta} = I_E(1-\alpha)$	
$I_C = \beta.I_B = \alpha.I_E$	$I_E = \frac{I_C}{\alpha} = I_B(1+\beta)$

Bipolar Transistor Summary

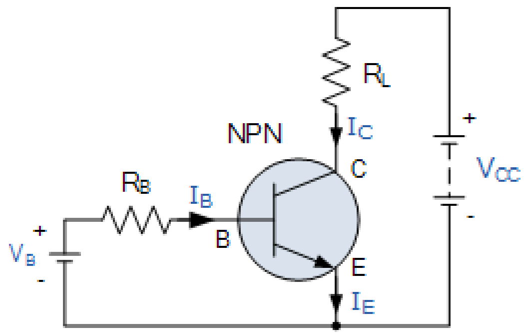
Then to summarise, the behaviour of the bipolar transistor in each one of the above circuit configurations is very different and produces different circuit characteristics with regards to input impedance, output impedance and gain whether this is voltage gain, current gain or power gain and this is summarised in the table below. The most commonly used transistor configuration is the **NPN Transistor**. We also learnt that the junctions of the bipolar transistor can be biased in one of three different ways – **Common Base**, **Common Emitter** and**Common Collector**. In this tutorial about bipolar transistors we will look more closely at the "Common Emitter" configuration using the **Bipolar NPN Transistor** with an example of the construction of a NPN transistor along with the transistors current flow characteristics is given below.

A Bipolar NPN Transistor Configuration



(Note: Arrow defines the emitter and conventional current flow, "out" for a Bipolar NPN Transistor.)

The construction and terminal voltages for a bipolar NPN transistor are shown above. The voltage between the Base and Emitter (V_{BE}), is positive at the Base and negative at the Emitter because for an NPN transistor, the Base terminal is always positive with respect to the Emitter. Also the Collector supply voltage is positive with respect to the Emitter (V_{CE}). So for a bipolar NPN transistor to conduct the Collector is always more positive with respect to both the Base and the Emitter.



NPN Transistor Connection

Then the voltage sources are connected to an NPN transistor as shown. The Collector is connected to the supply voltage V_{CC} via the load resistor, RL which also acts to limit the maximum current flowing through the device. The Base supply voltage V_B is connected to the Base resistor R_B, which again is used to limit the maximum Base current. So in a NPN Transistor it is the movement of negative current carriers (electrons) through the Base region that constitutes transistor action, since these mobile electrons provide the link between the Collector and Emitter circuits. This link between the input and output circuits is the main feature of transistor action because the transistors amplifying properties come from the consequent control which the Base exerts upon the Collector to Emitter current. Then we can see that the transistor is a current operated device (Beta model) and that a large current (Ic) flows freely through the device between the collector and the emitter terminals when the transistor is switched “fully-ON”. However, this only happens when a small biasing current (Ib) is flowing into the base terminal of the transistor at the same time thus allowing the Base to act as a sort of current control input.

The transistor current in a bipolar NPN transistor is the ratio of these two currents (Ic/Ib), called the *DC Current Gain* of the device and is given the symbol of hfe or nowadays Beta, (β). The value of β can be large up to 200 for standard transistors, and it is this large ratio between Ic and Ib that makes the bipolar NPN transistor a useful amplifying device when used in its active region as Ib provides the input and Ic provides the output. Note that Beta has no units as it is a ratio. Also, the current gain of the transistor from the Collector terminal to the Emitter terminal, Ic/Ie, is called Alpha, (α), and is a function of the transistor itself (electrons diffusing across the junction). As the emitter current Ie is the sum of a very small base current plus a very large collector current, the value of alpha α, is very close to unity, and for a typical low-power signal transistor this value ranges from about 0.950 to 0.999

α and β Relationship in a NPN Transistor

$$\text{DC Current Gain} = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \;\ldots\ldots\; (\text{KCL}) \quad \text{and} \quad \frac{I_C}{I_E} = \alpha$$

$$\text{Thus:} \quad I_B = I_E - I_C$$

$$I_B = I_E - \alpha I_E$$

$$I_B = I_E\,(1-\alpha)$$

$$\therefore \quad \beta = \frac{I_C}{I_B} = \frac{I_C}{I_E\,(1-\alpha)} = \frac{\alpha}{1-\alpha}$$

By combining the two parameters α and β we can produce two mathematical expressions that gives the relationship between the different currents flowing in the transistor.

$$\alpha = \frac{\beta}{\beta+1} \text{ or } \alpha = \beta(1-\alpha)$$

$$\beta = \frac{\alpha}{1-\alpha} \text{ or } \beta = \alpha(1+\beta)$$

$$\text{If } \alpha = 0.99 \quad \beta = \frac{0.99}{0.01} = 99$$

The values of Beta vary from about 20 for high current power transistors to well over 1000 for high frequency low power type bipolar transistors. The value of Beta for most standard NPN transistors can be found in the manufactures data sheets but generally range between 50 – 200.

The equation above for Beta can also be re-arranged to make Ic as the subject, and with a zero base current (Ib = 0) the resultant collector current Ic will also be zero, (β x 0). Also when the base current is high the corresponding collector current will also be high resulting in the base current controlling the collector current. One of the most important properties of the **Bipolar Junction Transistor** is that a small base current can control a much larger collector current.

Amplifier Classes

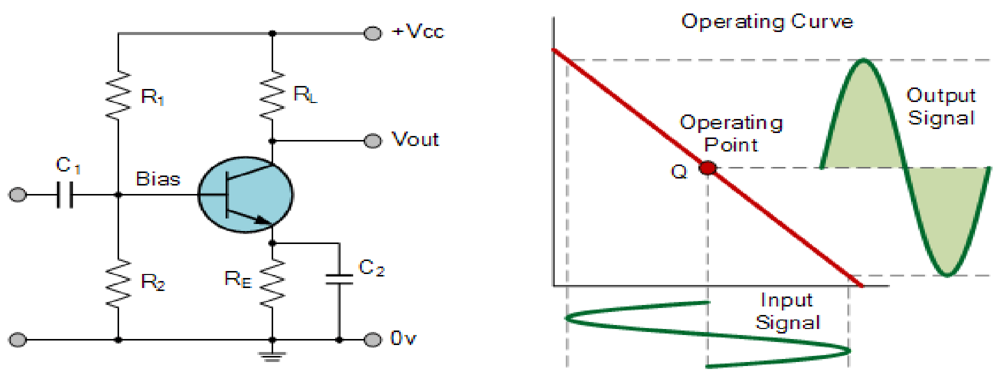
The classification of an amplifier as either a voltage or a power amplifier is made by comparing the characteristics of the input and output signals by measuring the amount of time in relation to the input signal that the current flows in the output circuit.For the transistor to operate within its “Active Region” some form of “Base Biasing” was required. This small Base Bias voltage added to the input signal allowed the transistor to reproduce the full input waveform at its output with no loss of signal.However, by altering the position of this Base bias voltage, it is possible to operate an amplifier in an amplification mode other than that for full waveform reproduction.

With the introduction to the amplifier of a Base bias voltage, different operating ranges and modes of operation can be obtained which are categorized according to their classification. These various mode of operation are better known as Amplifier Class.Audio power amplifiers are classified in an alphabetical order according to their circuit configurations and mode of operation. Amplifiers are designated by different classes of operation such as class "A", class "B", class "C", class "AB", etc. These different amplifier classes range from a near linear output but with low efficiency to a non-linear output but with a high efficiency.

No one class of operation is "better" or "worse" than any other class with the type of operation being determined by the use of the amplifying circuit. There are typical maximum efficiencies for the various types or class of amplifier, with the most commonly used being:

1) Class A Amplifier – has low efficiency of less than 40% but good signal reproduction and linearity.
2) Class B Amplifier – is twice as efficient as class A amplifiers with a maximum theoretical efficiency of about 70% because the amplifying device only conducts (and uses power) for half of the input signal.
3) Class AB Amplifier – has an efficiency rating between that of Class A and Class B but poorer signal reproduction than class A amplifiers.
4) Class C Amplifier – is the most inefficient amplifier class as only a very small portion of the input signal is amplified therefore the output signal bears very little resemblance to the input signal. Class C amplifiers have the worst signal reproduction.
5)

Class A Amplifier



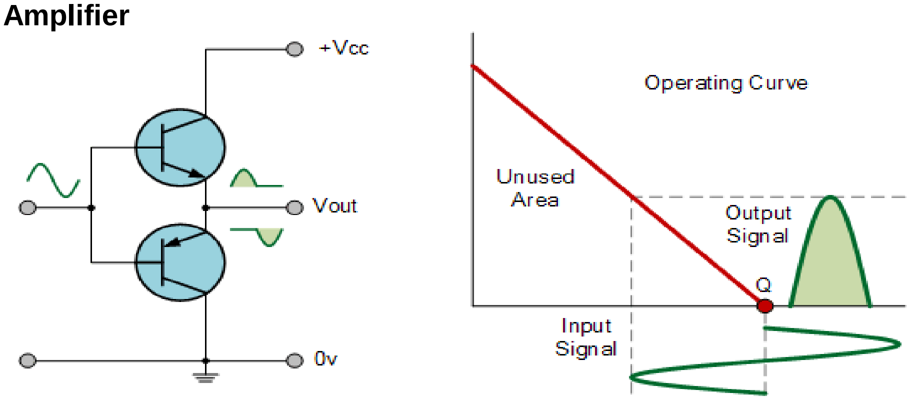
To achieve high linearity and gain, the output stage of a class A amplifier is biased "ON" (conducting) all the time. Then for an amplifier to be classified as "Class A" the zero signal idle current in the output stage must be equal to or greater than the maximum load current (usually a loudspeaker) required to produce the largest output signal.As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform. Then the class A amplifier is equivalent to a current source.Since a class A amplifier operates in the linear region, the transistors base (or gate) DC biasing voltage should by chosen properly to ensure correct operation and low distortion.

However, as the output device is "ON" at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier. Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30%, making them impractical for high-power amplifications. Also due to the high idling current of the amplifier, the power supply must be sized accordingly and be well filtered to avoid any amplifier hum and noise. Therefore, due to the low efficiency and over heating problems of Class A amplifiers, more efficient amplifier classes have been developed.

Class B Amplifier

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform.In the class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier. However, the price paid for the improvement in the efficiency is in the linearity of the switching device.

Class B Amplifier



When the input signal goes positive, the positive biased transistor conducts while the negative transistor is switched "OFF". Likewise, when the input signal goes negative, the positive transistor switches "OFF" while the negative biased transistor turns "ON" and conducts the negative portion of the signal. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal.

Then we can see that each transistor device of the class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

This push-pull design of amplifier is obviously more efficient than Class A, at about 50%, but the problem with the class B amplifier design is that it can create distortion at the zero-crossing point of the waveform due to the transistors dead band of input base voltages from -0.7V to +0.7.. Then in a class B amplifier, the output transistor is not "biased" to an "ON" state of operation until this voltage is exceeded.This means that the the part of the waveform which falls within this 0.7 volt window will not be reproduced accurately making the class B amplifier unsuitable for precision audio amplifier applications.

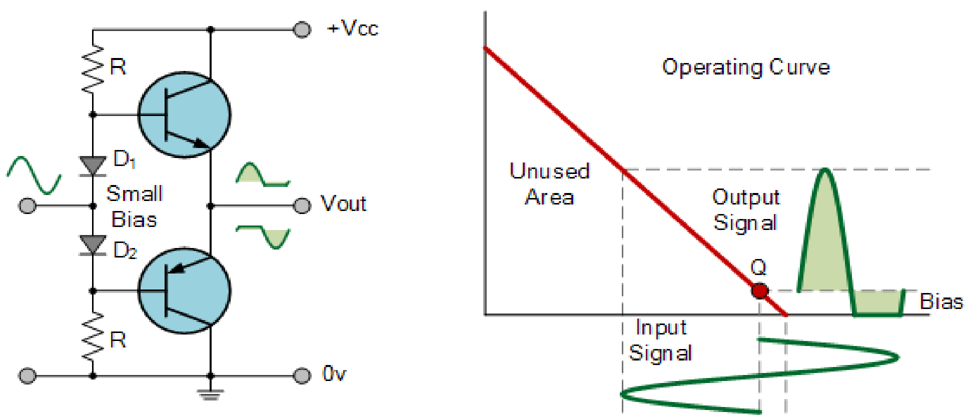
Class AB Amplifier

As its name suggests, the Class AB Amplifier is a combination of the “Class A” and the “Class B” type amplifiers we have looked at above. The AB classification of amplifier is currently one of the most common used types of audio power amplifier design. The class AB amplifier is a variation of a class B amplifier as described above, except that both devices are allowed to conduct at the same time around the waveforms crossover point eliminating the crossover distortion problems of the previous class B amplifier.

The two transistors have a very small bias voltage, typically at 5 to 10% of the quiescent current to bias the transistors just above its cut-off point. Then the conducting device, either bipolar of FET, will be “ON” for more than one half cycle, but much less than one full cycle of the input signal. Therefore, in a class AB amplifier design each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

In other words, the conduction angle of a class AB amplifier is somewhere between 180^o and 360^o depending upon the chosen bias point as shown.

Class AB Amplifier



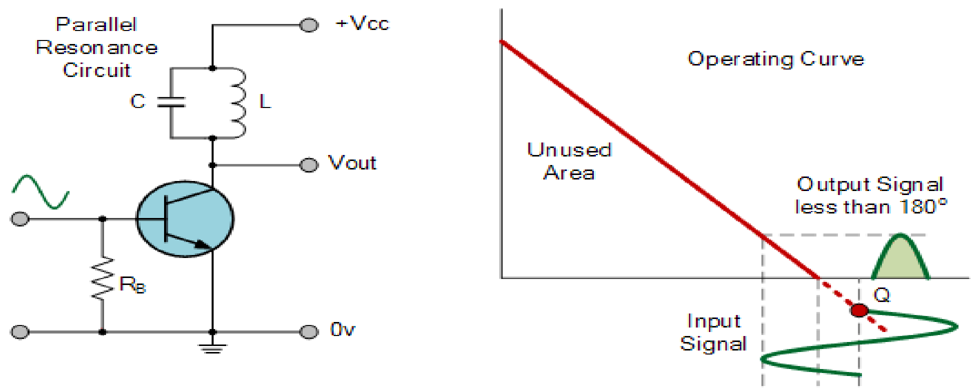
The advantage of this small bias voltage, provided by series diodes or resistors, is that the crossover distortion created by the class B amplifier characteristics is overcome, without the inefficiencies of the class A amplifier design. So the class AB amplifier is a good compromise between class A and class B in terms of efficiency and linearity, with conversion efficiencies reaching about 50% to 60%.

Class C Amplifier

The Class C Amplifier design has the greatest efficiency but the poorest linearity of the classes of amplifiers mentioned here. The previous classes,A, B and AB are considered linear amplifiers, as the output signals amplitude and phase are linearly related to the input signals amplitude and phase.However, the class C amplifier is heavily biased so that the output current is zero for more than one half of an input sinusoidal signal cycle with the transistor idling at its cut-off point. In other words, the conduction angle for the transistor is significantly less than 180 degrees, and is generally around the 90 degrees area.

While this form of transistor biasing gives a much improved efficiency of around 80% to the amplifier, it introduces a very heavy distortion of the output signal. Therefore, class C amplifiers are not suitable for use as audio amplifiers.

Class C Amplifier



Due to its heavy audio distortion, class C amplifiers are commonly used in high frequency sine wave oscillators and certain types of radio frequency amplifiers, where the pulses of current produced at the amplifiers output can be converted to complete sine waves of a particular frequency by the use of LC resonant circuits in its collector circuit.

Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30%, making them impractical for high-power amplifications. Also due to the high idling current of the amplifier, the power supply must be sized accordingly and be well filtered to avoid any amplifier hum and noise. Therefore, due to the low efficiency and over heating problems of Class A amplifiers, more efficient amplifier classes have been developed.

Possible Question

PART B

1. What is Transistor Biasing?
2. What is Voltage Divider Bias?
3. What is Class A amplifier?
4. What is Class B amplifier?
5. What is Class C amplifier ?
6. What is Cutoff and Saturation Regions of a transistor?
7. Define DC Load line.
8. Define Q-point.
9. Define Q-point
10. Define h-parameter

PART C

1. Analysis of a single-stage CE amplifier using Hybrid Model.
2. Derive the relations between α and β.
3. Explain the input and output characteristics of CB configuration.
4. Explain the input and output characteristics of CE configuration.
5. Explain the input and output characteristics of CC configuration.
6. Explain working principle of Class A amplifier.
7. Explain working principle of Class B amplifier.
8. Explain working principle of Class C amplifier.
9. Discuss DC Load line and Q-point.
10. Derive the expression for Current, Voltage and Power Gains of a transistor using h-parameter

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(For Candidates Admitted From 2017 Onwards)

DEPARTMENT OF PHYSICS

UNIT III: Objective Type/Multiple choice Questions each Question carries one Mark

SL.NO	QUESTION	OPTION –A	OPTION –B	OPTION –C	OPTION –D	ANSWER
1	In a transistor, signal is transferred from a …………… circuit	high resistance to low resistance	low resistance to high resistance	high resistance to high resistance	low resistance to low resistance	low resistance to high resistance
2	As the temperature of a transistor goes up, the base-emitter resistance ……………	Decreases	Increases	same	propotional	decreases
3	The voltage gain in a transistor connected in ………………. arrangement is the highest	CE	CB	CC	CBE	CE
4	The power gain in a transistor connected in ……………. arrangement is the highest	CE	CB	CC	CBE	CE
5	The most commonly used transistor arrangement is …………… arrangement	CE	CB	CC	CBE	CE
6	The emitter of a transistor is ………………… doped	heavily	moderately	lightly	no doping	heavily
7	The input impedance of a transistor is …………	low	high	0	very high	low
8	A transistor is a …………… operated device	current	voltage	both voltage and current	resistance	current

9	The element that has the biggest size in a transistor is ………………..	collector	base	emitter,	emitter and collector	collector
10	The base of a transistor is ………….. doped	heavily	moderately	lightly	no doping	lightly
11	The number of depletion layers in a transistor is …………	3	2	1	4	2
12	The device that exhibits negative resistance region is	FET	UJT	Triac	Diac	UJT
13	The UJT may be used as	amplifier	sawtooth generator	rectifier	switch	sawtooth generator
14	Which of the following is not a characteristic of UJT?	Intrinsic stand off ratio	Negative resistance	Peak-point voltage	Bilateral conduction	Bilateral conduction
15	When the JFET is no longer able to control the current, this point is called the	breakdown region	depletion region	saturation point	pinch-off region	breakdown region
16	With a JFET, a ratio of output current change against an input voltage change is called	gain	transconductance	siemens	resistivity	transconductance
17	Which type of JFET bias requires a negative supply voltage?	feedback	source	gate	voltage divider	gate
18	The type of bias most often used with E-MOSFET circuits is:	constant current	drain-feedback	voltage-divider	zero biasing	drain-feedback
19	The output of the comparator for CMOS IC’s is______	0.5V	1.2V	2.5V	4.5V	2.5V
20	Which component is considered to be an "OFF" device?	transistor	JFET	D-MOSFET	E-MOSFET	E-MOSFET
21	In N channel MOSFET which is the more negative of the elements?	source	gate	drain	source and drain	source

22	If the gate is given sufficiently large charge, electrons will be attracted to	drain region	channel region	switch region	bulk region	channel region
23	nMOS devices are formed in	p-type substrate of high doping level	n-type substrate of low doping level	p-type substrate of moderate doping level	n-type substrate of high doping level	p-type substrate of moderate doping level
24	Source and drain in nMOS device are isolated b	a single diode	two diodes	three diodes	four diodes	two diodes
25	In enhancement mode, device is in __________ condition	conducting	non conducting	partially conducting	insulating	non conducting
26	MOS transistor structure is	symmetrical	non symmetrical	semi symmetrical	pseudo symmetrical	symmetrical
27	nMOS is	donor doped	acceptor doped	no doping	insulating	acceptor doped
28	pMOS is	donor doped	acceptor doped	no doping	insulating	donor doped
29	Inversion layer in enhancement mode consists of excess of	positive carriers	negative carriers	both in equal quantity	neutral carriers	negative carriers
30	As source drain voltage increases, channel depth	increases	decreases	logarithmically increases	exponentially increses	decreases
31	If the n-MOS and p-MOS of the CMOS inverters are interchanged the output is measured at:	Source of the both transistor	Drains of the both transistor	Drain of n-MOS and source of p-MOS	Source of n-MOS and drain of p-MOS	Source of the both transistor
32	What will be the effect on output voltage if the positions of n-MOS and p-MOS in CMOS inverter circuit are exchanged?	Output is same	Output is reversed	Output is always high	Output is always low	Output is reversed
33	The volt is the units of emf that was named after its inventor __________	Alessandro volta	Alxender volta	Alexa volta	Alexandro volta	Alessandro volta
34	The term photo voltaic is in use since __________	1840	1844	1849	1850	1849

35	The region where the electrons and holes diffused across the junction is called _________	Depletion Junction	Depletion region	Depletion space	Depletion boundary	Depletion region
36	The amount of photo generated current increases slightly with increase in __________	Temperature	Photons	Diode current	Shunt current	Temperature
37	Solar cells are made from bulk materials that are cut into wafer of __________ thickness.	120-180µm	120-220µm	180-220µm	180-240µm	180-240µm
38	___________ photo voltaic devices in the form of thin films.	Cadmium Telluroide	Cadmium oxide	Cadmium sulphide	Cadmium sulphate	Cadmium Telluroide
39	___________ is a direct band gap material	Copper Indium Gallium Selenide	Copper Selenide	Copper Gallium Telluride	Copper Indium Gallium Diselenide	Copper Indium Gallium Selenide
40	Dye-sensitized solar cells are made from _________ organic dye.	Ruthium melallo	Aniline	Safranine	Induline	Ruth ium melallo
41	Quantum dot solar cells are based on ________	Gratzel cell	Solar cell	Voltaic cell	Galvanic cell	Gratzel cell

UNIT-IV

SYLLABUS

UNIT-IV Operational Amplifiers (Black Box approach):
Characteristics of an Ideal and Practical Op-Amp (IC 741), Open-loop and closed-loop Gain. CMRR, concept of Virtual ground. Applications of Op-Amps: Inverting and non-inverting Amplifiers, Adder, Subtractor, Differentiator, Integrator, Zero crossing detector.
Sinusoidal Oscillators: Barkhausen's Criterion for Self-sustained Oscillations. Determination of Frequency of RC Oscillator

Characteristics of Ideal Operational Amplifiers

An ideal op-amp would exhibit the following electrical characteristics:

1. Open loop Voltage Gain A0 is infinity.
2. Infinity input resistance Ri so that almost any signal source can be drive it and there is no loading of the preceding stage.
3. Zero output resistance R0 so that the output can be drive an infinity number of other devices.
4. Perfect Balance, i.e. the differential voltage in inverting and non-inverting terminals be zero.
5. Zero output voltage when input is zero.
6. Infinity bandwidth so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
7. Infinity common-mode rejection ratio so that the output common-mode noise voltage is zero.
8. Infinity slew rate so that output voltage changes occur simultaneously with input voltage changes.
9. Zero drift of characteristics with temperature

Characteristic of Practical Op-amp

There are practical op-amps that can be made to approximate some of these characteristics using a negative feedback arrangement. In practical, the input resistance, output resistance, and bandwidth can be brought close to ideal values by this method.

The practical op-amp has the following characteristics:

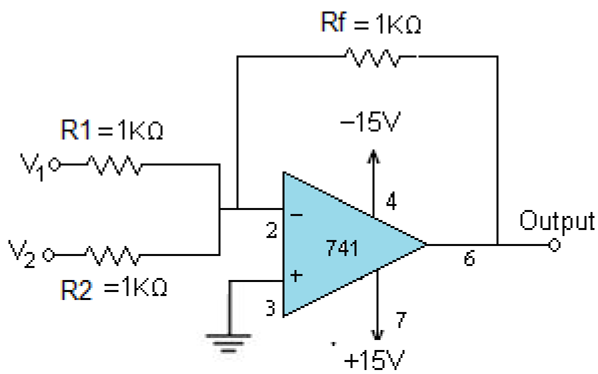
1. The open loop voltage gain A0 is maximum and finite, typical value for practical op-amp is considered to be 200,000.
2. The input impedance Zi is maximum and is finite i.e. in the order of 100k or more.
3. The output impedance Z0 is minimum not zero, in the order of 100 or less.
4. The CMRR is maximum and finite.
5. Bandwidth is maximum and finite i.e. it can amplify dc to 1 MHz signal.
6. Slight drift of characteristics due to the change in temperature not null.

7. Two terminal may be virtually ground not Vd = 0 exactly, for all conditions.
8. Maximum slow-rate and has the finite value.
9. Output is negligible due to dc-bias, when the input is zero.

Op-Amp Adder and Subtractor Circuits

The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called "virtual ground", i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

Adder Circuit:



1. Connect the circuit as per the diagram.
2. Apply the supply voltages of +15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown.
4. Apply two different signals (DC/AC) to the inputs.
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 adder circuit.
6. Notice that the output is equal to the sum of the two inputs.

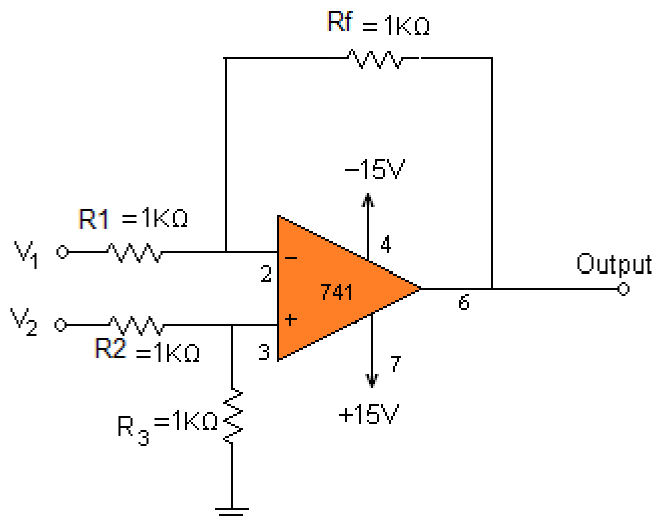
Calculation: Adder

- $V_o = -(V_1 + V_2)$
- If $V_1 = 2V$ and $V_2 = 2V$, then
- $V_o = -(2+2) = -4V$.

Subtractor:

The subtractor circuit, input signals can be scaled to the desired values by selecting appropriate values for the resistors. When this is done, the circuit is referred to as scaling amplifier. However in this circuit all external resistors are equal in value. So the gain of amplifier is equal to one. The output voltage V_o is equal to the voltage applied to the non-inverting terminal minus the voltage applied to the inverting terminal; hence the circuit is called a subtractor.

Subtractor circuit



1. Connect the circuit as per the diagram.
2. Apply the supply voltages of +15V to pin7 and pin4 of IC741 respectively.
3 Apply the inputs V_1 and V_2.
4. Apply two different signals (DC/AC) to the inputs.
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 subtractor circuit.
6. Notice that the output is equal to the difference of the two inputs

Calculation: Subtractor

- $V_o = V_2 – V_1$
- If V_1=4 and V_2 = 2, then
- V_o = 4 – 2 = -2

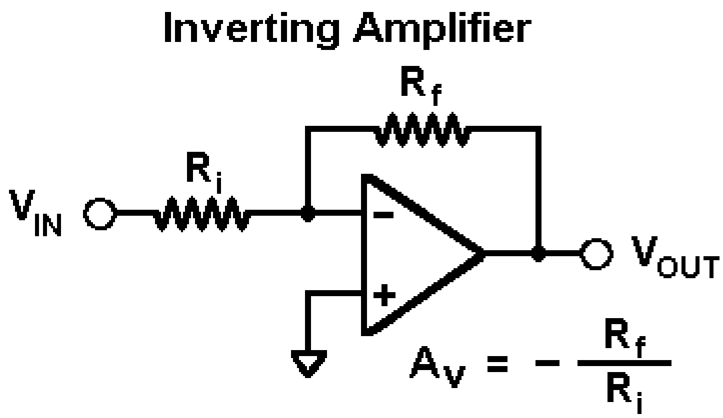
Inverting amplifier

Definition

Inverting amplifier is one in which the output is exactly 1800 out of phase with respect to input(i.e. if you apply a positive voltage, output will be negative). Output is an inverted(in terms of phase) amplified version of input.

Circuit operation

The inverting amplifier using opamp is shown in the figure below



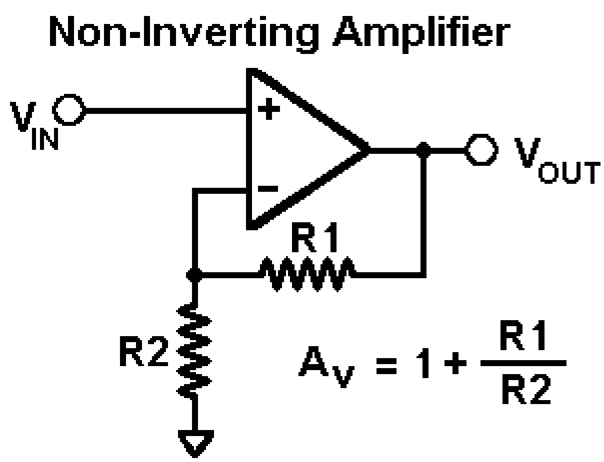
Applying KCL at inverting node we get (0-Vi)/Ri+(0-Vo)/Rf = 0
By rearranging the terms we will get Voltage gain Av = Vo/ Vi = – Rf/Ri .
Gain
Gain of inverting amplifier Av= – Rf/Ri.

Non Inverting amplifier

Non Inverting amplifier is one in which the output is in phase with respect to input(i.e. if you apply a positive voltage, output will be positive). Output is an Non inverted(in terms of phase) amplified version of input.

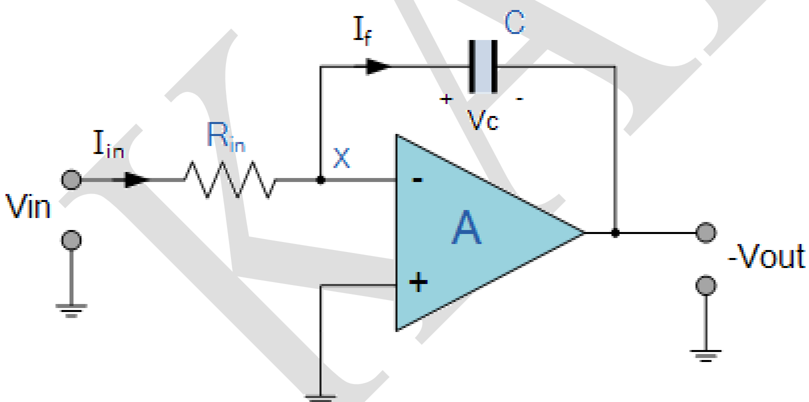
Circuit operation

The inverting amplifier using opamp is shown in the figure below



Assuming the opamp is ideal and applying the concept of virtual short, the voltage at the inverting terminal is equal to non inverting terminal.
Applying KCL at inverting node we get (Vi-Vo)/R2+(Vo-0)/R1 = 0
By rearranging the terms we will get Voltage gain Av = Vo/ Vi = (1+ Rf/Ri)
Gain
Gain of non inverting amplifier Av= (1+ Rf/Ri).

Op-amp Integrator Circuit

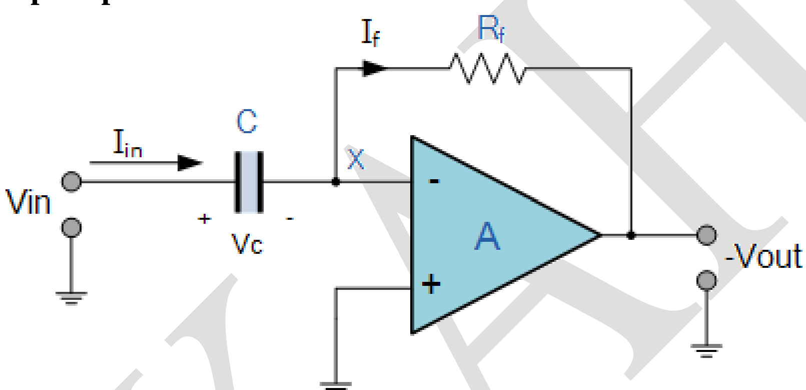


As its name implies, the Op-amp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration, that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.
When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between

the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of Xc/Rin is also very small giving an overall voltage gain of less than one, (voltage follower circuit).
As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, (τ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.
Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage, Vc developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

Op-amp Differentiator Circuit



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.
At low frequencies the reactance of the capacitor is "High" resulting in a low gain (Rf/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor Rf.

Ok, some math's to explain what's going on!. Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is:

$$\frac{dQ}{dt} = C\,\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current,i

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore\ -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

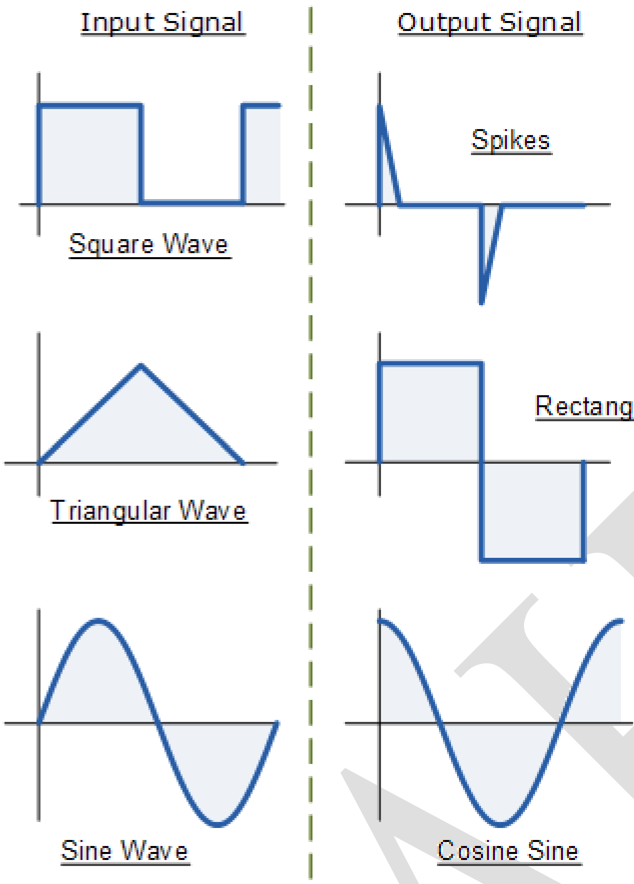
$$V_{OUT} = -R_F C\,\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant -Rf.C times the derivative of the input voltage Vin with respect to time. The minus sign indicates a 180o phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

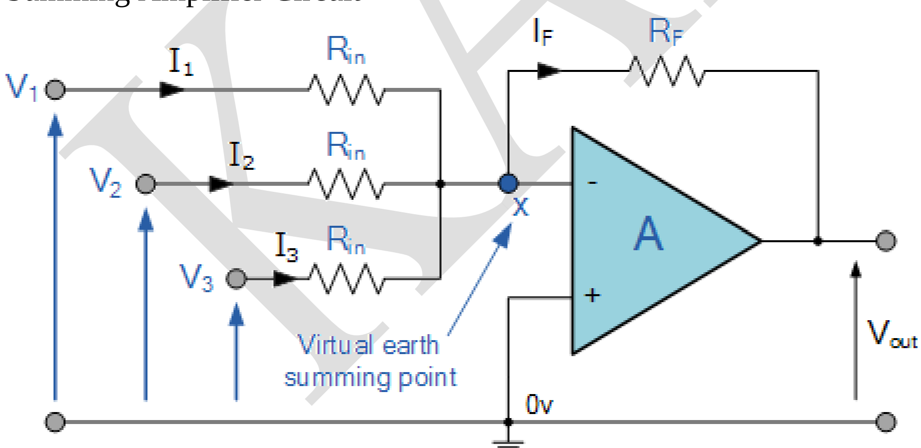
One final point to mention, the Op-amp Differentiator circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required.

Op-amp Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.



Summing Amplifier Circuit



In this simple summing amplifier circuit, the output voltage, (Vout) now becomes proportional to the sum of the input voltages, V1, V2, V3, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, (Rin) are equal in value, we can simplify the above equation to give an output voltage of:
Summing Amplifier Equation

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots .etc\right)$$

We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltagesV1, V2 and V3. We can also add more inputs if required as each individual input "see's" their respective resistance, Rin as the only input impedance.
This is because the input signals are effectively isolated from each other by the "virtual earth" node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and Rf is equal to Rin.
Note that when the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.
A Scaling Summing Amplifier can be made if the individual input resistors are "NOT" equal. Then the equation would have to be modified to:

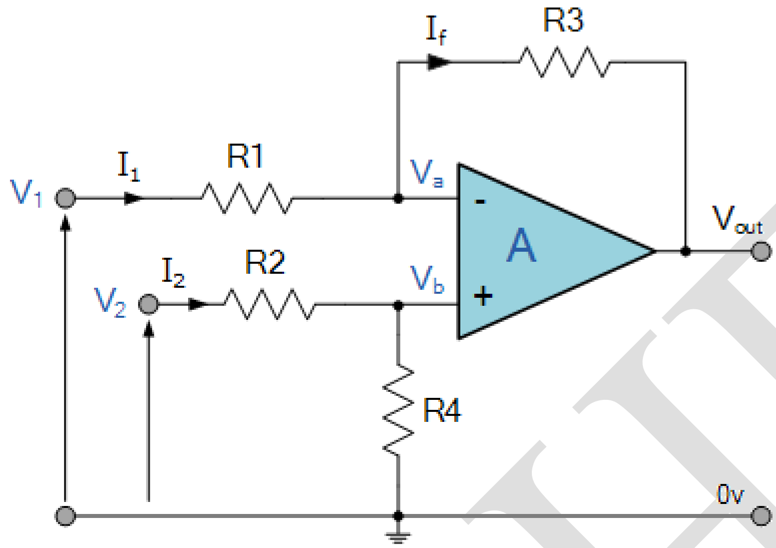
$$-Vout = V1\left(\frac{Rf}{R1}\right) + V2\left(\frac{Rf}{R2}\right) + V3\left(\frac{Rf}{R3}\right) \ldots .etc$$

To make the math's a little easier, we can rearrange the above formula to make the feedback resistor RF the subject of the equation giving the output voltage as:

$$-Vout = Rf\left(\frac{V1}{R1} + \frac{V2}{R2} + \frac{V3}{R3}\right) \ldots .etc$$

This allows the output voltage to be easily calculated if more input resistors are connected to the amplifiers inverting input terminal. The input impedance of each individual channel is the value of their respective input resistors, ie, R1, R2, R3 … etc.

Differential Amplifier



By connecting each input in turn to 0v ground we can use superposition to solve for the output

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

voltage Vout.
When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:
Differential Amplifier Equation

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

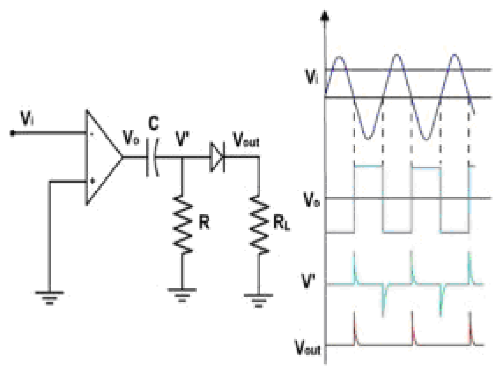
If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a Unity Gain Differential Amplifier and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = V2 – V1. Also note that if inputV1 is higher than input V2 the output voltage sum will be negative, and ifV2 is higher than V1, the output voltage sum will be positive.

Op amp zero crossing detector

In opamp zero crossing detectors the output responds almost discontinuously every time the input passes through zero. It consists of a comparator circuit followed by differentiator and diode arrangement.

Circuit operation

The circuit of zero crossing detector is shown in the figure below



Since the opamp is in open loop configuration Vo = Av*(Vi-0) the output of opamp i.e. Vo will be at Positive saturation voltage +Vcc when ever Vi > 0 V and is at negative saturation voltage -Vcc when Vi < 0 V. whenever the output of opamp transits from +Vcc to -Vcc the capacitor C charges to +Vcc if the output of opamp changes from -Vcc to +Vcc and it discharges through R to -Vcc if the output of opamp changes from -Vcc to +Vcc .The differentiator circuit(combination of capacitor and resistor) provides an output V' = R*C*dVo/dt consisting of peaks at times where the square wave crosses zero voltage. The diode is kept to filter off the zero crossings where input voltage crosses zero voltage in rising fashion

Possible Questions

PART B

1. Write short note on open-loop gain.
2. Write short note on closed-loop gain.
3. Write short note on Virtual ground.
4. Write short note on Zero crossing detector.
5. What is inverting amplifiers?
6. What is a non-inverting amplifier?
7. What are the ideal Characteristics of op-amp
8. What are the practical Characteristics of op-amp
9. What is a non-inverting amplifier?
10. How op-amp can be used as an integrator?
11. How op-amp can be used as a Differentiator?
12. How op-amp can be used as an adder?
13. How op-amp can be used as a Subtractor?

PART C

1. Explain the characteristics of an Ideal and Practical Op-Amp.
2. Explain the concept of Virtual ground.
3. Explain in detail about Differentiator and Integrator.
4. Explain in detail about Inverting and non-inverting amplifiers.
5. Explain in detail about Adder and Subtractor.

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(For Candidates Admitted From 2017 Onwards)

DEPARTMENT OF PHYSICS

UNIT IV: Objective Type/Multiple choice Questions each Question carries one Mark

Sl.NO	QUESTION	OPTION A	OPTION B	OPTION C	OPTION D	ANSWER
1	An ideal operational amplifier has_____	Unity open loop gain	Zero input impedance	Infinite output impedance	Infinite bandwidth	Infinite bandwidth
2	The gain of an operational amplifier_____at high frequencies because of capacitances within operational amplifier	Decreases	Increases	Zero	Infinite	Decreases
3	An operational amplifier can amplify_______	Only AC	Only DC	AC and DC	Any current	AC and DC
4	The two input terminals of an operational amplifier are known as_____	Positive & Negative	Differential & Non differential	Inverting & Non inverting	High & low	Inverting & Non inverting
5	The operational amplifier input is a ______ amplifier	Inverting	Non Inverting	Differential	Summing	Differential
6	The gain of an actual operational amplifier is around______	1000	10000	1,00,000	10,00,000	10,00,000
7	IC 741 is ______ operational amplifier	Frequency compensated	Amplitude compensated	Time compensated	Pulse Compensated	Frequency compensated
8	IC 741 offset Voltage adjustment range is____	15mV	10 mV	12 mV	14 mV	15mV
9	CMRR stands for ______	Common Modulation Rejection Ratio	Common Mode Rejection Ratio	Collector Mode Resictor Ratio	Collector Mode Rejection Ratio	Common Mode Rejection Ratio
10	The range of the input common-mode voltage is______	13V	12V	14V	10V	13V
11	Output Resistance of IC 741______	60 Ohm	50 Ohm	75 Ohm	80 Ohm	75 Ohm
12	PSRR Stands for ______	Power Sector Resistance Range	Pulse Signal Rejetion Ratio	Power Supply Resictor Ratio	Power Supply Rejection Ratio	Power Supply Rejection Ratio
13	CMRR is typically ______dB	100dB	90dB	75dB	60dB	90dB
14	Built in short circuit protection is guaranteed to withstand______of current	10 mA	50mA	25mA	100mA	25mA
15	Supply current in IC 741 is____mA	1.5	2.8	3.17	5.2	2.8

16	Power consumption in operational amplifier is________	85mW	75mW	50mW	100mW	85mW
17	The slew rate of operational amplifier is_____	Zero	5V/uS	1.5V/uS	0.5V/uS	0.5V/uS
18	The small voltage applied at the input terminals to make output voltage zero is called_____	Input bias current	Thermal drift	Input offset voltage	Input offset current	Input offset voltage
19	The total number of Inputs in IC741____	1	2	3	4	2
20	The power supply voltage to op-amp may ranges from_____	5v to 12v	5v to 22v	9v to 12v	5v to 30v	5v to 22v
21	In operational amplifier pin 2 is called____	Power supply terminal	Inverting input terminal	Non inverting input terminal	Output treminal	Inverting input terminal
22	In operational amplifier pin 3 is called____	Power supply terminal	Inverting input terminal	Non inverting input terminal	Output treminal	Non inverting input terminal
23	In operational amplifier pin 6 is called____	Power supply terminal	Inverting input terminal	Non inverting input terminal	Output treminal	Output treminal
24	In operational amplifier pin 7 and 4 are connected to ____	Power supply terminal	Inverting input terminal	Non inverting input terminal	Output treminal	Power supply terminal
25	In operational amplifier pin 1 and 5 are used for____	dc offset	ac offset	Connect with AFO	Connect with power supply	dc offset
26	Operational amplifier have _____ basic terminals	Two	Three	eight	one	eight
27	Operational amplifier have _____output impedance	High	Low	Zero	Infinite	Zero
28	Operational amplifier have _____open loop voltage gain	Infinite	Zero	High	Low	Infinite
29	Operational amplifier is a voltage controlled_____ source	Current	Voltage	Amplifier	Convertor	Voltage
30	The operational amplifier is a ______ terminal device	Single	Multi	Duel	widely	Multi
31	The operating temperature range of IC 741 is__	0*C to 70*c	70*c to 100*c	>100*c	<0*c	0*C to 70*c
32	An ideal op-amp has no current from source and its response is independent of_________	Voltage	Noise	Current	Temperature	Temperature
33	An op-amp with open loop gain of 90dB with dc signal has gain of_____through audio and radio frequencies	70dB	80dB	90dB	100dB	90dB
34	The rate of which the voltage across the capacitor in operational amplifier is given by_____	I/C	C/I	V/I	I/V	I/C

35	The input offset voltage is measured is_______	V	KV	mV	uV	mV
36	The common mode rejection ratio is measured in_____	V	mV	dB	uV	dB
37	The unit of slew rate is__	mV/sec	dB	V/uS	uV/Sec	V/uS
38	Op-amp IC 741 has a ______ slew rate	Low	High	Moderate	Unity	Low
39	The open-loop gain of the op-amp decreases at the rate of_____	(-10)dB decade	(-20)dB decade	(-30)dB decade	(-40)dB decade	(-20)dB decade
40	An oscillator produces……………. oscillations	Damped	Undamped	Modulated	unmodulated	Undamped
41	An oscillator employs ……………… feedback	Positive	Negative	Neither positive nor negative	Data insufficient	Positive
42	Hartley oscillator is commonly used in …	Radio receivers	Radio transmitters	TV receivers	transmitters	Radio receivers
43	In a phase shift oscillator, we use …………. RC sections	1	23	2	3	3
44	In a phase shift oscillator, the frequency determining elements are	L and C	R, L and C	R and C	R and L	R and C
45	An oscillator differs from an amplifier because it	Has more gain	Requires no input signal	Requires no d.c. supply	Always has the same input	Requires no input signal
46	One condition for oscillation is	A phase shift around the feedback loop of 180o	A gain around the feedback loop of one-third	A phase shift around the feedback loop of 0o	A gain around the feedback loop of less than 1	A phase shift around the feedback loop of 0o
47	A second condition for oscillations is …	A gain of 1 around the feedback loop	No gain around the feedback loop	The attention of the feedback circuit must be one-third	The feedback circuit must be capacitive	A gain of 1 around the feedback loop
48	For an oscillator to properly start, the gain around the feedback loop must initially be	1	>1	<1	0	>1
49	In Colpitt’s oscillator, feedback is obtained …	By magnetic induction	By a tickler coil	. From the centre of split	by self induction	From the centre of

				capacitors		split capacitors
50	………….. is a fixed frequency oscillator	Phase-shift oscillator	Hartely-oscillator	Colpitt's oscillator	Crystal oscillator	Crystal oscillator
51	For an oscillator to properly start, the gain around the feedback loop must initially be	1	>1	<1	0	>1
52	An oscillator converts …	dc. power into d.c. power	.d c. power into a.c. power	mechanical power into a.c. power	ac to ac	.d c. power into a.c. power
53	In an LC transistor oscillator, the active device is …	LC tank circuit	Biasing circuit	Transistor	transformer	Transistor
54	In an LC circuit, when the capacitor is maximum, the inductor energy is	. Minimum	Maximum	Half-way between maximum and minimum	moderate	Minimum
55	In an LC oscillator, the frequency of oscillator is ……………. L or C.	Proportional to square of	Directly proportional to	Independent of the values of	Inversely proportional to square root of	Inversely proportional to square root of
56	An LC oscillator cannot be used to produce ……………….. frequencies	High	Audio	Very low	Very high	Very low
57	Quartz crystal is most commonly used in crystal oscillators because	It has superior electrical properties	It is easily available	It is quite inexpensive	very costly	It has superior electrical properties
58	The signal generator generally used in the laboratories is ………….. oscillator	Wien-bridge	Hartely	Crystal	Phase shift	Wien-bridge
59	An important limitation of a crystal oscillator is …	Its low output	Its high Q	Less availability of quartz crystal	Its high output	Its low output
60	In an LC oscillator, if the value of L is increased four times, the frequency of oscillations is	Increased 2 times	Decreased 4 time	Increased 4 times	Decreased 2 times	Decreased 2 times

UNIT-IV

SYLLABUS

Introduction to CRO: Block Diagram of CRO. Applications of CRO: (1) Study of Waveform, (2) Measurement of Voltage, Current, Frequency, and Phase Difference. Power Supply: Half-wave Rectifiers. Centre-tapped and Bridge Full-wave Rectifiers Calculation of Ripple Factor and Rectification Efficiency, Basic idea about capacitor filter, Zener Diode and Voltage Regulation. Timer IC: IC 555 Pin diagram and its application as Astable and Monostable Multivibrator.

Cathode Ray Oscilloscope:

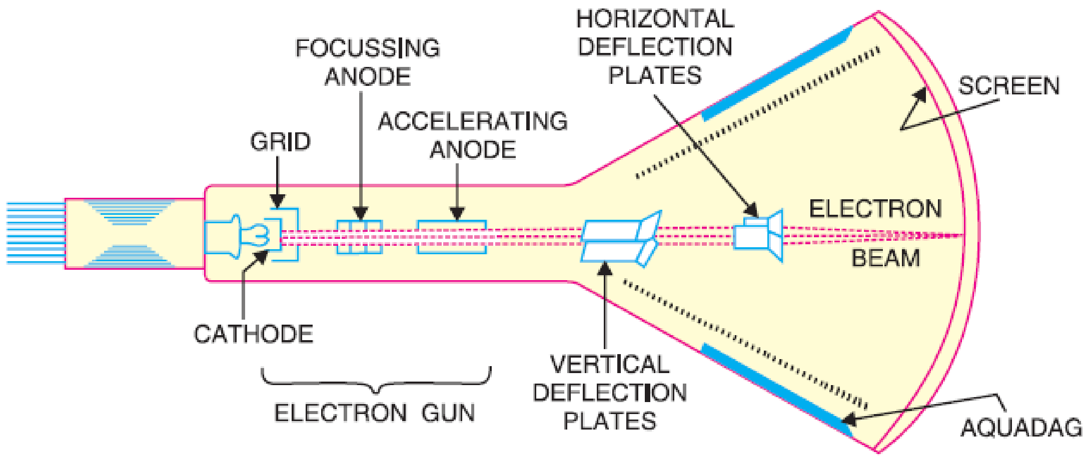
The cathode ray oscilloscope (commonly abbreviated as CRO) is an electronic device which is capable of giving a visual indication of a signal waveform. No other instrument used in the electronic industry is as versatile as the cathode ray oscilloscope. It is widely used for trouble shooting radio and television receivers as well as for laboratory work involving research and design. With an oscilloscope, the wave shape of a signal can be studied with respect to amplitude distortion and deviation from the normal. In addition, the oscilloscope can also be used for measuring voltage, frequency and phase shift.

In an oscilloscope, the electrons are emitted from a cathode accelerated to a high velocity and

brought to focus on a fluorescent screen. The screen produces a visible spot where the electron beam strikes. By deflecting the electron beam over the screen in response to the electrical signal, the electrons can be made to act as an electrical pencil of light which produces a spot of light wherever it strikes. An oscilloscope obtains its remarkable properties as a measuring instrument from the fact that it uses as an indicating needle a beam of electrons. As electrons have negligible mass, therefore, they respond almost instantaneously when acted upon by an electrical signal and can trace almost any electrical variation no matter how rapid. A cathode ray oscilloscope contains a cathode ray tube and necessary power equipment to make it operate.

Cathode Ray Tube:

A cathode ray tube (commonly abbreviated as CRT) is the heart of the oscilloscope. It is a vacuum tube of special geometrical shape and converts an electrical signal into visual one. A cathode ray tube makes available plenty of electrons. These electrons are accelerated to high velocity and are brought to focus on a fluorescent screen. The electron beam produces a spot of light wherever it strikes. The electron beam is deflected on its journey in response to the electrical signal under study. The result is that electrical signal waveform is displayed visually.



(i) Glass envelope. It is conical highly evacuated glass housing and maintains vacuum inside

and supports the various electrodes. The inner walls of CRT between neck and screen are usually coated with a conducting material, called aquadag. This coating is electrically connected to the accelerating anode so that electrons which accidentally strike the walls are returned to the anode. This prevents the walls of the tube from charging to a high negative potential.

(ii) Electron gun assembly.

The arrangement of electrodes which produce a focussed beam of electrons is called the electron gun. It essentially consists of an indirectly heated cathode, a control grid, a focussing anode and an accelerating anode. The control grid is held at negative potential w.r.t. cathode whereas the two anodes are maintained at high positive potential w.r.t. cathode. The cathode consists of a nickel cylinder coated with oxide coating and provides plenty of electrons. The control grid encloses the cathode and consists of a metal cylinder with a tiny circular opening to keep the electron beam small in size. The focussing anode focuses the electron beam into a sharp pin-point by controlling the positive potential on it. The positive potential (about 10,000 V) on the accelerating anode is much higher than on the focusing anode. For this reason, this anode accelerates the narrow beam to a high velocity. Therefore, the electron gun assembly forms a narrow, accelerated beam of electrons which produces a spot of light when it strikes the screen.

(iii) Deflection plate assembly. The deflection of the beam is accomplished by two sets of

deflecting plates placed within the tube beyond the accelerating anode as shown in Fig. set is the vertical deflection plates and the other set is the horizontal deflection plates.

The vertical deflection plates are mounted horizontally in the tube. By applying proper potential to these plates, the electron beam can be made to move up and down vertically on the fluorescent screen. The horizontal deflection plates are mounted in the vertical plane. An appropriate potential on these plates can cause the electron beam to move right and left horizontally on the screen.

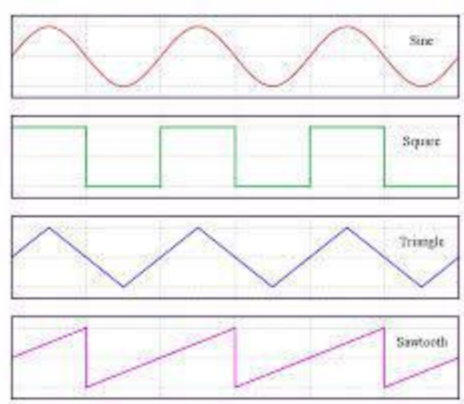
(*iv*) Screen. The screen is the inside face of the tube and is coated with some fluorescent material such as zinc orthosilicate, zinc oxide etc. When high velocity electron beam strikes the screen, a spot of light is produced at the point of impact. The colour of the spot depends upon the nature of fluorescent material. If zinc orthosilicate is used as the fluorescent material, green light spot is produced.

USE OF CRO FOR THE MEASUREMENT OF VOLTAGE, FREQUENCY, TIME PERIOD:

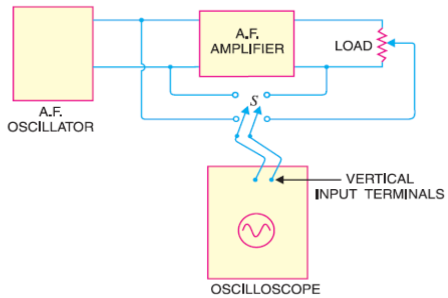
The modern cathode ray oscilloscope provides a powerful tool for solving problems in electrical measurements. Some important applications of CRO are :

1. Examination of waveforms
2. Voltage measurement
3. Frequency measurement

1. Examination of waveform.



One of the important uses of CRO is to observe the wave shapes of voltages in various types of electronic circuits. For this purpose, the signal under study is applied to vertical input (i.e., vertical deflection plates) terminals of the oscilloscope. The sweep circuit is set to internal so that sawtooth wave is applied to the horizontal input i.e. horizontal deflection plates. Then various controls are adjusted to obtain sharp and well defined signal waveform on the screen. Fig shows the circuit for studying the performance of an audio amplifier. With the help of switch S, the output and input of amplifier is applied in turn to the vertical input terminals. If the waveforms are identical in shape, the fidelity of the amplifier is excellent.



2. Voltage measurement. As discussed before, if the signal is applied to the vertical deflectionplates only, a vertical line appears on the screen. The height of the line is proportional to peak to-peak voltage of the applied signal. The following procedure is adopted for measuring voltages with CRO.

(i) Shut off the internal horizontal sweep generator.

(ii) Attach a transparent plastic screen to the face of oscilloscope. Mark off the screen with
vertical and horizontal lines in the form of graph.

(iii) Now, calibrate the oscilloscope against a known voltage. Apply the known voltage, say 10 V, to the vertical input terminals of the oscilloscope. Since the sweep circuit is shut off, you will get a vertical line. Adjust the vertical gain till a good deflection is obtained. Let the deflection sensitivity be V volts/mm.

(iv) Keeping the vertical gain unchanged, apply the unknown voltage to be measured to the vertical input terminals of CRO.

(v) Measure the length of the vertical line obtained. Let it be l mm. Then, Unknown voltage = l × V volts

3. Frequency measurement. The unknown frequency can be accurately determined with the help of a CRO. The steps of the procedure are as under :

(i) A known frequency is applied to horizontal input and unknown frequency to the vertical input.

(iv) The number of loops cut by the horizontal line gives the frequency on the vertical plates (fv) and the number of loops cut by the vertical line gives the frequency on the horizontal plates (fH).

$$\frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

For instance, suppose during the frequency measurement test, a pattern shown in Fig is obtained. Let us further assume that frequency applied to horizontal plates is 2000 Hz. If we draw horizontal and vertical lines, we find that one loop is cut by the horizontal line and two loops by the vertical line. Therefore,

$$\frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

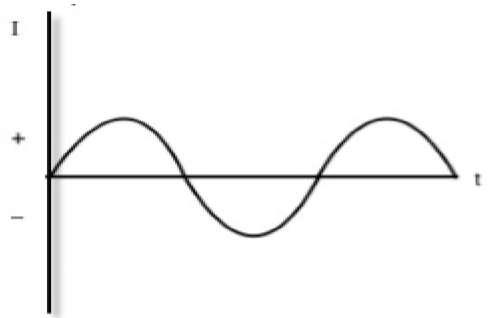
or $$\frac{f_v}{2000} = \frac{1}{2}$$

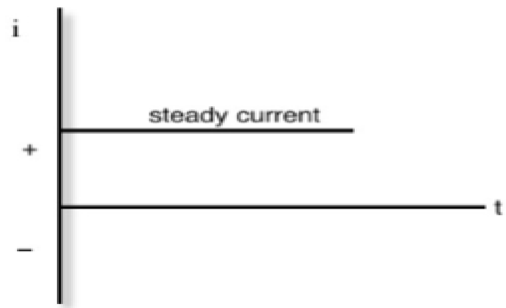
or $$f_v = 2000 \times 1/2 = 1000 \text{ Hz}$$

i.e. Unknown frequency is 1000 Hz.

Rectifier-Principle

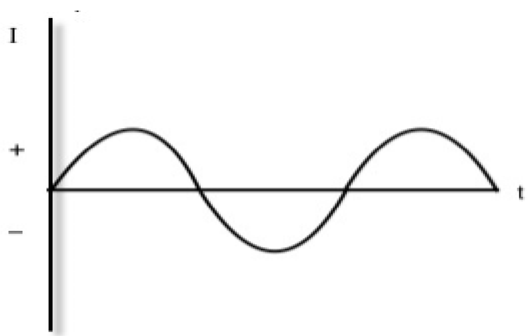
Majority of electronic devices require direct current sources for their operations. But domestic electric supply is available in alternating current form. Therefore, it has to be converted in direct current.Rectifier is a device which coverts alternating current to direct or steady current is known a rectifier.

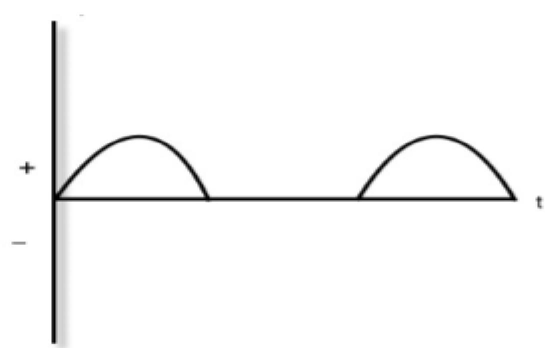




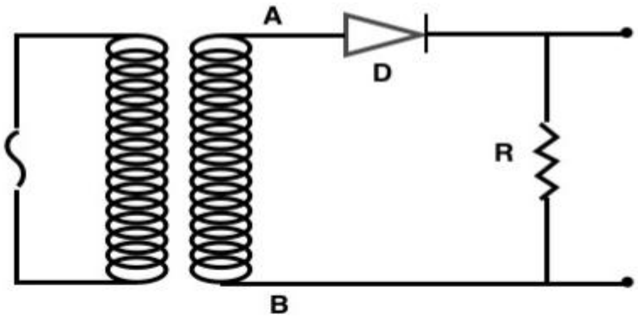
Half wave rectifier

Half wave rectifier converts only half cycle of alternating current to direct current, the remaining half cycle is wasted.





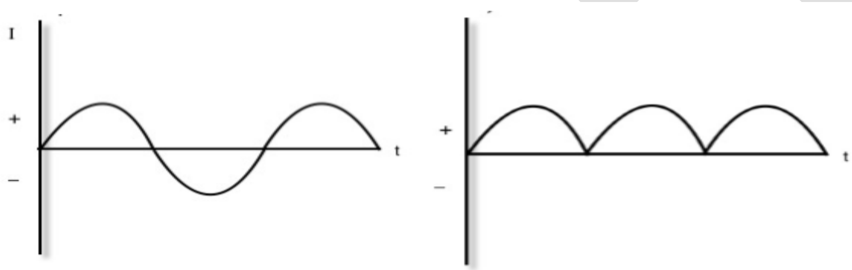
The input current is bidirectional and output current is unidirectional. The current obtained is pulsated or bumpy. Only a single diode is used in half wave rectifier.



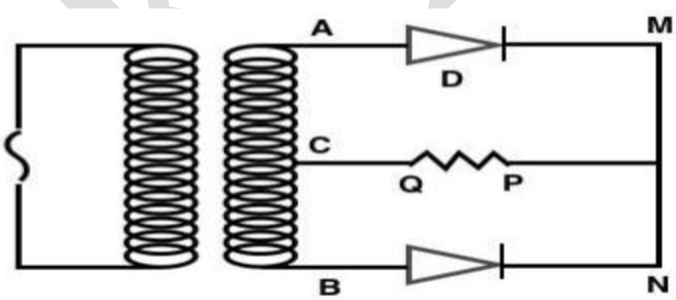
An A.C supply is provided to the transformer. The diode is connected in series with load (electronic device) resistance RL. During every positive half cycle of the A.C input, point A becomes positive w.r.t. point B, and diode becomes forward biased and current is allowed to flow. During every negative half cycle of the A.C input, point A becomes negative w.r.t. point B, and diode becomes reverse biased and current is not allowed to flow.

Full Wave-Rectifier

Full wave rectifier converts the complete cycle of alternating current to direct current. No input current is wasted.



The input current is bidirectional and output current is unidirectional. Two diode are required for full wave rectifier.

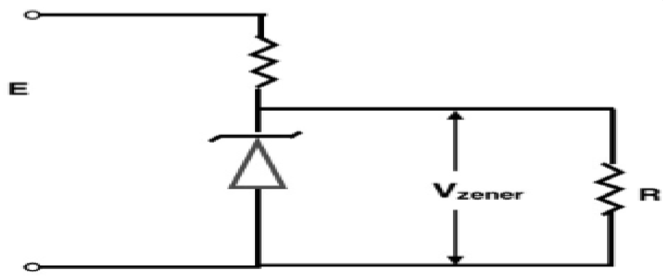


This rectifier requires centre tapped secondary transformer. During positive half cycle of A.C input, point A is positive w.r.t point C and point B is negative w.r.t. point C, therefore the diode D1 is forward biased and diode D2 is reverse biased. The current flows through diode D1 and passes through the load RL, path of current is AMPQCA.

During negative half cycle of A.C input, point B is positive w.r.t point C and point A is negative w.r.t point C, therefore the diode D2 is forward biased and diode D1 is reverse biased. The current flows through diode D2, and passes through the load RL, path of current is BNPQCB.

Zener–Diode

Zener diode is P-N junction diode. It is used for regulation of voltage supplied. It is highly doped and used in reverse biasing. Zener diode is designed to operate in breakdown region.



When reverse bias reaches a particular value, the current increases suddenly. This voltage is called Zener breakdown voltage or simply Zener voltage (VZ). Breakdown for a given Zener diode depends upon doping level of P and N regions. Generally, this value is small, such as 1.5V, 2V. It is clear from characteristic that, in breakdown region, voltage across Zener diode remains almost constant even when current through it changes by large amount.

IC 555

The 555 timer IC is an integral part of electronics projects. For a simple project 555 timer. For generating pulse. These provide time delays, as an oscillator and as a flip-flop among other applications. Depending on the manufacturer, the standard 555 package includes 25 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8). Variants consists of combining multiple chips on one board. However 555 is still the most popular. Let’s look at the pin diagram to have an idea about the timer IC before we talk about 555 timer working.

Pin diagram and description

Pin	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts
3	OUT	This output is driven to approximately 1.7 V below +*V*cc, or to GND.
4	RESET	A timing interval may be reset by driving this input to GND,
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 *V*cc).
6	THR	The timing (OUT high) interval ends when the voltage at threshold is greater than that at CTRL (2/3 *V*cc if CTRL is open).
7	DIS	Open collector output which may discharge a capacitor between intervals.
8	*V*cc	Positive supply voltage, which is usually between 3 and 15 V

Some important features of the 555 timer:

555 is used in almost every electronic circuit today. For a 555 timer working as a flip flop or as a multi-vibrator,Some of the major features are.

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature which is equivalent to 0.005 %/ °C.
- The cycle of the timer is adjustable.
- Also, the maximum power dissipation per package is 600 mW

555 timer working

The 555 generally operates in 3 modes. A-stable, Mono-stable and Bi-stable modes.

Astable mode

This means there will be no stable level at the output. So the output will be swinging between high and low. This character of unstable output is used as clock or square wave output for many applications.

Mono-stable mode

This configuration consists of one stable and one unstable state. The stable state can be chosen either high or low by the user. If the stable output is set at high(1), the output of the timer is high(1). At the application of an interrupt, the timer output turns low(0). Since the low state is unstable it goes to high(1) automatically after the interrupt passes. Similar is the case for a low stable mono-stable mode.

Bi-stable mode

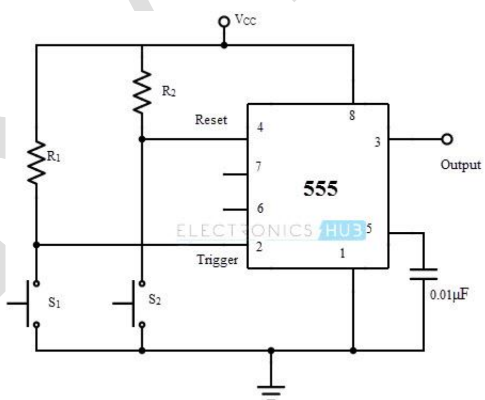
In bi-stable mode, both the output states are stable. At each interrupt, the output changes from low(0) to high(1) and vice versa, and stays there. For example, if we have a high(1) output, it will go low(0) once it receives an interrupt and stay low(0) till the next interrupt changes the status.

Bistable multivibrator

A Bistable multivibrator is a type of circuit which has two stable states (high and low). It stays in the same state until and unless an external trigger input is applied. Generally, a bistable multivibrator stays low until a trigger signal is applied and it stays high until a reset signal is applied. Bistable multi vibrators are also called as flip-flops or latches. The term flip-flop is used because it 'flips' to one state and stays there until a trigger is applied and once the trigger is applied it 'flops' back to the original state.

Bistable Multivibrator Circuit using 555 Timer

The circuit for a bistable multivibrator using the 555 timer is shown below



A bistable multivibrator is one of the easiest circuits that can be built using a 555 timer. It doesn't require a capacitor as the RC charging unit is not responsible for the generation of the output. The generation of high and low outputs is not dependent on the charging and discharging of the capacitor in the RC unit but rather it is controlled by the external trigger and reset signals.

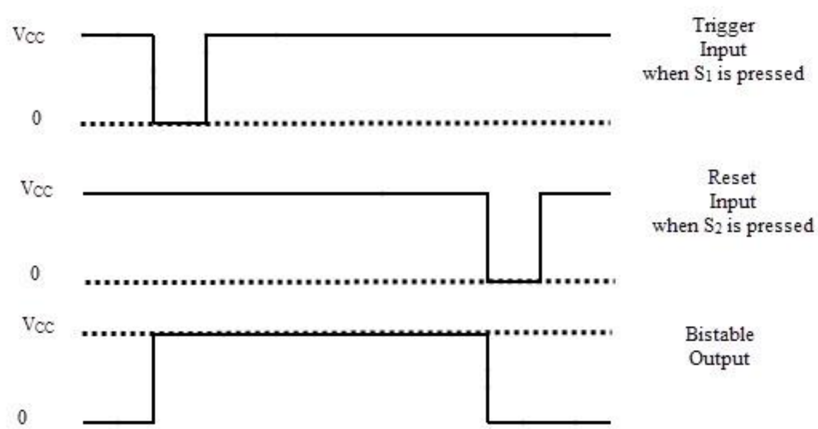
The explanation of the bi stable mode of operation of the 555 timer is as follows. The trigger and reset pins (pins 2 and 4 respectively) are connected to the supply through two resistors R1 and R2 so that they are always high. In all the previous cases, the reset pin is not used and in order to avoid any accidental reset, it is simply connected to VCC.

Two switches are connected between these pins and ground in order to make them go low momentarily. The switch at the trigger input will act as S (SET) input for the internal flip-flop. The switch at the reset input will act as reset for the internal flip-flop.

When the switch S1 is pressed, the voltage from VCC will bypass the trigger terminal and is shorted to ground through the resistor R1. Hence, the trigger pulse will momentarily go low and the output of the timer at pin 3 will become HIGH. The output stays HIGH because there is no input from the threshold pin (pin 6 is left open or better if connected to ground) and the output of the internal comparator (comparator 1) will not go high.

When the switch S2 is pressed, the voltage from VCC will bypass the reset terminal and is shorted to ground through the resistor R2. This pin is internally connected to the RESET terminal of the flip-flop. When this signal goes low for a moment, the flip-flop receives the reset signal and RESETs the flip-flop.

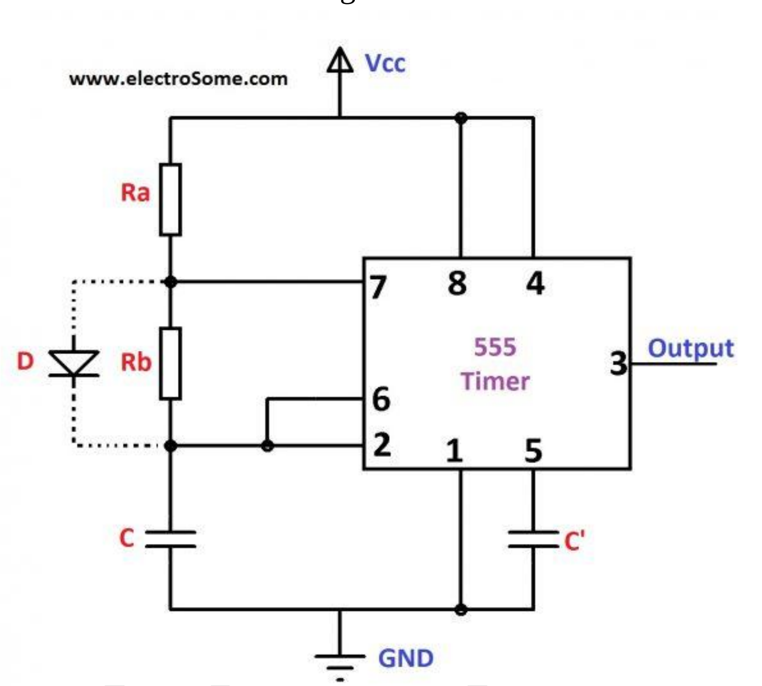
Hence, the output will become LOW and stays there until the trigger is applied. The waveforms of the bistable mode of operation of the 555 timer are shown below.



Astable Multivibrator using 555

An Astable Multivibrator is an oscillator circuit that continuously produces rectangular wave without the aid of external triggering. So Astable Multivibrator is also known as Free Running Multivibrator. Astable Multivibrator using 555 Timer is very simple, easy to design, very stable and low cost. It can be used for timing from microseconds to hours. Due to these reasons 555 has a large number of applications and it is a popular IC among electronics hobbyists.

Astable Multivibrator using 555 – Circuit



Astable Multivibrator using 555 Timer Circuit Diagram

Above figure shows the circuit diagram of a 555 Timer wired in Astable Mode. 8th pin and 1st pin of the IC are used to give power, Vcc and GND respectively. The 4th pin is RESET pin which is active low and is connected to Vcc to avoid accidental resets. 5th pin is the Control Voltage pin which is not used. So to avoid high frequency noises it is connected to a capacitor C' whose other end is connected to ground. Usually C' = 0.01µF. The Trigger (pin 2) and Threshold (pin 6) inputs are connected to the capacitor which determines the output of the timer. Discharge pin (pin 7) is connected to the resistor Rb such that the capacitor can discharge through Rb. Diode D connected in parallel to Rb is only used when an output of duty cycle less than or equal to 50% is required.

Since the Control Voltage (pin 5) is not used the comparator reference voltages will be 2/3 Vcc and 1/3 Vcc respectively. So the output of the 555 will set (goes high) when the capacitor voltage goes below 1/3 Vcc and output will reset (goes low) when the capacitor voltage goes above 2/3 Vcc.

Working

When the circuit is switched ON, the capacitor (C) voltage will be less than 1/3 Vcc. So the output of the lower comparator will be HIGH and of the higher comparator will be LOW. This SETs the output of the SR Flip-flop.

Thus the discharging transistor will be OFF and the capacitor C starts charging from Vcc through resistor Ra & Rb.

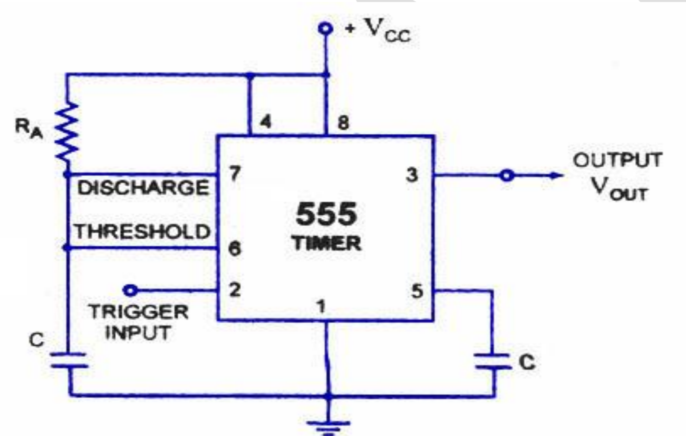
When the capacitor voltage will become greater than 1/3 Vcc (less than 2/3 Vcc), the output of both comparators will be LOW and the output of SR Flip-flop will be same as the previous condition. Thus the capacitor continuous to charge.

MONOSTABLE MULTIVIBRATOR

A monostable multivibrator (MMV) is often called a pulse generator circuit in which the duration of the pulse is determined by the R-C network, connected externally to the 555 timer. Here one state of output is stable while the other is unstable

to stable state energy is stored by an externally connected capacitor C.

The time taken in storage determines the pulse width. The schematic of a 555 timer in monostable mode of operation is shown in the figure



Circuit of The Timer 555 as a Monostable Multivibrator

Monostable Multivibrator Circuit details

Pin 1 is grounded. Trigger input is applied to pin 2. The input is kept at + VCC. To obtain transition of output from stable state to unstable state, a negative-going pulse and amplitude of greater than + 2/3 VCC is applied to pin 2. Output is taken from pin 3. Pin 4 is usually connected to + VCC Pin 5 is grounded through a 0.01 u F capacitor to avoid noise problem. Pin 6 (threshold) is shorted to pin 7. A resistor RA is connected between pins 6 and 8. At pins 7 a discharge capacitor is connected while pin 8 is connected to supply VCC.

WORKING

The operation of the circuit is explained below:

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor- C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 VCC, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward +VCC through resistance RA with a time constant equal to RAC. When the increasing capacitor voltage becomes slightly greater than +2/3 VCC, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure.

Possible Questions

PART B

1. What is zenor diode?
2. What is astable multivibrator?
3. What is monostable multivibrator?
4. What is the difference between half wave and full wave rectifier?
5. What is half wave rectifier?
6. What is the full wave rectifier?
7. What is voltage regulation ?
8.

PART C

1. Explain the working principle of CRO with the help of diagram.
2. Explain the working principle of centre tapped rectifier and calculate its efficiency and ripple factor
3. Explain the working principle of 555 timer with the help of diagram.
4. Explain working principle of Astable multivibrator using IC 555.
5. Explain the working principle of zener diode as a voltage regulator.
6. Explain working principle of Monostable multivibrator using IC 555.

KARPAGAM ACADEMY OF HIGHER EDUCATION

Coimbatore – 641021

(For Candidates Admitted From 2017 Onwards)

DEPARTMENT OF PHYSICS

UNIT V: Objective Type/Multiple choice Questions each Question carries one Mark

SL.NO	QUESTION	OPTION A	OPTION B	OPTION C	OPTION D	ANSWER
1	If peak voltage for a half wave rectifier circuit is 5V and diode cut in voltage is 0.7, then peak inverse voltage on diode will be?	5V	4.9V	4.3V	6.7V	4.3V
2	Transformer utilisation factor of a half wave rectifier is __________	0.234	0.279	0.287	0.453	0.287
3	If the input frequency of a half wave rectifier is 100Hz, then the ripple frequency will be__________	150Hz	200Hz	100Hz	300Hz	100Hz
4	Ripple factor of a half wave rectifier is_________(Im is the peak current and RL is load resistance)	1.414	1.21	1.4	0.48	1.21
5	CRO is used for measurement of ___________	AC as well as DC current	AC current only	DC current only	AC power only	AC as well as DC current
6	CRO is used in a radar for ___________	studying the pattern of flights	visualizing a target	measuring voltage	determining the distance between source and destination	visualizing a target
7	In medical applications CRO can be used for ___________	measuring the heart beats	monitoring the brain	improving the nervous system functioning	displaying cardiograms	displaying cardiograms
8	Curve tracers use CRO in ___________	diodes	passive devices	active devices	op amps	active devices
9	A CRO is used in check ___________	op amps	resistors	voltage	capacitance, inductance and diodes	capacitance, inductance and diodes
10	A CRO is used in labs for ___________	frequency measurement	voltage measurement	current measurement	resistance measurement	frequency measurement
11	Efficiency of a centre tapped full wave rectifier is __________	0.5	0.46	0.7	0.812	0.812
12	If input frequency is 50Hz for a full wave rectifier, the ripple frequency of it would be	100Hz	50Hz	25Hz	500Hz	100Hz

	__________					
13	Transformer utilisation factor of a half wave rectifier is __________	0.234	0.279	0.287	0.453	0.287
14	Ripple factor of a half wave rectifier is__________(Im is the peak current and RL is load resistance)	1.414	1.21	1.4	0.48	1.21
15	CRO is used in a radar for ___________	studying the pattern of flights	visualizing a target	measuring voltage	determining the distance between source and destination	visualizing a target
16	Curve tracers use CRO in ___________	diodes	passive devices	active devices	op amps	active devices
17	Transformer utilization factor of a centre tapped full wave rectifier is__________	0.623	0.678	0.693	0.625	0.693
18	Zener diodes are also known as	Voltage regulators	Forward bias diode	Breakdown diode	None of the mentioned	Breakdown diode
19	Which of the following is true about the resistance of a Zener diode?	It has an incremental resistance	It has dynamic resistance	The value of the resistance is the inverse of the slope of the i-v characteristics of the Zener diode	All of the mentioned	All of the mentioned
20	Which of the following is true about the temperature coefficient or TC of the Zener diode?	For Zener voltage less than 5V, TC is negative	For Zener voltage around 5V, TC can be made zero	For higher values of Zener voltage, TC is positive	All of the mentioned	All of the mentioned
21	Which of the following can be used in series with a Zener diode so that combination has almost zero temperature coefficient?	Diode	Resistor	Transistor	MOSFET	Diode
22	In Zener diode, for currents greater than the knee current, the v-i curve is almost	Almost a straight line parallel to y-axis	Almost a straight line parallel to x-axis	Equally inclined to both the axes with a positive slope	Equally inclined to both the axes with a negative slope	Almost a straight line parallel to x-axis

23	Zener diodes can be effectively used in voltage regulator. However, they are these days being replaced by more efficient	Operational Amplifier	MOSFET	Integrated Circuits	None of the mentioned	Integrated Circuits
24	Determine the time period of a monostable 555 multivibrator.	T = 0.33RC	T = 1.1RC	T = 3RC	T = RC	T = 1.1RC
25	Which among the following can be used to detect the missing heart beat?	Monostable multivibrator	Astable multivibrator	Schmitt trigger	None of the mentioned	Monostable multivibrator
26	A 555 timer in monostable application mode can be used for	Pulse position modulation	Frequency shift keying	Speed control and measurement	Digital phase detector	Speed control and measurement
27	How can a monostable multivibrator be modified into a linear ramp generator?	Connect a constant current source to trigger input	Connect a constant current source to trigger output	Replace resistor by constant current source	Replace capacitor by constant current source	Replace resistor by constant current source
28	When a capacitor charges:	the voltage across the plates rises exponentially	the circuit current falls exponentially	the capacitor charges to the source voltage in 5×RC seconds	all of the above	all of the above
29	The _________ is defined as the time the output is active divided by the total period of the output signal.	on time	off time	duty cycle	active ratio	duty cycle
30	Efficiency of bridge full wave rectifier is	0.812	0.5	0.406	0.453	0.812
31	Number of diodes used in a full wave bridge rectifier is	1	2	4	6	4
32	In an bridge full wave rectifier, the input sine wave is 250sin100 πt. The output ripple frequency of rectifier will be	50Hz	200Hz	100Hz	25Hz	100Hz
33	The cut-in point of a capacitor filter is__________	The instant at which the conduction starts	The instant at which the conduction stops	The time after which the output is not filtered	The time during which the output is perfectly filtered	The instant at which the conduction starts
34	The rectifier current is a short duration pulses which cause the diode to act as a__________	Voltage regulator	Mixer	Switch	Oscillator	Switch
35	The charge (q) lost by the capacitor during the discharge time for shunt capacitor filter.	IDC*T	IDC/T	IDC*2T	IDC/2T	IDC*T

36	Which of the following are true about capacitor filter?	It is also called as capacitor output filter	It is electrolytic	It is connected in parallel to load	It helps in storing the magnetic energy	It is electrolytic
37	The rms ripple voltage (Vrms) of a shunt filter is__________	IDC/2√3	IDC2√3	IDC/√3	IDC√3	IDC/2√3
38	How to obtain symmetrical waveform in Astable multivibrator?	Use clocked RS flip-flop	Use clocked JK flip-flop	Use clocked D-flip-flop	Use clocked T-flip-flop	Use clocked JK flip-flop
39	How does a monostable multivibrator used as frequency divider?	Using square wave generator	Using triangular wave generator	Using sawtooth wave generator	Using sine wave generator	Using square wave generator
40	Astable multivibrator operating at 150Hz has a discharge time of 2.5m. Find the duty cycle of the circuit.	0.5	0.75	0.9599	0.375	0.375
41	Free running frequency of Astable multivibrator?	f=1.45/(RA+2RC	f=1.45(RA+2RC	f=1.45C/(RA+2R	f=1.45 RA/(RA+R	f=1.45/(RA+2RC
42	How is frequency related to time period?	square proportional	not related	directly proportional	inversely proportional	directly proportional
43	How is error in measurement reduced?	using r.m.s value	using absolute value	using peak to peak value	using a voltmeter	using peak to peak value
44	By making use of a CRO	many characteristics of a signal can be measured	only a few characteristics of a signal can be measured	no characteristics of a signal can be measured	signal can only be displayed	many characteristics of a signal can be measured
45	How is the waveform adjusted?	by adjusting the voltage	through shift controls	by reducing the current	by means of a galvanometer	through shift controls
46	How many types of acquisition methods are there in a digital storage oscilloscope?	3	6	2	4	3
47	In which method of acquisition, pretrigger event is lost?	Real time sampling	Random repetitive sampling	Sequential repetitive sampling	Analog Sampling	Sequential repetitive sampling
48	What plays an important role in Real time sampling?	small memory and fast sampling	large memory and slow sampling	large memory and fast sampling	small memory and slow sampling	large memory and fast sampling
49	In Real time sampling what is the 3 dB bandwidth?	fs/4	fs/8	2fs	fs	fs/4
50	CRO is used in a radar for ___________	studying the pattern of flights	visualizing a target	measuring voltage	determining the distance between source and	visualizing a target

					destination	
51	A typical data acquisition system consists of ___________	op amps	sensors	rectifiers	transistors	sensors
52	The data acquisition system implies input data collection.	in mixed signal form	in analog form	in digital form	in the form of binary codes	in digital form
59	By making use of a CRO	many characteristics of a signal can be measured	only a few characteristics of a signal can be measured	no characteristics of a signal can be measured	signal can only be displayed	many characteristics of a signal can be measured
60	CRO is used in a radar for ___________	studying the pattern of flights	visualizing a target	measuring voltage	determining the distance between source and destination	visualizing a target
61	The data acquisition system implies input data collection.	in mixed signal form	in analog form	in digital form	in the form of binary codes	in digital form
62	How many types of acquisition methods are there in a digital storage oscilloscope?	3	6	2	4	3