KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University)
(Established Under Section 3 of UGC Act 1956)
Coimbatore - 641021.
(For the candidates admitted from 2016 onwards)

SUBJECT : DIGITAL, ANALOG CIRCUITS AND INSTRUMENTATION PRACTICAL

SEMESTER : V

SUBJECT CODE: 16PHU513A **CLASS** : III B.Sc.PHYSICS

Any 8 Experiments

1. To measure (a) Voltage, and (b) Frequency of a periodic waveform using CRO
2. To verify and design AND, OR, NOT and XOR gates using NAND gates.
3. To minimize a given logic circuit.
4. Half adder, Full adder and 4-bit Binary Adder.
5. Adder-Subtractor using Full Adder I.C.
6. To design an astable multivibrator of given specifications using 555 Timer.
7. To design a monostable multivibrator of given specifications using 555 Timer.
8. To study IV characteristics of PN diode, Zener and Light emitting diode
9. To study the characteristics of a Transistor in CE configuration.
10. To design a CE amplifier of given gain (mid-gain) using voltage divider bias.
11. To design an inverting amplifier of given gain using Op-amp 741 and study its frequency response. 12. To design a non-inverting amplifier of given gain using Op-amp 741 and study its Frequency Response.
13. To study Differential Amplifier of given I/O specification using Op-amp.
14. To investigate a differentiator made using op-amp.
15. To design a Wien Bridge Oscillator using an op-amp.

REFERENCE BOOKS:

1. Basic Electronics: A text lab manual, P.B. Zbar, A.P. Malvino, M.A. Miller, 1994, Mc-Graw Hill.
2. Electronics: Fundamentals and Applications, J.D. Ryder, 2004, Prentice Hall.
3. OP-Amps & Linear Integrated Circuit, R.A. Gayakwad, 4th Edn, 2000, Prentice Hall.
4. Electronic Principle, Albert Malvino, 2008, Tata Mc-Graw Hill.

EXP.NO:-1

NAND AS UNIVERSAL GATE

AIM:

To realize NOT, AND, OR and Ex-OR gates using only NAND gates

APPARATUS AND COMPONENTS:

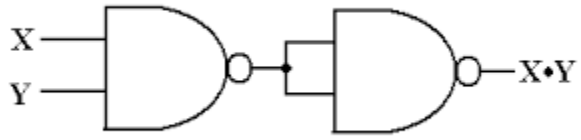
IC 7400, 5V, power supply, digital trainer kit, etc.

PROCEDURE:

Using NAND gates, logic gates such as NOT, AND, OR and Ex-OR the can be constructed. Hence NAND gate is called as universal building block.

The connections are made as shown below and the truth table of each gate is verified for different input combinations.

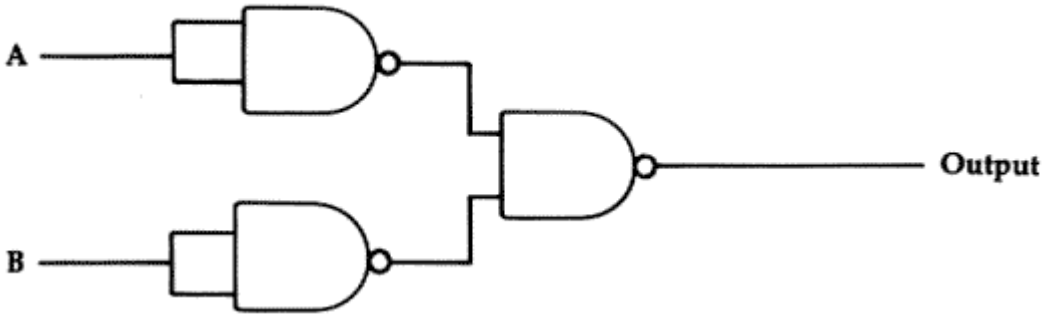
NAND AS AND:-



TRUTH TABLE:-

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

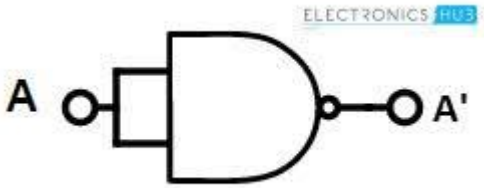
NAND AS OR:-



TRUTH TABLE:-

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

NAND AS NOT:-



TRUTH TABLE:-

Input	Output
A	Y
0	1
1	0

RESULT:

The logic gates like NOT, AND, OR and Ex-OR are realized using only NAND gates and their truth tables are verified.

EXP.NO.:-2

NOR AS UNIVERSAL GATE

AIM:

To realize NOT, AND, OR and Ex-OR gates using only NOR gates.

APPARATUS AND COMPONENTS:

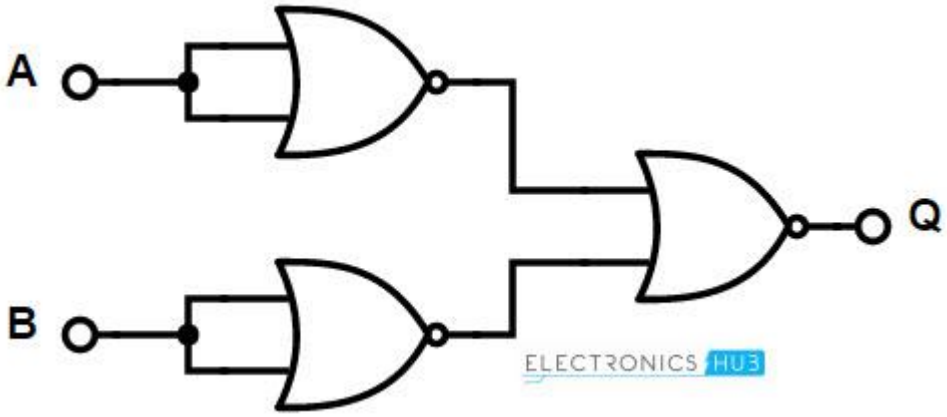
IC 7402, 5V power supply, digital trainer kit, etc.

PROCEDURE:

Using NOR gates, logic gates such as NOT, AND, OR and Ex-OR can be constructed. Hence NOR gate is also called as universal building block.

The connections are made as shown below and the truth table of each gate is verified for different input combinations.

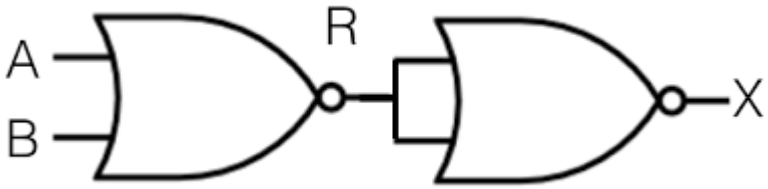
NOR AS AND:-



TRUTH TABLE

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

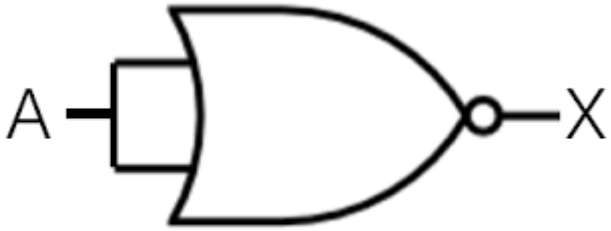
NOR AS OR:-



TRUTH TABLE:-

Input		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOR AS NOT:-



TRUTH TABLE:-

Input	Output
A	Y
0	1
1	0

RESULT:

The logic gates like NOT, AND, OR and Ex-OR are realized using only NOR gates and their truth tables verified.

EXP.NO.:-3

FULL ADDER AND FULL SUBTRACTOR

AIM:

To implement full adder and full subtractor using logic gates such as Ex-OR, AND, OR and NOT gates and also using NAND and NOR gates.

APPARATUS AND COMPONENTS:

IC 7486, IC 7408, IC 7432, IC 7404, IC 7400, IC 7402, 5V power supply, digital

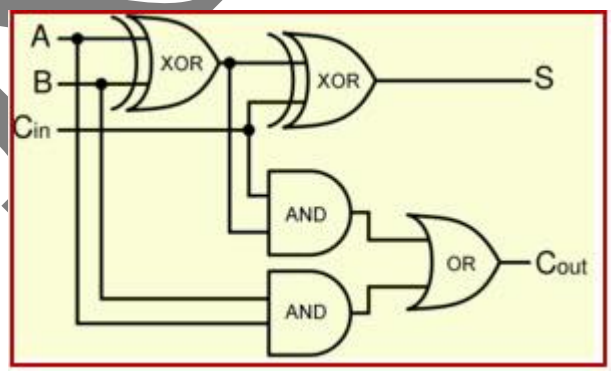
trainer kit, etc.

PROCEDURE:

FULL ADDER:

- A full adder is a logic circuit that adds three bits and produces two output sum and carry.
- The Boolean expressions for sum and carry are
  Sum = A
- The connections are made as shown in the fig 134.1. The output is using LED for different input combinations given through toggle switches.
- The full adder can be implemented using NAND and NOR gates as shown in fig.

CIRCUIT DIAGRAM:-



TRUTH TABLE:-

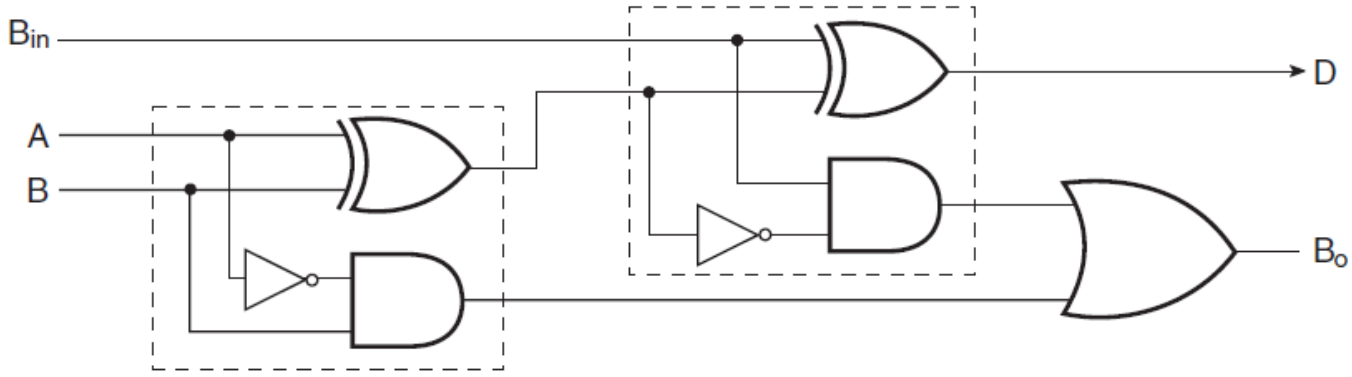
INPUTS			OUTPUT	
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

FULL SUBTRACTOR:

- A full subtractor is a logic circuit that performs subtraction with three bits and produces two outputs, difference and borrows.
- The Boolean expressions for diff and Br are
- The circuit connections are made as shown below and the output is verified for all the input combinations.
- Similar to a full adder, full subtractor can also be implemented using

NAND and NOR gates as shown in Fig.

CIRCUIT DIAGRAM:-



TRUTH TABLE:-

Minuend (A)	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

RESULT:

The full adder and full subtractor are constructed using Ex-OR, NAND and NOR gates and the truth tables are verified.

EXP.NO.:4

HALF ADDER AND HALF SUBTRACTOR

AIM:

To implement half adder and half subtractor using logic gates such as Ex-AND, OR and NOT gates and also using NAND and NOR gates.

APPARATUS AND COMPONENTS:

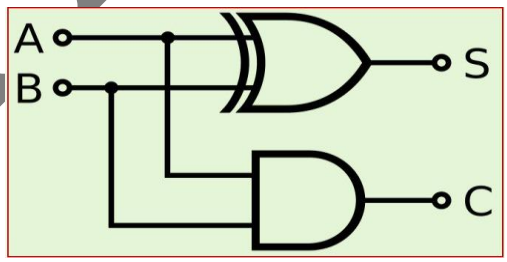
IC 7486, IC 7408, IC 7432, IC 7404, IC 7400, IC 7402, 5V power supply, digital trainer kit, etc.

PROCEDURE:

HALF ADDER:

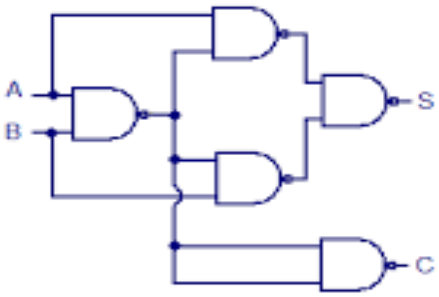
- An half adder is a logic circuit that adds two bits and produces two outputs sum and carry.
- The Boolean expressions for sum and carry are
- Thus the sum can be constructed using Ex-OR gate and the carry can implemented using AND gate.

HALF ADDER CIRCUIT:-

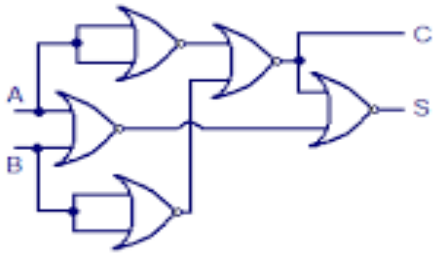


The connections are made as shown below The output is verified using LED for different input combinations given through toggle switched.
The half adder can also be implemented using NAND and NOR gates as shown below.

HALF ADDER WITH NAND AND NOR:-



Half adder using NAND logic



Half adder using NOR logic

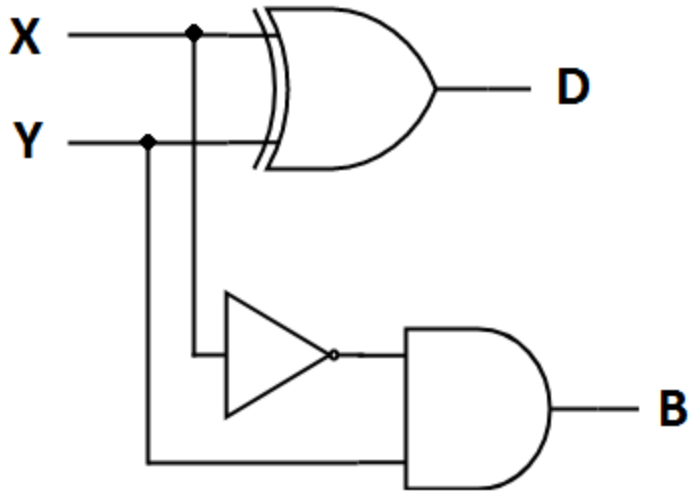
TRUTH TABLE FOR HALF ADDER

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF SUBTRACTOR:

- An half subtractor is a logic circuit that performs subtraction between two bits and produces two outputs, different and borrow.
- The Boolean expressions for diff and Br are
- The circuit connections are made as shown in the Fig 133.4 and the output is verified for all the input combinations.

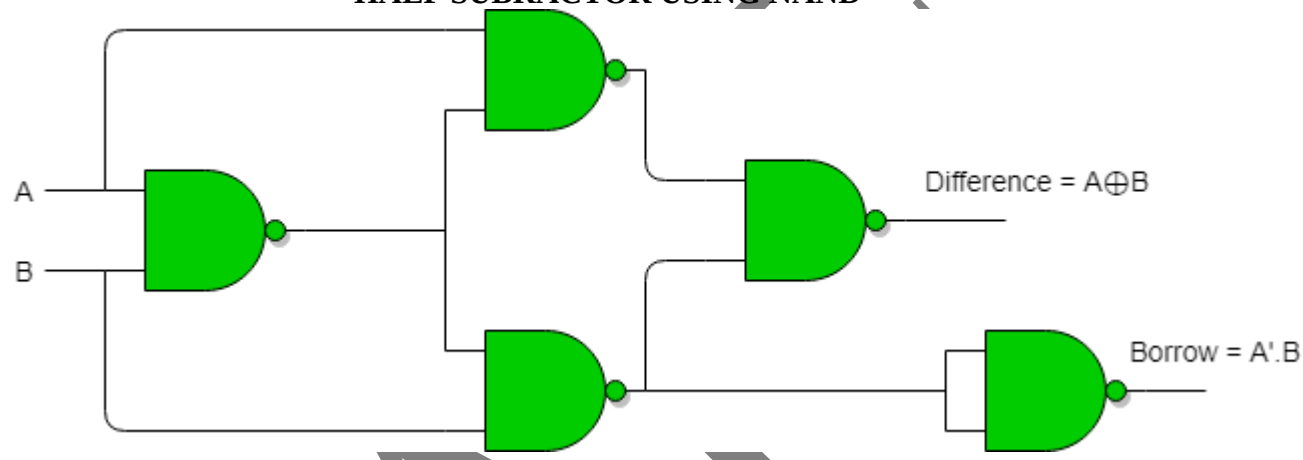
CIRCUIT FOR HALF SUBRACTOR:-



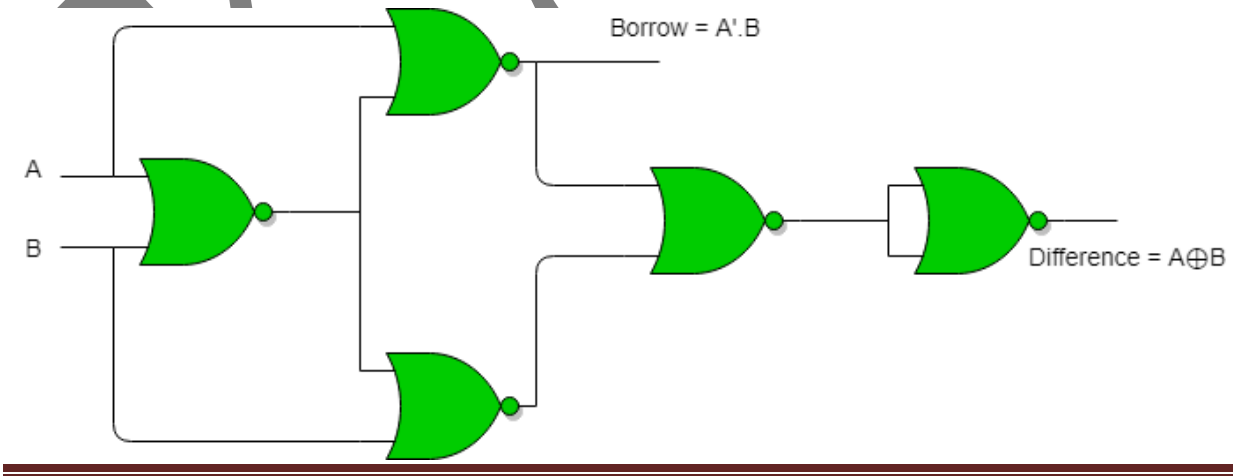
Similar to an half adder, an half subtractor can also be implemented using NAND and NOR gates as shown in Fig

HALF SUBRACTOR USING NAND AND NOR:-

HALF SUBRACTOR USING NAND



HALF SUBRACTOR USING NOR



TRUTH TABLE FOR HALF SUBRACTOR:-

Half Subtractor-Truth Table			
Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0
www.flintgroups.com			

RESULT:

The half adder and half subtractor are constructed and their truth tables are verified.

EXP.NO.:5

VERIFICATION OF LOGIC CIRCUIT

AIM:

To verify De Morgan's laws.

APPARATUS AND COMPONENTS:

IC 7400,IC 7404, IC7432, IC 7402, IC 7408, 5V power supply, digital trainer kit, etc.

PROCEDURE:

FIRST LAW:

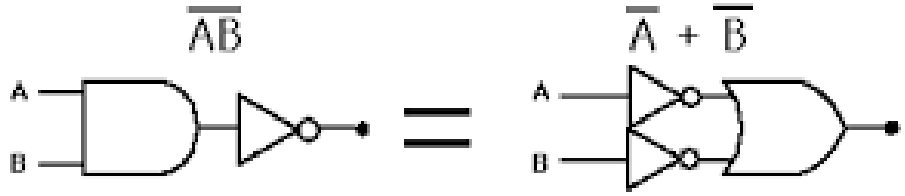
- De Morgan's first law states that the complement of the sum of two variables is equal to the product of individual complements. That is, if A and B are the two varibles, then

- For LHS expression, a NOR gate is used and for RHS expression. Two NOT gates and one AND gate are used.

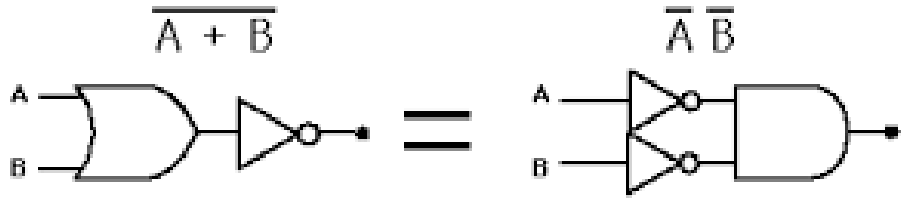
- The circuit connections are made as shown in Fig.

SECOND LAW:

DeMorgan's second law states that the complement of the product of two variables is equal to the sum of individual complements. That is, if A and B are the two varibles, then



A NAND gate is equivalent to an inversion followed by an OR



A NOR gate is equivalent to an inversion followed by an AND

TRUTH TABLE:-

A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

For LHS expression, a NAND gate is used and for RHS expression, two NO gates and one OR gate are used.

The circuit connections are made as shown in Fig.

RESULT:

The DeMorgan's laws are verified.

EXP.NO.:6

INVERTING AMPLIFIERS

AIM:

To study the linear applications of Inverting amplifier

APPARATUS REQUIRED:

1. Op – Amp IC 741
2. Dual Power Supply 15V,
3. Resistors
4. Capacitors
5. Function Generator
6. Cathode Ray Oscilloscope
7. Multimeter
8. Breadboard and Connecting Wires

THEORY:

Inverting Amplifier:

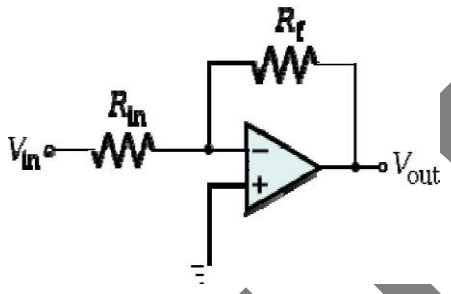
This is the most widely used of all the Op-amp circuits. The output V_0 is fed back to the inverting input through the $R_f - R_{in}$ network as shown in figure where R_f is the feedback resistor. The input signal V_i is applied to the inverting input terminal through R_{in} and non-inverting input terminal of Op-amp is grounded.The output V_0 is given by

$$V_0 = V_i (-R_f / R_{in})$$

Where, the gain of amplifier is $- R_f / R_{in}$

The negative sign indicates a phase-shift of 180 degrees between V_i and V_0. The effective input impedance is R_i. An inverting amplifier uses negative feedback to invert and amplify a voltage. The R_{in},R_f resistor network allows some of the output signal to be returned to the input. Since the output is 180° out of phase, this amount is effectively subtracted from the input, thereby reducing the input into the operational amplifier. This reduces the overall gain of the amplifier and is dubbed negative feedback

CIRCUIT DIAGRAM:



TABULATION:-

S.No.	Vin	Rf	Rin	OBSERVED OUTPUT=Vin(-Rf/Rin)

PROCEDURE:

- Make connections as given in figure.
- .connect the input to the inverting terminal of the op-amp
- Vary R_f and measure the corresponding V_0 and observe the phase of V_0 with respect to V0.
- Tabulate the readings and verify with theoretical values.

RESULT:-

The inverting amplifier is constructed and the output is verified.

EXP.NO.:7

NON-INVERTING AMPLIFIERS

AIM:

To study the linear applications of Non-Inverting amplifier

APPARATUS REQUIRED:

1. Op – Amp IC 741
2. Dual Power Supply 15V,
3. Resistors
4. Capacitors
5. Function Generator
6. Cathode Ray Oscilloscope
7. Multimeter
8. Breadboard and Connecting Wires

THEORY:-

Non – inverting amplifier

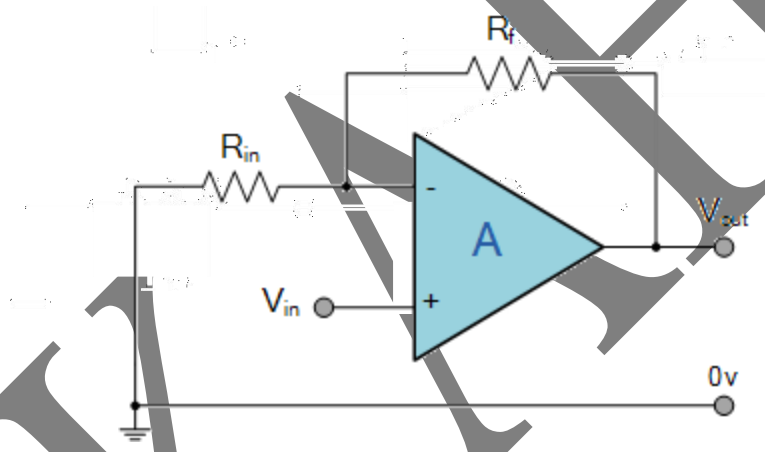
The circuit diagram of non – inverting amplifer is shown in figure. Here, the signal is applied to the non – inverting input terminal and feedback is give n to inverting terminal. The circuit a mplifiers the input signal without in verting it. T he output V_{out} is given by

The volt age gain is given by

$$A_{CL} = \frac{V_{0u}t}{Vin} = 1 + \frac{R_2}{R_1}$$

Compare d to the inverting amplifier, the inp ut resistance of the non-inverting is extremely large.

CIRCUIT DIAGRAM:



TABULATION:-

S.No.	Vin	Rf	Rin	OBSERVED OUTPUT=Vin(1+Rf/Rin)

PROCEDURE:

1. Make connections as given in figure.
2. .connect the input to the Non-inverting terminal of the op-amp
3. Vary R_f and measure the corresponding V_0 and observe the phase of V_0 with respect to V0.
4. Tabulate the readings and verify with theoretical values.

RESULT:-

The Non-inverting amplifier is constructed and the output is verified.

EXP.NO.:8

INTEGRATOR.

AIM:

To verify the linear op amp circuit Integrator.

APPARATUS REQUIRED:

1.Resistor

2.Capacitor

3.AFO

4.OpAmp

5.Dual Supply

6.CRO

7.Bread Board

INTEGRATOR:

The Integrator Amplifier is an operational amplifier circuit that performs the

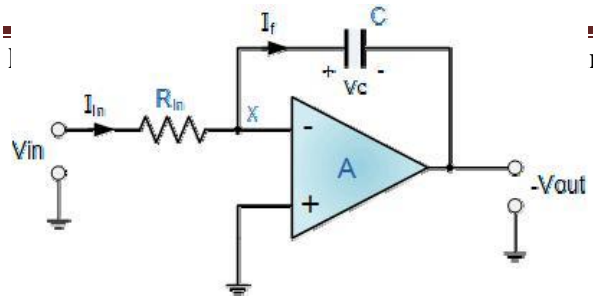
mathematictical operation of Integration**,** that is we can cause the output to respond to changes in the input voltage over time. The integrator amplifier acts like a storage element that "produces a voltage output which is proportional to the integral of its input voltage with respect to time". In other words the magnitude of the output signal is determined by the length of time a volta ge is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit (voltage follower circuit) giving an overall gain of less than one. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the feedback capacitor C begins to charge up, its reactance Xc decreases this results in the ratio of Xc/Rin increasing producing an output voltage that continues to increase until the capacitor is fully charged.

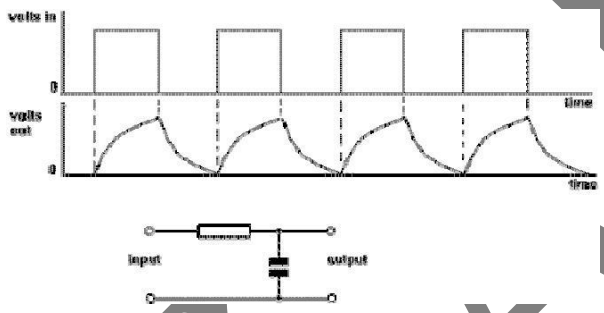
At this point the capacitor acts as an open circuit, blocking anymore flow of DC current. The ratio of feedback capacitor to input resistor (Xc/Rin) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation .Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between. The ideal voltage output for the Integrator Amplifier as:

$$V_{out} = -\frac{1}{R_{In}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{In}.C}$$

CIRCUIT DIAGRAM:



WAVEFORMS:



RESULT:-

The integrator circuit using op-amp has been constructed and its output is verified.