# KARPAGAM ACADEMY OF HIGHER EDUCATION

(Deemed to be University)
(Established Under Section 3 of UGC Act 1956)
Coimbatore - 641021.
(For the candidates admitted from 2018 onwards)

**SUBJECT** : **ELECTRONIC DEVICES AND CIRCUITS**

**SEMESTER** : **I** **SUBJECT CODE**: **18PHP102**
**CLASS** : **I M.Sc.PHYSICS**

**Scope:** This paper contains details of basic electronic components, their characteristics and applications in the construction of different electronic instruments. Other than ordinary transistors and diodes special devices are also explained.
**Objectives:** To give an idea about the basics of electronics and electronic devices, which is very important for knowing the basics of any modern instrument.

**UNIT -I**
**Electronic Devices**: Transistor Biasing and Stabilization with design problems, h-parameters and their applications in transistor circuit analysis for CE, CB and CC configurations; FET and MOSFETs: Characteristics and Biasing, Design of biasing circuits, Design and analysis of amplifiers, SCR, UJT, DIAC, TRIAC (construction & working).

**UNIT -II**
**Analog Devices**: Frequency response of amplifiers General concepts; bode plot; low frequency response: BJT and FET amplifiers; miller effect capacitance; high frequency response of BIT amplifiers; hybrid pie model: short circuit current gain, cut off frequency, and current gain with resistive load; high frequency response of FET amplifiers; frequency response of multistage amplifiers; square wave testing, Numerical problems.

**UNIT- III**
**Analog Circuits**: Analysis of compound configurations Cascade connection; Cascade connection; Darlington connection; Bootstrapping principle; Bootstrapped Emitter Follower; Bootstrapped Darlington Emitter Follower; Feedback pair; . CMOS circuits; Current source circuits; Current mirror circuits; Differential amplifier circuits; Numerical problems.

**UNIT- IV**
**Power Amplifiers**: Introduction, Series-fed Class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation, Class B amplifier distortion, Power transistor heat sinking, Class C and Class D amplifiers, Numerical problems.

**UNIT- V**

**Network Theory**: mesh and node analysis Kirchhoff's voltage and current law, Network Theorems- Thevein's theorem, Norton's theorem, Superposition Theorem, Maximum power transfer theorem, Problems based on network theorems

**Suggested Readings**


1. Boyle L. stad and Louis Nashelsky, 10th edition, 2013, Electronic devices and circuit theory, Prentice-Hall of India,Delhi.
2. Millman and Halkias, 48th reprint, 2008, Integrated electronics, Tata McGraw-Hill, New Delhi.
3. Malvino A.P., Electronics Principles, 10th edition, 2013, Tata McGraw Hill, New Delhi
4. Mottershed, 1st edition, 2002, Electronic devices and circuits : An introduction, Prentice-Halloflndia, New Delhi.
5. M. S. Ghausi1st edition, 2013, Electronic devices and circuits, CBS.
6. Donald L. Schilling, Charles Belove, 3rd edition, 2009, Electronic circuits discrete and integrated, Tata McGraw-Hill, New Delhi.
7. Millman and Grabel, 2nd edition, 2001, Microelectronics; Tata McGraw-Hill, New Delhi.
8. T.F. Bogart and J.S. beasely and G. Rico, 5th edition, 2000, Electronic devices and circuits, Prentice hall; New Delhi.Hall of India .
9. A.Nagoor Kani, 1st edition, 2014, Circuit theory, RBA publications.

## UNIT-I
## SYLLABUS

**Electronic Devices**: Transistor Biasing and Stabilization with design problems, h-parameters and their applications in transistor circuit analysis for CE, CB and CC configurations; FET and MOSFETs: Characteristics and Biasing, Design of biasing circuits, Design and analysis of amplifiers, SCR, UJT, DIAC, TRIAC (construction & working).

### TRANSISTOR BIASING

The proper flow of zero signal collector current and the maintenance of proper collector emitter voltage during the passage of signal is known as Transistor Biasing. The circuit which provides transistor biasing is called as Biasing Circuit.

**Need for DC biasing**

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the active region, to be operated as an amplifier.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this

problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

For a transistor to be operated as a faithful amplifier, the operating point should be stabilized.

**Factors affecting the operating point**

The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.

As temperature increases, the values of $I_{CE}$, $\beta$, $V_{BE}$ gets affected.

- $I_{CBO}$ gets doubled (for every $10^o$ rise)
- $V_{BE}$ decreases by 2.5mv (for every $1^o$ rise)

So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

**STABILIZATION**

The process of making the operating point independent of temperature changes or variations in transistor parameters is known as Stabilization.

Once the stabilization is achieved, the values of $I_C$ and $V_{CE}$ become independent of temperature variations or replacement of transistor. A good biasing circuit helps in the stabilization of operating point.

**Need for Stabilization**

Stabilization of the operating point has to be achieved due to the following reasons.

- Temperature dependence of $I_C$
- Individual variations
- Thermal runaway

Let us understand these concepts in detail.

**Temperature Dependence of $I_C$**

As the expression for collector current $I_C$ is

$IC=\beta IB+ICEOIC=\beta IB+ICEO$

$=\beta IB+(\beta+1)ICBO=\beta IB+(\beta+1)ICBO$

The collector leakage current $I_{CBO}$ is greatly influenced by temperature variations. To come out of this, the biasing conditions are set so that zero signal collector current $I_C$ = 1 mA. Therefore, the operating point needs to be stabilized i.e. it is necessary to keep $I_C$ constant.

**Individual Variations**

As the value of β and the value of $V_{BE}$ are not same for every transistor, whenever a transistor is replaced, the operating point tends to change. Hence it is necessary to stabilize the operating point.

## THERMAL RUNAWAY

As the expression for collector current $I_C$ is

$IC=\beta IB+ICEOIC=\beta IB+ICEO$

$=\beta IB+(\beta+1)ICBO=\beta IB+(\beta+1)ICBO$

The flow of collector current and also the collector leakage current causes heat dissipation. If the operating point is not stabilized, there occurs a cumulative effect which increases this heat dissipation. The self-destruction of such an unstabilized transistor is known as Thermal run away.

In order to avoid thermal runaway and the destruction of transistor, it is necessary to stabilize the operating point, i.e., to keep $I_C$ constant.

## STABILITY FACTOR

To maintain Stability in the output of the transistor, $I_C$ should be kept constant in spite of variations of $I_{CBO}$ or $I_{CO}$. The extent to which a biasing circuit is successful in maintaining this is measured by Stability factor. It denoted by S.

By definition, the rate of change of collector current $I_C$ with respect to the collector leakage current $I_{CO}$ at constant $\beta$ and $I_B$ is called Stability factor.

$S=dICdICOS=dICdICO$ at constant $I_B$ and $\beta$

Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. S=1 is the ideal value.

The general expression of stability factor for a CE configuration can be obtained as under.

$IC=\beta IB+(\beta+1)ICOIC=\beta IB+(\beta+1)ICO$

Differentiating above expression with respect to $I_C$, we get

$1=\beta dIBdIC+(\beta+1)dICOdIC1=\beta dIBdIC+(\beta+1)dICOdIC$

Or

$1=\beta dIBdIC+(\beta+1)S1=\beta dIBdIC+(\beta+1)S$

Since $dICOdIC=1SdICOdIC=1S$

Or

$S=\beta+11-\beta(dIBdIC)S=\beta+11-\beta(dIBdIC)$

Hence the stability factor S depends on β, $I_B$ and $I_C$.

**HYBRID PARAMETERS**

The hybrid parameters are generally used to determine amplifier characteristic parameters such as voltage gain, input and output resistance etc. Usually amplifier characteristic parameters may be determined by using current gain(β) and values of other circuit components. But hybrid methods had the following advantages:

1. Value of circuit components are easily available, and
2. The procedure followed is quite simple and easy to understand.

H-PARAMETERS OF LINEAR CIRCUIT

Every linear circuit having input and output can be analyzed as two port networks. In these networks there are four parameters called hybrid or h-parameters. Out of these four parameters, one is measured in ohm, one in mho and other two are dimension less. Since these parameters have mixed dimension, so they are called hybrid parameters.

Consider a linear circuit shown in Figure (a). in this circuit when input voltage 1 is applied, input current $i_1$ flows. Then output voltage $V_2$ and current $i_2$ appears. Both currents $i_1$ and $i_2$ are assumed to flow inside the box of the linear circuit. Both voltages $V_1$ and $V_2$ are assumed to be positive from the upper to lower terminals.

The linear circuit may be replaced by an equivalent circuit as shown in Figure (a). the equivalent circuit is called hybrid model of a linear circuit. In such as circuit, the input and the output voltages and currents (called variables) may be related by the set of the following twoequations:

$V_1 = h_{11}.i_1 + h_{12}.$

$V_2\ I_2 = h_{21}.i + h_{22}.V_2$

$V_1$ = input voltage $V_2$ = Output voltage $I_1$ = input current

$I_2$ = output current

And $h_{11}$, $h_{12}$, $h_{21}$ and $h_{22}$ are hybrid parameters

**DETERMINATION OF H-PARAMETERS**

The parameters $h_{11}$ and $h_{21}$ may be determined by short circuiting the output terminals of a given circuit. On the other hand, $h_{12}$ and $h_{22}$ may be determined by open circuiting the input terminals of the given circuit.

**Determination of $h_{11}$ and $h_{21}$**

These are determined by short circuiting the output terminals of a given circuit as shown in Figure (b). a shot circuit at the output terminal makes the voltage v2 equal to zero. Input voltage is given by relation,

$VI = h_{11}.i_1 + h_{12}.V_2$

Putting the value of $V_2$ (equal to zero) in the above equation, the input voltage,

$V_1 = h_{11}.i_1$ or $h_{11}=V_1/i_1$

Thus $h_{11}$ may be determined from the ratio $V_1/i_1$. The value of $i_1$ obtained by applying a voltage

at the input and then measuring the value of input current ($i_1$). Since $h_{11}$ is the ratio of voltage to current, therefore it has the units of ohms i.e. the same unit as that of a resistance. Because of this fact, $h_{11}$ is called input resistance of the circuit with output short circuited. Similarly, output current is given by the relation.

$I_2 = h_{21}.i_1 + h_{22}.V_2$

Again putting the value of $V_2$ the output current,

$I_2 = h_{21}. i1$ or $h_{21} = i_2/i_1$

Thus $h_{21}$ may be determined from the ratio $i_2/i_1$, the values of $i_2$ and $i_1$ may be obtained by applying a voltage at the input and then measuring the input current ($i_1$) and output current ($i_2$). Since $h_{21}$ is the ratio of currents, therefore it has no units. The parameter $h_{21}$ is called the forward current gain of the circuit with output short circuited.

**Determination of $h_{12}$ and $h_{22}$**

These are determined by open circuiting the input terminals of the given circuit as shown in Figure (b). an open circuit at the input terminals, makes the current ($i_1$) equal to zero. We also know that the input voltage is given by the relation.

$$V_1 = h_{11}.i_1 + h_{12}.V_2$$

Putting the value of $i_1$ in this equation, the output voltage will be

$V_1 = h_{12}. V_2$ or $h_{12} = V_1/V_2$

Thus $h_{12}$ may be determined from the ratio $V_1/V_2$. The value of $V_1$ may be obtained by applying a voltage ($V_2$) and the measuring the input voltage ($V_1$). Since, $h_{12}$ is a ratio of voltages, therefore it has no units. As $h_{12}$ is the ratio of input voltage ($V_1$) to the output voltage ($V_2$), therefore, its value known as the reverse voltage gain.

Similarly, the output current is given by the relation.

$I_2 = h_{21}.i_1 + h_{22}.V_2$

Again putting the value of $i_1$ (equal to zero) in this equation. The output currents will be,

$$I_2 = h_{22}. V_2 \text{ or } h_{22} = i_2/V_2$$

**The *h* Parameters of a Transistor**

Every linear circuit is associated with h parameters. When this linear circuit is terminated by load $r_L$, we can find input impedance, current gain, voltage gain, etc. in terms of h parameters. Fortunately, for small a.c. signals, the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal. Under such circumstances, the a.c. operation of the transistor can be described in terms of h parameters. The expressions derived for

input impedance, voltage gain etc. in the previous section shall hold good for transistor amplifier except that here $r_L$ is the a.c. load seen by the transistor.

There are four quantities required to describe the external behavior of the transistor amplifier. These are $v_1$, $i_1$, $v_2$ and $i_2$ shown on the diagram of Fig. These voltages and currents can be related by the following sets of equations :

$$v_1 = h_{11} i_1 + h_{12} v_2$$

$$i_2 = h_{21} i_1 + h_{22} v_2$$

The following points are worth noting while considering the behavior of transistor in terms of h parameters :

(i) For small a.c. signals, a transistor behaves as a linear circuit. Therefore, its a.c. operation can be described in terms of h parameters.

(ii) The value of h parameters of a transistor will depend upon the transistor connection (i.e. CB, CE or CC) used. For instance, a transistor used in CB arrangement may have $h_{11} = 20\ \Omega$. If we use the same transistor in CE arrangement, $h_{11}$ will have a different value. Same is the case with other h parameters.

(iii) The expressions for input impedance, .

$$r_L = R_C \parallel R_L$$

(iv) The values of h parameters depend upon the operating point. If the operating point is changed, parameter values are also changed.

(v) The notations $v_1$, $i_1$, $v_2$ and $i_2$ are used for general circuit analysis. In a transistor amplifier, we use the notation depending upon the configuration in which transistor is used. Thus for *CE* arrangement,

$$v_1 = V_{be} \;;\; i_1 = I_b \;;\; v_2 = V_{ce} \;;\; i_2 = I_c$$

Here $V_{be}$, $I_b$, $V_{ce}$ and $I_c$ are the R.M.S. values.

The numerical subscript notation for *h* parameters (*viz.* $h_{11}$, $h_{21}$, $h_{12}$ and $h_{22}$) is used in general circuit analysis.

## FIELD EFFECT TRANSISTOR

The field-effect transistor (FET) was first patented by Julius Edgar Lilienfeld in 1926 and by Oskar Heil in 1934. Field-Effect Transistors (FETs) are unipolar devices, and have two big advantages over bipolar transistors: one is that they have a near-infinite input resistance and thus offer near-infinite current and power gain

### Working Principle

In normal use, the drain terminal is connected to a positive supply and the gate is biased at a value that is negative (or equal) to the source voltage, thus reverse-biasing the JFET's internal p-n junction, and accounting for its very high input impedance.

With zero gate bias applied, a current flow from drain to source via a conductive 'channel' in the n-type bar is formed. When negative gate bias is applied, a high resistance region is formed within the junction, and reduces the width of the n-type conduction channel and thus reduces the magnitude of the drain-to-source current. As the gate bias is increased, the 'depletion' region

spreads deeper into the n-type channel, until eventually, at some 'pinch-off' voltage value, the depletion layer becomes so deep that conduction ceases.

Thus, the basic JFET passes maximum current when its gate bias is zero, and its current is reduced or 'depleted' when the gate bias is increased. It is thus known as a 'depletion-type' n-channel JFET. A p-channel version of the device can (in principle) be made by simply transposing the p and n materials.

**Types of Field Effect Transistors**

Field Effect transistor's are of mainly of two types based on construction features of the device

1. Junction Field Effect Transistor
2. Metal oxide semiconductor Field Effect Transistor.

JFET's are again subdivided into two types based on the type of channel namely p channel JFET and n- channel JFET. Similarly MOSFET's are divided into two types a) Enhancement mode MOSFET 2) Depletion mode MOSFET. In Enhancement mode MOSFET channel is induced by applying gate voltage contrary to the depletion mode MOSFET in which already existing channel is modulated by applying gate voltage like JFET.

**Types of JFET**

There are two types of JFET based on the type of channel i.e. based on the majority carrries flow.

- N- channel JFET

- P- channel JFET

The circuit symbol of P channel JFET and N channel JFET is as shown in the figure (a), (b) with the arrow on gate terminal shows the device polarity. Since JFET is a symmetric device either ends of N-channel can be used as source or drain. It is useful for the circuit design to show either of two terminals as source and other as drain. It is achieved here by placing gate terminal close to source.

N-channel JFET consists of a p+ type semiconductors grown by doping acceptor impurities on either side of N-type semiconductor as shown in the figure.

Current is allowed to flow through the length of the N-channel between the two p+ semiconductors. FET is a three terminal device with the terminals being source, gate and drain.

**Source**

It is there terminal where the majority carriers enter in to JFET bar. As for the FET bar concern this terminal is the source of majority carriers so it is called as source terminal and the current flow in this terminal is Is.

**Drain**

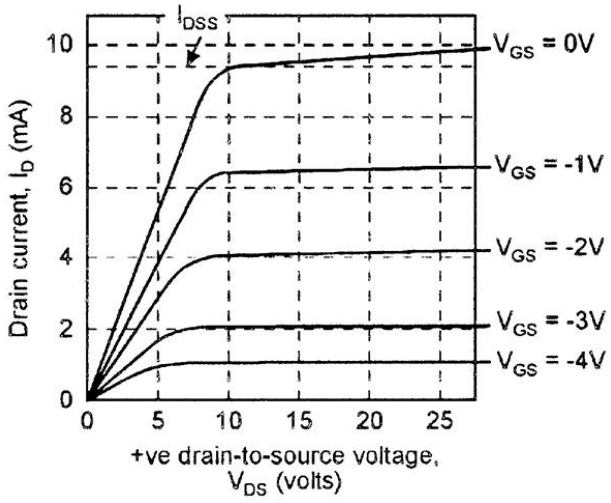
This terminal is the end terminal which collects the majority carriers sourced by the source. I.e. it is draining the majority carriers from FET bar and giving to the output terminal so it is called as drain terminal and the current in drain is $I_d$.

**Gate**

This important control element in FET as it acts like gate to the majority carriers flow. i.e. by operating the gate terminal voltage opening or closing of majority carries can be obtained, so this terminal called Gate terminal and the current in gate is $I_g$.

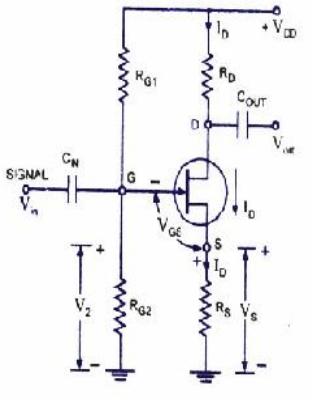
Practically FET is manufactured by doping donor impurities in p-type substrate. So along with these three terminals there exists substrate terminal which is often shorted to source. Both terminals of p+ type semiconductor are joined to form gate terminal. Metal contacts are provided for all the three terminals. Electrons flow from source to drain hence the conventional current of positive charge carriers flows from drain to source.

**Characteristics**




Ttransfer characteristics of an n-channel JFET.

**Potential-Divider Biasing.**




A slightly modified form of dc bias is provided by the circuit shown in figure. The resistors $R_{Gl}$ and $R_{G2}$ form a potential divider across drain supply $V_{DD}$. The voltage $V_2$ across $R_{G2}$provides the necessary bias. The additional gate resistor $R_{Gl}$ from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued $R_S$.

The gate is reverse biased so that $I_G = 0$ and gate voltage

$V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$

And

$V_{GS} = v_G - v_s = V_G - I_D R_s$

The circuit is so designed that ID Rs is greater than VG so that VGS is negative. This provides correct bias voltage.

The operating point can be determined as

$I_D = (V_2 - V_{GS})/ R_S$

And

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

**MOSFET**

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices. The MOSFET is a core of integrated circuit and it can be designed and fabricated in a single chip because of these very small sizes. The MOSFET is a four terminal device with source(S), gate (G), drain (D) and body (B) terminals. The body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor. The MOSFET is very far the most common transistor and can be used in both analog and digital circuits.

The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity present in the device is the main part.

The MOSFET can function in two ways

1. Depletion Mode
2. Enhancement Mode

**Depletion Mode:**When there is no voltage on the gate, the channel shows its maximum conductance. As the voltage on the gate is either positive or negative, the channel conductivity decreases.

**Enhancement mode:**When there is no voltage on the gate the device does not conduct. More is the voltage on the gate, the better the device can conduct.

**Working Principle of MOSFET:**

The aim of the MOSFET is to be able to control the voltage and current flow between the source and drain. It works almost as a switch. The working of MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p-type to n-type by applying positive or negative gate voltages respectively. When we apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage, a hole channel will be formed under the oxide layer.

**P-Channel MOSFET:**

The P- Channel MOSFET has a P- Channel region between source and drain. It is a four terminal device such as gate, drain, source, body. The drain and source are heavily doped p+ region and the body or substrate is n-type. The flow of current is positively charged holes. When we apply the negative gate voltage, the electrons present under the oxide layer with are pushed downward

into the substrate with a repulsive force. The depletion region populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from p+ source and drain region into the channel region.

**N- Channel MOSFET:**

The N-Channel MOSFET has a N- channel region between source and drain It is a four terminal device such as gate, drain , source , body. This type of MOSFET the drain and source are heavily doped n+ region and the substrate or body is P- type. The current flows due to the negatively charged electrons. When we apply the positive gate voltage the holes present under the oxide layer pushed downward into the substrate with a repulsive force. The depletion region is populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and sources the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage a hole channel will be formed under the oxide layer.

It is a multi-layer semiconductor device, hence the “silicon” part of its name. It requires a gate signal to turn it “ON”, the “controlled” part of the name and once “ON” it behaves like a

rectifying diode, the "rectifier" part of the name. In fact the circuit symbol for the *thyristor* suggests that this device acts like a controlled rectifying diode.

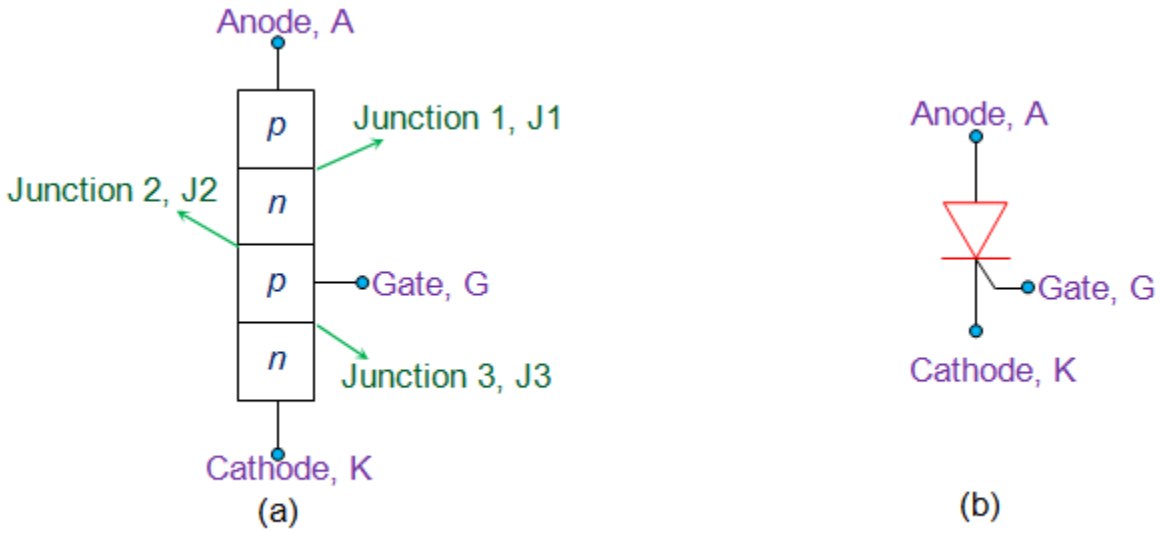



Figure 1 Silicon Controlled Rectifier (a) Layered Structure (b) Symbol

However, unlike the junction diode which is a two layer ( P-N ) semiconductor device, or the commonly used bipolar transistor which is a three layer ( P-N-P, or N-P-N ) switching device, the **Thyristor** is a four layer ( P-N-P-N ) semiconductor device that contains three PN junctions in series, and is represented by the symbol as shown.

Like the diode, the Thyristor is a unidirectional device, that is it will only conduct current in one direction only, but unlike a diode, the thyristor can be made to operate as either an open-circuit switch or as a rectifying diode depending upon how the thyristors gate is triggered. In other words, thyristors can operate only in the switching mode and cannot be used for amplification.

The thyristor is a three-terminal device labelled: “Anode”, “Cathode” and “Gate” and consisting of three PN junctions which can be switched “ON” and “OFF” at an extremely fast rate, or it can be switched “ON” for variable lengths of time during half cycles to deliver a selected amount of power to a load. The operation of the thyristor can be best explained by assuming it to be made up of two transistors connected back-to-back as a pair of complementary regenerative switches as shown.

The two transistor equivalent circuit shows that the collector current of the NPN transistor $TR_2$ feeds directly into the base of the PNP transistor $TR_1$, while the collector current of $TR_1$ feeds into the base of $TR_2$. These two inter-connected transistors rely upon each other for conduction as each transistor gets its base-emitter current from the other’s collector-emitter current. So until one of the transistors is given some base current nothing can happen even if an Anode-to-Cathode voltage is present.

When the thyristors Anode terminal is negative with respect to the Cathode, the centre *N-P* junction is forward biased, but the two outer *P-N* junctions are reversed biased and it behaves very much like an ordinary diode. Therefore a thyristor blocks the flow of reverse current until at some high voltage level the breakdown voltage point of the two outer junctions is exceeded and the thyristor conducts without the application of a Gate signal.

This is an important negative characteristic of the thyristor, as **Thyristors**can be unintentionally triggered into conduction by a reverse over-voltage as well as high temperature or a rapidly rising *dv/dt* voltage such as a spike.

If the Anode terminal is made positive with respect to the Cathode, the two outer *P-N* junctions are now forward biased but the centre *N-P* junction is reverse biased. Therefore forward current is also blocked. If a positive current is injected into the base of the NPN transistor $TR_2$, the

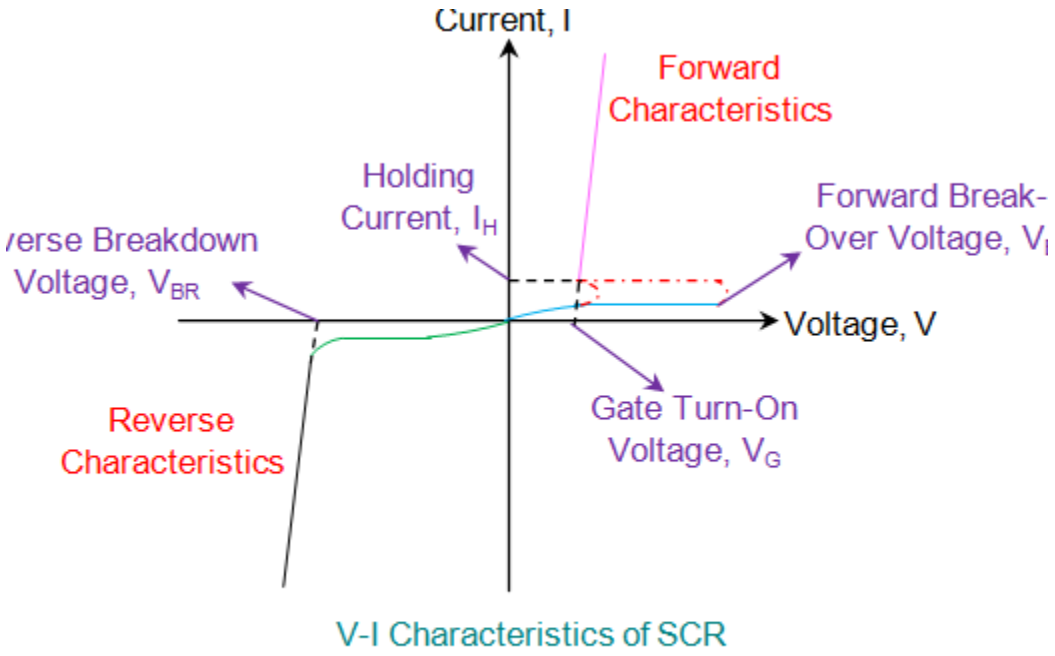
resulting collector current flows in the base of transistor $TR_1$. This in turn causes a collector current to flow in the PNP transistor, $TR_1$ which increases the base current of $TR_2$ and so on.

Very rapidly the two transistors force each other to conduct to saturation as they are connected in a regenerative feedback loop that can not stop. Once triggered into conduction, the current flowing through the device between the Anode and the Cathode is limited only by the resistance of the external circuit as the forward resistance of the device when conducting can be very low at less than 1Ω so the voltage drop across it and power loss is also low.

Then we can see that a thyristor blocks current in both directions of an AC supply in its "OFF" state and can be turned "ON" and made to act like a normal rectifying diode by the application of a positive current to the base of transistor, $TR_2$ which for a silicon controlled rectifier is called the "Gate" terminal.

The operating voltage-current **I-V** characteristics curves for the operation of a **Silicon Controlled Rectifier** are given as:

**Thyristor I-V Characteristics Curves**




V-I Characteristics of SCR

Once the thyristor has been turned "ON" and is passing current in the forward direction (anode positive), the gate signal looses all control due to the regenerative latching action of the two internal transistors. The application of any gate signals or pulses after regeneration is initiated will have no effect at all because the thyristor is already conducting and fully-ON.

Unlike the transistor, the SCR can not be biased to stay within some active region along a load line between its blocking and saturation states. The magnitude and duration of the gate "turn-on" pulse has little effect on the operation of the device since conduction is controlled internally. Then applying a momentary gate pulse to the device is enough to cause it to conduct and will remain permanently "ON" even if the gate signal is completely removed.

Therefore the thyristor can also be thought of as a *Bistable Latch* having two stable states "OFF" or "ON". This is because with no gate signal applied, a silicon controlled rectifier blocks current

in both directions of an AC waveform, and once it is triggered into conduction, the regenerative latching action means that it cannot be turned "OFF" again just by using its Gate.

Once the thyristor has self-latched into its "ON" state and passing a current, it can only be turned "OFF" again by either removing the supply voltage and therefore the Anode ($I_A$) current completely, or by reducing its Anode to Cathode current by some external means (the opening of a switch for example) to below a value commonly called the "minimum holding current", $I_H$.

The Anode current must therefore be reduced below this minimum holding level long enough for the thyristors internally latched pn-junctions to recover their blocking state before a forward voltage is again applied to the device without it automatically self-conducting. Obviously then for a thyristor to conduct in the first place, its Anode current, which is also its load current, $I_L$ must be greater than its holding current value. That is $I_L > I_H$.

Since the thyristor has the ability to turn "OFF" whenever the Anode current is reduced below this minimum holding value, it follows then that when used on a sinusoidal AC supply the SCR will automatically turn itself "OFF" at some value near to the cross over point of each half cycle, and as we now know, will remain "OFF" until the application of the next Gate trigger pulse.

Since an AC sinusoidal voltage continually reverses in polarity from positive to negative on every half-cycle, this allows the thyristor to turn "OFF" at the $180^o$ zero point of the positive waveform. This effect is known as "natural commutation" and is a very important characteristic of the silicon controlled rectifier.

Thyristors used in circuits fed from DC supplies, this natural commutation condition cannot occur as the DC supply voltage is continuous so some other way to turn "OFF" the thyristor must be provided at the appropriate time because once triggered it will remain conducting.

However in AC sinusoidal circuits natural commutation occurs every half cycle. Then during the positive half cycle of an AC sinusoidal waveform, the thyristor is forward biased (anode

positive) and a can be triggered "ON" using a Gate signal or pulse. During the negative half cycle, the Anode becomes negative while the Cathode is positive. The thyristor is reverse biased by this voltage and cannot conduct even if a Gate signal is present.

So by applying a Gate signal at the appropriate time during the positive half of an AC waveform, the thyristor can be triggered into conduction until the end of the positive half cycle. Thus phase control (as it is called) can be used to trigger the thyristor at any point along the positive half of the AC waveform and one of the many uses of a **Silicon Controlled Rectifier** is in the power control of AC systems as shown

**Static Characteristics of a Thyristor**

- Thyristors are semiconductor devices that can operate only in the switching mode.
- Thyristor are current operated devices, a small Gate current controls a larger Anode current.
- Conducts current only when forward biased and triggering current applied to the Gate.
- The thyristor acts like a rectifying diode once it is triggered "ON".
- Anode current must be greater than holding current to maintain conduction.
- Blocks current flow when reverse biased, no matter if Gate current is applied.
- Once triggered "ON", will be latched "ON" conducting even when a gate current is no longer applied providing Anode current is above latching current.

The **Unijunction Transistor**

The **Unijunction Transistor** or **UJT** for short, is another solid state three terminal device that can be used in gate pulse, timing circuits and trigger generator applications to switch and control either thyristors and triac's for AC power control type applications.

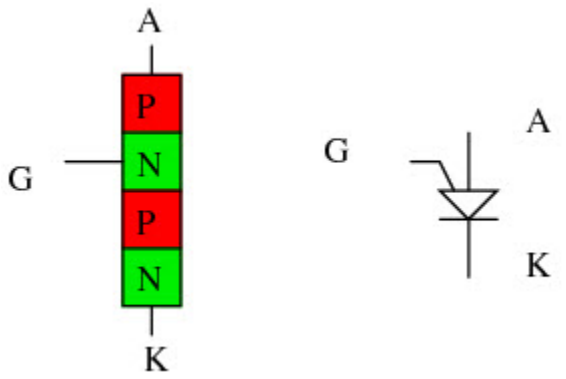
Like diodes, unijunction transistors are constructed from separate P-type and N-type semiconductor materials forming a single (hence its name Uni-Junction) PN-junction within the main conducting N-type channel of the device.

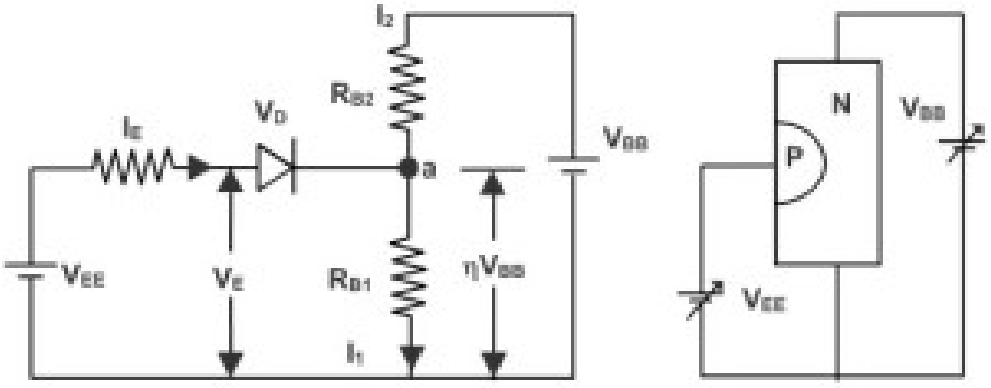
Although the *Unijunction Transistor* has the name of a transistor, its switching characteristics are very different from those of a conventional bipolar or field effect transistor as it can not be used to amplify a signal but instead is used as a ON-OFF switching transistor. UJT's have unidirectional conductivity and negative impedance characteristics acting more like a variable voltage divider during breakdown.

Like N-channel FET's, the UJT consists of a single solid piece of N-type semiconductor material forming the main current carrying channel with its two outer connections marked as *Base 2* ( $B_2$ ) and *Base 1* ( $B_1$ ). The third connection, confusingly marked as the *Emitter* ( E ) is located along the channel. The emitter terminal is represented by an arrow pointing from the P-type emitter to the N-type base.

The Emitter rectifying p-n junction of the unijunction transistor is formed by fusing the P-type material into the N-type silicon channel. However, P-channel UJT's with an N-type Emitter terminal are also available but these are little used.

The Emitter junction is positioned along the channel so that it is closer to terminal $B_2$ than $B_1$. An arrow is used in the UJT symbol which points towards the base indicating that the Emitter terminal is positive and the silicon bar is negative material. Below shows the symbol, construction, and equivalent circuit of the UJT.


A
P
N
P
N
K
G
G
A
K


$I_2$
$R_{B2}$
$V_D$
$I_E$
a
$V_{BB}$
$V_{EE}$
$V_E$
$R_{B1}$
$\eta V_{BB}$
$I_1$
N
P
$V_{BB}$
$V_{EE}$

Notice that the symbol for the unijunction transistor looks very similar to that of the junction field effect transistor or JFET, except that it has a bent arrow representing the Emitter( E ) input. While similar in respect of their ohmic channels, JFET's and UJT's operate very differently and should not be confused.

So how does it work? We can see from the equivalent circuit above, that the N-type channel basically consists of two resistors $R_{B2}$ and $R_{B1}$ in series with an equivalent (ideal) diode, D representing the p-n junction connected to their center point. This Emitter p-n junction is fixed in position along the ohmic channel during manufacture and can therefore not be changed.

Resistance $R_{B1}$ is given between the Emitter, E and terminal $B_1$, while resistance $R_{B2}$ is given between the Emitter, E and terminal $B_2$. As the physical position of the p-n junction is closer to terminal $B_2$ than $B_1$ the resistive value of $R_{B2}$ will be less than $R_{B1}$.

The total resistance of the silicon bar (its Ohmic resistance) will be dependent upon the semiconductors actual doping level as well as the physical dimensions of the N-type silicon channel but can be represented by$R_{BB}$. If measured with an ohmmeter, this static resistance would typically measure somewhere between about 4kΩ and 10kΩ's for most common UJT's such as the 2N1671, 2N2646 or the 2N2647.

These two series resistances produce a voltage divider network between the two base terminals of the unijunction transistor and since this channel stretches from $B_2$ to $B_1$, when a voltage is applied across the device, the potential at any point along the channel will be in proportion to its position between terminals $B_2$ and $B_1$. The level of the voltage gradient therefore depends upon the amount of supply voltage.

When used in a circuit, terminal $B_1$ is connected to ground and the Emitter serves as the input to the device. Suppose a voltage $V_{BB}$ is applied across the UJT between $B_2$ and $B_1$ so that $B_2$ is biased positive relative to $B_1$. With zero Emitter input applied, the voltage developed across $R_{B1}$ (the lower resistance) of the resistive voltage divider can be calculated as:

**Unijunction Transistor $R_{B1}$ Voltage**

For a unijunction transistor, the resistive ratio of $R_{B1}$ to $R_{BB}$ shown above is called the **intrinsic stand-off ratio** and is given the Greek symbol: **η** (eta). Typical standard values of η range from 0.5 to 0.8 for most common UJT's.

If a small positive input voltage which is less than the voltage developed across resistance, $R_{B1}$ ( $\eta V_{BB}$ ) is now applied to the Emitter input terminal, the diode p-n junction is reverse biased, thus offering a very high impedance and the device does not conduct. The UJT is switched "OFF" and zero current flows.

However, when the Emitter input voltage is increased and becomes greater than $V_{RB1}$ (or $\eta V_{BB}$ + 0.7V, where 0.7V equals the p-n junction diode volt drop) the p-n junction becomes forward biased and the unijunction transistor begins to conduct. The result is that Emitter current, $\eta I_E$ now flows from the Emitter into the Base region.

The effect of the additional Emitter current flowing into the Base reduces the resistive portion of the channel between the Emitter junction and the $B_1$terminal. This reduction in the value of $R_{B1}$ resistance to a very low value means that the Emitter junction becomes even more

forward biased resulting in a larger current flow. The effect of this results in a negative resistance at the Emitter terminal.

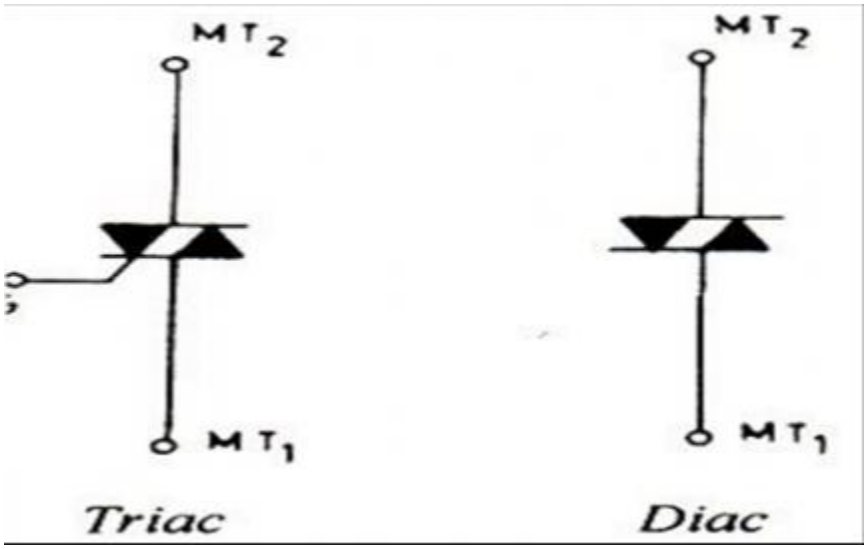
Likewise, if the input voltage applied between the Emitter and $B_1$ terminal decreases to a value below breakdown, the resistive value of $R_{B1}$ increases to a high value. Then the **Unijunction Transistor** can be thought of as a voltage breakdown device.

So we can see that the resistance presented by $R_{B1}$ is variable and is dependant on the value of Emitter current, $I_E$. Then forward biasing the Emitter junction with respect to $B_1$ causes more current to flow which reduces the resistance between the Emitter, E and $B_1$.

In other words, the flow of current into the UJT's Emitter causes the resistive value of $R_{B1}$ to decrease and the voltage drop across it, $V_{RB1}$ must also decrease, allowing more current to flow producing a negative resistance condition.

**DIAC and TRIAC**

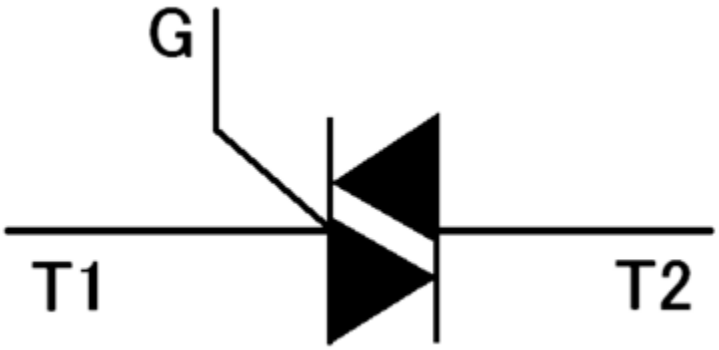
here are several applications where it is preferred to regulate the power fed to a load. For instance: using electrical methods controlling the speed of a motor or fan. But, these methods do not allow a fine control over the flow of power in a system additionally; there is an extensive wastage of power. In the present days, such devices have been developed which can allow a fine control over the flow of large blocks of power in a system. These devices perform as controlled switches and can complete the duties of controlled rectification, regulation and inversion of power in a load. The essential semiconductor switching devices are UJT, SCR, DIAC and TRIAC.




**Difference between Diac and Triac**

The differences between diac and triac mainly include what are a diac and triac, construction of triac and diac, working, characteristics and applications

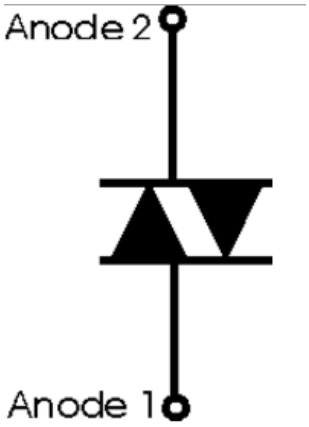
A Triac device comprises of two thyristors that are connected in opposite direction but in parallel but, it is controlled by the same gate. Triac is a 2-dimensional thyristor which is activated on both halves of the i/p AC cycle using + Ve or -Ve gate pulses. The three terminals of the Triac are MT1; MT2 & gate terminal (G). Generating pulses are applied between MT1 and gate terminals. The 'G' current to switch 100A from triac is not more than 50mA or so.




***TRIAC***

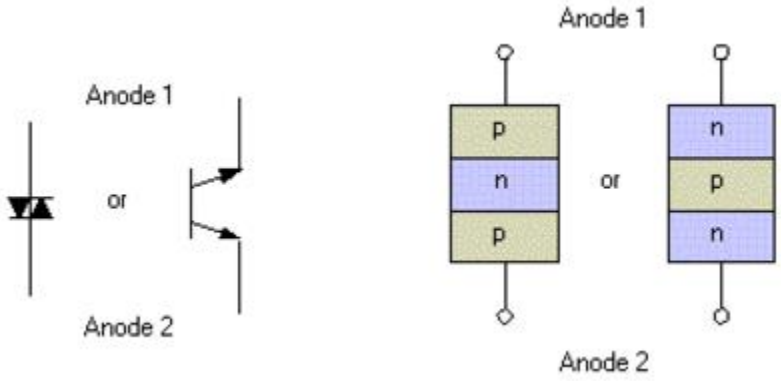
The DIAC is a bi-directional semiconductor switch that can be switched on in both polarities. The full form of the name DIAC is diode alternating current. Diac is connected back to back using two zener diodes and the main application of this DIAC is, it is widely used to help even activating of a TRIAC when used in AC switches, dimmer applications and starter circuits for florescent lamps

DIAC




**Construction and Operation of DIAC**

Basically, the DIAC is a two terminal device; it is a combination of parallel semiconductor layers that allows activating in one direction.This device is used to activating device for the triac. The basic construction of diac consist of two terminals namely MT1 and MT2. When the MT1 terminal is designed +Ve with respect to the terminal MT2, the transmission will take place to the p-n-p-n structure that is another four layer diaode. The diac can be performing for both the direction. Then symbol of the diac look like a transistor.




The DIAC is basically a diode that conducts after a 'break-over' voltage, selected VBO, and is exceeded. When the diode surpasses the break-over voltage, then it goes into the negative dynamic resistance of region. This causes in a reduce in the voltage drop across the diode with rising voltage. So there is a quick increase in the current level that is mannered by the device.

The diode leftovers in its transmission state until the current through it falls below, what is termed the holding current, which is usually chosen by the letters IH. The holding current, the DIAC reverts to its non-conducting state. Its behavior is bidirectional and thus its function takes place on both halves of an alternating cycle.

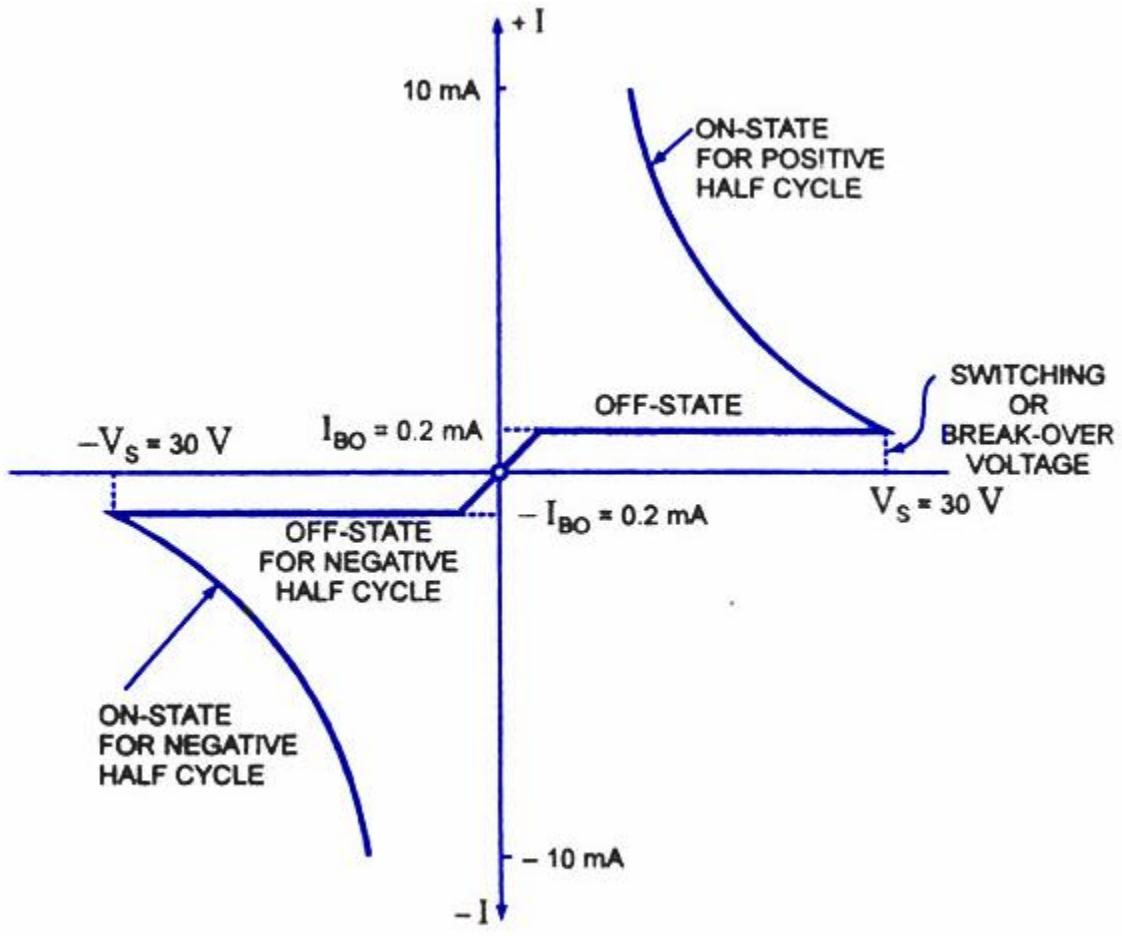
***Characteristics of DIAC***

V-I characteristics of a diac is shown below

Volt-ampere characteristic of a diac is shown in figure. Its looks like a letter Z due to symmetrical switching characteristics for each polarity of the applied voltage.

The diac performs like an open-circuit until its switching is exceeded. At that position the diac performs until its current decreases toward zero. Because of its abnormal construction, doesn't switch sharply into a low voltage condition at a low current level like the triac or SCR, once it

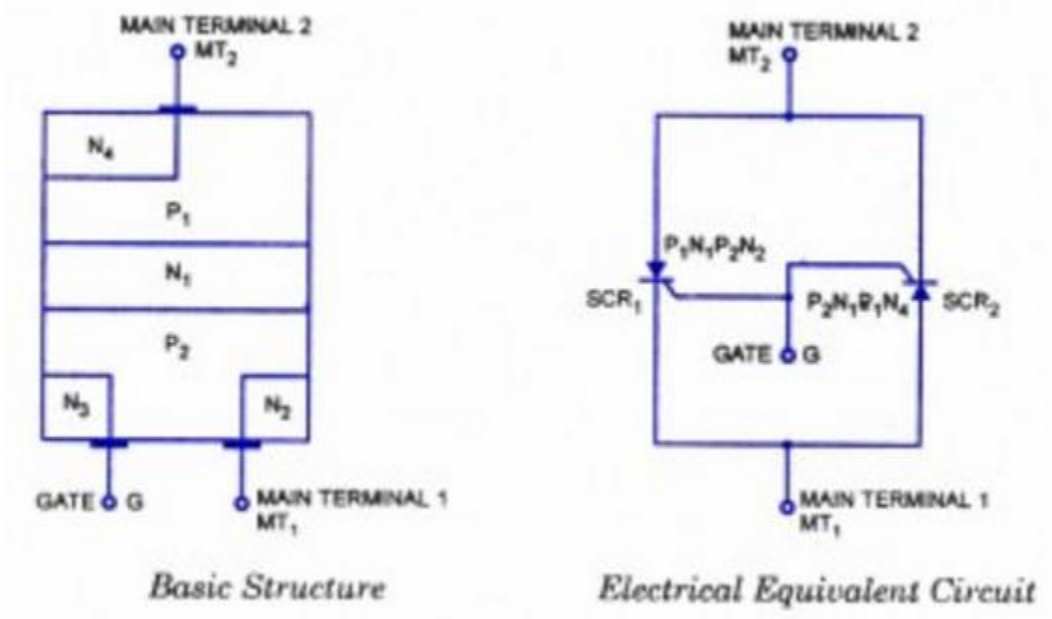
goes into transmission, the diac preserves an almost continuous –Ve resistance characteristic, that means, voltage reduces with the enlarge in current. This means that, unlike the triac and the SCR, the diac cannot be estimated to maintain a low voltage drop until its current falls below the level of holding current.




*V-I Characteristic of a Diac*

## Construction and Operation of TRIAC

Traic is a three terminal device and the terminals of the triac are MT1, MT2 and Gate. Here the gate terminal is the control terminal. The flow of current in the triac is bi directional that means current can flow in both the directions. The structure of triac is shown in the below figure. Here, in the structure of triac, two SCRs are connected in the anti parallel and it will acts like a switch for both the directions. In the above structure, the MT1 and gate terminals are near to each other. When the gate terminal is open, the triac will obstruct the both the polarities of the voltage across the MT1 & MT2.




*Basic Structure* *Electrical Equivalent Circuit*

### *haracteristics of TRIAC*

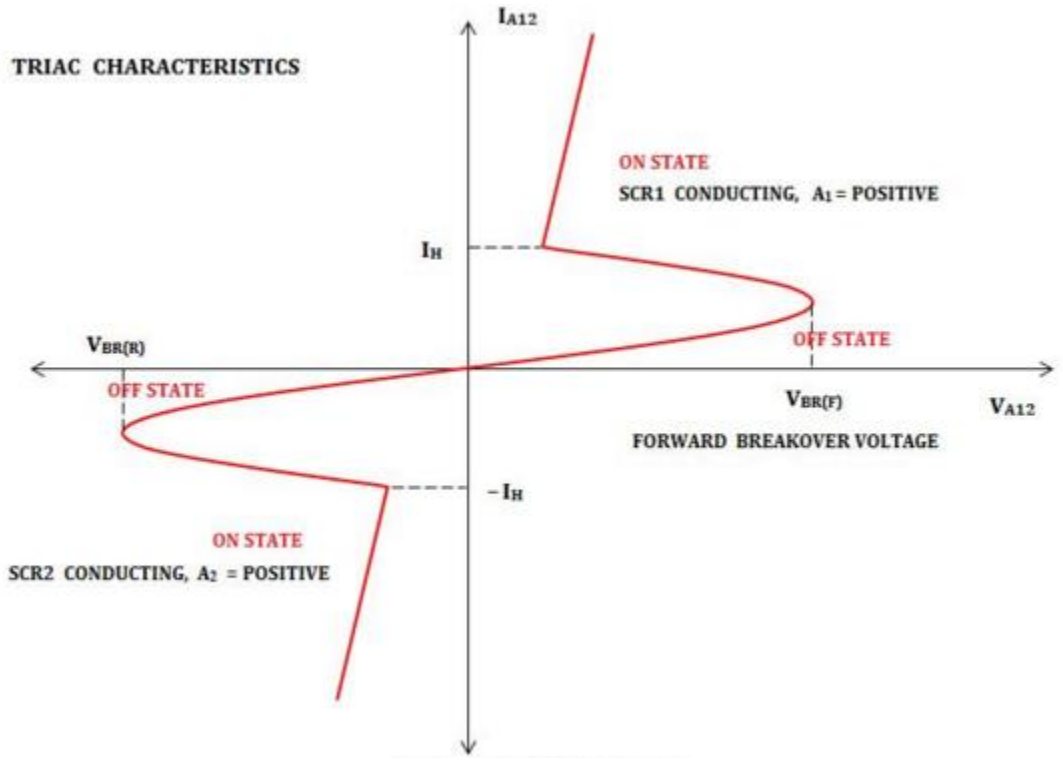
The V-I characteristics of TRIAC are discussed below

The triac is designed with two SCRs which are fabricated in the opposite direction in a crystal. Operating characteristics of triac in the 1st and 3rd quadrants are similar but for the direction of flow of current and applied voltage.

The V-I characteristics of triac in the first and third quadrants are basically equal to those of an SCR in the first quadrant.

It can be functioned with either +Ve or –Ve gate control voltage but in typical operation generally the gate voltage is +Ve in first quadrant and -Ve in third quadrant.

The supply voltage of the triac to switch ON depends upon the gate current. This allows utilizing a triac to regulate AC power in a load from zero to full power in a smooth and permanent manner with no loss in the device control.



**POSSIBLE QUESTIONS**

**PART-B (2 marks)**

1.define h parameters

2. Define stabilization of transistor.

3.Define transconductance

4.What are the difference between BJT and FET?

5.What are the different mode of operation of MOSFET?

6.What is enhanced mode of operation?

7. What is the need of transistor biasing?

8. Define PIV.

9. What do you mean by thermal runway?

10. What are the difference between MOSFET and FET?

**PART-C (6 marks)**

1. Explain the basic construction and operation of a transistor.
2. Explain the basic construction and operation of a SCR
3. Explain the basic construction and operation of a UJT
4. Explain the basic construction and operation of a DIAC
5. Explain the basic construction and operation of a TRIAC
6. Define h-parameters of a CE amplifier. How can these parameters be determined from the characteristic curve?

7. What is the condition for thermal stability? Explain.
8. Explain how a MOSFET is used as a load. Obtain the Volt-Ampere characteristic of this load graphically
9. List the three sources of instability of collector current. Define the three stability factors.
10. Explain $r_d$, $g_m$ and $\mu$ of a FET and how they are determined from the static characteristic?
11. Draw a typical common emitter amplifier and explain the function of each component in it.
12. Explain, how h-parameter can be obtained from the transistor characteristics.
13. Discuss the benefits of h-parameters.
14. Explain how a MOSFET is used as a load. Obtain the Volt-Ampere characteristic of this load graphically.

15.What specific capacitance has the greatest effect on the high frequency response of a cascade of FET amplifiers? Explain

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**UNIT I :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| QUESTIONS | CHOICE1 | CHOICE2 | CHOICE3 | CHOICE4 | ANSWER |
|---|---|---|---|---|---|
| **UNIT I** | | | | | |
| A transistor has how many pn junctions? | 1 | 2 | 3 | 4 | 2 |
| In an npn transistor, the majority carriers in the emitter are | free electrons | holes | neither | both | free electrons |
| The barrier potential across each silicon depletion layer is | 0V | 0.3V | 0.7V | 1V | 0.7V |
| The base of an npn transistor is thin and | Heavily doped | Lightly doped | Metallic | Doped by a pentavalent material | Lightly doped |
| The emitter of a transistor is generally doped the heaviest because it | has to dissipate maximum power | has to supply the charge carriers | is the first region of the transistor | must possess low resistance | has to dissipate maximum power |
| When a transistor is fully switched ON, it is said to be | shorted | saturated | open | cut-off | saturated |
| A FET consists of a | source | drain | gate | all the above | all the above |
| The extremely high input impedance of a MOSFET is primarily due to the | absence of its channel | negative gate-source voltage | depletion of current carriers | extremely small leakage current of its gate capacitor | extremely small leakage current of its gate capacitor |
| When a transistor is used as a switch, it is stable in which two distinct regions? | saturation and active | active and cutoff | saturation and cutoff | none of the above | saturation and cutoff |

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| | | | | | |
|---|---|---|---|---|---|
| The term BJT is short for | base junction transistor | binary junction transistor | both junction transistor | bipolar junction transistor | bipolar junction transistor |
| What are the two types of bipolar junction transistors? | npn and pnp | pnn and nnp | ppn and nnp | pts and stp | npn and pnp |
| The magnitude of dark current in a phototransistor usually falls in what range? | mA | mA | nA | pA | nA |
| Junction Field Effect Transistors (JFET) contain how many diodes? | 4 | 3 | 2 | 1 | 1 |
| When not in use, MOSFET pins are kept at the same potential through the use of: | shipping foil | nonconductive foam | conductive foam | a wrist strap | conductive foam |
| A MOSFET has how many terminals? | 2 or 3 | 3 | 4 | 3 or 4 | 3 or 4 |
| A very simple bias for a D-MOSFET is called: | self biasing | gate biasing | zero biasing | voltage-divider biasing | zero biasing |
| Hybrid means | mixed | single | iunique | none of the above | mixed |
| There are _____ h- parameters of a transistor. | two | four | three | none of the above | four |
| The h- parameter approach gives correct results for | large signals only | small signals only | both small and large signals | none of the above | small signals only |
| If the operating point changes, the h-parameters of transistor | also change | do not change | may or may not change | none of above | also change |
| The dc load line on a family of collector characteristic curves of a transistor shows the | saturation region. | cutoff region. | active region. | all of the above | all of the above |
| A transistor data sheet usually identifies $\beta_{DC}$ as | $h_{re}$. | $h_{fe}$. | $I_C$. | $V_{CE}$. | $h_{fe}$ |

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**UNIT I :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| | | | | | |
|---|---|---|---|---|---|
| When a transistor is used as a switch, it is stable in which two distinct regions? | saturation and active | active and cutoff | saturation and cutoff | none of the above | saturation and cutoff |
| For a silicon transistor, when a base-emitter junction is forward-biased, it has a nominal voltage drop of | 0.7 V. | 0.3 V. | 0.2 V. | $V_{CC}$. | 0.7 V |
| The value of $\beta_{DC}$ | is fixed for any particular transistor. | varies with temperature. | varies with $I_C$. | varies with temperature and $I_C$. | varies with temperature and $I_C$. |
| The term BJT is short for | base junction transistor. | binary junction transistor. | both junction transistor. | bipolar junction transistor. | bipolar junction transistor |
| A BJT has an $I_B$ of 50 μA and a βDC of 75; $I_C$ is: | 375 mA | 37.5 mA | 3.75 mA | 0.375 mA | 3.75 mA |
| A certain transistor has $I_C$ = 15 mA and $I_B$ = 167 μA; $\beta_{DC}$ is: | 15 | 167 | 0.011 | 90 | 90 |
| For normal operation of a pnp BJT, the base must be _____ with respect to the emitter and _____ with respect to the collector. | positive, negative | positive, positive | negative, positive | negative, negative | negative, positive |
| A transistor amplifier has a voltage gain of 100. If the input voltage is 75 mV, the output voltage is: | 1.33 V | 7.5 V | 13.3 V | 15 V | 7.5 V |
| A 35 mV signal is applied to the base of a properly biased transistor with an $r'_e$ = 8 Ω and $R_C$ = 1 kΩ. The output signal voltage at the collector is: | 3.5 V | 28.57 V | 4.375 V | 4.375 mV | 4.375 V |
| What is the order of doping, from heavily to lightly doped, for each region? | base, collector, emitter | emitter, collector, base | emitter, base, collector | collector, emitter, base | emitter, collector, base |

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**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| | | | | | |
|---|---|---|---|---|---|
| What are the two types of bipolar junction transistors? | npn and pnp | pnn and nnp | ppn and nnp | pts and stp | npn and pnp |
| Which of the following is true for an npn or pnp transistor? | $I_E = I_B + I_C$ | $I_B = I_C + I_E$ | $I_C = I_B + I_E$ | none of the above | $I_E = I_B + I_C$ |
| What is the ratio of $I_C$ to $I_B$? | $\beta_{DC}$ | $h_{FE}$ | $\alpha_{DC}$ | either $\beta_{DC}$ or $h_{FE}$, but not $\alpha_{DC}$ | either $\beta_{DC}$ or $h_{FE}$, but not $\alpha_{DC}$ |
| What is the ratio of $I_C$ to $I_E$? | $\beta_{DC}$ | $\beta_{DC} / (\beta_{DC} + 1)$ | $\alpha_{DC}$ | either $\beta_{DC} / (\beta_{DC} + 1)$ or $\alpha_{DC}$, but not $\beta_{DC}$ | either $\beta_{DC} / (\beta_{DC} + 1)$ or $\alpha_{DC}$, but not $\beta_{DC}$ |
| In what range of voltages is the transistor in the linear region of its operation? | $0 < V_{CE}$ | $0.7 < V_{CE} < V_{CE(max)}$ | $V_{CE(max)} > V_{CE}$ | none of the above | $0.7 < V_{CE} < V_{CE(max)}$ |
| What does DC vary with? | $I_C$ | $^oC$ | both $I_C$ and $^oC$ | $I_C$, but not $^oC$ | both $I_C$ and $^oC$ |
| What is (are) common fault(s) in a BJT-based circuit? | pens or shorts internal to the transistor | open bias resistor(s) | external opens and shorts on the circuit board | all of the above | all of the above |
| What is (are) general-purpose/small-signal transistors case type(s)? | TO-18 | TO-92 | TO-39 | all of the above | all of the above |
| The magnitude of dark current in a phototransistor usually falls in what | mA | µA | nA | pA | nA |

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| | | | | | |
|---|---|---|---|---|---|
| range? | | | | | |
| On the drain characteristic curve of a JFET for $V_{GS} = 0$, the pinch-off voltage is | below the ohmic area. | between the ohmic area and the constant current area. | between the constant current area and the breakdown region. | above the breakdown region. | between the ohmic area and the constant current area |
| For a JFET, the value of $V_{DS}$ at which $I_D$ becomes essentially constant is the | pinch-off voltage. | cutoff voltage. | breakdown voltage. | ohmic voltage. | pinch-off voltage |
| The value of $V_{GS}$ that makes $I_D$ approximately zero is the | pinch-off voltage. | cutoff voltage. | breakdown voltage. | ohmic voltage. | cutoff voltage |
| For a JFET, the change in drain current for a given change in gate-to-source voltage, with the drain-to-source voltage constant, is | breakdown. | reverse transconductance. | forward transconductance. | self-biasing. | forward transconductance |
| High input resistance for a JFET is due to | a metal oxide layer. | a large input resistor to the device. | an intrinsic layer. | the gate-source junction being reverse-biased. | the gate-source junction being reverse-biased |
| A dual-gated MOSFET is | a depletion MOSFET. | an enhancement MOSFET. | a VMOSFET. | either a depletion or an enhancement MOSFET. | either a depletion or an enhancement MOSFET |

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**DEPARTMENT OF PHYSICS**

**UNIT I :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| | | | | | |
|---|---|---|---|---|---|
| Which of the following devices has the highest input resistance? | diode | JFET | MOSFET | bipolar junction transistor | MOSFET |
| A self-biased n-channel JFET has a $V_D$ = 6 V. $V_{GS}$ = –3 V. Find the value of $V_{DS}$. | –3 V | –6 V | 3 V | 6 V | –6 V |
| A JFET data sheet specifies $V_{GS(off)}$ = –6 V and $I_{DSS}$ = 8 mA. Find the value of $I_D$ when $V_{GS}$ = –3 V. | 2 mA | 4 mA | 8 mA | none of the above | 2 mA |
| A JFET data sheet specifies $V_{GS(off)}$ = –10 V and $I_{DSS}$ = 8 mA. Find the value of $I_D$ when $V_{GS}$ = –3 V. | 2 mA | 1.4 mA | 4.8 mA | 3.92 mA | 3.92 mA |
| The JFET is always operated with the gate-source pn junction _____ -biased. | forward | reverse | all of the above | none of the above | reverse |
| What three areas are the drain characteristics of a JFET ($V_{GS}$ = 0) divided into? | ohmic, constant-current, breakdown | pinch-off, constant-current, avalanche | ohmic, constant-voltage, breakdown | none of the above | ohmic, constant-current, breakdown |
| What type(s) of gate-to-source voltage(s) can a depletion MOSFET (D-MOSFET) operate with? | zero | positive | negative | any of the above | any of the above |
| The _____ has a physical channel between the drain and source. | D-MOSFET | E-MOSFET | V-MOSFET | none of the above | D-MOSFET |
| All MOSFETs are subject to damage from electrostatic discharge (ESD). | TRUE | FALSE | | | TRUE |
| Midpoint bias for a D-MOSFET is $I_D$ = _____, obtained by setting $V_{GS}$ = 0. | $I_{DSS}$ / 2 | $I_{DSS}$ / 3.4 | $I_{DSS}$ | | $I_{DSS}$ |

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**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| | | | | | |
|---|---|---|---|---|---|
| In a self-biased JFET circuit, if $V_D = V_{DD}$ then ID = _____. | 0 | cannot be determined from information above | | | 0 |
| If $V_D$ is less than expected (normal) for a self-biased JFET circuit, then it could be caused by a(n) | open $R_G$. | open gate lead. | FET internally open at gate. | all of the above | all of the above |
| The resistance of a JFET biased in the ohmic region is controlled by | $V_D$. | $V_{GS}$. | $V_S$. | $V_{DS}$. | |
| | | | | | |
| **Prepared By-Ambili Vipin,Assistant Professor,Department of Physics** | | | | | |
| | | | | | |

## UNIT-II
## SYLLABUS

Frequency response of amplifiers General concepts; bode plot; low frequency response: BJT and FET amplifiers; miller effect capacitance; high frequency response of BIT amplifiers; hybrid pie model: short circuit current gain, cut off frequency, and current gain with resistive load; high frequency response of FET amplifiers; frequency response of multistage amplifiers; square wave testing. Numerical problems.

## FREQUENCY RESPONSE OF AMPLIFIERS - GENERAL CONCEPTS

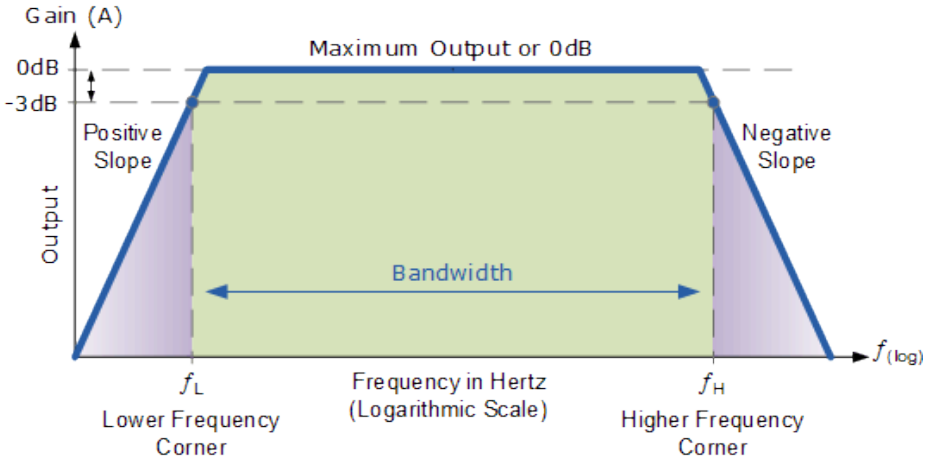
Frequency Response of an electric or electronics circuit allows us to see exactly how the output gain (known as the magnitude response) and the phase (known as the phase response) changes at a particular single frequency, or over a whole range of different frequencies from 0Hz, to many thousands of mega-hertz, (MHz) depending upon the design characteristics of the circuit.

Generally, the frequency response analysis of a circuit or system is shown by plotting its gain, that is the size of its output signal to its input signal, Output/Input against a frequency scale over which the circuit or system is expected to operate. Then by knowing the circuits gain, (or loss) at each frequency point helps us to understand how well (or badly) the circuit can distinguish between signals of different frequencies.

The frequency response of a given frequency dependent circuit can be displayed as a graphical sketch of magnitude (gain) against frequency ($f$). The horizontal frequency axis is usually plotted on a logarithmic scale while the vertical axis representing the voltage output or gain, is usually drawn as a linear scale in decimal divisions. Since a systems gain can be both positive and negative, the y-axis can therefore have both positive and negative values.

Graphical representations of frequency response curves are called Bode Plots and as such Bode plots are generally said to be a semi-logarithmic graphs because one scale (x-axis) is logarithmic and the other (y-axis) is linear (log-lin plot) as shown.

**Frequency Response Curve**




Frequency response of any given circuit is the variation in its behavior with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between $f_L$ and $f_H$ is called the circuit's bandwidth. So from this we are able to determine the voltage gain (in dB) for any sinusoidal input within a given frequency range.

As mentioned above, the Bode diagram is a logarithmic presentation of the frequency response. For example most modern audio amplifiers have a flat frequency response as shown above over the whole audio range of frequencies from 20 Hz to 20 kHz. This range of frequencies, for an audio amplifier is called its Bandwidth, (BW) and is primarily determined by the frequency response of the circuit.

Frequency points $f_L$ and $f_H$ relate to the lower corner or cut-off frequency and the upper corner or cut-off frequency points respectively were the circuits gain falls off at high and low frequencies. These points on a frequency response curve are known commonly as the -3dB (decibel) points. So the bandwidth is simply given as:

Bandwidth, (BW) = $f_H - f_L$

The decibel, (dB) which is $1/10^{th}$ of a bel (B), is a common non-linear unit for measuring gain and is defined as $20\log_{10}(A)$ where A is the decimal gain, being plotted on the y-axis. Zero decibels, (0dB) corresponds to a magnitude function of unity giving the maximum output. In other words, 0dB occurs when Vout = Vin as there is no attenuation at this frequency level and is given as:

$$V_{OUT/VIN} = 1$$

Therefore

$$20 \log(1) = 0 \text{ dB}$$

From the Bode plot above that at the two corner or cut-off frequency points, the output drops from 0dB to -3dB and continues to fall at a fixed rate. This fall or reduction in gain is known commonly as the roll-off region of the frequency response curve. In all basic single order amplifier and filter circuits this roll-off rate is defined as 20dB/decade, which is an equivalent to a rate of 6dB/octave. These values are multiplied by the order of the circuit.

These -3dB corner frequency points define the frequency at which the output gain is reduced to 70.71% of its maximum value. Then we can correctly say that the -3dB point is also the frequency at which the systems gain has reduced to 0.707 of its maximum value.

Frequency Response -3dB Point

$$-3\text{dB} = 20\log_{10}(0.7071)$$

The -3dB point is also known as the half-power points since the output power at this corner frequencies will be half that of its maximum 0dB value

$$P = V^2 / R = I^2 \times R$$

At $f_{L\ or}\ f_H$

V or I =70.71% maximum or 0.7071 max

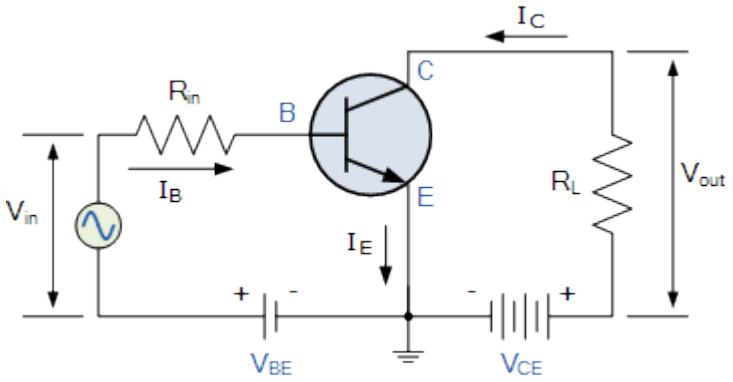
Therefore the amount of output power delivered to the load is effectively "halved" at the cut-off frequency and as such the bandwidth (BW) of the frequency response curve can also be defined as the range of frequencies between these two half-power points.

While for voltage gain we use $20\log_{10}$ (Av), and for current gain $20\log_{10}$ (Ai), for power gain we use $10\log_{10}$(Ap). Note that the multiplying factor of 20 does not mean that it is twice as much as 10 as the decibel is a unit of the power ratio and not a measure of the actual power level. Also gain in dB can be either positive or negative with a positive value indicating gain and a negative value attenuation.

BJT AND FET AMPLIFIERS;

An amplifier is one of the most commonly used electronic devices in the world. It's a basic building block of a vast number of circuits, and comes in various forms. Amplifiers can be defined simply as an electronic device that increases the power of a signal. In other words, it increases the amplitude of a signal, and makes it stronger than the given input. An amplifier is an electronic device that increases the voltage, current, or power of a signal.

BJT AMPLIFIERS



In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib.

As the load resistance ( RL ) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, ( β ).

As the emitter current for a common emitter configuration is defined asIe = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

Since the electrical relationship between these three currents, Ib, Ic and Ieis determined by the physical construction of the transistor itself, any small change in the base current ( Ib ), will result in a much larger change in the collector current ( Ic ).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminal.

By combining the expressions for both Alpha, α and Beta, β the mathematical relationship between these parameters and therefore the current gain of the transistor can be given as:

$$\text{Alpha } \alpha = Ic/Ie \text{ and } \beta = Ic/Ib$$

$$\text{Therefore } Ic = \alpha.Ie = \beta.Ib$$

$$\text{As } \alpha = \beta/\beta+1$$

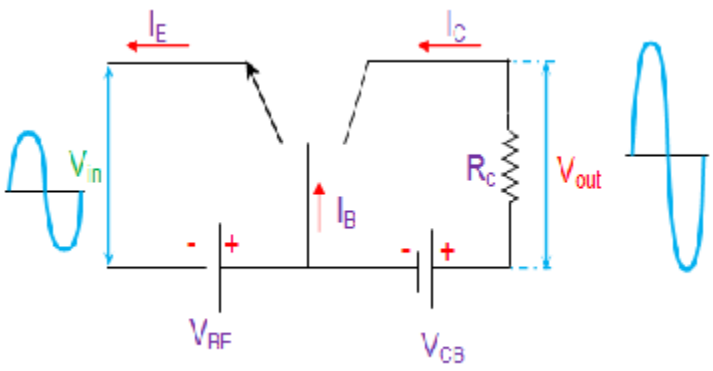
$$B = \alpha/\alpha-1$$

$$I_E = I_C + I_B$$

Where: "Ic" is the current flowing into the collector terminal, "Ib" is the current flowing into the base terminal and "Ie" is the current flowing out of the emitter terminal.

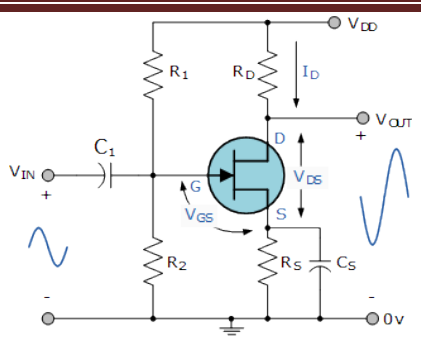
This type of bipolar transistor configuration has greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal is 180$^o$ "out-of-phase" with the input voltage signal.

Now consider the npn transistor with the input signal applied between its base and emitter terminals, while the output being collected across the load resistor RC, connected across the collector and the base terminals,




Make sure that the transistor is always operating in its active region by using appropriate voltage supplies, $V_{EE}$ and $V_{BC}$. Here a small change in the input voltage $V_{in}$ is seen to change the emitter current $I_E$ appreciably as the resistance of the input circuit is low (due to the forward bias condition). This in turn changes the collector current almost in the same range due to the fact that the magnitude of the base current is quite less for the case under consideration. This large change in $I_C$ causes a large voltage drop across the load resistor $R_C$ which is nothing but the output voltage. Hence one gets the amplified version of the input voltage across the output terminals of the device which leads to the conclusion that the circuit acts like a voltage amplifier.

FET AMPLIFIER




The input signal, (Vin) of the common source JFET amplifier is applied between the Gate terminal and the zero volts rail, (0v). With a constant value of gate voltage Vg applied the JFET operates within its "Ohmic region" acting like a linear resistive device. The drain circuit contains the load resistor, Rd. The output voltage, Vout is developed across this load resistance.

The efficiency of the common source JFET amplifier can be improved by the addition of a resistor, Rs included in the source lead with the same drain current flowing through this resistor. Resistor, Rs is also used to set the JFET amplifiers "Q-point".

When the JFET is switched fully "ON" a voltage drop equal to Rs x Id is developed across this resistor raising the potential of the source terminal above 0v or ground level. This voltage drop across Rs due to the drain current provides the necessary reverse biasing condition across the gate resistor, R2 effectively generating negative feedback.

So in order to keep the gate-source junction reverse biased, the source voltage, Vs needs to be higher than the gate voltage, Vg. This source voltage is therefore given as:

$$Vs = I_D \times Rs = V_G - V_{GS}$$

Then the Drain current, Id is also equal to the Source current, Is as "No Current" enters the Gate terminal and this can be given as:

$$I_D = V_S / R_s = V_{DD}/RD+Rs$$

This potential divider biasing circuit improves the stability of the common source JFET amplifier circuit when being fed from a single DC supply compared to that of a fixed voltage biasing circuit. Both resistor, Rs and the source by-pass capacitor, Cs serve basically the same function as the emitter resistor and capacitor in the common emitter bipolar transistor amplifier circuit, namely to provide good stability and prevent a reduction in the loss of the voltage gain. However, the price paid for a stabilized quiescent gate voltage is that more of the supply voltage is dropped acrossRs.

**Miller Effect Capacitance**

The Miller effect was named after John Milton Miller. When Miller published his work in 1920, he was working on vacuum tube triodes, however the same theory applies to more modern devices such as bipolar and MOS transistors.

In electronics, the Miller effect accounts for an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals. Although Miller effect normally refers to capacitance, any impedance connected between the input and another node exhibiting high gain can modify the amplifier input impedance via the Miller effect.

This increase in input capacitance is given by

$$C_M = C(1 - A_v)$$

where $A_V$ is the gain of the amplifier and C is the feedback capacitance.

The Miller effect is a special case of Miller's theorem.

**Derivation**

Consider an ideal voltage amplifier of gain $A_V$ with an impedance Z connected between its input and output nodes. The output voltage is therefore $V_0 = A_V V_i$ and the input current is

$$I_i = \frac{V_i - V_o}{Z} = \frac{V_i(1 - A_v)}{Z}.$$

As this current flows through the impedance Z, this equation shows that because of the gain of the amplifier a huge current flows in Z; in effect Z behaves as though it were much smaller than it is. The input impedance of the circuit is

$$Z_{in} = \frac{V_i}{I_i} = \frac{V_i Z}{V_i(1 - A_v)} = \frac{Z}{1 - A_v}.$$

If Z represents a capacitor, then

$$Z = \frac{1}{j\omega C}$$

and the resulting input impedance is

$$Z_{in} = \frac{1}{j\omega C(1 - A_v)} = \frac{1}{j\omega C_M} \quad \text{where} \quad C_M = C(1 - A_v).$$

Thus the effective or Miller capacitance $C_M$ is the physical C multiplied by the factor $(1-A_V)$.

HYBRID PIE MODEL:

The low frequency small signal model of bipolar junction transistor holds for frequencies below 1 MHz. For frequencies greater than 1 MHz the response of the transistor will be limited by internal and parasitic capacitances of the bipolar junction transistor. Hence at high frequencies, the low frequency small signal model of transistor has to be modified to include the effects of internal and parasitic capacitance's of bipolar junction transistor. These capacitances limit the usage of BJT at higher frequencies. Thus in order to estimate the gain and switching on and off times of BJT at higher frequencies the high frequency model of BJT has to be used to get reasonably accurate estimates. The high frequency hybrid pi model is also called as Giacoletto model named after L.J.Giacoletto who introduced it in 1969.

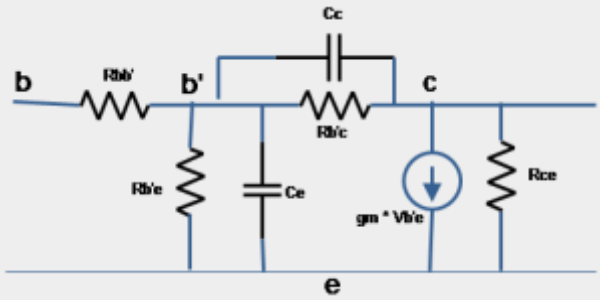
**High frequency effects on BJT**

- The gain decreases at high frequencies due to internal feedback capacitances. The highest frequency of operation of BJT will be limited by internal capacitance's of BJT.

- The on and off switching times of BJT will be high and speed will be limited due to internal charge storage effects.

**High frequency model of BJT**

The high frequency parameters of BJT may vary with operating point but the variation is negligible for small signal variations around the operating point. Following is the high frequency model of a transistor.




Where

B' = internal node in base

$R_{bb'}$ = Base spreading resistance

$R_{b'e}$ = Internal base node to emitter resistance

$R_{ce}$ = collector to emitter resistance

$C_e$ = Diffusion capacitance of emitter base junction

$R_{b'c}$ = Feedback resistance from internal base node to collector node

$g_m$ = Transconductance

$C_C$= transition or space charge capacitance of base collector junction.

**$R_{bb'}$** is the base spreading resistance of BJT which represents the bulk resistance of the material between the base terminal and the physical inaccessible internal node of BJT. Typically it is of the order of 100's of ohms.

**$R_{b'e}$** is the internal base node to emitter resistance. It accounts for the increase recombination base current as emitter current increases. It is in parallel with the collector circuit and hence reduces the collector current value from emitter current. This resistance will be high order of kilo

ohms as the decrease in the collector current due to base recombination currents will be very less.

**$R_{b'c}$** is the Feedback resistance from internal base node to collector node. It is included in the model to take in to account early effect.As collector to base reverse bias is increased(action) the effective width increases and collector current increases(feedback response).This feedback effect(early effect) is accounted for by $R_{b'c}$.

**$R_{ce}$** represents the bulk resistance of the material between collector to emitter.

**$C_e$** is the Diffusion capacitance of emitter base junction. Diffusion capacitance of emitter base junction is directly proportional to emitter bias current and forward base transit time. Forward transit time is defined as the average time the minority carrier spends in base. The Diffusion capacitance of emitter base junction accounts for the minority charge stored in base and is given as

$$C_e = \tau_F * I_E / V_T$$

where $I_E$ is emitter bias current

$V_T$ is voltage equivalent of temperature = k*T/e =26 mV at 27 Deg C

$\tau_F$ is forward base transit time given as $\tau_F = W^2/(2*D_B)$

W is effective base width

**$D_B$** is diffusion constant for minority carriers in base holes in PNP transistor and electrons in NPN transistor.

**$C_e$** is a function of temperature as $D_B = V_T*\mu$ ($\mu$ varies as $T^{-m}$) is a function of temperature. $C_e$ can be found theoretically from unit gain frequency and Transconductance as follows

$$C_e = g_m/(2*pi*f_T)$$

Unity gain frequency is defined as frequency at which the current gain of transistor reduces to unity. The 3 db higher cutoff frequency of BJT is termed as beta frequency of BJT denoted by $f_\beta$. The beta frequency and Unity gain frequency are related as

$$f_T = h_{fe} * f_\beta$$

where $h_{fe}$ is current gain of BJT in CE configuration.

$C_C$ represents the transition or space charge capacitance of base collector junction.The transition capacitance of base collector junction is given as

$$C_j = C_o/(1+V_{CB}/V_{BV})^n$$

where $C_o$ is the transition capacitance for zero collector to base bias

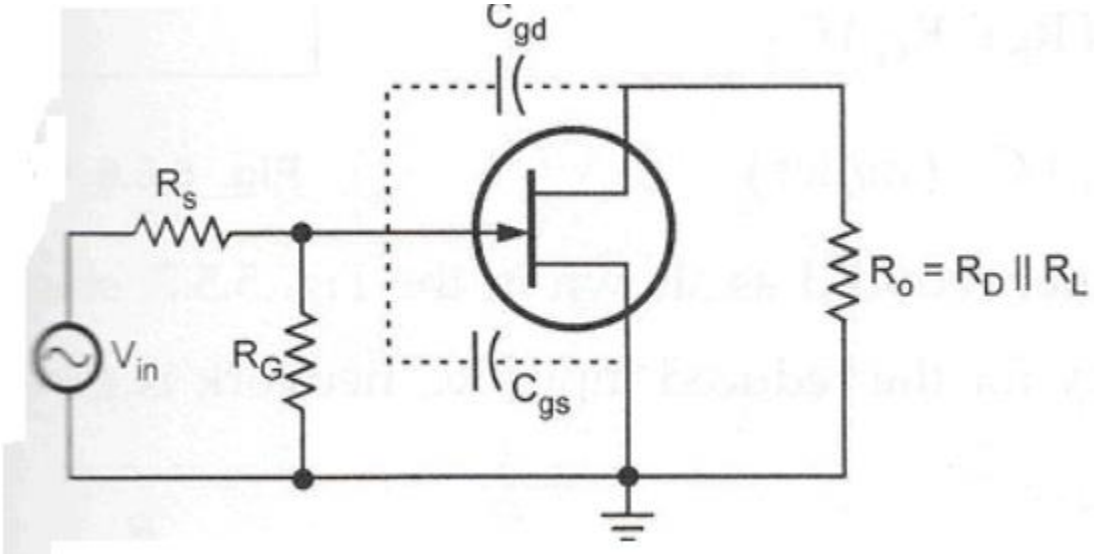
$V_{CB}$ is collector to base bias

$V_{BV}$ is the built in voltage across base collector junction

n is a constant called as grading coefficient varies form o.25 to 0.5.

The high frequency hybrid Pi or Giacoletto model of BJT is valid for frequencies less than the unit gain frequency.

**High Frequency Response Of Fet Amplifiers**



From above figure, it shows the high frequency equivalent circuit for the given amplifier circuit. It shows that at high frequencies coupling and bypass capacitors act as short circuits and do not affect the amplifier high frequency response. The equivalent circuit shows internal capacitances which affect the high frequency response.

Using Miller theorem, this high frequency equivalent circuit can be further simplified as follows:

The internal capacitance $C_{gd}$ can be splitted into $C_{in(miller)}$ and $C_{out(miller)}$ as shown in the following figure.

$$C_{in\,(miller)} = C_{gd}\,(A_v + 1)$$

$$C_{out\,(miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

Where

$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

There is a measurable amount of capacitance between each terminal pair of the FET. These capacitances each have a reactance that decreases as frequency increases. As the reactance of a given terminal capacitance decreases, more and more of the signal at the terminal is bypassed through the capacitance.

The high cutoff frequencies for the gate and drain circuits are then given by

$$f_{HG} = \frac{1}{2\pi R'_{in} C'_G} \qquad \text{and} \qquad f_{HD} = \frac{1}{2\pi R'_L C'_D}$$

where $R'_{in} = R_G \parallel R_{in}$ and $R'_L = R_D \parallel R_L$. At very high frequencies, the effect of $C'_G$ is to reduce the total impedance of the parallel combination of $R_1, R_2$ and $C'_G$ in Figure 3(b). The result is a reduced level of voltage across the gate-source terminals. Similarly, for the drain circuit, the capacitive reactance of $C'_D$ will decrease with frequency and consequently reduces the total impedance of the output parallel branches of Figure 3(b). It causes the output voltage to decrease as the reactance becomes smaller.

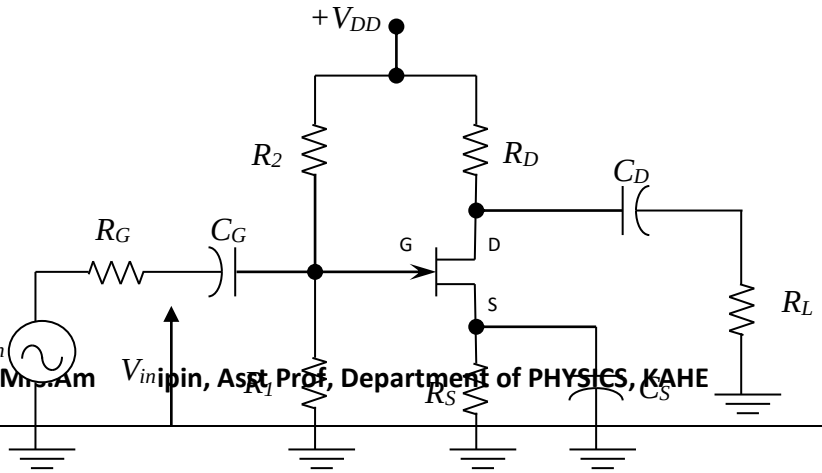
**Low Frequency Response of FET Amplifier**

In the low frequency region of a single stage FET amplifier as shown in Figure. It is the RC combinations formed by the network capacitors and the network resistive parameters that determine the cutoff frequency. There are three capacitors – two coupling capacitor $C_G$ and $C_D$, and one bypass capacitor, $C_S$. Let us assume that $C_G$, $C_D$ and $C_S$ are arbitrarily large and can be represented by short-circuit. The total resistance in series with $C_G$ is given by

$$R_{CG} = R_G + R_{in}$$

where $R_{in} = R_1 \parallel R_2$ is the input impedance of the amplifier circuit. The power supplied by the signal generator is $P_{in} = V_{gen}^2 / (R_G + R_{in})$. However, the reactance $X_{CG}$ of capacitance $C_G$ is not negligible at very low frequencies. The frequency at which $P_{in}$ is cut in half is when $X_{CG} = R_G + R_{in}$. Thus the lower half-power point for gate circuit occurs at frequency

$$f_{LG} = \frac{1}{2\pi R_{CG} C_G} = \frac{1}{2\pi (R_G + R_{in}) C_G}$$

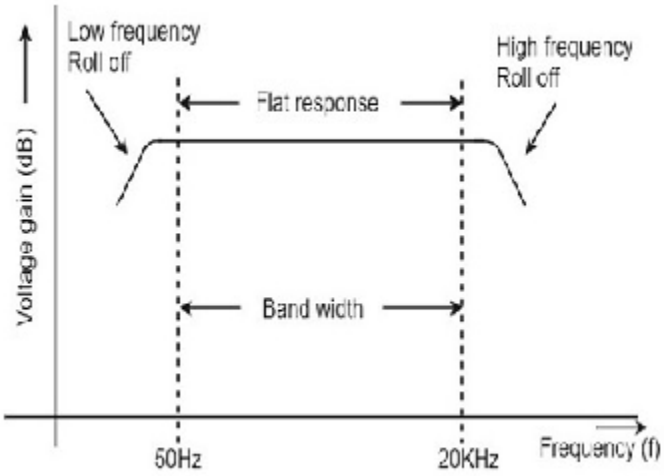


When $C_G$ and $C_S$ are arbitrarily large and can be represented by short-circuit, the drain circuit of the JFET amplifier is as shown in Figure 2(c). At high frequency where $C_D$ can also be represented by a short-circuit, the output power to load resistor $R_L$ is $P_{out} = V_D^2 / R_L$. At low frequencies where the reactance $X_{CD}$ of capacitance $C_D$ is not negligible, $P_{out}$ is cut in half when $X_{CD} = R_L$. Thus the lower half-power point for drain circuit occurs at frequency

$$f_{LD} = \frac{1}{2\pi R_L C_D}$$

At the half-power point, the output voltage reduces to 0.707 times its midband value. The actual lower cutoff frequency is the higher value between $f_{LG}$ (determined by $C_G$) and $f_{LD}$ (determined by $C_D$).

**Frequency Response Of Multistage Amplifiers**




The voltage gain of an amplifier varies with signal frequency. It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage.

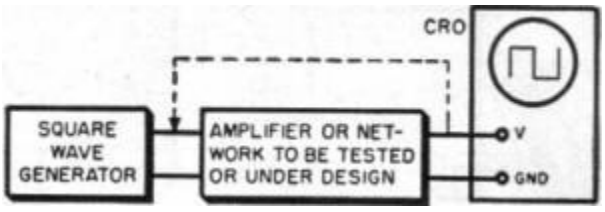
The curve between voltage gain and signal frequency of an amplifier is known as frequency response. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at f r , called resonant frequency. If the frequency of signal increases beyond f r , the gain decreases. The performance of an amplifier depends to a considerable extent upon its frequency response. While designing an amplifier, appropriate steps must be taken to ensure that gain is essentially uniform over some specified frequency range. For instance, in case of an audio amplifier, which is used to amplify speech or music, it is necessary that all the frequencies in the sound spectrum (i.e. 20 Hz to 20 kHz) should be uniformly amplified otherwise speaker will give a distorted sound output.

Although the gain of an amplifier can be expressed as a number, yet it is of great practical importance to assign it a unit. The unit assigned is bel or decibel (db). The common logarithm (log to the base 10) of power gain is known as bel power gain i.e.

Power gain = log 10 P out/P in

**Square Wave Testing**

Square waves are rich in odd numbered harmonics and have a very simple shape that makes it easy to observe frequency response limitations in amplifiers. Amplifiers generally have AC coupled sections that limit the low frequency response and have shunt capacitances either parasitic or intentional that limit high frequency response.




**Set-Up for Square Wave Testing**

Square-wave signal is applied to the input of an electrical circuit, whether a filter network, amplifier, or other system, and the system does not respond equally well to the fundamental and all higher harmonics, then the output signal obtained will be distorted in a fashion indicative of the response characteristics of the system under test. This is the basis of the square-wave test

technique. Square-wave testing provides an extremely rapid method for checking such network characteristics as frequency response, phase shift, transient response, etc. Because of the speed with which the square-wave test technique can be applied and information obtained, this method becomes quite valuable not only as an aid in the production testing and servicing of electronic equipment, but can be applied with equal, if not greater, value to the requirements of the practical design engineer.

## POSSIBLE QUESTIONS

### PART-B( 2 Marks)

1. What is the significance of square wave testing?
2. Explain miller effect capacitance.
3. Define cut off frequency.
4. Define current gain.
5. Define bandwidth.
6. What are the advantages of hybrid pie model?
7. Define short circuit current gain.
8. How to plot frequency response for an amplifier?
9. What is the application of square wave testing?
10. What is the significance of -3dB frequency?

## PART-C( 6 Marks)

1. Discuss the frequency response of an amplifier.
2. Discuss the effect of emitter bypass capacitor on low frequency response of BJT amplifiers.
3. What specific capacitance has the greatest effect on the high frequency response of a cascade of FET amplifiers? Explain.
4. Discuss the different methods of coupling of amplifier stages and bring out the relative merits and demerits
5. Explain why current gain is not computed in FET amplifiers?
6. Explain why the frequency response of amplifiers is plotted on a semilog scale?
7. Explain the selection of configuration for multistage amplifier.
8. Discuss high frequency response of multistage amplifiers
9. Explain the principle of hybrid pie model
10. Explain the miller effect capacitance

**KARPAGAM ACADEMY OF HIGHER EDUCATION**
**Coimbatore - 641021.**
**(For the candidates admitted from 2018onwards)**
**DEPARTMENT OF PHYSICS**
**UNIT II :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| QUESTIONS | CHOICE1 | CHOICE2 | CHOICE3 | CHOICE4 | ANSWER |
|---|---|---|---|---|---|
| **UNIT-II** | | | | | |
| A coupling capacitor is | A dc short | An ac open | A dc open and an ac short | A dc short and an ac open | A dc open and an ac short |
| In a bypass circuit, the top of a capacitor is | An open | A short | An ac ground | A mechanical ground | An ac ground |
| The capacitor that produces an ac ground is called a | Bypass capacitor | Coupling capacitor | DC open | AC open | Bypass capacitor |
| The output voltage of a CE amplifier is | Amplified | Inverted | 180° out of phase with the input | All of the above | All of the above |
| A common-gate amplifier is similar in configuration to which BJT amplifier? | common-emitter | common-collector | common-base | emitter-follower | common-base |
| A common-source amplifier is similar in configuration to which BJT amplifier? | common-base | common-collector | common-emitter | emitter-follower | common-emitter |
| An emitter-follower is also known as a | common-emitter amplifier | common-base amplifier | common-collector amplifier | Darlington pair | common-collector amplifier |
| When transistors are used in digital circuits they usually operate in the | active region | breakdown region | saturation and cutoff regions | linear region | saturation and cutoff regions |
| Which of the following elements are important in determining the gain of the system in the high-frequency region? | Interelectrode capacitances | Wiring capacitances | Miller effect capacitance | All of the above | All of the above |
| For audio systems, the reference level is generally accepted as _____. | 1 mW | 1 W | 10 mW | 100 mW | 1 mW |

| | | | | | |
|---|---|---|---|---|---|
| What is the normalized gain expressed in dB for the cutoff frequencies? | –3 dB | +3 dB | –6 dB | –20 dB | –3 dB |
| Which of the following configurations does not involve the Miller effect capacitance? | Common-emitter | Common-base | Common-collector | All of the above | Common-base |
| When transistors are used in digital circuits they usually operate in the | Active region | Saturation and cutoff regions | Breakdown region | Linear region | Saturation and cutoff regions |
| A current ratio of IC/IE is usually less than one and is called | Omega | Beta | Theta | Alpha | Alpha |
| A transistor may be used as a switching device or as a: | Tuning device | Rectifier | Fixed resistor | Variable resistor | Variable resistor |
| Most of the electrons in the base of an NPN transistor flow: | Into the collector | Into the emitter | Out of the base lead | Into the base supply | Into the collector |
| The BJT is a _____ device. The FET is a _____ device. | Bipolar, bipolar | Bipolar, unipolar | Unipolar, bipolar | Unipolar, unipolar | Bipolar, unipolar |
| The Bode plot is applicable to | All phase network | Minimum phase network | Maximum phase network | Lag lead network | Minimum phase network |
| For any inverting amplifier, the impedance capacitance will be _____ by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance. | Unaffected | Increased | Decreased | None of the above | Decreased |
| Which of the following configurations does not involve the Miller effect capacitance? | Common-emitter | Common-base | Common-collector | All of the above | Common-base |
| For the common-emitter amplifier ac equivalent circuit, all capacitors are | effectively shorts. | effectively open circuits. | not connected to ground. | connected to ground. | effectively shorts |
| For a common-emitter amplifier, the purpose of the emitter bypass capacitor is | no purpose, since it is shorted out by $R_E$. | to reduce noise. | to despike the supply voltage. | to maximize amplifier gain. | to maximize amplifier gain |
| For a common-emitter amplifier, the purpose of swamping is | to minimize gain. | to reduce the effects of $r'_e$ | to maximize gain. | no purpose. | to reduce the effects of $r'_e$ |

| | | | | | |
|---|---|---|---|---|---|
| An emitter-follower is also known as a | common-emitter amplifier. | common-base amplifier. | common-collector amplifier. | Darlington pair. | common-collector amplifier |
| In a common-base amplifier, the input signal is connected to the | base. | collector. | emitter. | output. | emitter |
| The differential amplifier produces outputs that are | common mode. | in-phase with the input voltages. | the sum of the two input voltages. | the difference of the two input voltages. | the difference of the two input voltages |
| The differential amplifier has | one input and one output. | two inputs and two outputs. | two inputs and one output. | one input and two outputs. | two inputs and two outputs |
| The dc emitter current of a transistor is 8 mA. What is the value of $r_e$? | 320 Ω | 13.3 kΩ | 3.125 Ω | 5.75 Ω | 3.125 Ω |
| An emitter-follower amplifier has an input impedance of 107 kΩ. The input signal is 12 mV. The approximate output voltage is (common-collector) | 8.92 V | 112 mV | 12 mV | 8.9 mV | 12 mV |
| A Darlington pair amplifier has | high input impedance and high voltage gain. | low input impedance and low voltage gain. | a voltage gain of about 1 and a low input impedance. | a low voltage gain and a high input impedance. | a low voltage gain and a high input impedance |
| You have a need to apply an amplifier with a very high power gain. Which of the following would you choose? | common-collector | common-base | common-emitter | emitter-follower | common-emitter |
| What is the most important r parameter for amplifier analysis? | $r_b'$ | $r_c'$ | $r_e'$ | none of the above | $r_e'$ |
| A common-emitter amplifier has _____ voltage gain, _____ current gain, _____ power gain, and _____ input impedance. | high, low, high, low | high, high, high, low | high, high, high, high | low, low, low, high | high, high, high, low |

| | | | | | |
|---|---|---|---|---|---|
| To analyze the common-emitter amplifier, what must be done to determine the dc equivalent circuit? | leave circuit unchanged | replace coupling and bypass capacitors with opens | replace coupling and bypass capacitors with shorts | replace $V_{CC}$ with ground | replace coupling and bypass capacitors with opens |
| When the bypass capacitor is removed from a common-emitter amplifier, the voltage gain | increases. | decreases. | has very little effect. | | decreases |
| A common-collector amplifier has _____ input resistance, _____ current gain, and _____ voltage gain. | high, high, low | high, low, low | high, low, high | | high, high, low |
| A Darlington pair provides beta _____ for _____ input resistance. | multiplication, decreased | multiplication, increased | division, decreased | | multiplication, increased |
| The total gain of a multistage amplifier is the _____. | sum of individual voltage gains | sum of dB voltage gains | none of the above | | sum of dB voltage gains |
| What is $r_e$ equal to in terms of *h* parameters? | $h_{re} / h_{oe}$ | $(h_{re} + 1) / h_{oe}$ | $h_{ie} – (h_{re} / h_{oe})(1 + h_{fe})$ | $h_{fe}$ | $h_{re} / h_{oe}$ |
| The advantage that a Sziklai pair has over a Darlington pair is | higher current gain. | less input voltage is needed to turn it on. | higher input impedance. | higher voltage gain. | less input voltage is needed to turn it on. |
| What is the device in a transistor oscillator? | LC tank circuit | Biasing circuit | Transistor | Feedback circuit | Transistor |
| When the collector supply is 5V, then collector cut off voltage under dc condition is | 20 V | 10 V | 2.5 V | 5 V | 5 V |
| The common base (CB) amplifier has a _____ compared to CE and CC amplifier. | Lower input resistance | Larger current gain | Larger voltage gain | Higher input resistance | Lower input resistance |

| | | | | | |
|---|---|---|---|---|---|
| When a FET with a lower transconductance is substituted into a FET amplifier circuit, what happens? | The current gain does not change | The voltage gain decreases | The circuit disamplifies | The input resistance decreases | The voltage gain decreases |
| At zero signal condition, a transistor sees_____ load. | dc | ac | both dc and ac | resistive | dc |
| What is the gain of an amplifier with negative feedback if the feedback factor is 0.01? | 10 | 1,000 | 100 | 500 | 100 |
| The current gain of an emitter follower is | Equal to 1 | Greater than 1 | Less than 1 | Zero | Less than 1 |
| The current in any branch of a transistor amplifier that is operating is | ac only | the sum of ac and dc | the difference of ac and dc | dc only | the sum of ac and dc |
| An ideal differential amplifiers common mode rejection ratio is | Infinite | Zero | Unity | Undetermined | Infinite |
| An open fuse circuit has a resistance equal to | Zero | Unity | At least 100Ω at standard | Infinity | Infinity |
| What is the purpose of dc conditions in a transistor? | To reverse bias the emitter | To forward bias the emitter | To set up operating point | To turn on the transistor | To set up operating point |
| The ac variations at the output side of power supply circuits are called _____. | Ripples | Pulses | Waves | Filters | Ripples |
| What is the purpose of the emitter capacitor? | To forward bias the emitter | To reduce noise in the amplifier | To avoid drop in gain | To stabilize emitter voltage | To avoid drop in gain |
| A common emitter circuit is also called _____ circuit. | Grounded emitter | Grounded collector | Grounded base | Emitter follower | Grounded emitter |
| The output signal of a common-collector amplifier is always | Larger than the input signal | In phase with the input signal | Out of phase with the input signal | Exactly equal to the input signal | In phase with the input signal |
| Calculate the ripples of the filter output if a dc and ac voltmeter is used and measures the output signal from a filter circuit of 25 VDC and 1.5 $V_{rms}$ | 5% | 10% | 50% | 6% | 6% |
| What is the ideal maximum voltage gain of a common collector amplifier? | Unity | Infinite | Indeterminate | Zero | Unity |

| | | | | | |
|---|---|---|---|---|---|
| The output power of a transistor amplifier is more than the input power due to additional power supplied by | Transistor | Collector supply | Emitter supply | Base supply | Collector supply |
| When a transistor amplifier feeds a load of low resistance, its voltage gain will be | Low | Very high | High | Moderate | Low |
| The capacitors are considered _____ in the ac equivalent circuit of a transistor amplifier. | Open | Partially open | Short | Partially short | Short |
| For highest power gain, what configuration is used? | CC | CB | CE | CS | CE |
| What is the most important characteristic of a common collector amplifier? | High input voltage | High input resistance | High output resistance | Its being an amplifier circuit | High input resistance |
| Which of the item below does not describe a common emitter amplifier? | High voltage gain | High current gain | Very high power gain | High input resistance | High input resistance |
| CC configuration is used for impedance matching because its | Input impedance is very high | Input impedance is very low | Output impedance is very low | Output impedance is zero | Input impedance is very high |
| Which of the following is the other name of the output stage in an amplifier? | Load stage | Audio stage | Power stage | RF stage | Power stage |
| When amplifiers are cascaded | The gain of each amplifier is increased | A lower supply voltage is required | The overall gain is increased | Each amplifier has to work less | The overall gain is increased |
| Ina common emitter amplifier, the capacitor from emitter to ground is called the | Coupling capacitor | Bypass capacitor | Decoupling capacitor | Tuning capacitor | Bypass capacitor |
| A class A power amplifier uses _____ transistor(s). | Two | One | Three | Four | One |
| What is the maximum collector efficiency of a resistance loaded class A power amplifier? | 50% | 78.50% | 25% | 30% | 25% |
| What is the maximum collector efficiency of a transformer coupled class A power amplifier? | 30% | 80% | 45% | 50% | 50% |

| | | | | | |
|---|---|---|---|---|---|
| Class C amplifiers are used as | AF amplifiers | Small signal amplifiers | RF amplifiers | IF amplifiers | RF amplifiers |
| Find the voltage drop developed across a D' Arsonval meter movement having an internal resistance of 1 kΩ and a full deflection current of 150uA. | 150 μV | 150 mV | 150 V | 200 mV | 150 mV |
| If the capacitor from emitter to ground in a common emitter amplifier is removed, the voltage gain | Increases | Decreases | Becomes erratic | Remains the same | Decreases |
| Comparatively, power amplifier has _____ β. | Large | Very large | Small | Very small | Small |
| The driver stage usually employs _____ amplifier. | Class A power | Class C | Push-pull | Class AB | Class A power |
| The push-pull circuit must use _____ operation. | Class A | Class B | Class C | Class AB | Class B |
| A complementary-symmetry amplifier has | One PNP and one NPN transistor | Two PNP transistors | Two NPN transistors | Two PNP and two NPN transistors | One PNP and one NPN transistor |
| Power amplifiers generally use transformer coupling because transformer coupling provides | Cooling of the circuit | Distortionless output | Impedance matching | Good frequency response | Impedance matching |
| The output transformer used in a power amplifier is a/an _____ transformer | 1:1 ratio | Step-down | Step-up | Isolation | Step-down |
| | | | | | |
| **Prepared By-Ambili Vipin,Assistant Professor,Department of Physics** | | | | | |
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**DEPARTMENT OF PHYSICS UNIT I :(Objective Type/Multiple choice Questions each Question carries one Mark ) UNIT II :(**

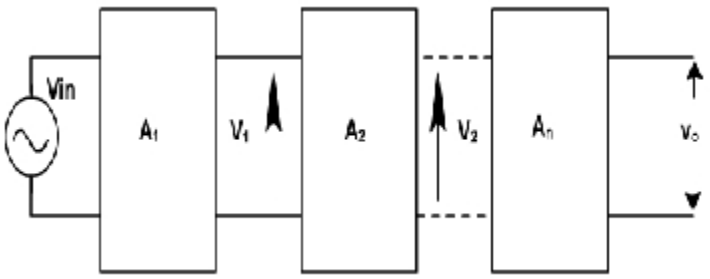
# UNIT-III

## SYLLABUS

**Analog Circuits**: Analysis of compound configurations Cascade connection; Cascade connection; Darlington connection; Bootstrapping principle; Bootstrapped Emitter Follower; Bootstrapped Darlington Emitter Follower; Feedback pair; . CMOS circuits; Current source circuits; Current mirror circuits; Differential amplifier circuits; Numerical problems.

## MULTIPLE AMPLIFIER - Analysis of compound configurations

To increases the voltage gain of the amplifier, multiple amplifier are connects in cascade. The output of one amplifier is the input to another stage. In this way the overall voltage gain can be increased, when number of amplifier stages are used in succession it is called a multistage amplifier or cascade amplifier. The load on the first amplifier is the input resistance of the second amplifier. The various stages need not have the same voltage and current gain. In practice, the earlier stages are often voltage amplifiers and the last one or two stages are current amplifiers. The voltage amplifier stages assure that the current stages have the proper input swing. The amount of gain in a stage is determined by the load on the amplifier stage, which is governed by the input resistance to the next stage. Therefore, in designing or analyzing multistage amplifier, we start at the output and proceed toward the input.




The overall voltage gain of cascade amplifier is the product of the voltage gain of each stage. That is, the overall voltage gain is A1 A2A3.

To represent the gain of the cascade amplifier, the voltage gains are represents in dB. The two power levels of input and output of an amplifier are compared on a logarithmic scale rather than linear scale. The number of bels by which the output power $P_2$ exceeds the input power $P_1$ is defined as

$$\text{No of bels} = \log_{10}\left(\frac{P_2}{P_1}\right)$$

$$\text{or No of dB} = 10 * \text{No. of bels}$$

$$= 10 \log_{10}\left(\frac{P_2}{P_1}\right)$$

Since,

$$P_1 = \frac{v_1^2}{R_{in}} \;\&\; P_2 = \frac{v_2^2}{R_0}$$

where $R_{in}$ is the input resistance of the amplifier and $R_0$ is the load resistance

$$dB = 10 \log_{10}\left(\frac{v_2^2 / R_0}{v_1^2 / R_{in}}\right)$$

In case $R_{in}$ and $R_0$ are equal, then power gain is given by

$$dB = 10 \log_{10}\left(\frac{v_2}{v_1}\right)^2 = 20 \log_{10}\left(\frac{v_2}{v_1}\right)$$

$$\therefore A_{dB} = A_{dB1} + A_{dB2} + \ldots\ldots$$

Because of dB scale the gain can be directly added when a number of stages are cascaded.

**Coupling:**

In a multistage amplifier the output of one stage makes the input of the next stage. Normally a network is used between two stages so that a minimum loss of voltage occurs when the signal passes through this network to the next stage. Also the dc voltage at the output of one stage should not be permitted to go to the input of the next. Otherwise, the biasing of the next stage are disturbed.

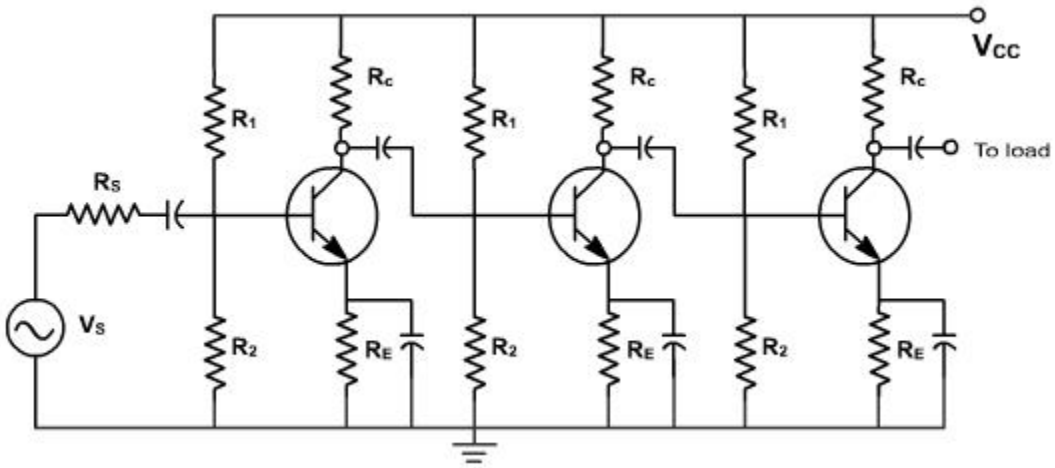
The three couplings generally used are.

1. RC coupling
2. Impedance coupling
3. Transformer coupling.

**RC coupling**

RC coupling the most commonly used method of coupling from one stage to the next. An ac source with a source resistance Rs drives the input of an amplifier. The grounded emitter stage amplifies the signal, which is then coupled to next CE stage the signal is further amplified to get larger output.

In this case the signal developed across the collector resistor of each stage is coupled into the base of the next stage. The cascaded stages amplify the signal and the overall gain equals the product of the individual gains.




The coupling capacitors pass ac but block dc. Because of this, the stages are isolated as for as dc is concerned. This is necessary to avoid shifting of Q-points. The drawback of this approach is the lower frequency limit imposed by the coupling capacitor.

The bypass capacitors are needed because they bypass the emitters to ground. Without them, the voltage gain of each stage would be lost. These bypass capacitors also place a lower limit on the frequency response. As the frequency keeps decreasing, a point is reached at which capacitors no longer look like a.c. shorts. At this frequency the voltage gain starts to decrease because of the local feedback and the overall gain of the amplifier drops significantly. These amplifiers are suitable for frequencies above 10 Hz.

**Darlington Pair**

The Darlington Pair is a useful circuit configuration for many applications within electronic circuits. This circuit configuration provides a number of advantages that other forms of transistor circuit are not able to offer and as a result it is used in many areas of electronics design.The Darlington Pair also occasionally referred to as a super-alpha pair is renowned as a method for obtaining a very high level of current gain, using just two transistors. It is able to provide levels of gain that are not possible using single transistors on their own, but it may not be used in all circumstances because it does have a number of limitations.

The circuit may be used in the form of discrete components, but there are also very many integrated circuit versions often termed a Darlington transistor that may also be used. These Darlington transistor components may be obtained in a variety of forms including those for high power applications where current levels of many amps may be required.The Darlington Pair has been in use for very many years. It was invented in 1953 by Sidney Darlington who was working at Bell Laboratories. He developed the idea of having two or three transistors in a single semiconductor chip, where the emitter of one transistor was connected directly to the base of the next, and all the transistors shared the same collector connection.

**Basics**

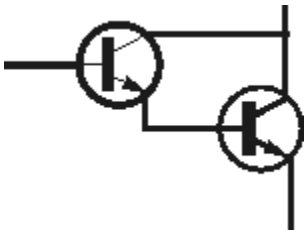
When using an emitter follower in a circuit, the level of current gain, and the input impedance of the circuit is limited by the current gain that can be achieved using a single transistor. The gain of the Darlington transistor pair is that gain of the two individual transistors multiplied together.

$$\beta = \beta1+\beta2+\beta3$$

In view of the fact that the terms β1and β2 on their own can be neglected, we obtain the more familiar equation.

$$\beta=\beta1.\beta2$$

The basic circuit is formed by taking the emitter of the input transistor and connecting it such that its emitter drives the base of the second and then connecting both collectors together. This circuit can be used as any single transistor would be in a variety of circuits, but particularly as an emitter follower.



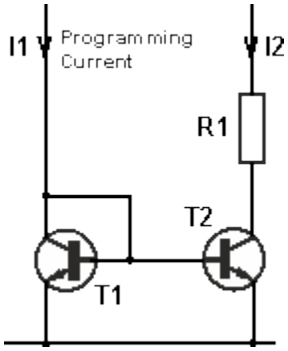
## CURRENT MIRROR

Current mirror circuits are widely used, especially within integrated circuit technology.The mirror circuit generally consists of two transistors, although other devices such

as FETs can be used, and some configurations do use more than two devices in the overall circuit to obtain better performance.The current mirror circuit gains its name because it copies or mirrors the current flowing in one active device in another, keeping the output current constant regardless of loading.

The current being mirrored can be a constant current, or it can be a varying signal dependent upon the requirement and hence the circuit.Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.

The basic circuit is shown in the diagram below. It comprises two transistors, one of which has the base and collector connected together. The base connections of both transistors are then linked, as are the emitters.




**Current Mirror Transistor Circuit**

In terms of the operation of the circuit, the base emitter junction of T1 acts like a diode because the collector and base are connected together.

The current into TI is set externally by other components, and as a result there is a given voltage built up across the base emitter junction of T1. As the base emitter voltage on both transistors is the same, the current in one transistor will exactly mirror that of the second, assuming that both transistors are accurately matched. Therefore the current flowing into T1 will be mirrored into T2 and hence into the load R1.

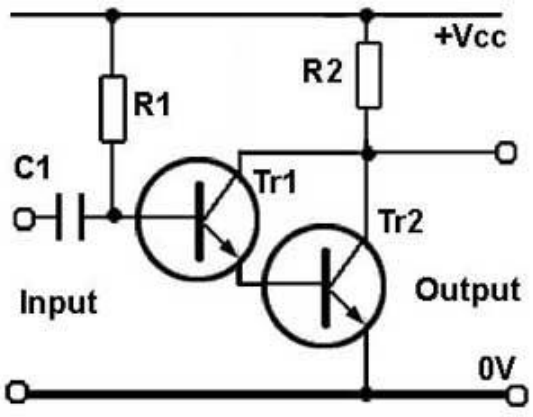
Circuit limitations

The circuit shown above is often quite adequate for most applications. However the circuit has some noticeable limitations under many circumstances:

- ***Current matching dependent on transistor matching:*** The current mirroring is dependent upon the matching of the transistors. Often the transistors need to be on the same substrate if they are to accurately mirror the current.
- ***Current varies with change in output voltage:*** This effect occurs because the output impedance is not infinite. This is because there is a slight variation of Vbe with the collector voltage at a given current in T2. Often the current may vary by about 25% the output compliance range.

**The Darlington Pair using Common Emitter Amplifiers**

The Darlington pair can also be used in common emitter mode, as shown in Fig.



Darlington transistors are also available as combined packages in both PNP and NPN types, complete with back emf protection diodes typically required when the Darlington configuration is used as a high current gain output device for switching high current inductive loads.

Darlington amplifiers are also available in integrated circuit form, such as theULN2803, which contains eight high current, Darlington amplifiers with open collector outputs, for interfacing between TTL (5V) logic circuits and high current/high voltage (up to 500mA and 50V) devices. When pin 10 is connected to +V each output is diode protected for driving inductive loads against back e.m.f.

**Bootstrapping**

*Bootstrapping* is a technique used in the design of transistor amplifier circuits to increase the input impedance and thereby reduce the loading effects on the input source. It typically involves the use of a *bootstrap capacitor*, which provides *positive feedback of* ac signals to the base junction of a transistor in an emitter follower circuit. Application of this feedback increases the effective value of the base resistance. The amount of increase is a factor determined by the voltage gain of the circuit.

Bootstrapping (Using positive feedback to feed part of the output back to the input, but without causing oscillation) is a method of apparently increasing the value of a fixed resistor as it appears to A.C. signals, and thereby increasing input impedance. A basic bootstrap amplifier is shown in Fig.where capacitor $C_B$ is the 'Bootstrap Capacitor', which provides A.C. feedback to a resistor in series with the base. The value of $C_B$ will be large, about 10 x the lowest frequency handled x the value of the series resistor ($10 f_{min} R3$).

Although positive feedback is being used, which would normally cause an amplifier to oscillate, the voltage gain of the emitter follower is less than 1, which prevents oscillation.

The base of the emitter follower is biased from a potential divider via R3. By feeding the output waveform back to the left hand side of R3 the voltage at this end of R3 is made to rise and fall in phase with the input signal at the base end of R3.

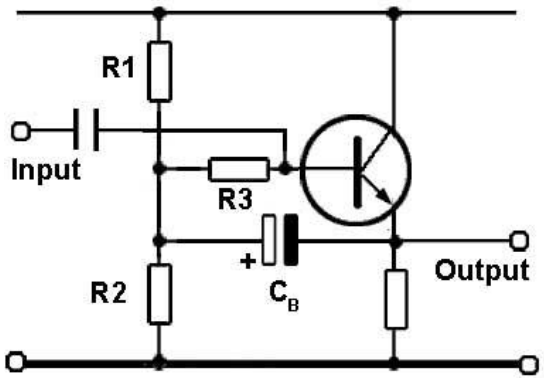
Because the output waveform of the emitter follower is a slightly less amplitude than the base waveform (due to the less than 1 gain of the transistor) there will be a very small signal current waveform across R3. Such a small current waveform suggests a very small current is flowing; therefore the resistance of R3 must be very high, much higher than in fact it is. The input impedance of the amplifier has therefore been increased.

The effective A.C. value of R3 is increased by R3 ÷ (1 $-A_o$) where $A_o$ is the open loop gain of the amplifier.

For example a 47KΩ resistor with bootstrapping would appear to be:

$$\text{The bootstrap value of R3, } = R3_B = \frac{R3}{(1 - A_o)}$$

The main drawback of this method of increasing input impedance compared with other methods is that the use of positive feedback is likely to increase noise and distortion.




**Bootstrapping applied to an Emitter Follower**

CMOS

Modern digital circuits (logic gates, memories, processors and other composite circuits) are currently being implemented with a complementary metal-oxide semiconductor (CMOS) technology (> 75% of all digital circuits). This technology combines complementary p-type (pMOS) and n-type (nMOS) metal-oxide semiconductor field effect transistors (MOSFETs) for the construction of various logic circuits.

CMOS technology was developed later than that of bipolar transistors. In the early years of its commercial application (1970s) it was an alternative to low power systems due to the particularly low energy consumption of logic circuits with bipolar transistors. On the other hand, the main disadvantage of CMOS circuits was their slow operation.

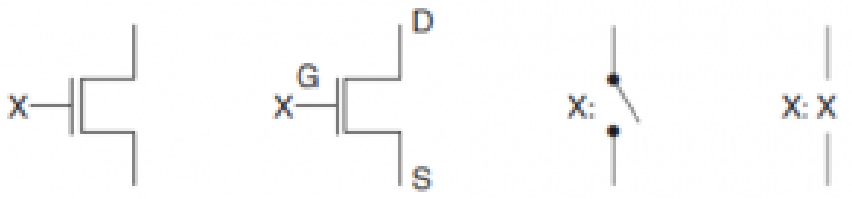
In the next decades ('80 -'90), both CMOS technology and bipolar technology followed the manufacturing tendency to shrink transistor dimensions and increase operating speeds. Bipolar technology has remained faster, but has not achieved a significant reduction in power consumption. CMOS technology, however, was ideal for logic circuits of great integration and low power consumption.

In the early 1990s, the construction dimensions of the integrated circuits reached 0.5µm. This allowed the construction of very large CMOS circuits, the performance of which at system level exceeded the individual efficiency of the bipolar transistors. Since then, CMOS technology has been dominant in the field of digital circuits.

CMOS (complementary metal-oxide-semiconductor) technology is used predominantly to create digital circuitry. The fundamental building blocks of CMOS circuits are P-type and N-type MOSFET transistors. A P-type MOSFET can be modeled as a switch that is closed when the input voltage is low (0 V) and open when the input voltage is high (5 V). A N-type MOSFET can be modeled as a switch that is closed when the input voltage is high (5 V) and open when the input voltage is low (0 V). The basic idea for CMOS technology is to combine P-type and N-type MOSFETs such that there is never a conducting path from the supply voltage (5 V) to ground. As a consequence, CMOS circuits consume very little energy. CMOS technology

employs two types of transistor: n-channel and p-channel. The two differ in the characteristics of the semiconductor materials used in their implementation and in the mechanism governing the conduction of a current through them.

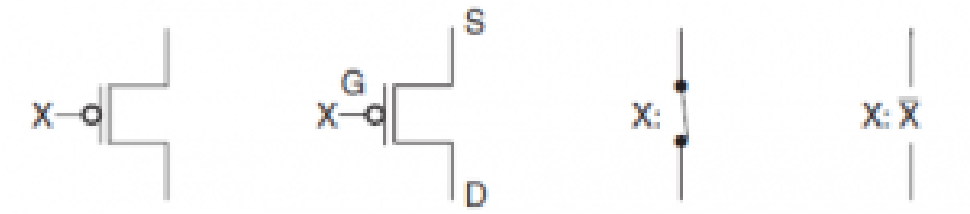
The transistor has three terminals: the gate (G), the source (S), and the drain (D). The voltage applied between G and S determines whether a path for current to flow exists between D and S. If a path exists, we say that the transistor is ON, and if a path does not exist, we say that the transistor is OFF. The n-channel transistor is ON if the applied gate-to-source voltage is H and OFF if the applied voltage is L. Here we will make the usual assumption that a 1 represents the H voltage range and a 0 represents the L voltage range. The notion of whether a path for current to flow exists is easily modeled by a switch. The switch consists of two fixed terminals corresponding to the S and D terminals of the transistor. In addition, there is a movable contact that, depending on its position, determines whether the switch is open or closed. The position of the contact is controlled by the voltage applied to the gate terminal G. Since we are looking at logic behavior, this control voltage is represented on the symbol by the input variable X on the gate terminal. For an n-channel transistor, the contact is open (no path exists) for the input variable X equal to 0 and closed (a path exists) for the input variable X equal to 1. Such a contact is traditionally referred to as being normally open, that is, open without a positive voltage applied to activate or close it.




The symbol for a p-channel transistor is shown in Figure bolow. The positions of the source S and drain D are seen to be interchanged relative to their positions in the n-channel transistor. The voltage applied between the gate G and the source S determines whether a path exists between the drain and source. The negation indicator

or bubble appears as a part of the symbol. This is because, in contrast to the behavior of an n-channel transistor, a path exists between S and D in the p-channel transistor for input variable X equal to 0 (at value L) and does not exist for input variable X equal to 1 (at value H).

This behavior is represented by the model which has a normally closed contact through which a path exists for X equal to 0. No path exists through the contact for X equal to 1.




The popular CMOS family include,

4000A,

4000B,

4000UB,

54/74C,

54/74HC,

54/74HCT,

54/74AC

54/74ACT

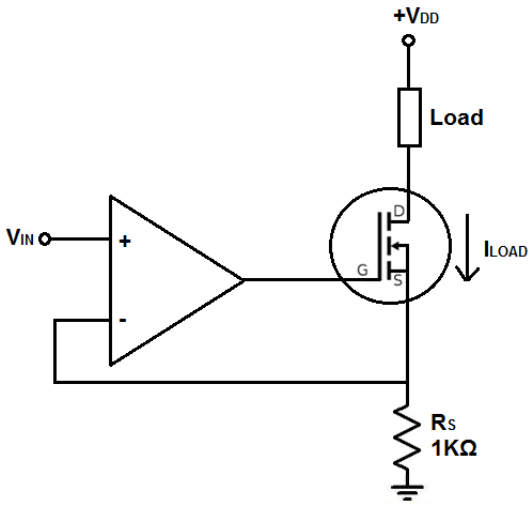
The 4000A CMOS family has been replaced by its high-voltage versions in the 4000B and 4000UB CMOS families, with the former having buffered and the latter having unbuffered outputs. 54/74C, 54/74HC, 54/74HCT, 54/74AC and 54/74ACT are CMOS logic

families with pin-compatible 54/74 TTL series logic functions.

CURRENT SOURCE CIRCUIT

A current source circuit is a circuit which can output a stable, steady current, without fluctuating much. For example, we may want a steady source of 10mA, in that case we need a current source of 10mA.

There are many reasons to want a steady flow of current. It may be for accuracy where a different current may cause some loss of precision. It may be component protection, in which too little current and the circuit doesn't work or too much current and circuit components are damaged.




The inverting input of the op amp samples the voltage across resistor Rs and then compares it with the voltage applied to the noinverting input.

This op amp circuit is basically wired to function as a voltage follower. A voltage follower is a circuit in which the output voltage is the same as the input voltage. It's called a voltage follower because the output voltage follows, or mimics, the input voltage.

When the noninverting terminal receives an input voltage and the inverting terminal is connected to the output of the op amp, this is the setup of a voltage follower. When the circuit is connected as a voltage follower, the output voltage resists changes unless the input voltage changes. So if the input voltage is steady at a certain value, the output voltage does everything possible to maintain the same voltage as the input. It strongly resists urges to voltage change. Therefore, if the load current going through the drain and source of the transistor changes, the voltage output by the op amp changes to adjust for this change in current, so that the output voltage (voltage across the resistor $R_S$) is constant, which ends up bringing the load current back to its baseline value. Since the output of the op amp is connected to the gate of the MOSFET, the voltage at the gate of the MOSFET changes if there are changes in the load current. If there is an increase in load current, the op amp outputs a higher voltage (remember this is a depletion-type MOSFET). This, in turn, lowers the current so that it goes back to its baseline value. If there is a decrease in load current, the op amp outputs a lower voltage. This, in turns, increases the current so that it goes back to its baseline value.

The chief formula for this circuit is, $I_{LOAD} = V_{IN}/R_S$

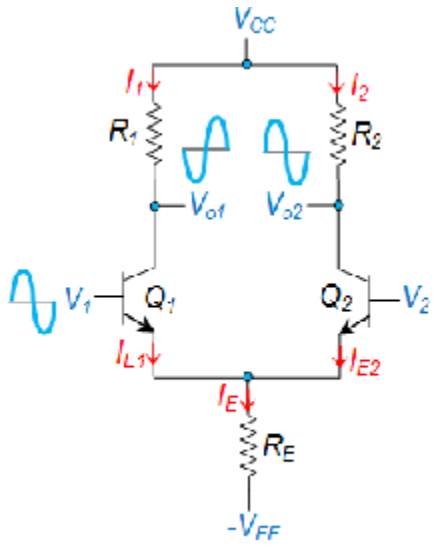
So whatever voltage you feed into the noninverting terminal of the op amp over the resistor $R_S$ determines the load current, $I_{LOAD}$

**Differential Amplifier** is a device which is used to amplify the difference between the voltages applied at its inputs. Such circuits can be of two types viz.,

1. Differential amplifiers built using transistors, either Bipolar Junction Transistors(BJTs) or Field Effect Transistors (FETs)
2. Differential amplifiers built using Op-Amps.

Figure 1 shows such a circuit made of two BJTs ($Q_1$ and $Q_2$) and two power supplies of opposite polarity viz., $V_{CC}$ and $-V_{EE}$ which uses three resistors among which two are the collector resistors, $R_{C1}$ and $R_{C2}$ (one for each transistor) while one is the emitter resistor $R_E$ common to both transistors. Here the input signals ($V_1$ and $V_2$)

are applied to the base of the transistors while the output is collected across their collector terminals ($V_{o1}$ and $V_{o2}$).




**A BJT Differential Amplifier**

In this case, if the $V_1$ at $Q_1$ is sinusoidal, then as $V_1$ goes on increasing, the transistor starts to conduct and this results in a heavy collector current $I_{C1}$increasing the voltage drop across $R_{C1}$, causing a decrease in $V_{o1}$. Due to the same effect, even $I_{E1}$ increases which increases the common emitter current, $I_E$resulting in an increase of voltage drop across $R_E$.

This means that the emitters of both transistors are driven towards positive which inturn implies that the base of $Q_2$ would start to become more and more negative. This results in a decrease of collector current, $I_{C2}$ which inturn decreases the voltage drop across the collector resistor $R_{C2}$, resulting in an increase in the output

voltage $V_{o2}$. This indicates that the changes in the sinusoidal signal observed at the input of transistor $Q_1$ is reflected as such across the collector terminal of $Q_2$ and appear with a phase difference of $180^o$ across the collector terminal of $Q_1$. The differential amplification can be driven by considering the output in-between the collector terminals of the transistors, $Q_1$ and $Q_2$.

On the other hand, an Op-Amp operating in differential mode can readily act as a **differential amplifier** as it results in an output voltage given by

$$V_0 = A_d(V_1 - V_2)$$

Where $V_1$ and $V_2$ represent the voltages applied at its inverting and non-inverting input terminals (can be taken in any order) and $A_d$ refers to its differential gain. As per this equation, the output of the OpAmp must be zero when the voltages applied at its terminals are equal to each other. However practically it will not be so as the gain will not be same for both of the inputs. Thus, in real scenario, the mathematical expression for the output of the differential amplifier can be given as

$$V_0 = A_d(V_1 - V_2) + A_C\left(\frac{V_1 + V_2}{2}\right)$$

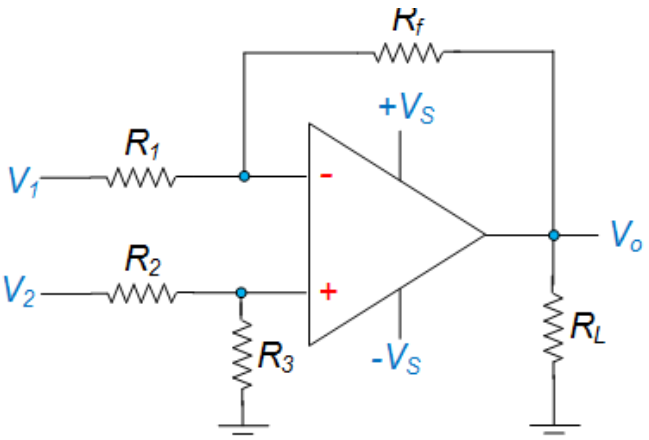
Where $A_C$ is called the common mode gain of the amplifier. Thus, functionally-good difference amplifiers are expected to exhibit a high common mode rejection ratio (CMRR) and high impedance.

However, it is to be noted that an Op-Amp can be suitably configured to result in a much practical **differential amplifier**, as shown by Figure 2. If closely observed, one can note that this circuit is just a combination of inverting and non-inverting amplifier. Hence its output voltage will be equal to the sum of the output voltages produced by the Op-Amp circuit operating as an inverting amplifier and the Op-Amp circuit operating as a non-inverting amplifier. Thus, one gets,

$$V_0 = -\frac{R_f}{R_1}V_1 + V_2\frac{R_f}{R_2+R_3}\left(1+\frac{R_f}{R_1}\right)$$

Now, if $R_1 = R_2$ and $R_3 = R_f$, then

$$V_0 = -\frac{R_f}{R_1}V_1 + V_2\frac{R_f}{R_1+R_f}\left(\frac{R_1+R_f}{R_1}\right)$$




**Differential Amplifier Using an Op-Amp**

$$V_0 = -\frac{R_f}{R_1}V_1 + V_2\frac{R_f}{R_1}$$

$$V_0 = -\frac{R_f}{R_1}(V_1 - V_2)$$

**KARPAGAM ACADEMY OF HIGHER EDUCATION**
**Coimbatore - 641021.**
**(For the candidates admitted from 2018onwards)**
**DEPARTMENT OF PHYSICS**
**UNIT III :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| QUESTIONS | CHOICE1 | CHOICE2 | CHOICE3 | CHOICE4 | ANSWER |
|---|---|---|---|---|---|
| | | | | | |
| An emitter follower has a voltage gain that is | Much less than one | Approximately equal to one | Greater than one | Zero | Approximately equal to one |
| The input impedance of the base of an emitter follower is usually | Low | High | Shorted to ground | Open | High |
| The ac base voltage of an emitter follower is across the | Emitter diode | DC emitter resistor | Load resistor | Emitter diode and external ac emitter resistance | Emitter diode and external ac emitter resistance |
| The output voltage of an emitter follower is across the | Emitter diode | DC collector resistor | Load resistor | Emitter diode and external ac emitter resistance | Load resistor |
| The differential amplifier has | one input and one output | two inputs and two outputs | two inputs and one output | one input and two outputs | two inputs and one output |
| The differential amplifier produces outputs that are | common mode | in-phase with the input voltages | the sum of the two input voltages | the difference of the two input voltages | the difference of the two input voltages |

| | | | | | |
|---|---|---|---|---|---|
| Which factor does not affect CMOS loading? | Charging time associated with the output resistance of the driving gate | Discharging time associated with the output resistance of the driving gate | Output capacitance of the load gates | Input capacitance of the load gates | Output capacitance of the load gates |
| Which transistor element is used in CMOS logic? | FET | MOSFET | Bipolar | Unijunction | MOSFET |
| A Darlington pair is used for | low distortion | high frequency range | high power gain | high current gain | high current gain |
| What is the effect of cascading amplifier stages? | increase in the voltage gain and increase in the bandwidth | increase in the voltage gain and reduction in the bandwidth | decrease in the voltage gain and increase in the bandwidth | increase in the voltage gain and reduction in the bandwidth | increase in the voltage gain and reduction in the bandwidth |
| An open-drain gate is the CMOS counterpart of _____. | an open-collector TTL gate | a tristate TTL gate | a bipolar junction transistor | an emitter-coupled logic gate | an open-collector TTL gate |
| Which factor does not affect CMOS loading? | Charging time associated with the output resistance of the driving gate | Discharging time associated with the output resistance of the driving gate | Output capacitance of the load gates | Input capacitance of the load gates | Output capacitance of the load gates |
| The decibel gain of a cascaded amplifier equals to | product of individual gains | sum of individual gains | ration of stage gains | product of voltage and current gains | sum of individual gains |
| The most desirable feature of transformer coupling is its | higher voltage gain | wide frequency range | ability to provide impedance matching between stages | ability to eliminate hum from the output | ability to provide impedance matching between stages |
| A transformer coupled amplifier would give | maximum voltage gain | impedance matching | maximum current gain | larger bandwidth | impedance matching |

| | | | | | |
|---|---|---|---|---|---|
| One of the advantages of a Darlington pair is that it has enormous _____ transformation capacity. | Voltage | current | impedance | power | impedance |
| Bootstrapping is used in emitter follower configurations to | stabilize the voltage gain against process variations | increase current gain | reduce the output resistance | increase the input resistance | increase the input resistance |
| Cascading amplifier stages to obtain a high gain is best done with | **common emitter stages** | common base stages | common collector stages | a combination of successive common base and common emitter stages | |
| Which of the following is a concern when using CMOS type devices? | mechanical shock | **electrostatic discharge** | fan out | under voltage | |
| The original CMOS line of circuits is the | 5400 series | **4000 series** | 74C00 series | 74HCOO series | |
| Which of the following is a concern when using CMOS type devices? | mechanical shock | electrostatic discharge | fan out | under voltage | electrostatic discharge |
| Which of the following is not a solution to interface problems between CMOS and TTL? | pull-up resistor | pull-down resistor | level-shifter | buffer | pull-down resistor |
| Which of the following is not a common logic family used today? | RTL | ECL | TTL | CMOS | RTL |
| The output current for a LOW output is called a(n) | exit current. | sink current. | ground current. | fan-out. | sink current. |
| Which of the following are not characteristics of TTL logic gates? | Totem-pole output | Bipolar transistors | CMOS transistors | Multiemitter transistors | CMOS transistors |
| A family of logic devices designed for extremely high speed applications is called | NMOS. | ECL. | PMOS. | TTL. | ECL. |
| Unused inputs on TTL, AND, and NAND gates | degrade the gate's noise immunity. | if left open will have the same effect as HIGH inputs. | should be tied HIGH. | All of the above are correct. | All of the above are correct. |
| The lower transistor of a totem-pole output is OFF when the gate output is | HIGH. | malfunctioning. | LOW. | over driven. | HIGH. |

| | | | | | |
|---|---|---|---|---|---|
| The input transistor on a TTL circuit is unusual in that it has | multiple bases. | no collector. | no base. | multiple emitters. | multiple emitters. |
| The difference between VOH and VIH voltages is known as | input margin. | noise margin. | output differential. | input level. | noise margin. |
| Te maximum output voltage recognized as a LOW by a TTL gate is | 2.0 V. | 0.8 V. | 2.4 V. | | |
| The upper transistor of a totem-pole output is OFF when the gate output is | logic 1. | malfunctioning. | HIGH. | LOW. | LOW. |
| The major advantage of TTL logic circuits over CMOS is | lower propagation delay. | the ability to output higher voltages. | more modern design. | very low power consumption | lower propagation delay. |
| The maximum current for a HIGH output on a standard TTL gate is | -10 µA. | -400 µA. | -1 µA. | -10 mA. | -400 µA. |
| The maximum current for a LOW output on a standard TTL gate is | 16 µA. | 40 mA. | 100 µA. | 16 mA. | 16 mA. |
| The major advantage of CMOS logic circuits over TTL is | very low power consumption. | the ability to produce several output voltage levels. | lower propagation delay. | much higher propagation delay. | very low power consumption. |
| The abbreviated designation for input current with a LOW input is | VIH. | IIH. | IIL. | IOL. | IIL. |
| Fan-out for a typical TTL gate is _____. | 10 | 4 | 54 | 100 | 10 |
| In order to interface an FPGA with an external device, you must set the value of the | sink current. | external power supply. | source current. | all of the above | all of the above |
| The abbreviated designator for a LOW output voltage is | VOH. | VIL. | VOL. | VIH. | VOL. |
| The lower transistor of a totem-pole output is saturated when the gate output is | HIGH. | LOW. | malfunctioning. | over driven. | LOW. |
| The abbreviation TTL means | transistor-transceiver latch. | three-transistor logic. | two-transistor logic. | transistor-transistor logic. | transistor-transistor logic. |
| Typical TTL HIGH level output voltage is | 0.3 V. | 5.0 V. | 3.4 V. | 4.8 V. | 3.4 V. |

| | | | | | |
|---|---|---|---|---|---|
| The standard 74XX TTL IC family was originally developed in the | 1970s. | 1960s. | 1950s. | 1940s. | 1960s. |
| The minimum output voltage recognized as a HIGH by a TTL gate is | 0.8 V. | 2.4 V. | 5.0 V. | 2.0 V. | 2.4 V. |
| An open-collector TTL gate | can sink current but cannot source current. | can source current but cannot sink current. | cannot source or sink current. | can sink more current than a standard TTL gate. | can sink current but cannot source current. |
| The minimum input voltage recognized as a HIGH by a TTL gate is | 0.8 V. | 2.4 V. | 2.0 V. | 5.0 V | 2.0 V. |
| Which of the following digital IC logic families is most susceptible to static discharge? | RTL | ECL | MOS | TTL | MOS |
| Each input on a TTL gate is connected to the transistor's | base. | collector. | gate. | emitter. | emitter. |
| The time it takes for an input signal to pass through internal circuitry and generate the appropriate output effect is known as | propagation delay. | rise time. | fan-out. | fall time | propagation delay. |
| In a common emitter, unbypassed resister provides | voltage shunt feedback | current series feedback | Negative voltage feedback | positive current feedback | voltage shunt feedback |
| The bandwidth of an RF tuned amplifier is dependent on | | Q –factor of the tuned i/p circuit | Quiescent operating point | Q-factor of the o/p and i/p circuits as well as quiescent operating point | Q –factor of the tuned o/p circuit |
| Negative feedback in an amplifier | Reduces gain | Increase frequency &phase distortion | Reduces bandwidth | Increases noise | Reduces gain |
| An amplifier without feedback has a voltage gain of 50, input resistance is 1 KΩ & Output resistance of 2.5KΩ.The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a | 1/11KΩ | 1/5KΩ | 5KΩ | 11KΩ | 1/5KΩ |

| | | | | | |
|---|---|---|---|---|---|
| feedback factor of 0.2 is | | | | | |
| The fan out of a MOS logic gate is higher than that of TTL gates because of its | Low input impedance | high output impedance | Low output impedance | High input impedance | High input impedance |
| Transformer coupling can be used in _____ amplifiers | Only power | Only voltage | Either power or voltage | Neither power nor voltage | Either power or voltage |
| When negative current feedback is applied to an amplifier, its output impedance | increases | remains unchanged | decreases | becomes zero | increases |
| The quiescent current of a FET amplifier is | IDS | id | ID | Id | ID |
| The total decibel voltage gain of two cascaded voltage amplifier where individual voltage gains are 10 and 100 is | 20 | 60 | 800 | 1000 | 60 |
| The frequency response of the combined amplifier can be compared with | An OR gate | A negative feedback amplifier | A positive filter | An AND gate | An AND gate |
| Minimum interference with frequency response can be given by | Direct coupling | RC coupling | Transformer coupling | Instrumentation and control | Direct coupling |
| The impedance of a load must match the impedance of the amplifier so that | Minimum power is transferred to the load | The efficiency can be maintained at low level | The signal-to-noise ratio is maximized | Maximum power is transferred to the load | Maximum power is transferred to the load |
| The ratio output rms power in watts to the input dc power in watts in the different amplifier class is called _____. | Gain | Amplification factor | Efficiency | Phase power | Efficiency |
| Consider a zener diode with a slope resistance of 10 Ω in series with a 90 Ω resistor fed from a dc supply containing a ripple voltage of 20mV peak-to-peak. Compute for the ripple voltage in load | 1 mV p-p | 2 mV p-p | 1 V p-p | 6mV p-p | 2 mV p-p |

| | | | | | |
|---|---|---|---|---|---|
| The _____ of a common collector configuration is unity | Voltage gain | Current gain | Power gain | Input impedance | Voltage gain |
| Transmit time is the time taken by the electrons on holes to pass from | Emitter to collector | Collector to emitter | Base to emitter | Base to collector | Emitter to collector |
| For BJT power transistors, the collector terminal is always connected to the transistor's case | for easy circuit connection. | to prevent shorts. | because the collector terminal is the critical terminal for heat dissipation. | because the collector terminal is located nearest the case. | because the collector terminal is the critical terminal for heat dissipation |
| Quiescent power is the power dissipation of a transistor | with no signal input. | with no load. | under full load. | along the dc load line. | with no signal input |
| A class B amplifier operates in the linear region for | slightly more than 180° of the input cycle. | 360° of the input cycle. | slightly less than 180° of the input cycle. | much less than 180° of the input cycle. | slightly less than 180° of the input cycle |
| In a class AB amplifier, if the $V_{BE}$ drops are not matched to the diode drops or if the diodes are not in thermal equilibrium with the transistors, this can result in | a current mirror. | diode separation. | crossover distortion. | thermal runaway. | thermal runaway |
| Which amplifier is commonly used as a frequency multiplier? | class A | class B | class C | all of the above | class C |
| The least efficient amplifier among all classes is | class B. | class A. | class AB. | class C. | class B |
| A class A amplifier has a voltage gain of 30 and a current gain of 25. What is the power gain? | 30 | 25 | 1.2 | 750 | 750 |
| You have an application for a power amplifier to operate on FM radio frequencies. The most likely choice would be a _____ amplifier. | class A | class B | class C | class AB | class C |

| | | | | | |
|---|---|---|---|---|---|
| A class A amplifier with $R_C$ = 3.3 kΩ and $R_E$ = 1.2 kΩ has a $V_{CC}$ = 20 V. Find $I_{C(sat)}$. | 4.4 mA | 6.1 mA | 16.7 mA | 20 mA | 4.4 mA |
| A class C amplifier has a tank circuit in the output. The amplifier is conducting only 28°. The output voltage is | 0 V. | a dc value equal to $V_{CC}$. | a sine wave. | a square wave with a frequency determined by the tank. | a sine wave. |
| In practice, the efficiency of a capacitively coupled class A amplifier is about _____%. | 25 | 40 | 70 | 10 | 10 |
| The Q-point is at cutoff for class _____ operation. | A | B | C | AB | B |
| Class _____ amplifiers are normally operated in a push-pull configuration in order to produce an output that is a replica of the input. | A | B | C | AB | AB |
| The maximum efficiency of a class B amplifier is _____ percent. | 50 | 25 | 70 | 79 | 79 |
| A class _____ amplifier is biased slightly above cutoff and operates in the linear region for slightly more than 180º of the input cycle. | A | B | C | AB | AB |
| Which class of amplifier operates in the linear region for only a small part of the input cycle? | A | B | C | AB | C |
| The principal advantage(s) of MOSFETs over BJTs is (are) | their biasing networks are simpler. | their drive requirements are simpler. | they can be connected in parallel for added drive capability. | all of the above | all of the above |
| The principal advantage(s) of BJTs over MOSFETs is (are) that | voltage drop across the transistor is important. | they are not as prone to ESD. | both of the above | none of the above | both of the above |
| The class _____ amplifier is biased below cutoff. | A | AB | B | C | B |

| | | | | | |
|---|---|---|---|---|---|
| **Prepared By-Ambili Vipin,Assistant Professor,Department of Physics** | | | | | |

## UNIT-IV

## SYLLABUS

**Power Amplifiers**: Introduction, Series-fed Class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation, Class B amplifier distortion, Power transistor heat sinking, Class C and Class D amplifiers, Numerical problems

## INTRODUCTION TO POWER AMPLIFIERS:

Power amplifier is an output stage of amplifier optimized to provide high output power gain.

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small and needs to be amplified sufficiently to operate an output device. In small-signal amplifiers the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

### Classification of Power Amplifier

One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal.

There are mainly four types of amplifiers based on conduction angle. They are

a) Class A amplifiers

b) Class B amplifiers

c) Class AB amplifiers

d) Class C amplifiers

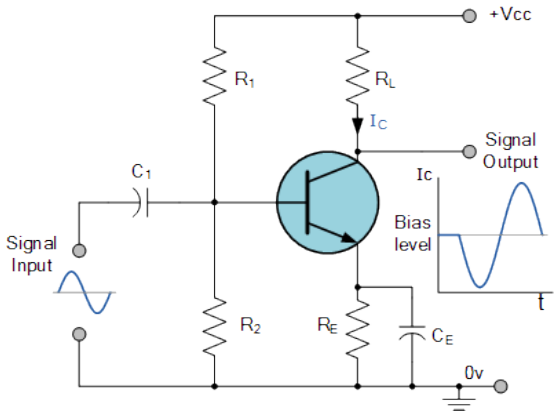
Class A amplifier: In class-A amplifiers the collector is biased at a value greater than the amplitude of AC signal current. Hence the conduction angle is 360 Degrees i.e. the Class A stage conducts for the entire cycle for the input signal.

Class B amplifier: Class B amplifiers are biased at zero DC bias collector current. Hence it conducts only for half of the input signal cycle, so the conduction angle for class B amplifier is 180 Degrees.

Class AB amplifier: In class AB amplifiers the biasing current is non zero but much smaller than the peak current of the sine wave signal. As a result the transistor conducts for interval slightly greater than half a cycle. The conduction angle is slightly greater than 180 Degrees.

Class C amplifier: In class C amplifier the transistor conducts for an interval less than the half cycle. Hence the conduction angle is less than 180 Degrees.

**Class A amplifier:**



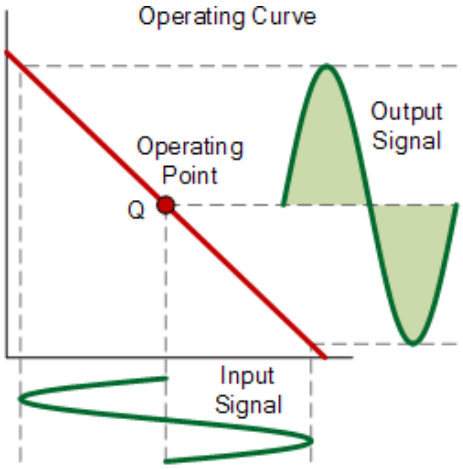

The main function of the power amplifier, which are also known as a "large signal amplifier" is to deliver power, which is the product of voltage and current to the load. Basically a power amplifier is also a voltage amplifier the difference being that the load resistance connected to the output is relatively low.

The most commonly used type of power amplifier configuration is the Class A Amplifier. The Class A amplifier is the simplest form of power amplifier that uses a single switching transistor in the standard common emitter circuit configuration as seen previously to produce an inverted output. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude of the output signal.

This means then that the Class A Amplifier configuration is the ideal operating mode, because there can be no crossover or switch-off distortion to the output waveform even during the negative half of the cycle. Class A power amplifier output stages may use a single power transistor or pairs of transistors connected together to share the high load current.

It uses a single-ended transistor for its output stage with the resistive load connected directly to the Collector terminal. When the transistor switches "ON" it sinks the output current through the Collector resulting in an inevitable voltage drop across the Emitter resistance thereby limiting the negative output capability.

The efficiency of this type of circuit is very low (less than 30%) and delivers small power outputs for a large drain on the DC power supply. A Class A amplifier stage passes the same load current even when no input signal is applied so large heat sinks are needed for the output transistors.



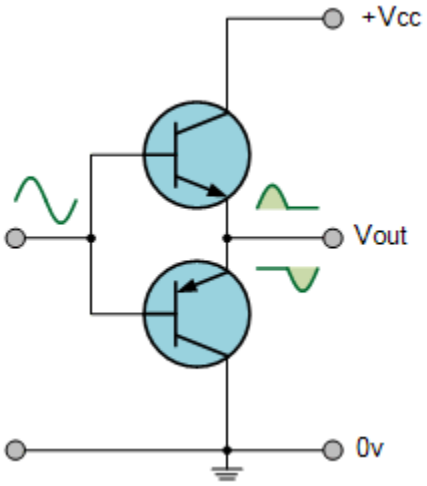

To achieve high linearity and gain, the output stage of a class A amplifier is biased "ON" (conducting) all the time. Then for an amplifier to be classified as "Class A" the zero signal idle current in the output stage must be equal to or greater than the maximum load current (usually a loudspeaker) required to produce the largest output signal.

As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform. Then the class A amplifier is equivalent to a current source.Since a class A amplifier operates in the linear region, the transistors base (or gate) DC biasing voltage should by chosen properly to ensure correct operation and low distortion. However, as the output device is "ON" at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier.

Due to this continuous loss of power class A amplifiers create tremendous amounts of heat adding to their very low efficiency at around 30%, making them impractical for high-power

amplifications. Also due to the high idling current of the amplifier, the power supply must be sized accordingly and be well filtered to avoid any amplifier hum and noise. Therefore, due to the low efficiency and overheating problems of Class A amplifiers, more efficient amplifier classes have been developed.

**Class B Amplifier**




Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform.

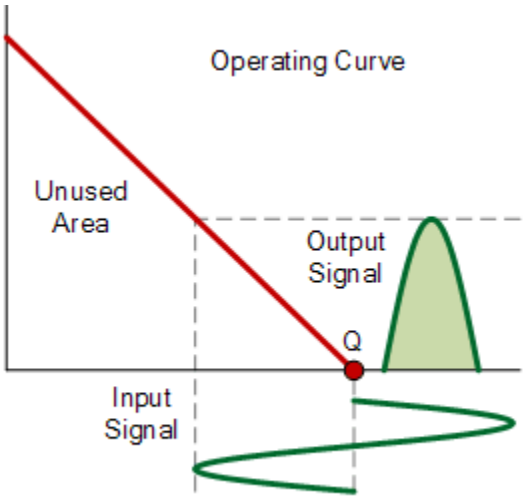
In the case of class B amplifier, there is no DC base bias current as its quiescent current is zero, so that the dc power is small and therefore its efficiency is much higher than that of the class A amplifier.

When the input signal goes positive, the positive biased transistor conducts while the negative transistor is switched "OFF". Likewise, when the input signal goes negative, the

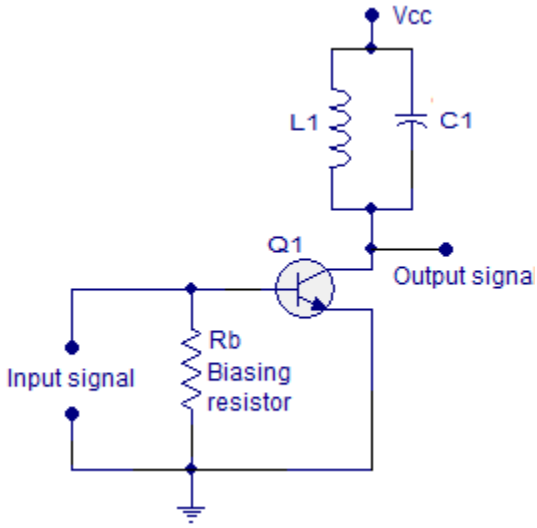
positive transistor switches "OFF" while the negative biased transistor turns "ON" and conducts the negative portion of the signal. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal.

Then we can see that each transistor device of the class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

This push-pull design of amplifier is obviously more efficient than Class A, at about 50%, but the problem with the class B amplifier design is that it can create distortion at the zero-crossing point of the waveform due to the transistors dead band of input base voltages from -0.7V to +0.7.



## Class C Amplifier

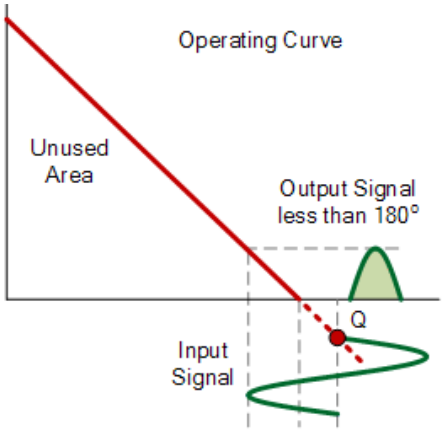



The Class C Amplifier design has the greatest efficiency but the poorest linearity of the classes of amplifiers.

The class C amplifier is heavily biased so that the output current is zero for more than one half of an input sinusoidal signal cycle with the transistor idling at its cut-off point. In other words, the conduction angle for the transistor is significantly less than 180 degrees, and is generally around the 90 degrees area. While this form of transistor biasing gives a much improved efficiency of around 80% to the amplifier, it introduces a very heavy distortion of the output signal. Therefore, class C amplifiers are not suitable for use as audio amplifiers. Due to its heavy audio distortion, class C amplifiers are commonly used in high frequency sine wave oscillators and certain types of radio frequency amplifiers, where the pulses of current produced at the amplifiers output can be converted to complete sine waves of a particular frequency by the use of LC resonant circuits in its collector circuit.

Biasing resistor Rb pulls the base of Q1 further downwards and the Q-point will be set some way below the cut-off point in the DC load line. As a result the transistor will start conducting only after the input signal amplitude has risen above the base emitter voltage (Vbe~0.7V) plus the downward bias voltage caused by Rb. That is the reason why the major portion of the input signal is absent in the output signal.

Inductor L1 and capacitor C1 forms a tank circuit which aids in the extraction of the required signal from the pulsed output of the transistor. Actual job of the active element (transistor) here is to produce a series of current pulses according to the input and make it flow through the resonant circuit. Values of L1 and C1 are so selected that the resonant circuit oscillates in the frequency of the input signal. Since the resonant circuit oscillates in one frequency (generally the carrier frequency) all other frequencies are attenuated and the required frequency can be squeezed out using a suitably tuned load. Harmonics or noise present in the output signal can be eliminated using additional filters. A coupling transformer can be used for transferring the power to the load.



**Power transistor heat sinking**

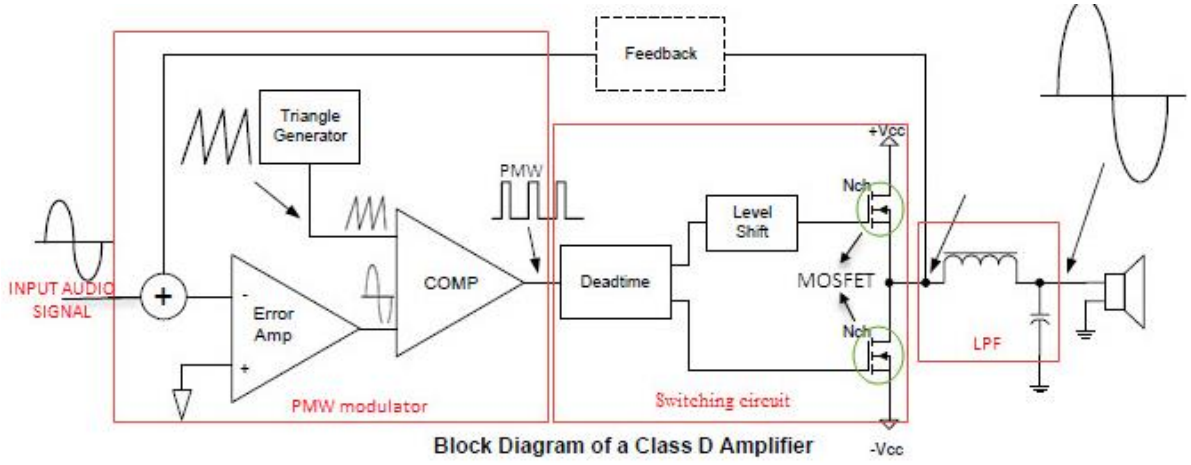
A heat-sink is designed to remove heat from a transistor and dissipate it into the surrounding air as efficiently as possible. Heat-sinks take many different forms, such as finned aluminium or copper sheets or blocks, often painted or anodised matt black to help dissipate heat more quickly. Good physical contact between the transistor and heat-sink is essential, and a heat transmitting grease (heat-sink compound) is smeared on the contact area before clamping the transistor to the heat-sink.

The heat-sink chosen must be able to dissipate heat from the transistor to the surrounding air, quickly enough to prevent the junction temperature of the transistor exceeding its maximum permitted typically 100 to 150°C.Each heat-sink has a parameter called its Thermal Resistance ($R_{th}$) measured in °C/Watt and the lower the value of $R_{th}$ the faster heat is dissipated. Other factors affecting heat dissipation include the power (in Watts) being dissipated by the transistor, the efficiency of heat transfer between the internal transistor junction and the transistor case, and the case to the heat-sink.

The difference between the temperature of the heat-sink and the air temperature surrounding the heat-sink (the ambient temperature) must also be taken into account. Therefore any heat-sink with a thermal resistance lower or equal to the calculated value should be considered, but to avoid continually running the transistor at, or close to the maximum permitted temperature, which is almost guaranteed to shorten the life of the transistor, it is advisable to use a heat-sink with a lower thermal resistance where possible.

## Class-D Amplifier

A class-D amplifier or switching amplifier is an electronic amplifier in which the amplifying devices operate as electronic switches, and not as linear gain devices as in other amplifiers. Class-D amplifiers work by generating a train of square pulses of fixed amplitude but varying width and separation, or varying number per unit time, representing the amplitude variations of the analog audio input signal. When it is in the "ON" state it will conduct current but have almost zero voltage across the switches, therefore no heat is dissipated due to power consumption.




Block Diagram of a Class D Amplifier

## PMW Modulator

A comparator has two inputs, namely Input A and Input B. When Input A is higher in voltage than Input B, the output of the comparator will go to its maximum positive voltage(+Vcc). When Input A is lower in voltage than Input B, the output of the comparator will go to its maximum negative voltage(-Vcc). One input (Input A) is supplied with the signal to be amplified. The other input (Input B) is supplied with a precisely generated triangle wave. When the signal is instantaneously higher in level than the triangle wave, the output goes positive. When the signal is instantaneously lower in level than the triangle wave, the output goes negative. The result is a chain of pulses where the pulse width is proportional to the instantaneous signal level. This is known as 'pulse width modulation', or PWM.

## Switching Circuit

Even though, the output of the comparator is a digital representation of the input audio signal, it doesn't have the power to drive the load (speaker). The task of this switching circuit is to provide enough power gain, which is essential for an amplifier. The switching circuit is generally designed by using MOSFETs. It is very crucial to design that the switching circuits produce signals that do not overlap or else you run into the problem of shorting your supply straight to ground or if using a split supply shorting the supplies. This is known as shoot through, but it can be prevented by introducing non-overlapping gate signals to the MOSFETs. The non-overlapping time is known as Dead time. In designing these signals we must keep the dead time as short as possible to maintain an accurate low-distortion output signal, but must be long enough to maintain both MOSFETs from conducting at the same time. The time that the MOSFETs are in linear mode must also be reduced which will help insure that the MOSFETs are working synchronously rather than both conducting at the same time.

## Output Low Pass Filter

The final stage of a Class D amplifier is the output filter which attenuates and removes the harmonics of the switching signal frequency. This can be done with a common low passfilter arrangement, but the most common is an inductor and capacitor combination. A 2ndorderfilter is desired so that we have a -40dB/Decade roll-off. The range of cutoff frequencies is between 20 kHz to about 50 kHz due to the fact that humans cannot hear anything above 20 kHz. Below figure shows the second order Butterworth filter. The main reason we choose a Butterworth filter is because it requires the least amount of components and has a flat response with a sharp cut off frequency.

## POSSIBLE QUESTIONS

### PART-B (2 Marks)

1. What are the advantages of Multistage amplifiers?

2. How can we classify multi stage amplifier?
3. What do you mean by heat sinking?
4. Define PWM.
5. What is called low pass filter?
6. Define collector efficiency.
7. What is called Class –A amplifier?
8. What is called Class –B amplifier?
9. What is called Class –C amplifier?
10. What is called Class –D amplifier?

**PART-C (6 marks)**

1. Explain the terms: (i) collector efficiency, (ii) power dissipation capability and (iii) overall gain.
2. State clearly the meaning of class A, B and C as applied to power amplifiers. What is meant by the angle of flow?
3. Discuss class A transformer coupled amplifier.
4. Explain class A power amplifier. How power is distributed in it?
5. Explain about heat sinks in power amplifiers.
6. Derive the working principle of class B – power amplifiers.
7. What do you understand by cross-over distortion? How can it be eliminated in Class B-operation?
8. What is the basis for the classification of power amplifiers? Mention the different types of power amplifiers.
9. Draw a circuit for class C amplifier and discuss its working.
10. Draw a circuit for class D amplifier and discuss its working.

**KARPAGAM ACADEMY OF HIGHER EDUCATION**
**Coimbatore - 641021.**
**(For the candidates admitted from 2018onwards)**
**DEPARTMENT OF PHYSICS**
**UNIT IV :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| QUESTIONS | CHOICE1 | CHOICE2 | CHOICE3 | CHOICE4 | ANSWER |
|---|---|---|---|---|---|
| | | | | | |
| For Class-B operation, the collector current flows for | The whole cycle | Half the cycle | Less than half a cycle | Less than a quarter of a cycle | Half the cycle |
| Transformer coupling is an example of | Direct coupling | AC coupling | DC coupling | Impedance coupling | AC coupling |
| Class-C amplifiers are almost always | Transformer-coupled between stages | Operated at audio frequencies | Tuned RF amplifiers | Wideband | Tuned RF amplifiers |
| Heat sinks reduce the | Transistor power | Ambient temperature | Junction temperature | Collector current | Junction temperature |
| Which type of power amplifier is biased for operation at less than 180º of the cycle? | Class A | Class B or AB | Class C | Class D | Class C |
| What is the maximum efficiency of a class A circuit with a direct or series-fed load connection? | 90% | 78.50% | 50% | 25% | 25% |
| The Q-point is at cutoff for class _____ operation. | A | B | C | AB | B |
| Which of the following is (are) power amplifiers? | Class A | Class B or AB | Class C or D | All of the above | All of the above |
| The output of a class-B amplifier | is distortion free | consists of positive half cycle only | is like the output of a full wave rectifier | comprises short duration current pulses | consists of positive half cycle only |

| | | | | | |
|---|---|---|---|---|---|
| Crossover distortion occurs in _____ amplifiers. | push-pull | class A | class B | class AB | push-pull |
| The main use of a class C amplifier is | as an RF amplifier | as stereo amplifier | in communication sound equipment | as distortion generator | as an RF amplifier |
| The decibel is a measure of | power | voltage | current | sound level | sound level |
| The output stage of a multistage amplifier is also called | Mixer stage | Power stage | Detector stage | F stage | Power stage |
| _____ coupling is generally employed in power amplifiers | Transformer | RC | direct | Impedance | Transformer |
| The maximum efficiency of resistance loaded class A power amplifier is | 5% | 50% | 30% | 25% | 25% |
| Class _____ power amplifier has the highest collector efficiency | C | A | B | AB | B |
| Power amplifiers handle _____ signals compare to voltage amplifiers. | Small | Very small | Large | None of the above | Large |
| In class B operation, at what fraction of VCC should the level of VL(p) be to achieve the maximum power dissipated by the output transistor? | 0.5 | 0.636 | 0.707 | 1 | 0.636 |
| In class A operation, the operating point is generally located _____ of the d.c. load line. | At cut off point | At the middle | At saturation point | None of the above | At the middle |
| The output transformer used in a power amplifier is a _____ transformer. | 1:1 ratio | Step-up | Step-down | None of the above | Step-down |
| For BJT power transistors, the collector terminal is always connected to the transistor's case | for easy circuit connection. | to prevent shorts. | because the collector terminal is the critical terminal for heat dissipation. | because the collector terminal is located nearest the case. | because the collector terminal is the critical terminal for heat dissipation |

| | | | | | |
|---|---|---|---|---|---|
| Quiescent power is the power dissipation of a transistor | with no signal input. | with no load. | under full load. | along the dc load line. | with no signal input |
| A class B amplifier operates in the linear region for | slightly more than 180° of the input cycle. | 360° of the input cycle. | slightly less than 180° of the input cycle. | much less than 180° of the input cycle. | slightly less than 180° of the input cycle |
| In a class AB amplifier, if the $V_{BE}$ drops are not matched to the diode drops or if the diodes are not in thermal equilibrium with the transistors, this can result in | a current mirror. | diode separation. | crossover distortion. | thermal runaway. | thermal runaway |
| Which amplifier is commonly used as a frequency multiplier? | class A | class B | class C | all of the above | class C |
| The least efficient amplifier among all classes is | class B. | class A. | class AB. | class C. | class B |
| A class A amplifier has a voltage gain of 30 and a current gain of 25. What is the power gain? | 30 | 25 | 1.2 | 750 | 750 |
| You have an application for a power amplifier to operate on FM radio frequencies. The most likely choice would be a _____ amplifier. | class A | class B | class C | class AB | class C |
| A class A amplifier with $R_C$ = 3.3 kΩ and $R_E$ = 1.2 kΩ has a $V_{CC}$ = 20 V. Find $I_{C(sat)}$. | 4.4 mA | 6.1 mA | 16.7 mA | 20 mA | 4.4 mA |
| A class C amplifier has a tank circuit in the output. The amplifier is conducting only 28°. The output voltage is | 0 V. | a dc value equal to $V_{CC}$. | a sine wave. | a square wave with a frequency determined by the tank. | a sine wave. |
| In practice, the efficiency of a capacitively coupled class A amplifier is about _____%. | 25 | 40 | 70 | 10 | 10 |
| The Q-point is at cutoff for class _____ operation. | A | B | C | AB | B |
| Class _____ amplifiers are normally operated in a push-pull configuration in order to produce an output that is a replica of the input. | A | B | C | AB | AB |

| | | | | | |
|---|---|---|---|---|---|
| The maximum efficiency of a class B amplifier is _____ percent. | 50 | 25 | 70 | 79 | 79 |
| A class _____ amplifier is biased slightly above cutoff and operates in the linear region for slightly more than 180º of the input cycle. | A | B | C | AB | AB |
| Which class of amplifier operates in the linear region for only a small part of the input cycle? | A | B | C | AB | C |
| The principal advantage(s) of MOSFETs over BJTs is (are) | their biasing networks are simpler. | their drive requirements are simpler. | they can be connected in parallel for added drive capability. | all of the above | all of the above |
| The principal advantage(s) of BJTs over MOSFETs is (are) that | voltage drop across the transistor is important. | they are not as prone to ESD. | both of the above | none of the above | both of the above |
| The class _____ amplifier is biased below cutoff. | A | AB | B | C | B |
| Power amplifiers primarily provide sufficient power to an output load, typically from _____ to _____. | a few kW, tens of kW | 500 W, 1 kW | 100 W, 500 W | a few W, tens of W | a few W, tens of W |
| The main feature(s) of a large-signal amplifier is (are) the _____. | circuit's power efficiency | maximum amount of power that the circuit is capable of handling | impedance matching to the output | All of the above | All of the above |
| In _____ power amplifiers, the output signal varies for a full 360º of the cycle. | class A | class B or AB | class C | class D | class A |
| In class B power amplifiers, the output signal varies for _____ of the cycle. | 360º | 180º | between 180º and 360º | less than 180º | 180º |
| _____ amplifiers have the highest overall efficiency. | Class A | Class B or AB | Class C | Class D | Class D |
| Class D operation can achieve power efficiency of over _____. | 90% | 78.50% | 50% | 25% | 90% |
| The beta of a power transistor is generally _____. | more than 200 | 100 to 200 | less than 100 | 0 | less than 100 |

| | | | | | |
|---|---|---|---|---|---|
| A form of class A amplifier having maximum efficiency of _____ uses a transformer to couple the output signal to the load. | 90% | 78.50% | 50% | 25% | 50% |
| The reflected impedance seen from one side of the transformer to the other side is _____. | $N_1/N_2$ | $(N_1/N_2)^2$ | $(N_1/N_2)^{1/3}$ | $N_1 \times N_2$ | $(N_1/N_2)^2$ |
| In a class A transformer-coupled power amplifier, _____ winding resistance of the transformer determine(s) the dc load line for the circuit. | the ac | the dc | both the ac and dc | neither the ac nor dc | the dc |
| The slope of the ac load line in the class A transformer-coupled transistor is _____. | $-1/R_L$ (load resistor) | $1/(a^2R_L)$ | $-1/(a^2R_L)$ | $1/R_L$ | $-1/(a^2R_L)$ |
| The amount of power dissipated by the transistor is the _____ of that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. | product | difference | average | | difference |
| A class A amplifier dissipates _____ power when the load is drawing maximum power from the circuit. | the least | about the same | the most | None of the above | the least |
| In a class A transformer-coupled amplifier, the _____ the value of $V_{CEmax}$ and the _____ the value of $V_{CEmin}$, the _____ the efficiency to (from) the theoretical limit of 50%. | larger, smaller, farther | larger, smaller, closer | smaller, larger, closer | None of the above | larger, smaller, closer |
| In class B operation, the current drawn from a single power supply has the form of _____ rectified signal. | a full-wave | a half-wave | both a full-wave and a half-wave | None of the above | a full-wave |
| The highest efficiency is obtained in class B operation when the level of $V_L(p)$ is equal to _____. | $0.25V_{CC}$ | $0.50V_{CC}$ | $V_{CC}$ | $2V_{CC}$ | $V_{CC}$ |
| _____ transistors can be used to build a class B amplifier. | npn and pnp | nMOS and pMOS | Both npn and pnp or nMOS and pMOS | None of the above | Both npn and pnp or nMOS and pMOS |

| | | | | | |
|---|---|---|---|---|---|
| The complementary Darlington-connected transistor for a class B amplifier provides _____ output current and _____ output resistance. | higher, higher | higher, lower | lower, lower | lower, higher | higher, lower |
| The fundamental component is typically _____ any harmonic component. | larger than | the same as | smaller than | None of the above | larger than |
| In Fourier technique, any periodic distorted waveform can be represented by _____ the fundamental and all harmonic components. | multiplying | subtracting | dividing | adding | adding |
| Improvement in production techniques of power transistors have _____. | produced higher power ratings in small-sized packaging cases | increased the maximum transistor breakdown voltage | provided faster-switching power transistors | All of the above | All of the above |
| The greater the power handled by the power transistor, _____ the case temperature. | the higher | the lower | there is no change in | None of the above | the higher |
| The _____ has the hottest temperature in a power transistor. | heat sink | case | junction | None of the above | junction |
| A heat sink provides _____ thermal resistance between case and air. | a high | a low | the same | None of the above | a low |
| A _____ power amplifier is limited to use at one fixed frequency. | class A | class B or AB | class C | class D | class C |
| Which of the following is (are) power amplifiers? | Class A | Class B or AB | Class C or D | All of the above | All of the above |
| By how much does the output signal vary for a class AB power amplifier? | 360º | 180º | Between 180º and 360º | Less than 180º | Between 180º and 360º |
| Which type of power amplifier is biased for operation at less than 180º of the cycle? | Class A | Class B or AB | Class C | Class D | Class C |
| Which type of amplifier uses pulse (digital) signals in its operation? | Class A | Class B or AB | Class C | Class D | Class D |
| Which of the power amplifiers has the lowest overall efficiency? | Class A | Class B or AB | Class C | Class D | Class A |
| Which of the following describe(s) a power amplifier? | It can handle large power. | It can handle large current. | It does not provide much voltage | All of the above | All of the above |

| | | | | | |
|---|---|---|---|---|---|
| | | | gain. | | |
| _____ amplifiers primarily provide sufficient power to an output load to drive a speaker from a few watts to tens of watts. | Small-signal | Power | None of the above | All of the above | Power |
| The main features of a large-signal amplifier is the circuit's _____. | power efficiency | maximum power limitations | impedance matching to the output device | All of the above | All of the above |
| Class AB operation is _____ operation. | similar to class A | similar to class B | similar to class C | d. None of the above | None of the above |
| Which operation class is generally used in radio or communications? | A | B | AB | C | Class C |
| Categorize the power efficiency of each class of amplifier, from worst to best. | A, B, AB, D | A, AB, D, B | A, AB, B, D | | A, AB, B, D |
| What is the maximum efficiency of a class A circuit with a direct or series-fed load connection? | 90% | 78.50% | 50% | 25% | 25% |
| What is the ratio of the secondary voltage to the primary voltage with the turn ratio in the winding | $N_2/N_1$ | $(N_1/N_2)2$ | $(N_1/N_2)1/3$ | $N_1 \times N_2$ | $N_2/N_1$ |
| Calculate the effective resistance seen looking into the primary of a 20:1 transformer connected to an 8- Ω load. | 3.2 kΩ | 3.0 kΩ | 2.8 kΩ | 1.8 kΩ | 3.2 kΩ |
| What transformer turns ratio is required to match an 8-speaker load so that the effective load resistance seen at the primary is 12.8 k? | 20:01 | 40:01:00 | 50:01:00 | 60:01:00 | 40:01:00 |
| Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 15 V and an output of V(p) = 10 V. | 25% | 33.30% | 50% | 78.50% | 33.30% |
| The maximum efficiency of a transformer-coupled class A amplifier is _____. | a. 25% | b. 50% | c. 78.5% | d. 63.6% | 50% |
| What is the maximum efficiency of a class B circuit? | a. 90% | b. 78.5% | c. 50% | d. 25% | 78.50% |

| | | | | | |
|---|---|---|---|---|---|
| How many transistors must be used in a class B power amplifier to obtain the output for the full cycle of the signal? | 0 | 1 | 2 | 3 | 2 |
| In class B operation, at what fraction of $V_{CC}$ should the level of $V_L(p)$ be to achieve the maximum power dissipated by the output transistor? | 0.5 | 0.636 | 0.707 | 1 | 0.636 |
| Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. | TRUE | FALSE | | | TRUE |
| Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC}$ = 20 V with peak output voltage of $V_L(p)$ = 18 V. Assume $R_L$ = 16 Ω. | 78.54% | 75% | 70.69% | 50% | 70.69% |
| Which of the following is (are) the disadvantage(s) of a class B complementary-symmetry circuit? | It needs two separate voltage sources. | There is crossover distortion in the output signal. | It does not provide exact switching of one transistor off and the other on at the zero-voltage condition. | All of the above | All of the above |
| Which of the push-pull amplifiers is presently the most popular form of the class B power amplifier? | Quasi-complementary | Transformer-coupled | Complementary-symmetry | None of the above | Quasi-complementary |
| nMOS and pMOS transistors can be used for class B. | TRUE | FALSE | | | TRUE |
| Calculate the harmonic distortion component for an output signal having fundamental amplitude of 3 V and a second harmonic amplitude of 0.25 V. | a. 3.83% | b. 38.3% | c. 83.3% | d. 8.33% | 8.33% |
| Which of the following instruments displays the harmonics of a distorted signal? | Digital multimeter | Spectrum analyzer | Oscilloscope | Wave analyzer | Spectrum analyzer |
| Which of the following instruments allows more precise measurement of the harmonic | a. Digital multimeter | b. Spectrum analyzer | c. Oscilloscope | d. Wave analyzer | Wave analyzer |

| | | | | | |
|---|---|---|---|---|---|
| components of a distorted signal? | | | | | |
| What is the maximum temperature rating for silicon power transistors? | 50º to 80º | 100º to 110º | 150º to 200º | 250º to 300º | 150º to 200º |
| Which of the power amplifiers is not intended primarily for large-signal or power amplification? | Class A | Class B or AB | Class C | Class D | Class C |
| Determine what maximum dissipation will be allowed for a 70-W silicon transistor (rated at 25ºC) if derating is required above 25ºC by a derating factor of 0.6 W/ºC at a case temperature of 100º. | 25 W | 30 W | 35 W | 40 W | 25 W |
| A silicon power transistor is operated with a heat sink ($\theta_{SA}$ = 1.5ºC/W). The transistor, rated at 150 W (25ºC), has $\theta_{JC}$ = 0.5º C/W, and the mounting insulation has $\theta_{CS}$ = 0.6 ºC/W. What is the maximum power that can be dissipated if the ambient temperature is 50ºC and $T_{Jmax}$ = 200 ºC? | 61.5 W | 60.0 W | 57.7 W | 55.5 W | 57.7 W |
| Which of the following transistors has been quite popular as the driver device for class D amplification? | BJT | FET | UJT | MOSFET | MOSFET |
| | | | | | |
| **Prepared By-Ambili Vipin,Assistant Professor,Department of Physics** | | | | | |

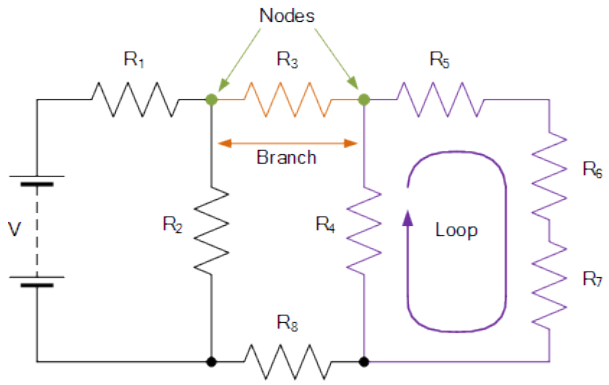
## UNIT-V

## SYLLABUS

**Network Theory**: mesh and node analysis Kirchhoff's voltage and current law, Network Theorems- Thevein's theorem, Norton's theorem, Superposition Theorem, Maximum power transfer theorem, Problems based on network theorems

## NETWORK THEORY

Network analysis is any structured technique used to mathematically analyze a circuit (a "network" of interconnected components).




Simple circuits are using Ohm's law alone to find the voltages or currents circulating within the circuit .But sometimes in complex circuits such as bridge or T networks, we cannot simply use Ohm's Law alone to find the voltages or currents circulating within the circuit. For these types of calculations we need certain rules which allow us to obtain the circuit equations and for this we can use Kirchhoffs Circuit Law.

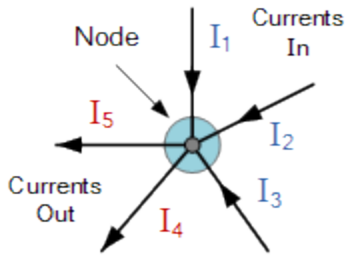
In 1845, a German physicist, Gustav Kirchhoff developed a pair or set of rules or laws which deal with the conservation of current and energy within electrical circuits. These two rules are commonly known as: Kirchhoffs Circuit Laws with one of Kirchhoffs laws dealing with the current flowing around a closed circuit, Kirchhoffs Current Law, (KCL) while the other law deals with the voltage sources present in a closed circuit, Kirchhoffs Voltage Law, (KVL).

**Kirchhoffs First Law – The Current Law, (KCL)**

Kirchhoffs Current Law or KCL, states that the "total current or charge entering a junction or node is exactly equal to the charge leaving the node as it has no other place to go except to leave, as no charge is lost within the node". In other words the algebraic sum of ALL the currents entering and leaving a node must be equal to zero, $I_{(exiting)} + I_{(entering)} = 0$. This idea by Kirchhoff is commonly known as the Conservation of Charge.

**Kirchhoffs Current Law**

Currents Entering the Node
Equals
Currents Leaving the Node




$$I_1 + I_2 + I_3 + (-I_4 + -I_5) = 0$$

Here, the 3 currents entering the node, $I_1$, $I_2$, $I_3$ are all positive in value and the 2 currents leaving the node, $I_4$ and $I_5$ are negative in value. Then this means we can also rewrite the equation as;

$$I_1 + I_2 + I_3 - I_4 - I_5 = 0$$

The term Node in an electrical circuit generally refers to a connection or junction of two or more current carrying paths or elements such as cables and components. Also for current to flow either in or out of a node a closed circuit path must exist. We can use Kirchhoff's current law when analysing parallel circuits.

**Kirchhoffs Second Law – The Voltage Law, (KVL)**

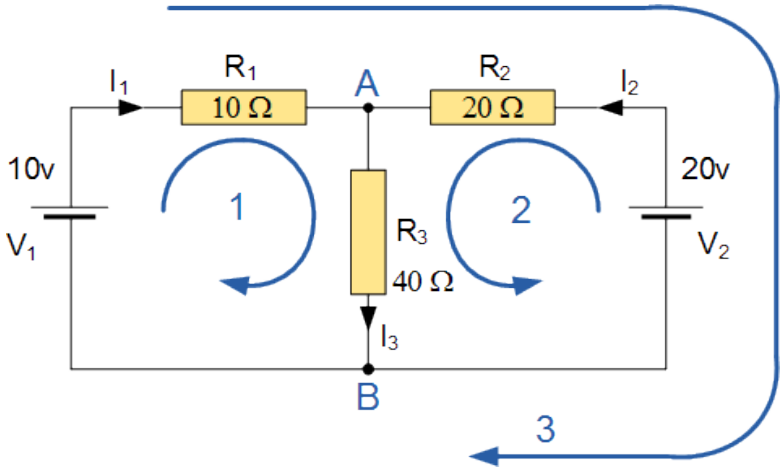
Kirchhoffs Voltage Law or KVL, states that "in any closed loop network, the total voltage around the loop is equal to the sum of all the voltage drops within the same loop" which is also equal to zero. In other words the algebraic sum of all voltages within the loop must be equal to zero. This idea by Kirchhoff is known as the Conservation of Energy.

**Common DC Circuit Theory Terms:**

- Circuit – a circuit is a closed loop conducting path in which an electrical current flows.
- Path – a single line of connecting elements or sources.
- Node – a node is a junction, connection or terminal within a circuit were two or more circuit elements are connected or joined together giving a connection point between two or more branches. A node is indicated by a dot.
- Branch – a branch is a single or group of components such as resistors or a source which are connected between two nodes.
- Loop – a loop is a simple closed path in a circuit in which no circuit element or node is encountered more than once.
- Mesh – a mesh is a single open loop that does not have a closed path. There are no components inside a mesh.

Problem

Find the current flowing in the 40Ω Resistor, $R_3$




The circuit has 3 branches, 2 nodes (A and B) and 2 independent loops.

Using Kirchhoffs Current Law, KCL the equations are given as;

$$\text{At node A :} \quad I_1 + I_2 = I_3$$

$$\text{At node B :} \quad I_3 = I_1 + I_2$$

Using Kirchhoffs Voltage Law, KVL the equations are given as;

$$\text{Loop 1 is given as :} \quad 10 = R_1 I_1 + R_3 I_3 = 10I_1 + 40I_3$$

$$\text{Loop 2 is given as :} \quad 20 = R_2 I_2 + R_3 I_3 = 20I_2 + 40I_3$$

$$\text{Loop 3 is given as :} \quad 10 - 20 = 10I_1 - 20I_2$$

As $I_3$ is the sum of $I_1 + I_2$ we can rewrite the equations as;

$$\text{Eq. No 1 :} \quad 10 = 10I_1 + 40(I_1 + I_2) = 50I_1 + 40I_2$$

Eq. No 2 : $20 = 20I_2 + 40(I_1 + I_2) = 40I_1 + 60I_2$

We now have two "Simultaneous Equations" that can be reduced to give us the values of $I_1$ and $I_2$

Substitution of $I_1$ in terms of $I_2$ gives us the value of $I_1$ as -0.143 Amps

Substitution of $I_2$ in terms of $I_1$ gives us the value of $I_2$ as +0.429 Amps

As : $I_3 = I_1 + I_2$

The current flowing in resistor $R_3$ is given as : -0.143 + 0.429 = 0.286 Amps

and the voltage across the resistor $R_3$ is given as : 0.286 x 40 = 11.44 volts

The negative sign for $I_1$ means that the direction of current flow initially chosen was wrong, but never the less still valid. In fact, the 20v battery is charging the 10v battery.

**MESH ANALYSIS**

An easier method of solving the above circuit is by using Mesh Current Analysis or Loop Analysis which is also sometimes called Maxwell´s Circulating Currents method. Instead of labelling the branch currents we need to label each "closed loop" with a circulating current.

As a general rule of thumb, only label inside loops in a clockwise direction with circulating currents as the aim is to cover all the elements of the circuit at least once. Any required branch current may be found from the appropriate loop or mesh currents as before using Kirchhoff´s method.

For example: : $i_1 = I_1$ , $i_2 = -I_2$ and $I_3 = I_1 - I_2$

**Steps to solve problems using Mesh analysis**

- Label all the internal loops with circulating currents. ($I_1$, $I_2$, …$I_L$ etc)
- Write the [ L x 1 ] column matrix [ V ] giving the sum of all voltage sources in each loop.
- Write the [ L x L ] matrix, [ R ] for all the resistances in the circuit as follows;
    - $R_{11}$ = the total resistance in the first loop.
    - $R_{nn}$ = the total resistance in the Nth loop.
    - $R_{JK}$ = the resistance which directly joins loop J to Loop K.
- Write the matrix or vector equation [V] = [R] x [I] where [I] is the list of currents to be found.

**NODAL VOLTAGE ANALYSIS**

Nodal Voltage Analysis uses the "Nodal" equations of Kirchhoff's first law to find the voltage potentials around the circuit. So by adding together all these nodal voltages the net result will be equal to zero. Then, if there are "n" nodes in the circuit there will be "n-1" independent nodal equations and these alone are sufficient to describe and hence solve the circuit.

At each node point write down Kirchhoff's first law equation, that is: "the currents entering a node are exactly equal in value to the currents leaving the node" then express each current in terms of the voltage across the branch. For "n" nodes, one node will be used as the reference node and all the other voltages will be referenced or measured with respect to this common node.

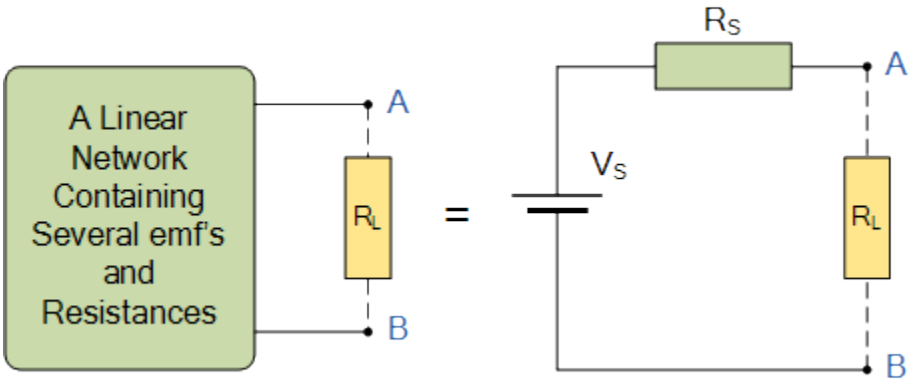
**The basic procedure for solving Nodal Analysis equations is as follows:**

- Write down the current vectors, assuming currents into a node are positive. ie, a (N x 1) matrices for "N" independent nodes.
- Write the admittance matrix [Y] of the network where:
    - $Y_{11}$ = the total admittance of the first node.
    - $Y_{22}$ = the total admittance of the second node.
    - $R_{JK}$ = the total admittance joining node J to node K.
- For a network with "N" independent nodes, [Y] will be an (N x N) matrix and that Ynn will be positive and Yjk will be negative or zero value.

- The voltage vector will be (N x L) and will list the "N" voltages to be found.

**THEVENIN'S THEOREM**

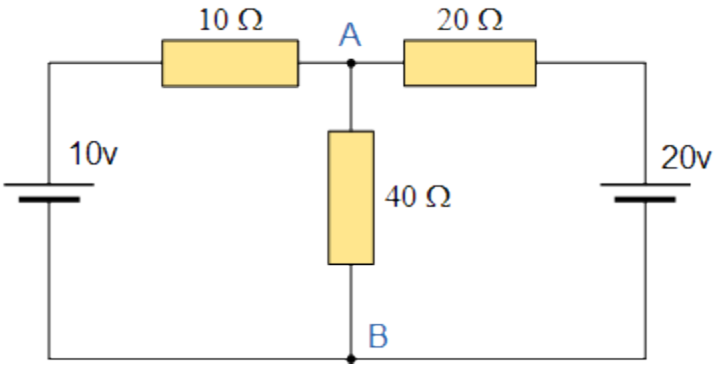
Thevenin's Theorem states that "Any linear circuit containing several voltages and resistances can be replaced by just one single voltage in series with a single resistance connected across the load". In other words, it is possible to simplify any electrical circuit, no matter how complex, to an equivalent two-terminal circuit with just a single constant voltage source in series with a resistance (or impedance) connected to a load as shown below. Thevenin's Theorem is especially useful in the circuit analysis of power or battery systems and other interconnected resistive circuits where it will have an effect on the adjoining part of the circuit.




**The basic procedure for solving a circuit using Thevenin's Theorem is as follows:**

- Remove the load resistor $R_L$ or component concerned.
- Find $R_S$ by shorting all voltage sources or by open circuiting all the current sources.
- Find $V_S$ by the usual circuit analysis methods.
- Find the current flowing through the load resistor $R_L$.

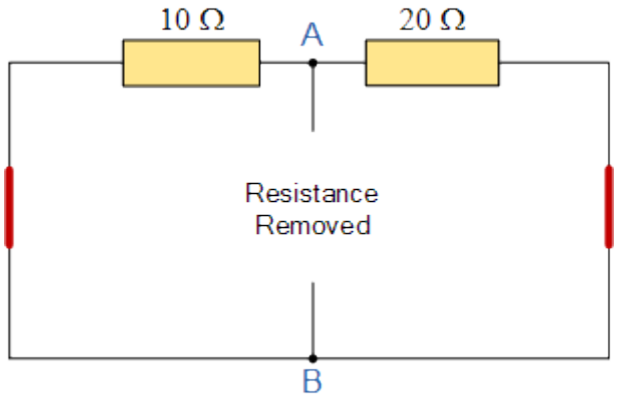
**Example**




we have to remove the centre 40Ω load resistor connected across the terminals A-B, and remove any internal resistance associated with the voltage source(s). This is done by shorting out all the

voltage sources connected to the circuit, that is v = 0, or open circuit any connected current sources making i = 0. The reason for this is that we want to have an ideal voltage source or an ideal current source for the circuit analysis.

The value of the equivalent resistance, Rs is found by calculating the total resistance looking back from the terminals A and B with all the voltage sources shorted. We then get the following circuit.



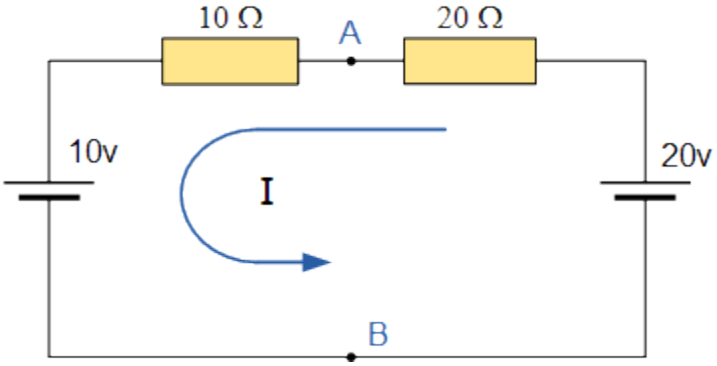

Find the Equivalent Resistance (Rs)

10Ω Resistor in Parallel with the 20Ω Resistor

$$Rt=R1xR2/R1+R2 = \Omega 6.67$$

The voltage Vs is defined as the total voltage across the terminals A and B when there is an open circuit between them. That is without the load resistor $R_L$ connected.

Find the Equivalent Voltage (Vs)




We now need to reconnect the two voltages back into the circuit, and as $V_S = V_{AB}$ the current flowing around the loop is calculated as:

$$I=V/R = 20v-10v/20\Omega+10\Omega = 0.33 \text{ amps}$$

This current of 0.33 amperes (330mA) is common to both resistors so the voltage drop across the 20Ω resistor or the 10Ω resistor can be calculated as:

$$V_{AB} = 20 - (20\Omega \times 0.33\text{amps}) = 13.33 \text{ volts.}$$

or

$$V_{AB} = 10 + (10\Omega \times 0.33\text{amps}) = 13.33 \text{ volts, the same.}$$

Then the Thevenin's Equivalent circuit would consist or a series resistance of 6.67Ω's and a voltage source of 13.33v.

and from this the current flowing around the circuit is given as:

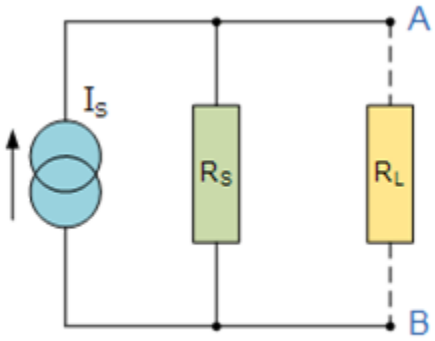
$$I=V/R = 13.33 \text{ V}/6.67\Omega+40\Omega=0.286 \text{ amps}$$

which again, is the same value of 0.286 amps, we found using Krichoff's circuit law

**NORTONS THEOREM**

Nortons Theorem states that "Any linear circuit containing several energy sources and resistances can be replaced by a single Constant Current generator in parallel with a Single Resistor".

As far as the load resistance, $R_L$ is concerned this single resistance, $R_S$ is the value of the resistance looking back into the network with all the current sources open circuited and $I_S$ is the short circuit current at the output terminals



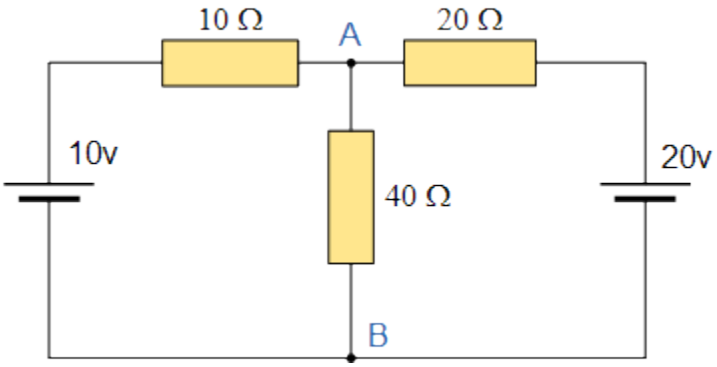

The value of this "constant current" is one which would flow if the two output terminals where shorted together while the source resistance would be measured looking back into the terminals.

**The basic procedure for solving a circuit using Nortons Theorem is as follows:**

- Remove the load resistor $R_L$ or component concerned.
- Find $R_S$ by shorting all voltage sources or by open circuiting all the current sources.
- Find $I_S$ by placing a shorting link on the output terminals A and B.

- Find the current flowing through the load resistor $R_L$.

**EXAMPLE**




To find the Norton equivalent of the above circuit we firstly have to remove the centre 40Ω load resistor and short out the terminals A and B to give us the following circuit.

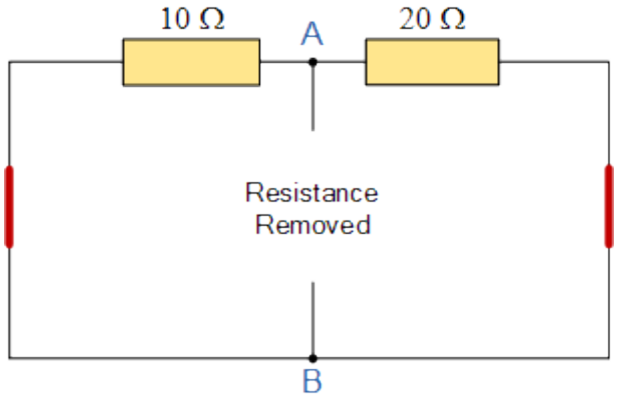
When the terminals A and B are shorted together the two resistors are connected in parallel across their two respective voltage sources and the currents flowing through each resistor as well as the total short circuit current can now be calculated as:

with A-B Shorted Out

$$I1=10v/10\Omega= 1 \text{ amp}, I2= 20V/20\Omega$$

$$\text{Therefore, } I_{\text{short-circuit}} = I1+I2 = 2 \text{ amps}$$

If we short-out the two voltage sources and open circuit terminals A and B, the two resistors are now effectively connected together in parallel. The value of the internal resistor Rs is found by calculating the total resistance at the terminals A and B giving us the following circuit.



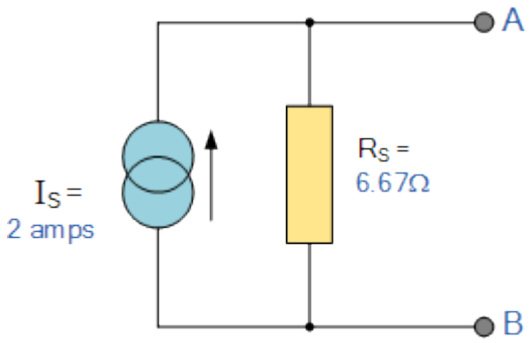

Find the Equivalent Resistance (Rs)

10Ω Resistor in parallel with the 20Ω Resistor

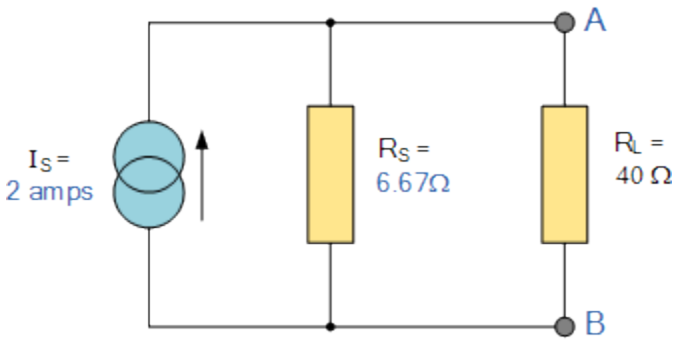
$$R_T = R1xR2/R1+R2=20x10/20+10 =6.67\Omega$$

Having found both the short circuit current, Is and equivalent internal resistance, Rs this then gives us the following Nortons equivalent circuit.

**Nortons equivalent circuit.**




To solve with the original 40Ω load resistor connected across terminals A and B as shown below.




Again, the two resistors are connected in parallel across the terminals A and B which gives us a total resistance of:

$$R_T = R1xR2/R1+R2 = 6.67x40/6.67+40 = 5.72\Omega$$

The voltage across the terminals A and B with the load resistor connected is given as:

$$V_{A-B} = IxR = 2x5.72 = 11.44v$$

Then the current flowing in the 40Ω load resistor can be found as:

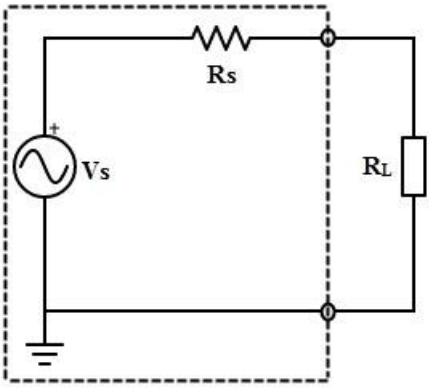
$$I = V/R = 11.4/40 = 0.286 \text{ amps}$$

which again, is the same value of 0.286 amps, we found using Krichoff's circuit law

**MAXIMUM POWER TRANSFER THEOREM**

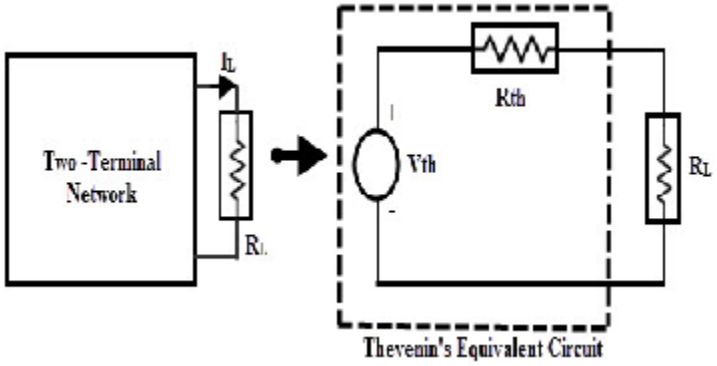
The maximum power transfer theorem states that in a linear, bilateral DC network, maximum power is delivered to the load when the load resistance is equal to the internal resistance of a source.

If it is an independent voltage source, then its series resistance (internal resistance Rs) or if it is independent current source, then its parallel resistance (internal resistance Rs) must equal to the load resistance RL to deliver maximum power to the load.




The maximum power transfer theorem ensures the value of the load resistance, at which the maximum power is transferred to the load.

Consider the below two terminal network to which the condition for maximum power is determined , by obtaining the expression of power absorbed by load with use of mesh or nodal current methods and then derive the resulting expression with respect to load resistance RL.



The original two terminal circuit is replaced with a Thevenin's equivalent circuit across the variable load resistance. The current through the load for any value of load resistance is

$$I_L = \frac{V_{Th}}{R_{Th} + R_L}$$

The power absorbed by the load is

$$P_L = I_L^{\,2} \times R_L$$

$$= \left[\frac{V_{Th}}{R_{Th} + R_L}\right]^2 \times R_L$$

Form the above expression the power delivered depends on the values of $R_{TH}$ and $R_L$. However the Thevenin's equivalent is constant, the power delivered from this equivalent source to the load entirely depends on the load resistance $R_L$. To find the exact value of RL, we apply differentiation to $P_L$ with respect to $R_L$ and equating it to zero as

$$\frac{dP(R_L)}{dR_L} = V_{Th}^{\,2}\left[\frac{(R_{Th} + R_L)^2 - 2R_L \times (R_{Th} + R_L)}{(R_{Th} + R_L)^4}\right] = 0$$

$$\Rightarrow (R_{Th} + R_L) - 2R_L = 0$$

$$\Rightarrow R_L = R_{Th}$$

Therefore, this is the condition of matching the load where the maximum power transfer occurs when the load resistance is equal to the Thevenin's resistance of the circuit. By substituting the $R_{th} = R_L$ in equation 1 we get

The maximum power delivered to the load is,

$$P_{\max} = \left[\frac{V_{Th}}{R_{Th} + R_L}\right]^2 \times R_L \Big|_{R_L = R_{Th}}$$

$$= \frac{V_{Th}^{\ 2}}{4 R_{Th}}$$

Total power transferred from source is

$$P_T = I_L^2 (R_{TH} + R_L)$$

$$= 2\, I_L^2 R_L \ \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Hence , the maximum power transfer theorem expresses the state at which maximum power is delivered to the load , that is , when the load resistance is equal to the Thevenin's equivalent resistance of the circuit. Below figure shows a curve of power delivered to the load with respect to the load resistance.

**SUPERPOSITION THEOREM**

For analyzing the linear electric circuits that consists of two or more independent sources (Voltage or current or both), superposition theorem is extremely used (particularly for time domain circuits with elements operated at different frequencies). If a linear DC circuit has more than one independent source, we can find the current (through a resistance) and voltage (across the resistance) by using nodal or mesh analysis methods. Alternatively, we can use the superposition theorem that adds each individual source effect on the value of the variable to be determined. This means superposition theorem considers the each source in a given circuit

separately for finding the value of the variable (whether current or voltage) and finally produce the resultant variable by adding all the variables caused by each source effect. Even though it is of complex procedure, but still can be applied for any linear circuit.

The superposition theorem states that in any linear bilateral network that consisting of two or more independent sources, current through (or voltage across) an element is the algebraic sum of the currents through (voltages across) that element caused by each independent source acting alone with all other sources is replaced by their internal resistances.

**Steps to Analyze Superposition Theorem**

1. Consider the various independent sources in a given circuit.

2. Select and retain one of the independent sources and replace all other sources with their internal resistances or else replace the current sources with open circuits and voltage sources with short circuits.

3. To avoid confusion re-label the voltage and current notations suitably.

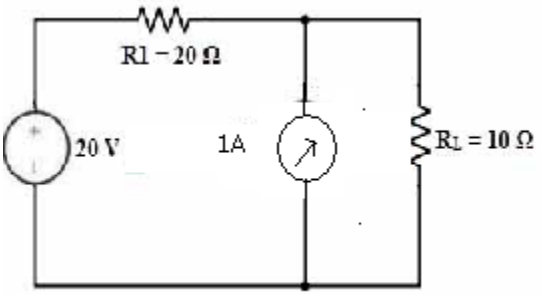
4. Find out the desired voltage/currents due to the one source acting alone using various circuit reduction techniques.

5. Repeat the steps 2 to 4 for each independent source in the given circuit.

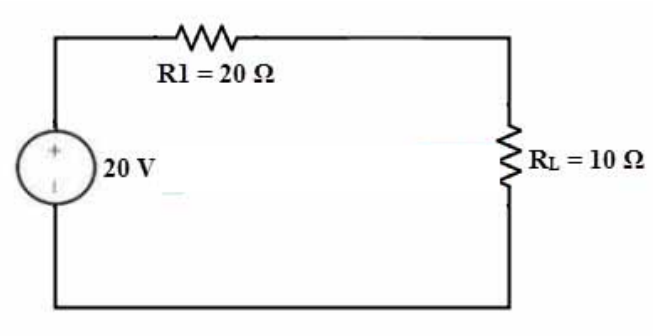
6. Algebraically add all the voltages/currents that are obtained from each individual source (Consider the voltage signs and current directions while adding).

**Example :**

Let us consider the below simple DC circuit to apply the superposition theorem such that we will obtain the voltage across the resistance 10 Ohms (load terminals). Consider that in a given circuit there are two independent sources as voltage and current sources as shown in figure.




First, we retain one source at a time that means , only voltage source is acting in the circuit and the current source is replaced with internal resistance (infinite) so it becomes open circuited as shown in figure.



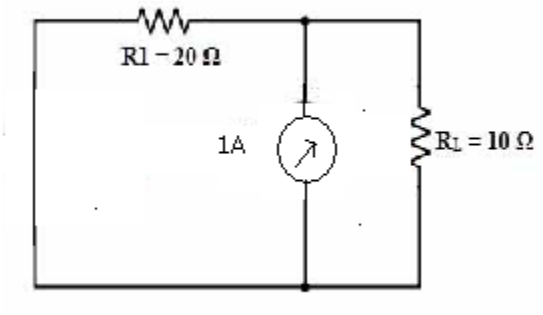

Consider $V_{L1}$ is the voltage across the load terminals with voltage source acting alone, then

$$V_{L1} = Vs \times R_L / (R_L + R_1)$$

$$= 20 \times 10 / (10 + 20)$$

= 6. 66 Volts

Retain the current source alone and replace the voltage source with its internal resistance (zero) so it becomes a short circuited as shown in figure




Consider that $V_{L2}$ is the voltage across the load terminals when current source acting alone. Then

$$V_{L2} = I_L \times R_L$$

$$I_L = I \times R_1 / (R_1 + R_L)$$

=1x20/20+30

= 0.4 Amps

$$V_{L2} = 0.4 \times 10$$

= 4 Volts

Therefore, according the superposition theorem, the voltage across the load is the sum of $V_{L1}$ and $V_{L2}$

$$V_L = V_{L1} + V_{L2}$$

$$= 6.66 + 4$$

$$= 10.66 \text{ Volts}$$

## POSSIBLE QUESTIONS

**PART-B( 2 Marks)**

1. Define Kirchhoff's voltage law.
2. Define Kirchhoff's current law.
3. State Thevein's theorem.
4. State Norton's theorem.
5. State Superposition Theorem.
6. State Maximum power transfer theorem.
7. State Ohm's law.
8. What are the advantages of Network analysis?
9. What is called linear network?
10. What is called linear bilateral network?

**PART-C ( 6 Marks)**

1. State and explain Kirchhoff's laws using neat diagrams.
2. State superposition theorem. Prove this theorem in a case of general network.
3. State Thevenin's theorem and prove it in the case of two terminal network.
4. What is the maximum power transfer theorem? Show that power lost in the internal generator is equal to the power delivered to the load, and the power efficiency is only 50%.
5. State and explain Norton's theorem.
6. Give the statement of Norton's theorem. Prove that the interchange of voltage and current sources with the help of Thevenin's and Norton's theorems and give a method of circuit analysis.
7. What is called Mesh analysis? Discuss the steps to solve problems using Mesh analysis with an example.
8. What is called Nodal analysis? Discuss the steps to solve problems using Nodal analysis with an example.

**KARPAGAM ACADEMY OF HIGHER EDUCATION**
**Coimbatore - 641021.**
**(For the candidates admitted from 2018onwards)**
**DEPARTMENT OF PHYSICS**
**UNIT V :(Objective Type/Multiple choice Questions each Question carries one Mark )**
**PART-A (Online Examination)**
**ELECTRONIC DEVICES AND CIRCUITS**

| QUESTIONS | CHOICE1 | CHOICE2 | CHOICE3 | CHOICE4 | ANSWER |
|---|---|---|---|---|---|
| **UNIT V** | | | | | |
| Kirchhoff's Voltage Law states that the total voltage around a closed loop must be | 0 | ½ | 1 | 2 | 0 |
| The algebraic sum of _____ in a network of conductors meeting at a point is zero. | Voltages | currents | Resistances | Inductances | currents |
| Maximum power transfer theorem is also known as | Jacobi's law | Thompson's law | Phillips law | Jackson's law | Jacobi's law |
| The _____ theorem is a way to determine the currents and voltages present in a circuit that has multiple sources. | Norton | Super position | Thevenin | Maximum power transfer | Super position |
| The concept on which Superposition theorem is based is | reciprocity | duality | non-linearity | linearity | linearity |
| Kirchhoff s law is applicable to | passive networks only | a.c. circuits only | d.c. circuits only | both a.c. as well d.c. circuits | both a.c. as well d.c. circuits |
| For maximum transfer of power, internal resistance of the source should be | equal to load resistance | less than the load resistance | greater than the load resistance | none of the above | equal to load resistance |
| Kirchhoffs current law is applicable to only | junction in a network | closed loops in a network | electric circuits | electronic circuits | junction in a network |
| Kirchhoff's voltage law is related to | junction currents | battery emfs | IR drops | both b & c | both b & c |
| Superposition theorem can be applied only to circuits having | resistive elements | passive elements | non-linear elements | linear bilateral elements | linear bilateral elements |

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| The concept on which superposition theorem is based on | reciprocity | duality | non-linearity | linearity | linearity |
| Which of the following is non-linear circuit parameter? | Inductance | condenser | wire wound resistor | transistor | Inductance |
| Node analysis can be applied for | planar networks | Non-planar networks | Both a & b | electric networks | Both a & b |
| Mesh analysis is applicable for | planar networks | Non-planar networks | Both a & b | electric networks | planar networks |
| The superposition theorem is applicable to | voltage only | current only | current and voltage | current, voltage and power | current, voltage and power |
| Kirchhoff's current law is applicable only to | junction in a network | closed loops in a network | electric circuits | electronic circuits | junction in a network |
| Maximum power output is obtained from a network when the load resistance is equal to the output resistance of the network as seen from the terminals of the load".The above statement is associated with | Millman's theorem | Thevenin's theorem | Superposition theorem | Maximum power transfer theorem | Maximum power transfer theorem |
| Kirchhoffs current law is applicable to only | junction in a network | closed loops in a network | electric circuits | electronic circuits | junction in a network |
| Superposition theorem is based on | Reciprocity | duality | non-linearity | Linearity | Linearity |
| The Norton current is sometimes called the | shorted-load current | open-load current | Thevenin current | Thevenin voltage | shorted-load current |
| Kirchhoff s current law states that | net current flow at the junction is positive | Hebraic sum of the currents meeting at the junction is zero | no curreht can leave the junction without some current entering it. | total sum of currents meeting at the junction is zero | Hebraic sum of the currents meeting at the junction is zero |
| According to Kirchhoffs voltage law, the algebraic sum of all IR drops and e.m.fs. in any closed loop of a network is always | negative | ositive | determined by battery e.m.fs. | zero | zero |

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| Kirchhoffs current law is applicable to only | junction in a network | closed loops in a network | electric circuits | electronic circuits | junction in a network |
| Kirchhoffs voltage law is related to | junction currents | battery e.m.fs. | IR drops | both (b) and (c) | both (b) and (c) |
| Superposition theorem can be applied only to circuits having | resistive elements | passive elements | non-linear elements | linear bilateral elements | linear bilateral elements |
| The concept on which Superposition theorem is based is | eciprocity | duality | non-linearity | linearity | linearity |
| Thevenin resistance Rth is found | by removing voltage sources along with their internal resistances | by short-circuiting the given two terminals | between any two 'open' terminals | between same open terminals as for Etk | between same open terminals as for Etk |
| An ideal voltage source should have | large value of e.m.f. | small value of e.m.f. | zero source resistance | infinite source resistance | zero source resistance |
| For a voltage source | terminal voltage is always lower than source e.m.f. | terminal voltage cannot be higher than source e.m.f. | the source e.m.f. and terminal voltage are equal | | terminal voltage cannot be higher than source e.m.f. |
| To determine the polarity of the voltage drop across a resistor, it is necessary to know | value of current through the resistor | direction of current through the resistor | value of resistor | e.m.fs. in the circuit | direction of current through the resistor |
| "Maximum power output is obtained from a network when the load resistance is equal to the output resistance of the network as seen from the terminals of the load". The above statement is associated with | Millman's theorem | Thevenin's theorem | Superposition theorem | Maximum power transfer theorem | Maximum power transfer theorem |

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| "Any number of current sources in parallel may be replaced by a single current source whose current is the algebraic sum of individual source currents and source resistance is the parallel combination of individual source resistances". The above statement is associated with | Thevenin's theorem | Millman's theorem | Maximum power transfer theorem | None of the above | Millman's theorem |
| "In any linear bilateral network, if a source of e.m.f. E in any branch produces a current I in any other branch, then same e.m.f. acting in the second branch would produce the same current / in the first branch".The above statement is associated with | compensation theorem | superposition theorem | reciprocity theorem | none of the above | reciprocity theorem |
| Which of the following is non-linear circuit parameter ? | Inductance | Condenser | Wire wound resistor | Transistor | Inductance |
| A capacitor is generally a | bilateral and active component | active, passive, linear and nonlinear component | linear and bilateral component | non-linear and active component | linear and bilateral component |
| "In any network containing more than one sources of e.m.f. the current in any branch is the algebraic sum of a number of individual fictitious currents (the number being equal to the number of sources of e.m.f.), each of which is due to separate action of each source of e.m.f., taken in order, when the remaining sources of e.m.f. are replaced by conductors, the resistances of which are equal to the internal resistances of the respective sources". The above statement is associated with | Thevenin's theorem | Norton's theorem | Superposition theorem | None of the above | Superposition theorem |
| Kirchhoff s law is applicable to | passive networks only | a.c. circuits only | d.c. circuits only | both a.c. as well d.c. circuits | both a.c. as well d.c. circuits |

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| Kirchhoff s law is not applicable to circuits with | lumped parameters | passive elements | distributed parameters | non-linear resistances | distributed parameters |
| Kirchhoff s voltage law applies to circuits with | nonlinear elements only | linear elements only | linear, non-linear, active and passive elements | linear, non-linear, active, passive, time varying as wells as time-in-variant elements | linear, non-linear, active, passive, time varying as wells as time-in-variant elements |
| The resistance LM will be | 6.66 Q | 12 Q | 18Q | 20Q | 6.66 Q |
| For high efficiency of transfer of power, internal resistance of the source should be | equal to the load resistance | less than the load resistance | more than the load resistance | none of the above | less than the load resistance |
| Efficiency of power transfer when maximum transfer of power c xurs is | 100% | 80% | 75% | 50% | 50% |
| If resistance across LM in Fig. 2.30 is 15 ohms, the value of R is | 10 Q | 20 Q | 30 Q | 40 Q | 30 Q |
| For maximum transfer of power, internal resistance of the source should be | equal to load resistance | less than the load resistance | greater than the load resistance | none of the above | equal to load resistance |
| If the energy is supplied from a source, whose resistance is 1 ohm, to a load of 100 ohms the source will be | a voltage source | a current source | both of above | none of the above | a voltage source |
| The circuit whose properties are same in either direction is known as | unilateral circuit | bilateral circuit | irreversible circuit | reversible circuit | bilateral circuit |
| In a series parallel circuit, any two resistances in the same current path must be in | series with each other | parallel with each other | series with the voltage source.' | parallel with the voltage source | series with each other |
| The circuit has resistors, capacitors and semi-conductor diodes. The circuit will be known as | non-linear circuit | linear circuit | bilateral circuit | none of the above | non-linear circuit |

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| A non-linear network does not satisfy | superposition condition | homogeneity condition | both homogeneity as well as superposition condition | homogeneity, superposition and associative condition | both homogeneity as well as superposition condition |
| An ideal voltage source has | zero internal resistance | open circuit voltage equal to the voltage on full load | terminal voltage in proportion to current | terminal voltage in proportion to load | zero internal resistance |
| A network which contains one or more than one source of e.m.f. is known as | linear network | non-linear network | passive network | active network | passive network |
| The superposition theorem is applicable to | linear, non-linear and time variant responses | linear and non-linear resistors only | linear responses only | none of the above | linear responses only |
| Which of the following is not a nonlinear element ? | Gas diode | Heater coil | Tunnel diode | Electric arc | |
| Application of Norton's theorem to a circuit yields | equivalent current source and impedance in series | equivalent current source and impedance in parallel | equivalent impedance | equivalent current source | equivalent current source and impedance in series |
| Millman's theorem yields | equivalent resistance | equivalent impedance | equivalent voltage source | equivalent voltage or current source | equivalent voltage or current source |
| The superposition theorem is applicable to | voltage only | current "only | both current and voltage | current voltage and power | current voltage and power |
| Between the branch voltages of a loop the Kirchhoff s voltage law imposes | non-linear constraints | linear constraints | no constraints | none of the above | linear constraints |

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| A passive network is one which contains | only variable resistances | only some sources of e.m.f. in it | only two sources of e.m.f. in it | no source of e.m.f. in it | no source of e.m.f. in it |
| A terminal where three on more branches meet is known as | node | terminus | combination | anode | node |
| Which of the following is the passive element ? | Capacitance | Ideal current source | Ideal voltage source | All of the above | Capacitance |
| Which of the following is a bilateral element ? | Constant current source | Constant voltage source | Capacitance | None of the above | Capacitance |
| A closed path made by several branches of the network is known as | branch | loop | circuit | junction | loop |
| A linear resistor having 0 < R < °o is a | current controlled resistor | voltage controlled resistor | both current controlled and voltage controlled resistor | none of the above | both current controlled and voltage controlled resistor |
| A star circuit has element of resistance R/2. The equivalent delta elements will be | R/6 | fi? | 2R | 4R | fi? |
| A delta circuit has each element of value R/2. The equivalent elements of star circuit with be | RIG | R/3 | 2R | 3R | RIG |
| In Thevenin's theorem, to find Z | all independent current sources are short circuited and independent voltage sources are open circuited | all independent voltage sources are open circuited and all independent current sources are short circuited | all independent voltage and current sources are short circuited | all independent voltage sources are short circuited and all independent current sources are open circuited | all independent voltage sources are short circuited and all independent current sources are open circuited |

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| While calculating Rth in Thevenin's theorem and Norton equivalent | all independent sources are made dead | only current sources are made dead | only voltage sources are made dead | all voltage and current sources are made dead | all independent sources are made dead |
| The number of independent equations to solve a network is equal to | the number of chords | the number of branches | sum of the number of branches and chords | sum of number of branches, chords and nodes | the number of chords |
| The superposition theorem requires as many circuits to be solved as there are | sources, nodes and meshes | sources and nodes | sources | nodes | sources |
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