

## SEMESTER – III

18PHP312

ADVANCED ELECTRONICS PRACTICAL

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### ANY TEN EXPERIMENTS

1. Microprocessor – LED interfacing, Musical tone generator interface
2. Microprocessor – Stepper motor interfacing, ADC interface wave form generation
3. Microprocessor –Traffic control simulation
4. Microprocessor –Hex Key board interfacing
5. Multiplexer and de-multiplexer
6. Ring counter using IC's
7. 4-bit binary adder
8. 4-bit binary subtractor
9. Half adder and Half subtractor
10. Full adder and full subtractor
11. BCD counter, using IC 7490 and 7473.
12. A/D Converters any one method, D/A converter – Binary weighted, Ladder methods

### REFERENCES

1. Ramesh Gaonkar ,2013, Microprocessor Architecture Programming and Applications with 8085, 6<sup>th</sup> edition, PENRAM International Pvt Ltd
2. [www.mathworks.com](http://www.mathworks.com)

### Half adder and Half subtractor

#### AIM

1. To design and set up half adder and half subtractor using a. EXOR gates and AND gates
- b. NAND gates

#### COMPONENTS REQUIRED

IC Trainer kit, IC 7400, IC 7486

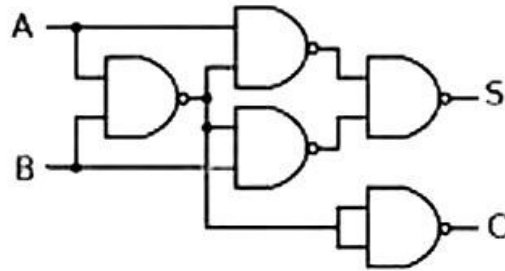
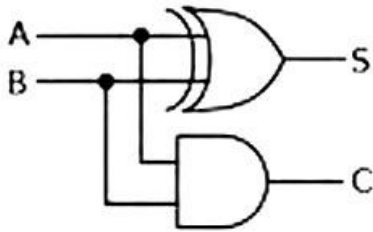
#### PROCEDURE

The simplest binary adder is called half adder. Half adder has two input bits and two output bits. One output bit is the sum and the other is the carry. They are represented by 'S' and 'C' respectively in logic symbol.

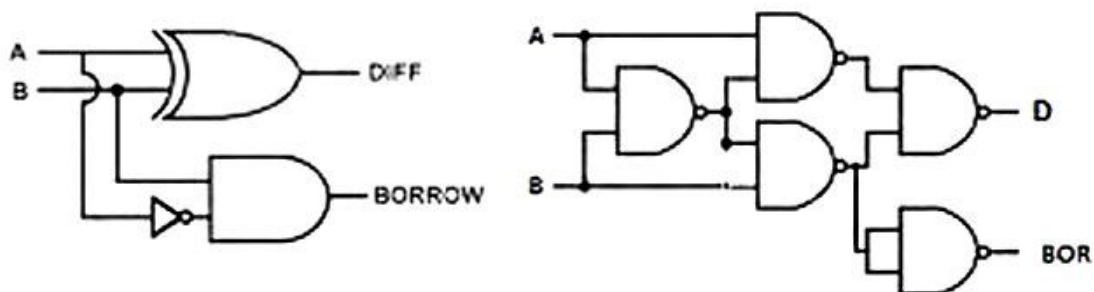
The simplest binary subtractor is called half Subtractor. It has two input bits and two output bits. One output bit is the Difference and the other is borrowed. They are represented by 'D' and 'B' respectively in logic symbol

**Truth table of Half Adder and Half Subtractor**

Truth table of Half Adder				Truth table of Half Subtractor			
Inputs		Output		Inputs		Output	
A	B	S	C	A	B	D	BOR
0	0	0	0	0	0	0	0
0	1	1	0	0	1	1	1
1	0	1	0	1	0	1	0
1	1	0	1	1	1	0	0



**Logic Gate circuits of Half adder for NAND gate**



**Logic Gate circuits of Half subtractor for NAND gate**

**RESULT**

Half adder and Half subtractor are constructed and their truth tables are verified.

### Full adder and Full subtractor

#### AIM

1. To design and set up full adder and full subtractor using
  - a. EXOR gates and AND gates
  - b. NAND gates

#### COMPONENTS REQUIRED

IC Trainer kit, ICS 7400, IC 7486

#### PRINCIPLE

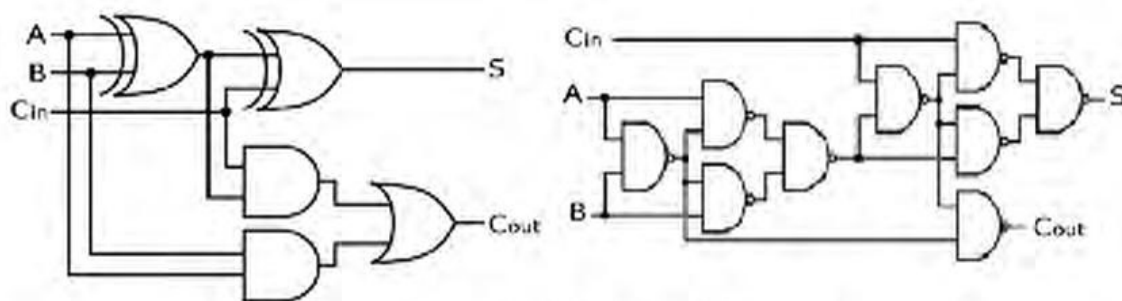
A half adder has no provision to add a carry from the lower order bits when binary numbers are added. When two input bits and a carry are to be added the number of input bits becomes three and the input combination increases to eight. For this full adder is used. Like half adder it also has a sum bit and a carry bit. The new carry generated is represented by 'Cout' and the carry generated from the previous addition is represented by 'Cin'.

When two input bits and a borrow have to be subtracted the number of input bits equal to three and the input combinations increases to eight, for this a full subtractor is used.

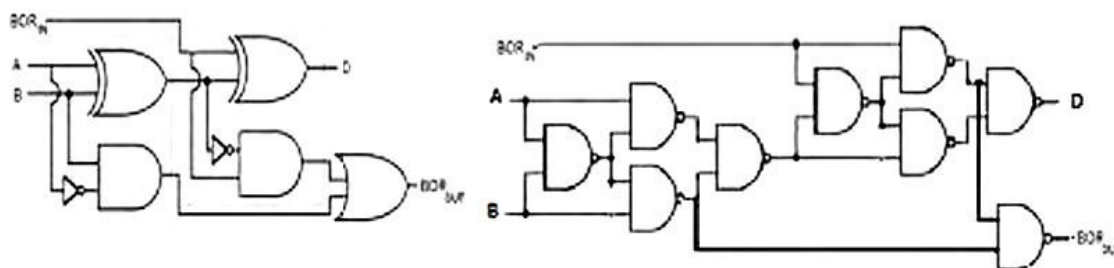
**Truth table of Full Adder and Full Subtractor**

Truth table of Full Adder					Truth table of Full Subtractor				
Inputs			Output		Inputs			Output	
A	B	Cin	S	Cout	A	B		D	
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	1	1
0	1	0	1	0	0	1	0	1	1

0	1	1	0	1		0	1	1	0	1
1	0	0	1	0		1	0	0	1	0
1	0	1	0	1		1	0	1	0	0
1	1	0	0	1		1	1	0	0	0
1	1	1	1	1		1	1	1	1	1



**Logic Gate circuits of Full adder for NAND gate**



**Logic Gate circuits of Full subtractor for NAND gate**

## PROCEDURE

1. Verify whether all the wires and components are in good condition
2. Set up full adder circuit and feed all the input combinations
3. Observe the output corresponding to input combinations and enter it in the Truth table
4. Repeat the above steps for Full subtractor circuits

## RESULT

Full adder and Full subtractor circuit was constructed and the truth table was verified

## Digital Comparator

### AIM

To design and setup single bit comparator using logic gates and verify the truth table.

### PRINCIPLE

Digital or Binary Comparators compares the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

The digital comparator accomplishes this using several logic gates that operate on the principles of Boolean algebra. The purpose of a Digital Comparator is to compare a set of variables or unknown numbers, for example A ( $A_1, A_2, A_3, \dots A_n$ , etc) against that of a constant or unknown value such as B ( $B_1, B_2, B_3, \dots B_n$ , etc) and produce an output condition or flag depending upon the result of the comparison. There are two main types of Digital Comparator available and these are.

**Identity Comparator** - an *Identity Comparator* is a digital comparator that has only one output terminal for when the inputs  $A = B$

**Magnitude Comparator** - a *Magnitude Comparator* is a type of digital comparator that has three output terminals, one each for equality ( $A = B$ ), greater than ( $A > B$ ) and less than ( $A < B$ )

This is useful if we want to compare two variables and want to produce an output when any of the above three conditions are achieved. For example, produce an output from a counter when a certain count number is reached. Consider the truth table of simple 1-bit

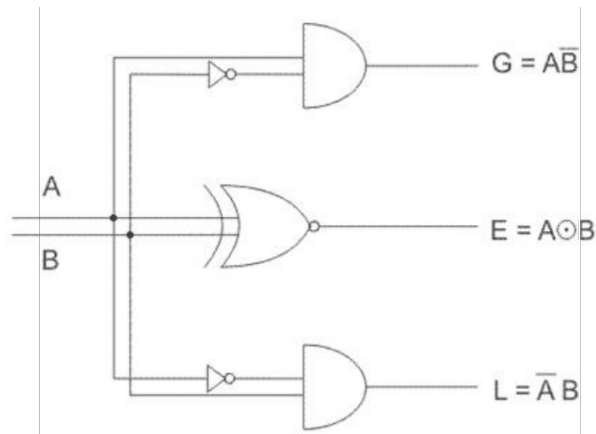
comparator.

#### Truth table of digital- comparator

INPUT		OUTPUT		
B	A	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1



Digital comparators actually use Exclusive-NOR gates within their design for comparing their respective pairs of bits. When we are comparing two binary or BCD values or variables against each other, we are comparing the "magnitude" of these values, logic "0" against a logic "1" which is where the term Magnitude Comparator comes from.



## RESULT

Designed and setup single bit comparator using logic gates and verified the truth table.

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**BCD to Excess – 3 code convertor**

**AIM**

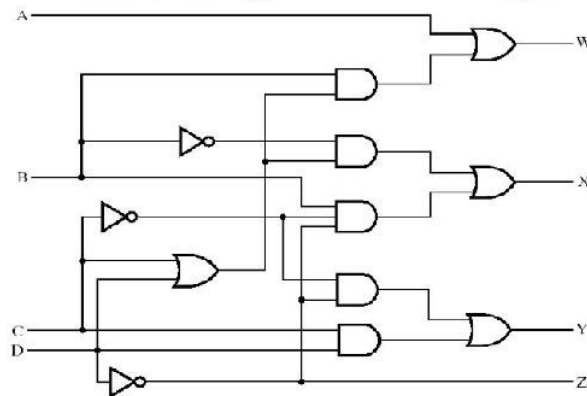
To design and set up the circuit of BCD to Excess-3 converter

**COMPONENTS REQUIRED**

IC Trainer kit, IC 7486, IC 7408, IC 7404, IC 7432

**PRINCIPLE**

The Excess-3 code for a decimal digit is the binary combination corresponding to the decimal digit plus 3. For example, the excess-3 code for decimal digit 5 is the binary combination for  $5+3=8$ , which is 1000. Each BCD digit four bits with the bits with the bits, from most significant to least significant, labelled A,B,C,D. As the same for excess-3 labeled W,X,Y,Z.



**BCD Logic circuit**

**Truth Table of BCD Logic circuit**

Input (BCD)				Output (Excess-3)			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1

0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

### PROCEDURE

1. Test all the components using multi meter and digital IC tester
2. Verify the truth table of the circuit by feeding input bit combinations

### RESULT

The circuit of BCD to Excess-3 converter has set up and verified the result.

### **Multiplexer and de Multiplexer**

#### **AIM**

To design Multiplexer and Demultiplexer and verify their truth tables.

#### **COMPONENTS REQUIRED: -**

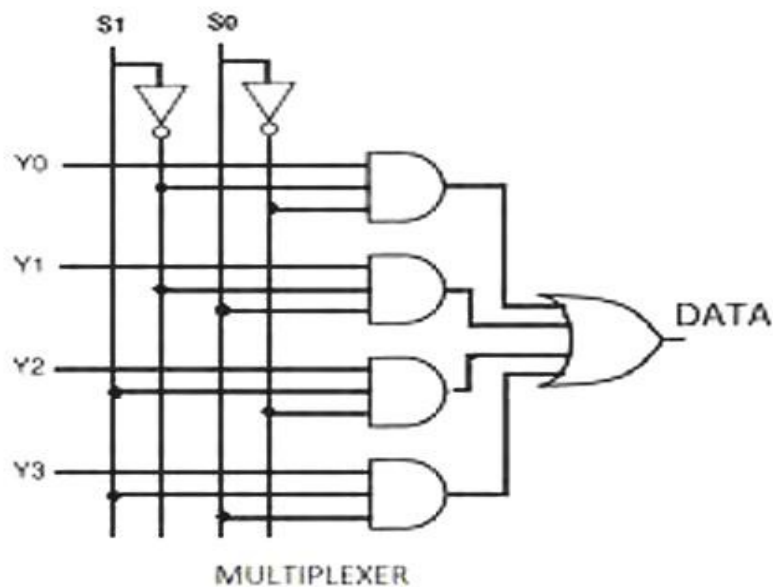
Digital IC trainer kit, IC

#### **PRINCIPLE**

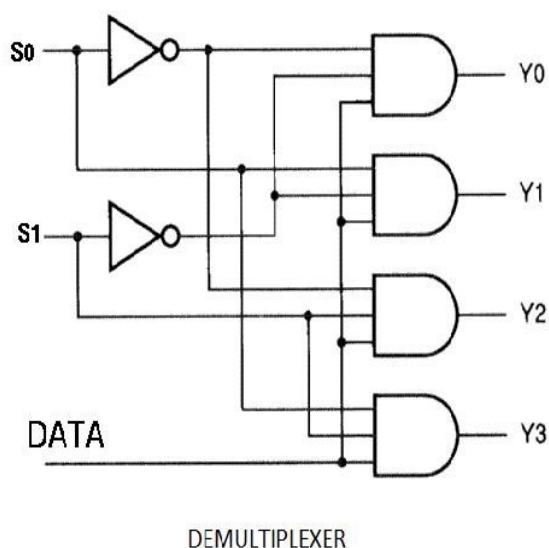
In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of  $2^n$  inputs has  $n$  select lines, which are used to select which input line to send to the output. An electronic multiplexer can be considered as a multiple-input, single-output switch. Multiplexers are mainly used to increase the amount of data that can be sent over the network

within a certain amount of time and bandwidth. A multiplexer is also called a data selector.

Conversely, a demultiplexer (or demux) is a device taking a single input signal and selecting one of many data-output-lines, which is connected to the single input. An electronic demultiplexer can be considered as a single-input, multiple-output switch. A multiplexer is often used with a complementary de multiplexer on the receiving end.



TRUTH TABLE		
S1	S0	DATA
0	0	Y0
0	1	Y1
1	0	Y2
1	1	Y3



TRUTH TABLE						
INPUTS			OUTPUTS			
DATA	S1	S0	Y3	Y2	Y1	Y0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

### PROCEDURE:

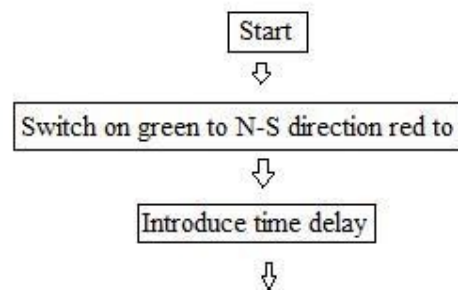
1. Connections are made as per the circuit diagram
2. Switch on the power supply
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

**RESULT:**

Multiplexer and Demultiplexer are constructed and verified the truth tables.

**MICROPROCESSOR – TRAFFIC CONTROL STIMULATION**

**Aim :** To interfaces traffic light controller with microprocessor 8085



MEMORY ADDRESS	MNEMONICS		COMMENTS
	OPCODE	OPERAN	
8500	MVI	A, 30	All ports as o/p
8502	OUT	25	
8504	MVI	A, 0F	
8506	OUT	21	
8508	MVI	A, 8D	For green
850A	CAL	20 Introduce Amber delay	
850C	L	8569	Sequence delay
850F	CAL	885F Amber delay	
8512	L	A, 49 Switch on Red in N-S direction & green in E-N sides	For stopping N –
8514	MVI	20 Introduce time delay	side Sequence
8516	OUT	20 Introduce Amber delay	delay Amber
8519	CAL	8569 Introduce Amber delay	delay
851C	CAL	855F Switch on Red for N-S direction & right green for free-left in all sides and stopping	
851E	L	A, 49 Introduce Amber signal and Amber delay	F-W sides for right turn in N sides
8520	CAL	20 Switch on Red for N-S direction & right turn in E-N sides	
8522	L	A, 01 Introduce time delay and Amber delay	
8524	CAL	20	
8527	MVI	8569 Switch on Red for all direction & green for pedestor	
8529	OUT	A, 00 Introduce time delay	
852B	MVI	22	
852E	OUT	855	For amber delay
8530	CAL	F	For stopping vehicle in N-S direction
8532	L	A,	
8534	MVI	89	For right turn in t-w sides
8536	OUT	20	
8539	CAL	A, 02	Sequence delay
853B	L	22	
853D	MVI	8569	



**KARPAGAM ACADEMY OF HIGHER EDUCATION**  
**CLASS: II MSC PHYSICS**  
**COURSE NAME: ADVANCED ELECTRONICS PRACTICAL**  
**COURSE CODE: 17PHP312** **BATCH-2018-2020**

854E	MVI	C, 10	For amber signal all sides  Delay count
8550	CALL	856F	
8553	MVI	A, 30	
8555	OUT	20	
8557	MVI	C, 08	
8559	CALL	856F	
855C	JMP	850 A	
855F	MVI	A, 39	
8561	OUT	20	
8563	MVI	C, 08	
8565	CALL	856F	
8568	RET		

**Delay program :**

MEMORY ADDRESS	MNEMONICS	
	OPCODE	OPERAND
8569	MVI	B, 40
856B	CALL	856F
856E	RET	
856F	MVI	C, FF
8571	MVI	A, FF
8573	NOP	
857A	DCR	A
8575	JNZ	8573
8578	DCR	C
8579	MOV	A,B
857C	JNZ	8571
857D	ORA	B
857E	JZ	8583
8581	DCR	B
8582	JZ	856F
8585	RET	

**Result :** The traffic control system is stimulated using microprocessor 8085









