#### **Experiment No:1**

#### Date:

#### **TRANSISTOR AS A SWITCH**

#### AIM

To observe the action of a Transistor as an electronic switch and measure the voltage across the transistor when it is ON and when it is OFF.

## **APPARATUS:**

NPN transistor, Resistance, Regulated power supply, Bread board and connecting wires.

#### THEORY

Based on the voltage applied at the base terminal of a transistor switching operation is performed. When a sufficient voltage ( $V_{in} > 0.7 V$ ) is applied between the base and emitter, collector to emitter voltage is approximately equal to 0. Therefore, the transistor acts as a short circuit. The collector current  $V_{cc}/R_c$  flows through the transistor. Similarly, when no voltage or zero voltage is applied at the input, transistor operates in cutoff region and acts as an open circuit. This is the basic principle of switching operation of transistor. In this type of switching connection; load is connected to the switching output with a reference point. Thus, when the transistor is switched ON, current will flow from source to ground through the load.

# PROCEDURE

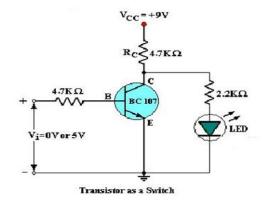
1. Construct the circuit as shown in the diagram

2. Connect '0' volts to the input terminals.

3. Measure the voltage across collector to emitter (VCE), collector to base (VCB) and base to emitter (VBE).

4. Connect '5' volts to the input terminals. Measure the voltage across collector to emitter (VCE), collector to base (VCB) and base to emitter (VBE).

# **CIRCUIT DIAGRAM**



# **TABULAR FORMS:**

Input voltage (V)	VCE (V)	VCB (V)	VBE (V)	Mode ON/OFF	Mode of LED
0 V 5V					

# RESULT

Studied the characteristics of transistor as an electronic switch

# Experiment No:2 Date:

#### . JUNCTION FIELD EFFECT AMPLIFIER

#### AIM:

To construct JFET amplifier and plot the frequency response curve.

#### **APPARATUS:**

JFET transistor (BMW10), Resistance, Regulated power supply, function generator, CRO, Bread board and connecting wires.

# THEORY

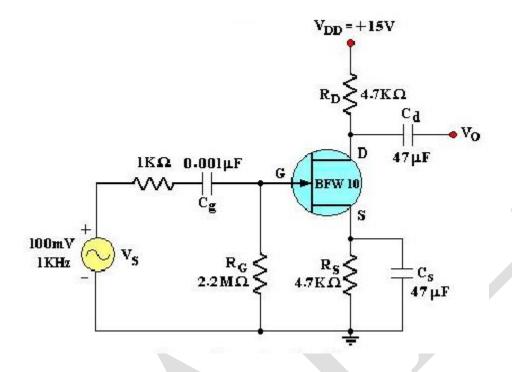
. One of the important operations of JFET is amplification. It amplified the weak signal connected to the gate terminals. Gate - source junction (input) is always reverse biased, so that a small change in the reverse bias on the gate produces a large change in drain current. This process will make JFET act as amplifier. Advantages of JFET amplifier over bipolar transistors are extremely high input impedance and low noise output.

# **PROCEDURE:**

1. Connect the circuit as shown in the Diagram.

- 2. Set input voltage (1 V) from the Signal Generator
- 3. Observe the output wave form from CRO
- 4. Vary the frequency from Signal Generator in appropriate steps and note down the corresponding O/P Voltage Vo.
- 4. Calculate the Voltage Gain Av = Vo/Vi and note down in the tabular form.
- 5. Plot the frequency response curve on a Semi-log Graph sheet
- 6 Find out the Bandwidth B.W = f2 f1.

# **CIRCUIT DIAGRAM**

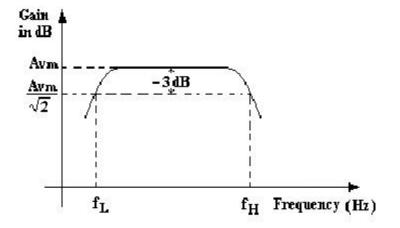


# **TABULAR FORMS:**

# Input Voltage= ..... V

		Voltage Gain	Av in dB
S.No Frequency (Hz)	O/P Voltage, Vo (V)	Av =Vo/Vi	= 20 log (Av)

# **MODEL GRAPH**



# RESULT

Junction field effect transistor amplifier is constructed and plot the frequency response curve. Bandwidth = Experiment No:3 Date:

#### SCR CHARACTERISTICS

#### AIM:

To obtain the V-I characteristics of SCR and to find the break over voltage

#### **APPARATUS:**

TYN604, Resistance, Regulated power supply, Voltmeters, Ammeters, Bread board and connecting wires.

#### THEORY

**Silicon Controlled Rectifier (SCR)** is a unidirectional semiconductor device made of silicon which can be used to give a selected power to the load by switching it ON for variable amount of time. It is a four-layer solid-state current-controlling device.

There are three modes of operation for an SCR depending upon the biasing .

#### Forward blocking mode

In this mode of operation, the anode is given a positive voltage while the cathode is given a negative voltage, to keep the gate at zero potential. Now the junction **J1** and **J3** are forwardbiased, and **J2** is reverse-biased, so that only a small leakage current flows from the anode to the cathode until the applied voltage reaches its break over value, at which **J2** undergoes avalanche breakdown, and conduction starts, and below break over voltage it provide high resistance to the current and is said to be in the off state.

#### Forward conduction mode

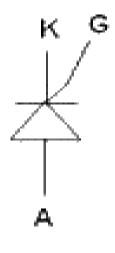
We can bring SCR from blocking mode to conduction mode in two ways: either by increasing the voltage across anode to cathode beyond break over voltage or by applying positive pulse at gate. Once SCR starts conducting, no more gate voltage is necessary to keep it in the on state. There are two ways to turn it off: In first case, decrease the current through it below a minimum value called the holding current and I second case, with the gate turned off, short out the anode and cathode temporarily with a push-button switch or transistor across the junction.

#### **Reverse blocking mode**

SCRs are existing with reverse blocking capability, the reverse blocking voltage rating and forward blocking voltage rating are the same. The main application for reverse blocking SCR is in current-source inverters.

SCRs unable to block the reverse voltage are known as **asymmetrical SCR**, or **ASCR**. ASCRs are used where either a reverse conducting diode is applied in parallel or where reverse voltage would never occur .

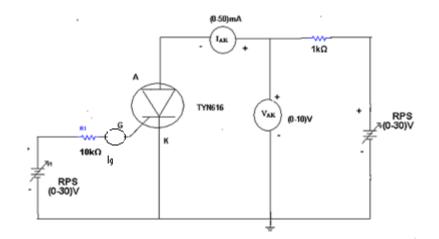
## SYMBOL



#### **PROCEDURE:**

- 1. Connect the circuit as shown in the diagram.
- 2. Keep the Ig constant and by varying the output source note down the corresponding change in  $I_a$  and  $V_{ak}$ .
- 3. Repeat the above steps for different values of Ig
- 4. Note the forward breakover voltage (VBO), latching current (IL) and holding current (IH).
- 5. Plot the output characteristics.

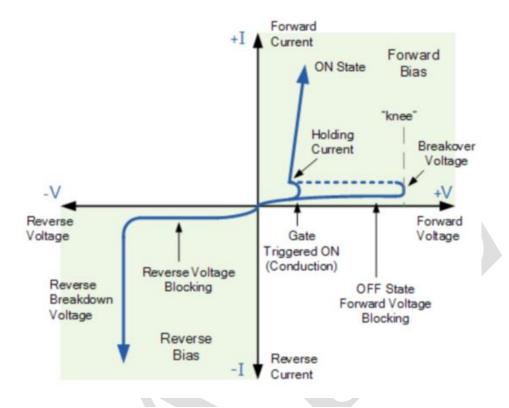
#### **CIRCUIT DIAGRAM**



# **TABULAR FORM:**

S. No	Ig =1 mA		Ig= 2mA	
	Vak	Ia	Vak	Ia

## **MODEL GRAPH**



#### RESULT

Thus the V-I characteristics of SCR was obtained and graph was drawn.

# Experiment No:4 Date:

#### **INSTRUMENTATION AMPLIFIER**

#### AIM

Construct and verify linear operational amplifier such as an instrumentation amplifier.

#### **APPARATUS**

Op-amp(IC 741), Resistors, Capacitors Constant Dual power supply, multimeter, Signal Generators, CRO, Bread board and connecting wires.

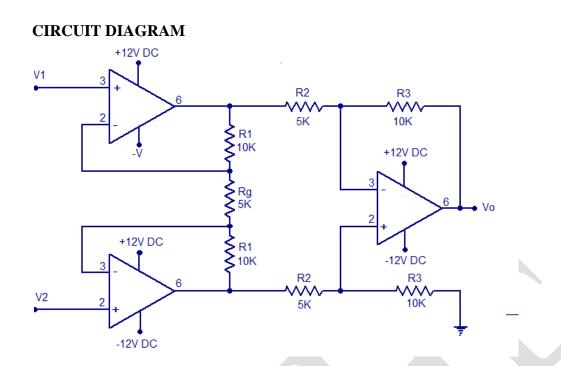
#### THEORY

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation amplifiers are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc.

# Gain (Av) = Vo / (V2 - V1) = (1 + (2R1/Rg)) x (R3/R2)

## PROCEDURE

- 1. Connect the circuit as shown in the diagram
- Apply the supply voltages of +15V to pin 7 and -15V to pin 4 of IC 741 respectively. Connect the ground to the ground point.
- 3. Apply DC voltage from regulated power supply to inputs  $V_1$  and  $V_2$ .
- 4. Note down the Vo using Voltmeter.
- 5. Compare theoretical and practical gain.



# **TABULAR FORM**

Input Voltage	Input Voltage	Output Voltage	Gain=Vo/(V2-	Gain =(1+2
V1 in volts	V1 in volts	V0 in volts	<b>V1</b> )	R1/Rg)x(R3/R2)
		•	•	

RESULT

Instrumentation amplifier circuit is constructed using operational amplifier and compared practical and theoretical gain.

# Experiment No:5 Date:

## **FLIP FLOPS**

**Aim:** - Verification of state tables of R-S flip-flop, J - K flip-flop, T Flip-Flop, D Flip-Flop Using NAND and NOR gates.

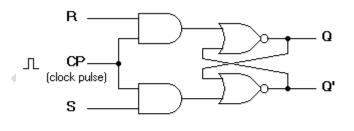
Apparatus: - IC 7400 (NAND Gate), IC 7402 (NOR Gate), IC 7408 (AND Gate).

# Theory: -

In case of sequential circuits the effect of all previous inputs on the outputs is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit . The relationship that exists among the inputs, outputs, present and next states can be specified by either the state table or the state diagram. State Table: - The state table representation of a sequential circuit consists of three sections labelled present state next state and output. The present state designates the state of flip – flops before the occurrence of a clock pulse. The next state shows the states of flip - flops after the clock pulse, and the output section lists the value of the output variables during the present state.

Flip-Flop:-The basic one bit digital memory circuit is known as flip-flop. It can store either 0 or 1. Flip-flops are classifieds according to the number of inputs.

**R-S Flip-Flop:-** The circuit is similar to SR latch except enable signal is replaced by clock pulse.



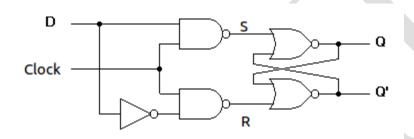
**R-S Flip-Flop** 

<b>Clock Pulse</b>	S	R	Q(t+1)
0	x	x	Qt
1	0	0	Qt

1	1	0	Set
1	0	1	Reset
1	1	1	Indeterminate ?

# D Flip-Flop: -

A D FF has a single data input. This type of FF is obtained from the SR FF by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making then complement of each other.

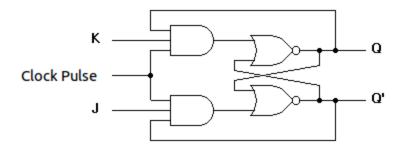


D-Flip Flop

Clock Pulse D input Q(t+1)				
0	Х	0		
1	0	0		
1	1	1		

**J-K Flip-Flop:-** In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other.

Logic Diagram

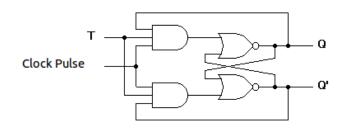


J-K flip Flop

# Characteristic table for J-K flip flop

Clock Pulse	J	K	Q(t+1)
0	X	x	NC
1	0	0	NC
1	0	1	Reset
1	1	0	Set
1	1	1	Toggle (Qt)'

**T Flip-Flop:-** T flip-flop is known as toggle flip-flop. The T flip-flop is modification of the J-K flip-flop. Both the JK inputs of the JK flip – flop are held at logic 1 and the clock signal continuous to change.



T-Flip Flop

<b>Clock Pulse</b>	Q(t+1)	
0	x	NC
1	0	NC
1	1	Toggle (Qt)'

Procedure:-

Connections are made as per circuit diagram.

Verify truth- tables for various combinations of input .

IC Implementation IC 7476 Functional table

# INPUTS OUTPUT

PRESET	CLEAR	CLOCK	J	K	Q	Q'
L	L	Х	X	Χ	Η	Н
L	Н	Х	X	X	Η	L
Н	L	X	X	Χ	L	Н
Н	Н	L	0	0	0	Q'
Н	Н	L	1	0	1	0
Н	Н	L	0	1	0	1
Н	Н	L	1	1	Тоз	ggle
Н	Н	0	x	x	Q	Q'

# **RESULT:** -

Study and verified truth-tables of various flip-flops.

# Experiment No:6 Date:

## LOG AND ANTILOG AMPLIFIERS

## AIM

To understand the behavior of logarithmic and antilogarithmic amplifiers.

# APPARATUS

Resistors: 100KΩ ,Diodes,IC 741:,Breadboard and Multimeter

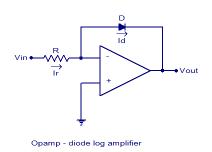
## Theory:

Log amplifiers are widely used for analog signal compression applications. When a diode used in the feedback loop of an operational amplifier is forward biased by a constant current of magnitude i =v /R then it develops a potential  $VD = VT \times Ln(Vi/R I_0)$  across the diode. Note that the input voltage and diode voltage are related in a logarithmic fashion. If we take the diode voltage as an output voltage then the input and output will be related in a logarithmic fashion. The base emitter junction of a bipolar junction transistor can be used as diode when collector and base are shorted. So a transistor can also be used in the feedback loop of an op-amp. Antilog is inverse operation of log operation so; antilog amplifiers can be designed by reversing the arrangement of diodes and resistors in the log amplifiers. It is important to note that a single polarity of current can only forward bias the diode. That means the log operation or antilog operation is single quadrant operation.

# PROCEDURE

- 1. Set the supply voltage at +12V.
- 2. Set the input voltage to 1V.
- 3. See the voltage across the diode. Note the negative sign.
- 4. Increase the input voltage in the step of 1V up to 20V.
- 5. Plot the characteristics of input voltage and output voltage.
- 6. Reverse the polarity of the diode and see the effect for positive input

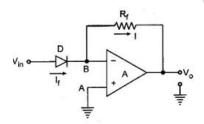
# Log amplifier



# PROCEDURE

- 1. Set the input voltage to 100mV.
- 2. See the voltage across the Resistor. Note the negative sign.
- 3. Increase the input voltage in the step of 50mV up to 500mV.
- 4. Plot the characteristics of input voltage and output voltage.
- 5. Reverse the polarity of the diode and see the effect for positive input voltage.

#### Anti log amplifier



Basic antilog amplifier

## RESULT

Logarithmic and antilogarithmic amplifiers using diode is constructed and plot the characteristics curve.

# **Experiment No:7**

#### Date:

#### ASTABLE MULTIVIBRATOR

## AIM

To study the operation of IC555 Timer as monostable multivibrator.

#### **APPARATUS**

IC 555, Resistors, Capacitors, Power supply, CRO, Bread board and connecting wires.

## THEORY

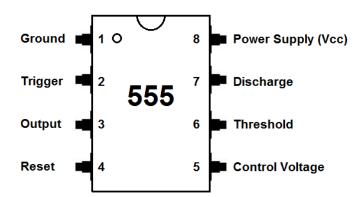
An Astable Multivibrator is a free running oscillator circuit that continuously produces rectangular wave without the help of external triggering. It has no stable state.

T charges= 0.69 (RA+RB) C

T discharge= 0.69 RBC

The total time period is T=T charges+ T discharge

# PIN DIAGRAM

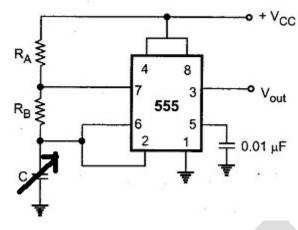


#### PROCEDURE

- 1. Make the connections as shown in the figure.
- 2. Switch on the power supply and observe the output wave form from CRO

3. Change the value of capacitor using a variable capacitance box and measure the time period of the signal and calculate the frequency.

# **CIRCUIT DIAGRAM**

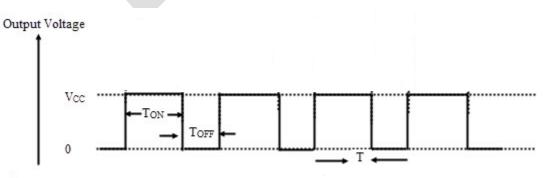


RA=10KΩ, RB=100KΩ, C1=0.01µf

# **TABULAR FORMS**

Value of the	Time per	Length of	Time period	Practical	Theoretical
capacitor	division	the wave	(T mS)	Frequency	Frequency
				F=1/T in Hz	

# **MODEL GRAPH**



#### RESULT

Performance of astable multivibrator using 555 timer is studied.

# **Viva-Questions**

- 1. Define multivibrator
- 2. What is astable multivibrator?
- 3. Explain the working principle of astable multivibrator.
- 4. Explain the origin of name IC555.
- 5. Explain the working principle of IC 555

#### **Experiment No:8**

#### Date:

#### DIFFERENTIAL EQUATIONS USING OPERATIONAL AMPLIFIER

## AIM

Design and construct an analog computer circuit to solve the differential equation using Op-amp.

## APPARATUS

Op amp-IC 741, Resistors, Capacitors, AFO, , Multimeter, Regulated power supply, Breadboard and connecting wires.

## THEORY

The op amp circuit can solve mathematical equations fast, including calculus problems such as differential equations. To solve a differential equation by finding v(t), for example, you could use various op amp configurations to find the output voltage  $v_o(t) = v(t)$ .

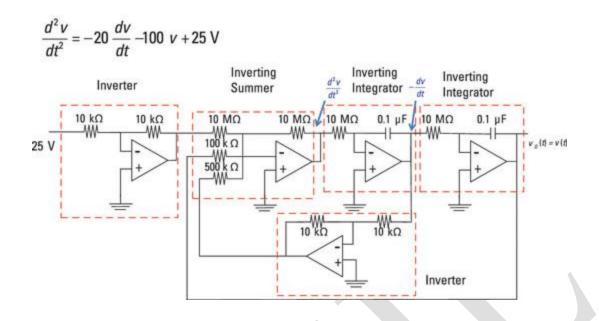
## PROCEDURE

1. The circuit connection is made as shown in the circuit. Note that three op amps are used: one as a summing amplifier, one as an integrator, and one as an inverting amplifier. Also, switches and DC voltages, shown as batteries, are included in the circuit in order to (1) the initial condition of y(0) = -1m (Vo2(0) = -1V) to the feedback capacitor during "reset", i.e., t < 0, and (2) the step input of 2m (V1 = 2V) to the input of the integrator during "operation", i.e., t ≥ 0.

2. Apply input voltage using a variable power supply

3. measure the output voltage using multimeter.

# CIRCUIT DIAGRAM



# **TABULAR FORMS**

InputVoltages(Volt)	Output Voltage

# RESULT

An analog computer circuit to solve the differential equation using Op-amp is constructed and verified the output.

# **Experiment No:9**

## Date:

#### SHIFT REGISTERS

# AIM

To set up and verify the performance of shift registers using D FF

# **COMPONENTS REQUIRED:**

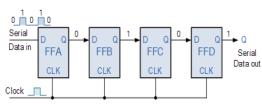
Digital IC trainer kit, IC 7476, IC 7408

# PRINCIPLE

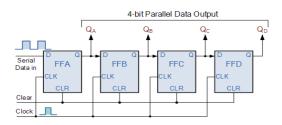
Registers are simply a group of flip flops that can be used to store a binary number. A shift register is nothing but a register which can accept binary number and shift it. The data can be entered in the shift register either in serial or in parallel. The output can be taken either in serial or in parallel. Since there are two ways to shift data in to a register and two ways to shift data out of the register four types of registers can be constructed.

# **CIRCUIT DIAGRAM**

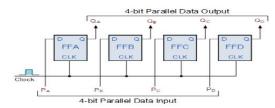
1. Serial In Serial Out (SISO)



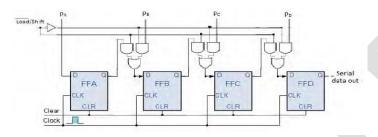
2. Serial In Parallel Out (SIPO)



3. Parallel In Parallel Out (PIPO)



4. Parallel In Serial Out (PISO)



# PROCEDURE

Test all the components using multimeter and digital IC tester 2. Set up serial input shift register using D FF. Clear all FF using clear pin. Feed 1011 to the serial input starting from LSB using the PRESET and CLEAR pins.

# RESULT

The performance of shift registers using D FF are set up and studied

#### PG PROGRAM 2018-2019 (EVEN)

#### SYLLABUS ELECTRONICS PRACTICAL – II SEMESTER – II (18PHP212) L T P C

# ANY TEN EXPERIMENTS

- 1. Characteristics and an application of SCR
- 2. Study of various types of flip-flops (R-S, J-K, Master Slave J-K)
- 3. Shift register Digital IC's
- 4. Schmitt trigger
- 5. Op-amp Simultaneous Addition and Subtraction
- 6. Op-amp V to I, I to V converter
- 7. V-I characteristics of a schotkky diode
- 8. V-I characteristics of photoconductive diode.
- 9. Op-amp Log and Antilog amplifier.
- 10. Op-amp Analog computation second order differential equation
- 11. Op-amp comparator Zero crossing detector, Window detector, time marker
- 12. 555 Timer application monostable, linear, Astable multivibrators.
- 13. Virtual Lab (Flip flop, Logic gates)

#### RERERENCES

- 1. Ouseph C.C., U.J. Rao and V. Vijayendran 2007, Practical Physics and Electronics, S.Viswanathan (Printers & Publishers) Pvt. Ltd., Chennai
- Singh S.P., 2003, Advanced Practical Physics 1, 13<sup>th</sup> Edition, Pragathi Prakashan, Meerut
- 3. Singh S.P., 2000, Advanced Practical Physics 2, 12<sup>th</sup> Edition, Pragathi Prakashan, Meerut
- 4. Gupta S.L. and V.Kumar, 2002, Practical Physics, 25<sup>th</sup> Edition, Pragathi Prakashan, Meerut
- 5. Ramakant A. Gayakwad, 2002, Op-amp and Linear Integrated Circuits ,4<sup>th</sup> Edition, Prentice Hall