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A Novel Paradigm to Eliminate Timing Violations using AHL

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Abstract

Objectives: This Paper presents a novel low power design approach for multipliers to eliminate timing violations. There are two major issues which are concentrated in this paper are positive bias temperature instability and negative bias temperature instability. Both the things affect the speed of transistor and leads to timing violations, which intern leads to the failure of an entire system. **Methods:** In this work, bypassing multiplier is used with adaptive hold logic. The implementation is done in 180 nm deep submicron CMOS technology. **Findings:** power consumption and error rate is studied after employing the AHL. **Improvements:** The experimental result shows that the performance of multipliers with AHL improved 72.8% when compared to existing methods and consumes less power.

Keywords: AHL, Bypass Multipliers, Low Power Design, Instability, Timing Violations

1. Introduction

Digital multipliers are the most important building blocks of many digital systems. As an example nothing can be done in signal processing units without multipliers. In most cases the multiplication will be implemented as successive addition. Timing violation of a multiplier is a serious issue that has to be addressed well. The timing violations of the multipliers are mostly because of two things which are positive bias temperature instability and negative bias temperature instability. VLSI domain will no longer consider about the size, the moore's law exceeded already[1]. So the power consumption is the ground where most of the researchers are playing. Low power design becomes challenging task. In older days cost and performance is considered primarily and power consumption is considered secondarily but now a days the scenario changed in opposite way[2].Power consumption plays an important role because most of electronic devises are battery operated; they are small and have more functionality. Normally in most of the systems like signal processing units the performance will depend on multiplier blocks, since the multiplication is fundamental function for digital signal processing. The performance of multiplier not only affects the throughput but also the power consumption of the system. This issue is not only concerned for digital signals processors but also general purpose processors(GPP).

Power dissipation of a system can be given as,

$$P_{total} = P_{switching} + P_{shortcircuit} + P_{static} + P_{leakage} \quad (1)$$

Here the $\mathbf{P_{switching}}$ is power dissipated due to switching activity. It plays a vital role in these calculations so it is the dominating factor. Ideally either PMOS or NMOS will be in ON state at any instance, but in practical cases both PMOS and NMOS will be in ON state for some time. Power dissipation due to that is represented as $\mathbf{P_{shortcircuit.}}$ Static power is represented here as $\mathbf{P_{static}}$ it depends on number of transistors used in a circuit. Finally charging and discharging of load capacitance determines the dynamic power consumption of a circuit.

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