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A Novel VLSI Based Radix-2 Single Path Delay Commutator (R2SDC) FFT Architecture Design

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Abstract

The aim is to design a new architecture called "Novel Radix-2 Single path Delay Commutator (R2SDC)" for improving the architectural performances of Fast Fourier Transformation (FFT) technique. In proposed new architecture, only commutator structures and complex multipliers are used to convert the time domain signals into frequency domain signals. In order to match the frequency response, delay elements are used appropriately. Traditional pipelined architectures have multiple complex multiplication units for performing frequency transformation techniques. But, proposed R2SDC structure has single complex multiplication unit per stage. Data flow structures of R2SDC architecture has been designed through Very Large Scale Integration (VLSI) System design environment. Proposed novel architecture called R2SDC FFT offers 21.4% improvements in hardware slices, 26.76% improvements in Look Up Tables (LUTs), 23.49% improvements in maximum output required time after clock and 31.88% improvements in power consumptions than traditional pipelined Radix-2 Single path Delay Feedback (R2SDF) FFT architecture. Also proposed architecture offers 4.61% improvements in hardware slices, 6.52% improvements in LUTs and 10.10% improvements in power consumption than combined SDC-SDF FFT architecture. In future, proposed R2DSC FFT architecture will be useful in Orthogonal Frequency Division Multiplexing (OFDM) architecture for estimating the frequency response of digital signals. It will be useful in large distance communications based applications.

Keywords: Analog to Digital Converter, Combined Single path Delay Feedback –Single path Delay Commutator, Orthogonal Frequency Division Multiplexing, Radix-2 Single path Delay Commutator, Very Large Scale Integration

1. Introduction

Fast Fourier Transformation (FFT) Processor is used to convert the time domain signals into frequency domain signals. In Analog to Digital Converter (ADC), output response is obtained in digital form. For transmitting the information across over the long distance, it is essential to convert the time domain signals into frequency domain signals. In order to exhibit the frequency transformation, different types of parallel and pipelined FFT architectures has been proposed by various researches. In the FFT calculation, twiddle factor multiplication plays an important role for converting one form of signals into another form of signals.

Most of the research works have been suggested the Reconfigurable Complex Multiplier for performing different values of twiddle factor multiplication. Two crucial architectures are available for performing the frequency transformation techniques. One of them is Radix-2 Single path Delay Feedback (R2SDF) FFT and another one of them is Radix-2 Multi-path Delay Commutator (R2MDC) FFT. In R2SDF FFT, single path delays have been used in every stage for performing butterfly operation. In every stage, single Processing Element (PE) structures have been used for performing addition and subtraction values whereas in traditional FFT structures, N*m PEs are used to perform addition and subtraction. Unlike R2SDF FFT, R2MDC FFT has multi-path delay structures in every

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stage. Commutator is used to convert one form of digital signals into another form of digital signals. With the help of Commutator signal, it can be possible to reduce the silicon chip size and power consumption. Similarly, with the help of feedback signal, it can be possible to increase speed of FFT processors.

From the above consecution, it is clear that both R2SDF FFT and R2MDC FFT have different types of advantages in terms of VLSI crucial factors. However, it requires best Frequency Transformation architecture which has combined advantages like less area utilization, high speed and lower power consumption for 3G and 4G based wireless communication signals. To meet the above requirements, a Novel Fully Radix-2 Single path Delay Commutator (R2SDC) FFT architectures have been introduced in this paper. Modified Bit Parallel Multiplier (MBPM) has been used for performing the multiplication of twiddle factor values.

Large endeavours have been suggested the Radix-2 FFT for exhibiting the frequency transformation techniques. Radix-2 FFT calculation has less complexity than other structures. High throughput and an area efficient architecture of Radix-2 FFT have been proposed in[2]. Scalable FFT processor has been designed in[8]. Multi-in Multi-out (MIMO) OFDM architecture has been considered in that article for the real time application of FFT processors. FFT plays a significant role in OFDM architecture. To perform long distance communication, it is essential to implement the frequency transformation techniques. In general FFT architecture, Memory (Storage) size should be in high. To reduce the memory size of FFT processor, conflict free memory processing based FFT architectures has been designed in[6].

Parallel FFT processor has more disadvantages in utilization of hardware and speed of processing. In order to overcome the problem of parallel FFT, Pipelined FFT processor such as R2SDF and R2MDC FFT structures has been introduced in[3]. Pipelined Radix-2^k FFT[3] structures have been developed with the help of Feedforward structures in those research articles. Feedforward structure provides 26ns for performing 8-point FFT. Further to reduce the hardware utilization, MDC structures have been introduced in[9]. Developed MDC based FFT structure of[9], uses fully pipelined structures, but it has independent multiplier for performing twiddle factor multiplication. In[4], a novel shared multiplier has been developed for improving the architecture of complex multiplier.

In[1,7] combined SDC-SDF FFT architecture has been developed to increase the throughput and speed of FFT processor further. This is a novelty architecture in which both SDC and SDF based pipelined structures have been explained in a detailed manner.

2. R2SDF FFT Architecture

Radix-2 Single path Delay Feedback (R2SDF) FFT is a stream-like processor (Pipelined Processor) in which single path delay has been used in every stage to perform the butterfly operation of FFT processor. Data Flow structure of eight point R2SDF FFT structures have been illustrated in Figure 1.

As shown in Figure 1, eight point data inputs are sequentially given to the R2SDF FFT processor. Sequence of inputs is getting feedback through delay elements for performing the butterfly operation. In the place of twiddle factor multiplier, Bit Parallel Multiplier (BPM) has been implemented. Speed of the FFT processor can be improved due to pipelining process. However, it utilizes more hardware in terms of Slices and LUTs. For implementing 8-point FFT, R2SDF processor requires three numbers of processing elements. In order to reduce the hardware utilization, Multipath Delay Commutator (MDC) structures has been preferred by various research.

3. R2MDC FFT Architecture

Like R2SDF FFT, Rfadix-2 Multipath Delay Commutator (R2MDC) FFT is a stream-like processor (Pipelined Processor) in which commutator structures have been used with the multi-path delay structures. Data Flow structure of eight point R2MDC FFT structures have been illustrated in Figure 2.

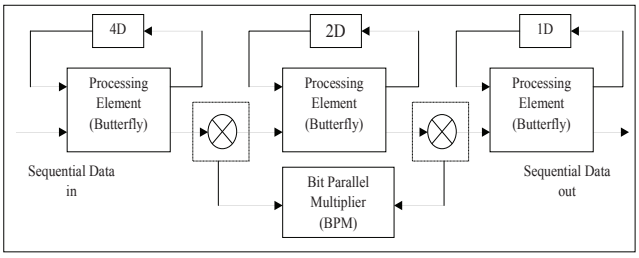


Figure 1. Data flow structure of eight point R2SDF FFT architecture.

Commutator has been used to convert one form of data signals into another form of data signals. Processing Element (PE) structure of R2MDC FFT has the same architectural performance as R2SDF FFT. Like R2SDF FFT, R2MDC FFT has sequential data input and sequential data output. When compared to the R2SDF FFT processor, R2MDC FFT processor has more advantage in less area utilization and lower power consumption. However, it requires more delay elements for controlling the signals at appropriate clock cycles.

4. Mixed R2SDC-R2SDF FFT Architecture

Both R2SDF FFT and R2MDC FFT have different types of advantages in terms of VLSI crucial factor like less area utilization, high speed and lower power consumption. In order to combine these two advantages, a combined SDC-SDF FFT architecture has been proposed in[7]. In the combined SDC-SDF FFT, both delay commutator and delay feedback structures are combined to provide the FFT calculation. The structure of mixed SDC-SDF FFT has been illustrated in Figure 3 as in[7].

As shown in Figure 3, all the stages of mixed SDC-SDF FFT except final stage have the SDC block in which single delay commutator function has been performed before performing signed addition and signed subtraction operation. The one of the most disadvantages of mixed SDC-SDF FFT structure is large number delay path to produce the frequency transformation signals at appropriate clock periods. However, practical implementation of SDC-SDF FFT architecture provides best performances in terms of less silicon area utilization, high speed and lower power consumption than R2SDF FFT architecture performance.

However, the final stage of SDF FFT structure reduces the performance improvement due to increasing the hardware complexity. In order to overcome this problem, final stage of SDF FFT has been replaced by SDC FFT by this research work.

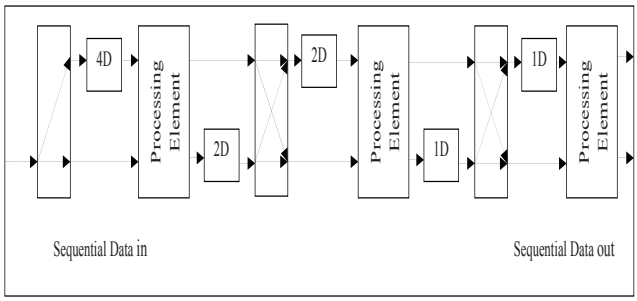


Figure 2. Data flow structure of eight point R2MDC FFT architecture.

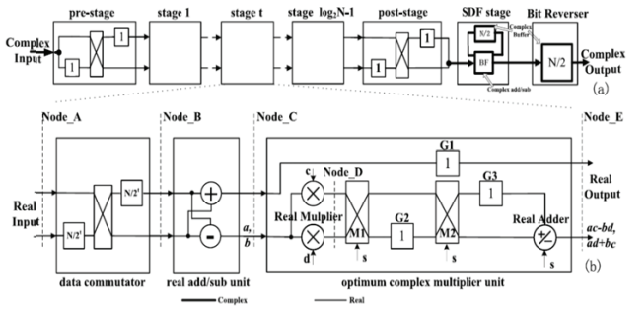


Figure 3. Structure of mixed SDC-SDF FFT.

5. Proposed R2SDC FFT Architecture

In the proposed design, a fully novel R2SDC FFT architecture has been designed. When compared to R2SDF, R2MDC and Mixed SDC-SDF FFT architecture, a novel R2SDC FFT design has more computational data flow structures. However, it provides best synthesis performances in terms of less area utilization, high speed and lower power consumption. Data flow logic of SDC has been illustrated in Figure 4.

In the combined SDC-SDF FFT architecture, final stage has SDF data flow path. In the proposed design, entire architecture has been designed with the help of only SDC architecture. Hence, the proposed architecture named as "R2SDC FFT" architecture. In every stage,

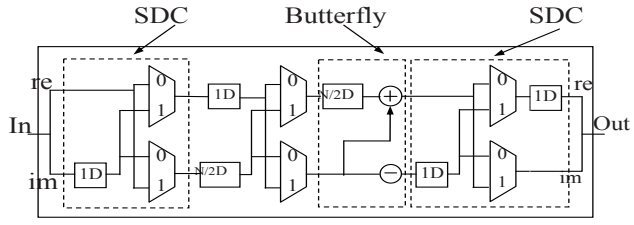


Figure 4. Data flow logic of SDC.

single path delay and commutator structures have been combined for calculating FFT computations. The architecture of 8-point R2SDC FFT has been illustrated in Figure 5.

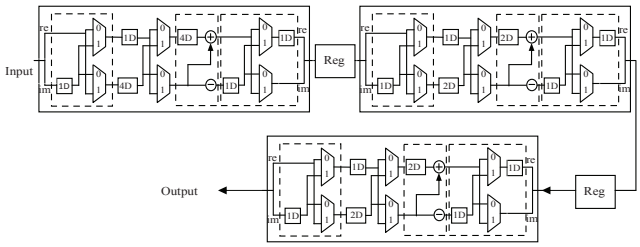


Figure 5. Architecture of 8-point R2SDC FFT.

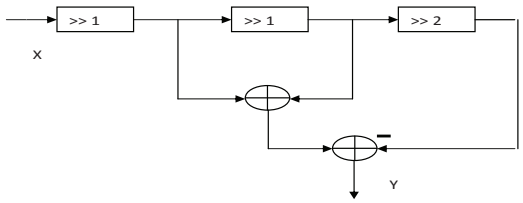


Figure 6. Modified BPM structure for the twiddle factor value 0.707.

In the place of twiddle factor multiplier, Modified Bit Parallel Multiplier (MBPM) has been used for calculating the multiplication results. Two main number of twiddle factor values such as 0.707 and -0.707 are involved in the complex multiplication of FFT structures. Modified BPM structure for the twiddle factor value 0.707 has been illustrated in Figure 6.

When integrating this modified BPM structure into R2SDC FFT structure, the performances has been improved than Mixed R2SDC FFT structure. In addition pipeline registers are used to improve the speed of the processor further.

6. Simulation Results

Simulation result of proposed novel R2SDC FFT architecture has been validated by using ModelSim 6.3C tool. The simulation result of 8-point proposed R2SDF FFT has been illustrated in Figure 7. As shown in Figure 7, eight point data inputs are given in a sequential manner. Similarly, eight point data outputs are obtained in a sequential manner after the 15th clock cycle. However, the synthesis performances are increased rapidly than other pipelined structure. Register Transfer Logic (RTL) view of Proposed R2SDC FFT architecture has been illustrated in Figure 8.

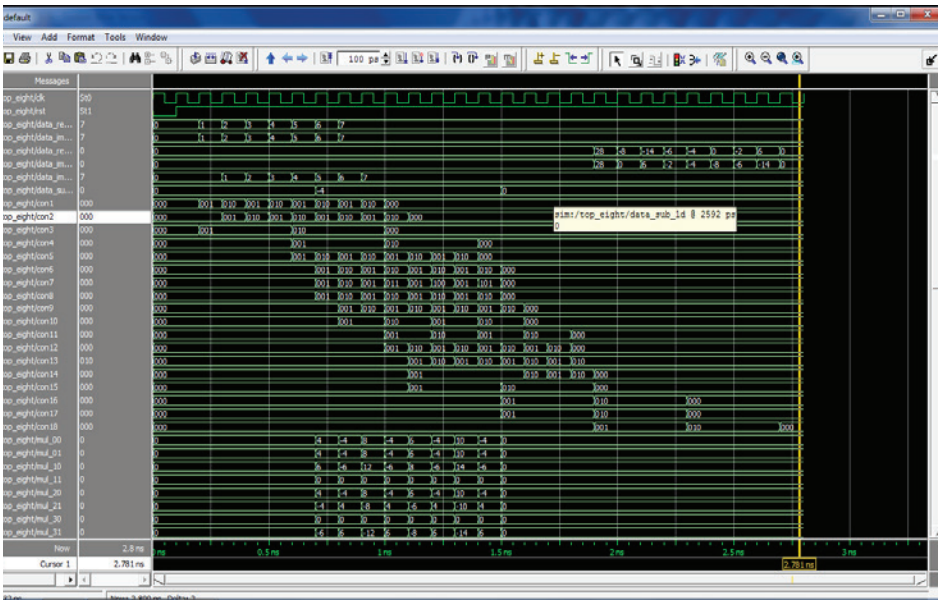


Figure 7. Simulation result of proposed R2SDC FFT architecture.

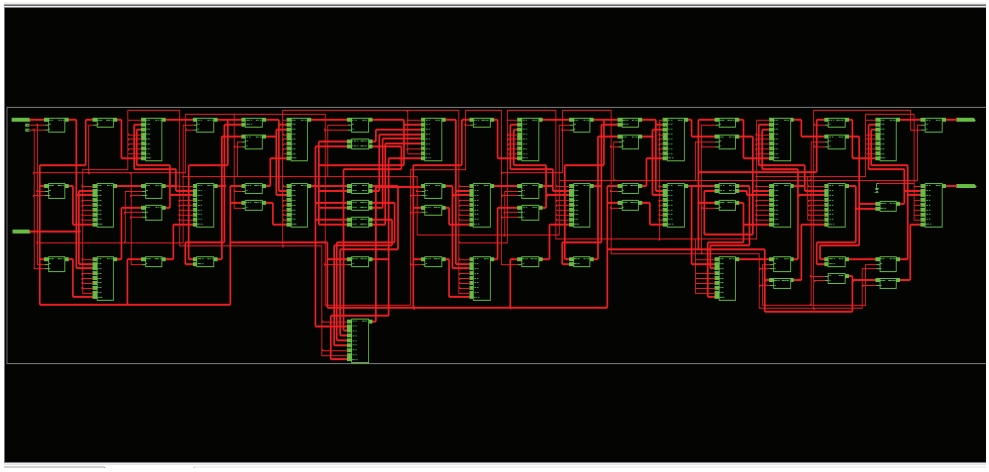


Figure 8. RTL view of proposed R2SDC FFT.

Table 1. Comparison of performance of R2SDF, Mixed SDC-SDF and R2SDC FFT

Types/Parameters	Slices	LUTs	Maximum Output required time after clock (ns)	Maximum Combinational Path Delay (ns)	Frequency (MHz)	Power (mW)
Traditional R2SDF FFT	500	822	27.951	21.374	54.144	966
Mixed SDC-SDF FFT	412	644	12.884	11.557	43.181	732
Proposed R2SDC FFT	393	602	21.385	22.069	45.416	658

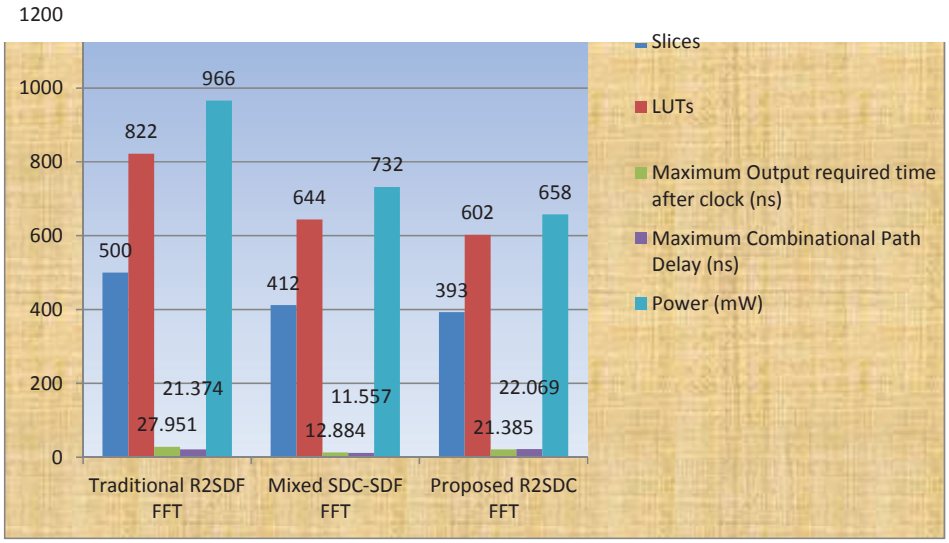
7. Performance Evaluation

Synthesis results of proposed R2SDC FFT has been estimated by using Xilinx 12.4i (Family: Spartan 3, Device: Xc3s200, Package: PQ 208, Speed: -5) design tool. Synthesis results of traditional R2SDF FFT, Mixed SDC-SDF FFT architecture has been analyzed and compared in Table 1.

Proposed R2SDC FFT offers 21.4% reduction in Slices, 26.76% reduction in LUTs, 23.49% reduction in Maximum output required time after clock and 31.88% reduction in power consumption than traditional R2SDF FFT. Similarly, 4.61% reduction in Slices, 6.52% reduction in LUTs and 10.10% reduction in power consumption than Mixed SDC-SDF FFT. Hence, the proposed R2SDF FFT architecture provides best performances in reducing the hardware complexity and power consumption than traditional FFT structures. The performances are graphically illustrated in Figure 9.

8. Conclusion

In this paper, a novel R2SDC FFT architecture is developed with the help of Verilog Hardware Description Language (Verilog HDL). The main aim of this proposed work is to reduce the hardware complexity and power consumption of Frequency Transformation Techniques (FFT). When compared to other traditional FFT architectures, R2SDC FFT has more data path complexity. However, practical implementation of proposed work gives rise in performance in terms of VLSI main factors. Proposed R2SDC FFT design gives 21.4% reduction in Slices, 26.76% reduction in LUTs, 23.49% reduction in Maximum output required time after clock and 31.88% reduction in power consumption than traditional R2SDF FFT design. Like that, proposed R2SDC FFT design gives 4.61% reduction in Slices, 6.52% reduction in LUTs and 10.10% reduction in power consumption than Mixed SDC-SDF FFT.



X axis – Methods (Traditional R2SDF, Mixed SDC-SDF, Proposed R2SDC)

Y axis – Slices, LUTs (1 unit = 200), Delays (1 unit = 200ns), Power (1 unit = 200mW)

Figure 9. Performance evaluation of traditional R2SDF FFT, Mixed SDC-SDF FFT and proposed R2SDC FFT in graphical view.

9. References

1. Begum SP, Yousuf S. I/O order FFT using SDC-SDF architecture based on pipeline architecture. IJCSME. 2015; 2(5):42–8.
2. Cheng C, Parhi K. High-throughput VLSI architecture for FFT computation. IEEE Transactions on Circuits and Systems II: Express Briefs. 2007 Oct; 54(10):863–7.
3. Garrido M, Grajal J, Sanchez M, Gustafsson O. Pipelined Radix 2k-Feedforward FFT architectures. Very Large Scale Integration (VLSI) Systems (VLSI). IEEE Transactions on Very Large Scale Integration Systems. 2013 Jan; 21(1):23–32.
4. Kim EJ, Lee JH, Sunwoo MH. Novel shared multiplier scheduling scheme for area-efficient FFT/IFFT Processors. IEEE Transactions on Very Large Scale Integration Systems. 2015 Sep; 23(9):1689–99.
5. Bhakthavatchalu R, Kannan SK, Nirmala Devi M. Verilog design of programmable JTAG controller for Digital VLSI IC's. Indian Journal of Science and Technology. 2015 Aug; 8(17):1–7.
6. Tsai PY, Lin CY. A generalized conflict-free memory addressing scheme for continuous-flow parallel-processing FFT processors with rescheduling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2011 Dec; 19(12):2290–302.
7. Wang Z, Liu X, He B, Yu F. A combined SDC-SDF architecture for normal I/O pipelined Radix-2 FFT. IEEE Transactions on Very Large Scale Integration System. 2015 May; 23(5):973–7.
8. Yang G, Jung Y. Scalable FFT processor for MIMO-OFDM based SDR systems. 5th IEEE International Symposium on Wireless Pervasive Computing (ISWPC), IEEE; Modena, Italy. 2010 May 5-7. p. 517–21.
9. Yang KJ, Tsai SH, Chuang GC. MDC FFT/IFFT processor with variable length for MIMO-OFDM systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2013 Apr; 21(4):720–31.