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## Materials Science in Semiconductor Processing

journal homepage: [www.elsevier.com/locate/mssp](http://www.elsevier.com/locate/mssp)Impact of annealing treatment on structural and dc electrical properties of spin coated tungsten trioxide thin films for Si/WO<sub>3</sub>/Ag junction diodeM. Raja<sup>a</sup>, J. Chandrasekaran<sup>a,\*</sup>, M. Balaji<sup>a</sup>, B. Janarthanan<sup>b</sup><sup>a</sup> Department of Physics, Sri Ramakrishna Mission Vidyalaya College of Arts and Science, Coimbatore 641020, Tamil Nadu, India<sup>b</sup> Department of Physics, Karpagam University, Coimbatore 641021, Tamil Nadu, India

## ARTICLE INFO

## Article history:

Received 18 May 2016

Received in revised form

8 August 2016

Accepted 11 August 2016

## Keywords:

Annealing temperature

P-n junction diodes

Tungsten trioxide

J-V-T characterization

Gaussian distribution

## ABSTRACT

We report on the effect of the thermal annealing on structural and electrical properties of p-Si/n-WO<sub>3</sub>/Ag junction diode. According to the XRD pattern, the WO<sub>3</sub> films exposed that the crystalline phase transformation of monoclinic to orthorhombic structure for an increasing annealing temperature. The SEM images show an abrupt change in the plate like grain growth and surface morphology. From the UV-visible analysis, the band gap energy decreases for the higher annealing temperature. The dc electrical characterization shows that the conductivity ( $\sigma_{dc}$ ), activation energy ( $E_a$ ) and pre-exponential factor ( $\sigma_0$ ) values vary function of temperature. The Si/WO<sub>3</sub>/Ag contact junction diode parameters of ideality factor ( $n$ ), barrier height ( $\Phi_B$ ), leakage current density ( $J_0$ ) and series resistance ( $R_s$ ) were examined by the J-V method, Cheung's and Norde functions as a function of annealing temperature according to the thermionic emission method (TE). The values of  $n$  and  $\Phi_B$  decrease with increasing annealing temperature and better the device performance on an optimized annealing temperature at 873 K. The temperature dependent of experimental  $n$  and  $\Phi_B$  revealed the presence of inhomogeneity at WO<sub>3</sub>-Ag interface. This behavior is modeled by assuming the existence of Gaussian distribution (GD) of barrier heights in temperature range 303–423 K.

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## 1. Introduction

The p-n junction diode is an emerging technology that employs in industrial and academic fields of microelectronics and photovoltaic devices. In recent years, interest in research for the development of renewable technologies by eco-friendly and low cost n-type transition metal oxide semiconductor (TMOS) based p-n junction devices. The p-Si/n-TMO based diodes have attracted world for their better charge transport capabilities [1–5]. ZnO, TiO<sub>2</sub>, SnO<sub>2</sub>, MoO<sub>3</sub> and WO<sub>3</sub> are the most standard semiconductor metal oxides used in the optoelectronic devices. Among them, tungsten trioxide (WO<sub>3</sub>) is used in many electronic devices owing to its tunable properties of chemical composition, surface morphological, optical absorption in visible range and high thermal stability [6,7]. To achieve a better film surface, porosity, crystal structure and phase modifications of WO<sub>3</sub> thin films, the various heat treatment (sintering, calcination and thermal annealing, etc.) processes are followed [8–10]. Predominantly, the annealing

temperature influences on the electrical and optical properties of WO<sub>3</sub> owing to densification of the grains with higher packing density, subsequently minimize the lattice defects and other structural deformations [11–13]. Kumar et al. [14] reveals that the annealing temperature influence on the structural, electrical and optical properties of the thermally evaporated WO<sub>3</sub> thin films. Doucette et al. [15] grown multi-domained heteroepitaxial WO<sub>3</sub> films on Si (100) substrates using a (111)-oriented BaF<sub>2</sub> buffer layer at the WO<sub>3</sub>-Si interface. Ahn group [16] improved crystallinity and enhanced light absorption in the long-wavelength region of the WO<sub>3</sub> thin films by varying annealing temperature and it was used for photo-electrochemical applications. The WO<sub>3</sub> films annealed at high temperature, exhibits structural and well developed grain size in the sol-gel process [17,18].

From the J-V characteristics of the p-n junction diode interface engineering process and charge transport mechanism usually deviate from the ideal thermionic emission (TE) model [19–22]. So that the main technological issue in the J-V characteristics at ambient temperature does not provide a detailed information about the conduction mechanism, charge transport mechanism across the p-n layers (Poole-Frenkel emission, hopping

\* Corresponding author.

E-mail address: [jchandraravind@yahoo.com](mailto:jchandraravind@yahoo.com) (J. Chandrasekaran).<http://dx.doi.org/10.1016/j.mssp.2016.08.007>

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