A STATE OF APPRAOCHES ON MINIMIZATION OF BOOLEAN FUNCTIONS

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Abstract:

Minimization of Boolean Functions (BF) may be older topic but still it is very popular in various fields such as PLA design, Built in Self Test (BIST), designing control systems, etc. Simplifying BFs influences several factors like circuit size, cost and computational speed while designing a digital circuit. The main idea behind this technique is the elimination of redundant pairs in the Boolean expression. It is a way of logic optimization which enables to minimize the area of complex logic in Integrated Circuits (ICs). Minimizing BFs reduces the area, cost, energy consumption, heat generation and increases the computational speed and reliability. Large numbers of researches are carried and large numbers of techniques have been proposed in this field. The absence of comprehensive survey in this field motivated to perform this study. This paper reviews various minimization techniques for BFs. These techniques are reviewed with their objective, methodology, implementation and advantages. At the end of the paper, a comparison is also made on the reviewed approaches.

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